Sashwath Nalin Kanth

40 COMMONS DR., APT# 04, SHREWSBURY, MA- 01545

Email: nsash1993@gmail.com Mobile: +1 469-664-4915.

Linkedin: www.linkedin.com/in/sashwath-nalin-kanth-29521810a

Objective

To apply my Digital and Analog integrated circuits design and verification skills and work on cutting edge projects.

Education

THE UNIVERSITY OF TEXAS AT DALLAS, Richardson, Texas, USA.
Master of Science in Electrical engineering, GPA **3.778/4.0,** December 2017

Anna University (Velammal Engineering College), Chennai, Tamil Nadu, India.
Bachelor of Engineering in Electrical and Electronics Engineering, GPA **8.512 / 10.0**, April 2015

Work experience:

SILICON DESIGN ENGINEER, Netronome Systems, Boxborough, MA, February 2018 - present

Some of my general responsibilities:

- Working with the Network Block Interface (NBI) team, implementing logic for traffic management and packet DMAs
- Working with verification engineers to fix RTL bugs and help with debugging other regression failures
- Working with the physical design team to resolve synthesis or timing issues that require a fix in the RTL.
- Maintain and update documentation for NBI related blocks
- Maintenance and upgrading CDL test benches to meet the new design requirement and fixing CDL tests
- Responsible for creation and maintenance of Latest builds for the Emulator
- Working with the software (Board Support Package) team to debug emulation issues.

Tasks/feature improvements related project KestrelPlus:

1) Removed the packet modifier block from NBI's architecture to reduce the area and power.

2) The Packet modifier was being used for deleting offsets that were prepended to each packet and append zeros to pad short packets (size < 64B). I reimplemented these two features as a part of the Traffic Manager egress DMA logic.

4) Increased the mini-packet interface (packet transfer interface between NBI and MAC islands) from transfer 16B to 32B per cycle to increase the throughput for packets in egress.

3) Modified the egress flow control logic to support removal of the Packet Modifier and upgraded mini-packet interface.

4) Upgraded the Traffic-manager reorder buffer to support higher performance requirement for KestrelPlus, by doubling the reordering capacity from 4K total packet descriptors to 8K descriptors.

5) Traffic Manager support for increasing sequence numbers from 4K to 64K.

6) Modified NBI ingress packet DMA engine to support increase in packet-numbers from 256 to 4K and sequence number from 4K to 64K.

7) Modified the logic that used to send packet allocation request and response command to support the new fields in the command as requested by Software.

8) Re-design the buffer allocator logic in the ingress DMA engine to support 300Mpps and 200Gbps. Replaced the bubble sort logic that was used to selected a memory target, with two different modes of operation: a round robin mode and max., select mode. Either of these modes can be used picked by software through a CSR.

Sashwath Nalin Kanth

40 COMMONS DR., APT# 04, SHREWSBURY, MA- 01545

Email: nsash1993@gmail.com Mobile: +1 469-664-4915.

Linkedin: www.linkedin.com/in/sashwath-nalin-kanth-29521810a

ENGINEERING INTERN, Netronome Systems, Boxborough, MA, January 2017 – August 2017

- Acquired training on running simulation on the emulator, extracting waves by assisting with the debugging of packet source-sink (PKSS) and wire application tests.
- Cleaned and re-structured RTL source code for Island Master Bridge (IMB) block, in the process, learnt about DSF-CPP bus architecture.
- Reduced the memory size of Cluster Local Scratch (CLS) and integrated the block into the Cluster Target Memories (CTM) hierarchy.
- Automated the migration of standard cell instantiations from Intel libraries to SMIC, TSMC libraries, and developed corresponding mapping tables, Python scripts.
- Implemented a UART interface on the emulator, worked with engineers from Cadence to bring up the feature.

ENGINEERING INTERN, Netronome Systems, Boxborough, MA, May 2016– August 2016

- Got acquainted with CDL Hardware description language - an open HDL invented by Netronome's CTO.
- Worked with the NBI team on issues related to coverage and helped with debugging issues on the packet reordering logic
- Debugged ECC related issues in reorder memory.

Coursework and Interests:

VLSI design, Application specific IC design, Advanced Digital Logic, Computer architecture, Microprocessors, Analog IC design, RF IC design, Power Management circuits, Active semiconductor devices, and Fundamentals of Semiconductor devices, Quantum physical electronics.

Online courses that reflect my hobbies and other fields of interests:

' SOC Verifica,on using SystemVerilog ',

' Machine Learning, Data Science and Deep Learning with Python ' ,

' The Complete JavaScript Course 2019: Build Real Projects', 'Deutsch Intensiv - Intensive German Course for Beginners'.

More info and links to the certificate on my linked page: **www.linkedin.com/in/sashwath-nalin-kanth-29521810a**

Technology Skills

- **Programming Languages/HDL:** Verilog, System Verilog- UVM, python, HTML, C, C++, Java, Javascript, SQL, Embedded C, Octave, Spice, VHDL, MATLAB.
- **Software:** MS Office- Word, Power point, Excel, MATLAB /Simulink, Labview.
- **Circuit and RTL Design/simulation Tools:**
  Cadence: Virtuoso layout editor, Schematic capture: Spectre, Assura, Encounter APR, Innovus, Genus
  Synopsys: HSPICE, Design Compiler, TetraMax -
  ATPG, Xilinx ISE, Quartus Prime, ModelSim.

Academic projects

MINI STEREO DIGITAL AUDIO PROCESSOR, M.S Electrical Engineering, Year- September 2016.

- Developed behavioral model, test-bench and architecture for an FIR audio signal processor.
- Developed and verified using ModelSim and Xilinx ISE.

DSP COMPUTATIONAL MODEL, M.S Electrical Engineering, Year- September 2016.

- Developed a computational model based on convolution function for a digital filter.
- Used as a software model for the MSDAP, implemented in C.

Sashwath Nalin Kanth

40 COMMONS DR., APT# 04, SHREWSBURY, MA- 01545

Email: nsash1993@gmail.com Mobile: +1 469-664-4915.

Linkedin: www.linkedin.com/in/sashwath-nalin-kanth-29521810a

TRIVIUM CIPHER, M.S Electrical Engineering, Year- April 2016.

- Designed a synchronous stream cipher-Trivium that can generate up to 2^{64} bits of key stream from an 80-bit secret key and an 80-bit initial value vector. Complete Custom layout of the design was implemented using Cadence- Virtuoso.

LOW NOISE AMPLIFIER, M.S Electrical Engineering, Year- April 2016.

- Designed a low noise amplifier operating at 2.4 to 2.5 GHz, 1.2 V, with a transducer gain of 13.9 dB. Developed a layout for the LNA using Cadence Virtuoso.

ON-CHIP SPIRAL INDUCTOR MODEL, M.S Electrical Engineering, Year – April 2016.

- Developed a MATLAB based model to aid the design of on-chip spiral inductors
- The model compute the inductance, Q-factor for given dimensions of the spiral inductor.

FAST-SETTLING OP-AMP FOR A SWITCHED-CAPACITOR PIPELINE ADC, M.S Electrical Engineering, Year-Dec 2015.

- Designed an op-amp using 0.25um, 2.5V CMOS technology to be used with switched-capacitor pipeline ADC.

WIRELESS POWER TRANSFER WITH SELF-REGULATED VOLTAGE FOR BIO-MEDICAL IMPLANTS, Bachelor of Engineering, Year-April 2015.

- Implemented a wireless power transfer system, to wirelessly recharge a battery driving a bio-medical implant.
- The battery voltage levels were monitored wirelessly using Bluetooth, and Labview in a remote system.
- A microcontroller (PIC16F877A) was used to monitor the voltage levels.

RFID BASED PARKING SYSTEM, Bachelor of Engineering, Year- 2012.