1. Description

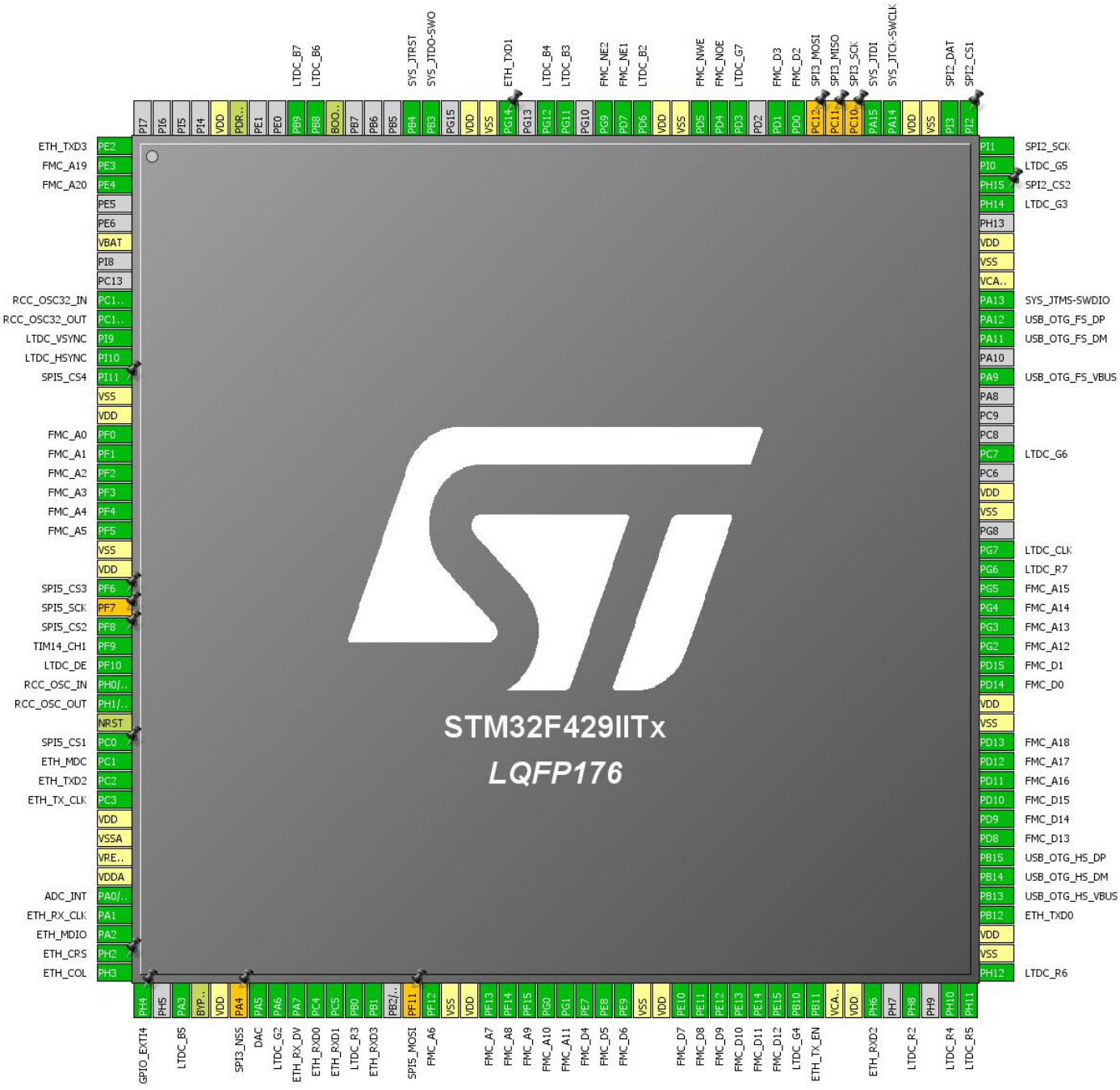
1.1. Project

Project Name	429IIT6
Board Name	No information
Generated with:	STM32CubeMX 4.24.0
Date	02/22/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429IITx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	ETH_TXD3	
2	PE3	I/O	FMC_A19	
3	PE4	I/O	FMC_A20	
6	VBAT	Power		
9	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
10	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
11	PI9	I/O	LTDC_VSYNC	
12	PI10	I/O	LTDC_HSYNC	
13	PI11 *	I/O	GPIO_Output	SPI5_CS4
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
24	PF6 *	I/O	GPIO_Output	SPI5_CS3
25	PF7 **	I/O	SPI5_SCK	
26	PF8 *	I/O	GPIO_Output	SPI5_CS2
27	PF9	I/O	TIM14_CH1	
28	PF10	I/O	LTDC_DE	
29	PH0/OSC_IN	I/O	RCC_OSC_IN	
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
32	PC0 *	I/O	GPIO_Output	SPI5_CS1
33	PC1	I/O	ETH_MDC	
34	PC2	I/O	ETH_TXD2	
35	PC3	I/O	ETH_TX_CLK	
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
40	PA0/WKUP	I/O	ADC1_IN0	ADC_INT

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	PA1	I/O	ETH_RX_CLK	
42	PA2	I/O	ETH_MDIO	
43	PH2	I/O	ETH_CRS	
44	PH3	I/O	ETH_COL	
45	PH4	I/O	GPIO_EXTI4	
47	PA3	I/O	LTDC_B5	
48	BYPASS_REG	Reset		
49	VDD	Power		
50	PA4 **	I/O	SPI3_NSS	
51	PA5	I/O	DAC_OUT2	DAC
52	PA6	I/O	LTDC_G2	
53	PA7	I/O	ETH_RX_DV	
54	PC4	I/O	ETH_RXD0	
55	PC5	I/O	ETH_RXD1	
56	PB0	I/O	LTDC_R3	
57	PB1	I/O	ETH_RXD3	
59	PF11 **	I/O	SPI5_MOSI	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
79	PB10	I/O	LTDC_G4	
80	PB11	I/O	ETH_TX_EN	
81	VCAP_1	Power		

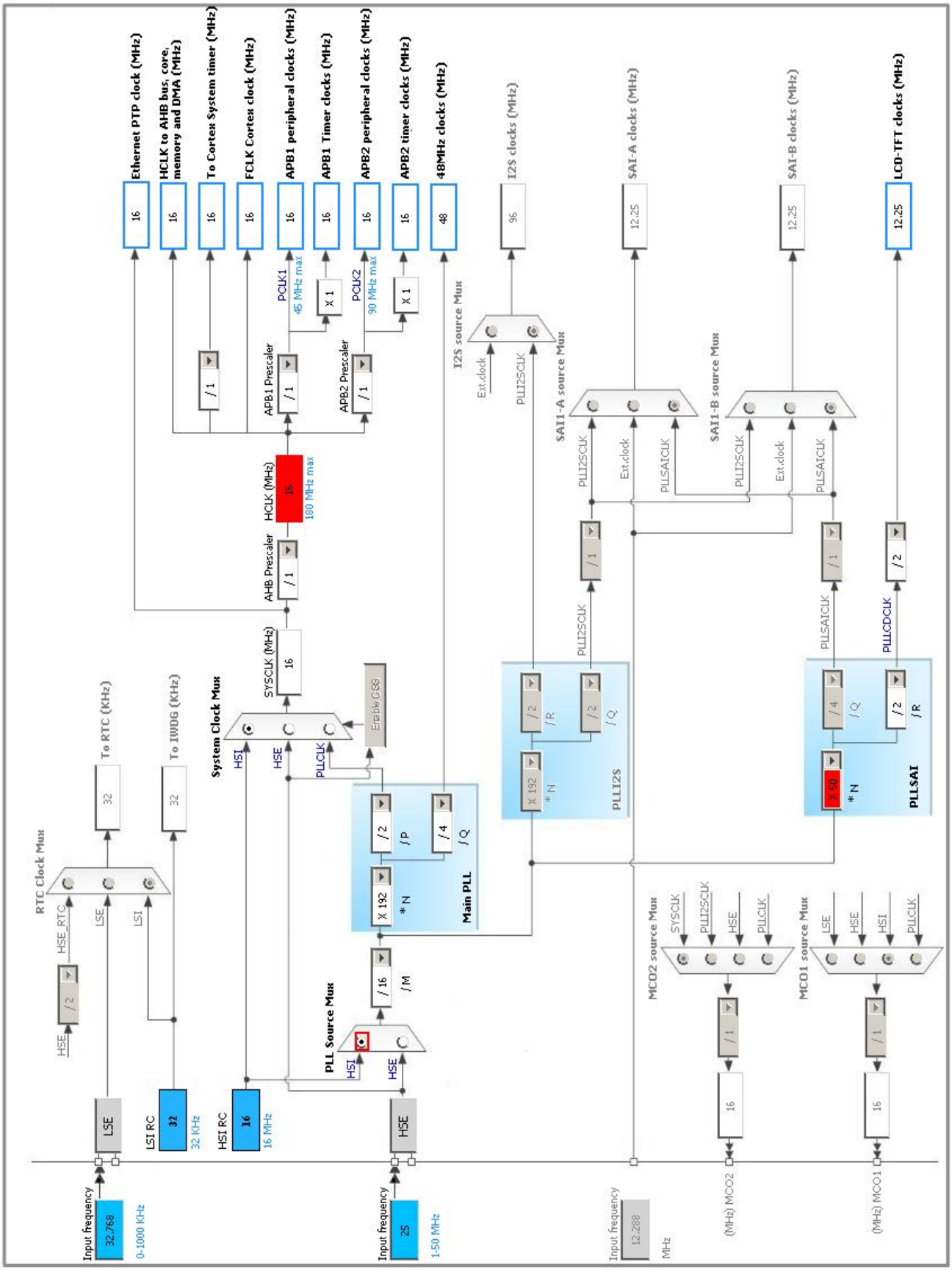
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
82	VDD	Power		
83	PH6	I/O	ETH_RXD2	
85	PH8	I/O	LTDC_R2	
87	PH10	I/O	LTDC_R4	
88	PH11	I/O	LTDC_R5	
89	PH12	I/O	LTDC_R6	
90	VSS	Power		
91	VDD	Power		
92	PB12	I/O	ETH_TXD0	
93	PB13	I/O	USB_OTG_HS_VBUS	
94	PB14	I/O	USB_OTG_HS_DM	
95	PB15	I/O	USB_OTG_HS_DP	
96	PD8	I/O	FMC_D13	
97	PD9	I/O	FMC_D14	
98	PD10	I/O	FMC_D15	
99	PD11	I/O	FMC_A16	
100	PD12	I/O	FMC_A17	
101	PD13	I/O	FMC_A18	
102	VSS	Power		
103	VDD	Power		
104	PD14	I/O	FMC_D0	
105	PD15	I/O	FMC_D1	
106	PG2	I/O	FMC_A12	
107	PG3	I/O	FMC_A13	
108	PG4	I/O	FMC_A14	
109	PG5	I/O	FMC_A15	
110	PG6	I/O	LTDC_R7	
111	PG7	I/O	LTDC_CLK	
113	VSS	Power		
114	VDD	Power		
116	PC7	I/O	LTDC_G6	
120	PA9	I/O	USB_OTG_FS_VBUS	
122	PA11	I/O	USB_OTG_FS_DM	
123	PA12	I/O	USB_OTG_FS_DP	
124	PA13	I/O	SYS_JTMS-SWDIO	
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
129	PH14	I/O	LTDC_G3	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
130	PH15 *	I/O	GPIO_Output	SPI2_CS2
131	PI0	I/O	LTDC_G5	
132	PI1	I/O	SPI2_SCK	
133	PI2 *	I/O	GPIO_Output	SPI2_CS1
134	PI3	I/O	SPI2_MOSI	SPI2_DAT
135	VSS	Power		
136	VDD	Power		
137	PA14	I/O	SYS_JTCK-SWCLK	
138	PA15	I/O	SYS_JTDI	
139	PC10 **	I/O	SPI3_SCK	
140	PC11 **	I/O	SPI3_MISO	
141	PC12 **	I/O	SPI3_MOSI	
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
145	PD3	I/O	LTDC_G7	
146	PD4	I/O	FMC_NOE	
147	PD5	I/O	FMC_NWE	
148	VSS	Power		
149	VDD	Power		
150	PD6	I/O	LTDC_B2	
151	PD7	I/O	FMC_NE1	
152	PG9	I/O	FMC_NE2	
154	PG11	I/O	LTDC_B3	
155	PG12	I/O	LTDC_B4	
157	PG14	I/O	ETH_TXD1	
158	VSS	Power		
159	VDD	Power		
161	PB3	I/O	SYS_JTDO-SWO	
162	PB4	I/O	SYS_JTRST	
166	BOOT0	Boot		
167	PB8	I/O	LTDC_B6	
168	PB9	I/O	LTDC_B7	
171	PDR_ON	Reset		
172	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. DAC

mode: OUT2 Configuration

5.2.1. Parameter Settings:

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

5.3. ETH

Mode: MII

5.3.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

5.3.2. Advanced Parameters:

External PHY Configuration:

PHY	DP83848_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***

Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x10 ***
MII Interrupt Control Register	**0x11 ***
MII Interrupt Status and Misc. Control Register	**0x12 ***
PHY Link mask	**0x0001 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***
PHY Enable interrupts	**0x0002 ***
PHY Enable output interrupt events	**0x0001 ***
Enable Interrupt on change of link status	**0x0020 ***
PHY link status interrupt mask	**0x2000 ***

5.4. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: NOR Flash

Address: 21 bits

Data: 16 bits

NOR Flash/PSRAM/SRAM/ROM/LCD 2

Chip Select: NE2

Memory type: NOR Flash

Address: 21 bits

Data: 16 bits

5.4.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	NOR Flash
Bank	Bank 1 NOR/PSRAM 1

Write operation	Disabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

5.4.2. NOR/PSRAM 2:

NOR/PSRAM control:

Memory type	NOR Flash
Bank	Bank 1 NOR/PSRAM 2
Write operation	Disabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

5.5. LTDC

Display Type: RGB666 (18 bits)

5.5.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3

Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

5.5.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

Layer 1 - Alpha constant for blending	0
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

5.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : BYPASS Clock Source

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 3
Power Over Drive	Disabled

5.7. SPI2

Mode: Transmit Only Master

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.8. SYS

Debug: JTAG (5 pins)

Timebase Source: SysTick

5.9. TIM14

mode: Activated

Channel1: PWM Generation CH1

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable

CH Polarity	High

5.10. USB_OTG_FS

Mode: Host_Only

mode: Activate_VBUS

5.10.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Signal start of frame	Disabled

5.11. USB_OTG_HS

Internal FS Phy: Host_Only

mode: Activate_VBUS

5.11.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Signal start of frame	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	ADC_INT
DAC	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	DAC
ETH	PE2	ETH_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC2	ETH_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC3	ETH_TX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_RX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PH2	ETH_CRS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PH3	ETH_COL	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_RX_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB1	ETH_RXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PH6	ETH_RXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
FMC	PE3	FMC_A19	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE4	FMC_A20	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD11	FMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD12	FMC_A17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD13	FMC_A18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_A14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_A15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG9	FMC_NE2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
LTDC	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH8	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH11	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH12	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH14	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PI1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI2_DAT
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		SWCLK				
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
	PB4	SYS_JTRST	n/a	n/a	n/a	
TIM14	PF9	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USB_OTG_HS	PB13	USB_OTG_HS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
Single Mapped Signals	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA4	SPI3_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF11	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PI11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI5_CS4
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI5_CS3
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI5_CS2
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI5_CS1
	PH4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PH15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_CS2
	PI2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_CS1

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line4 interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
SPI2 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
USB On The Go FS global interrupt	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		
USB On The Go HS End Point 1 In global interrupt	unused		
USB On The Go HS global interrupt	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429IITx
Datasheet	024030_Rev9

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Pack Report