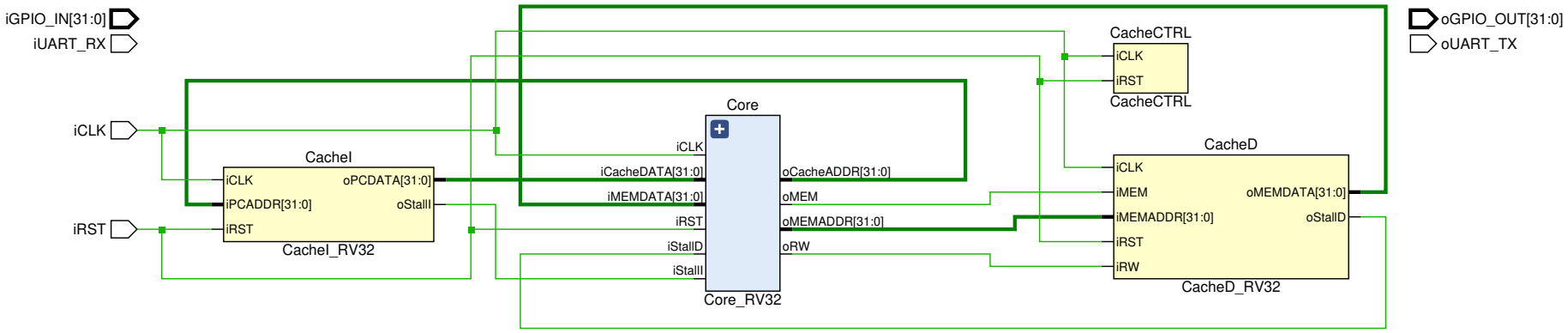
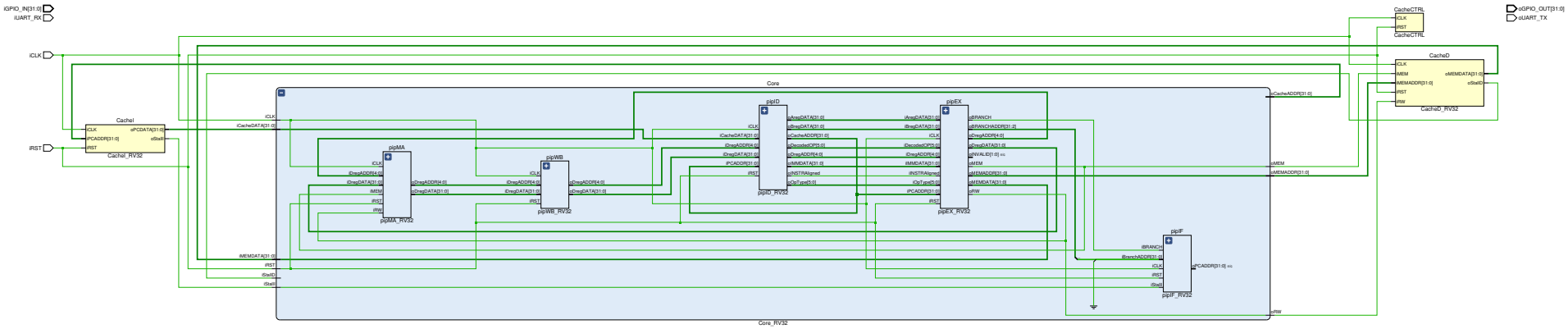
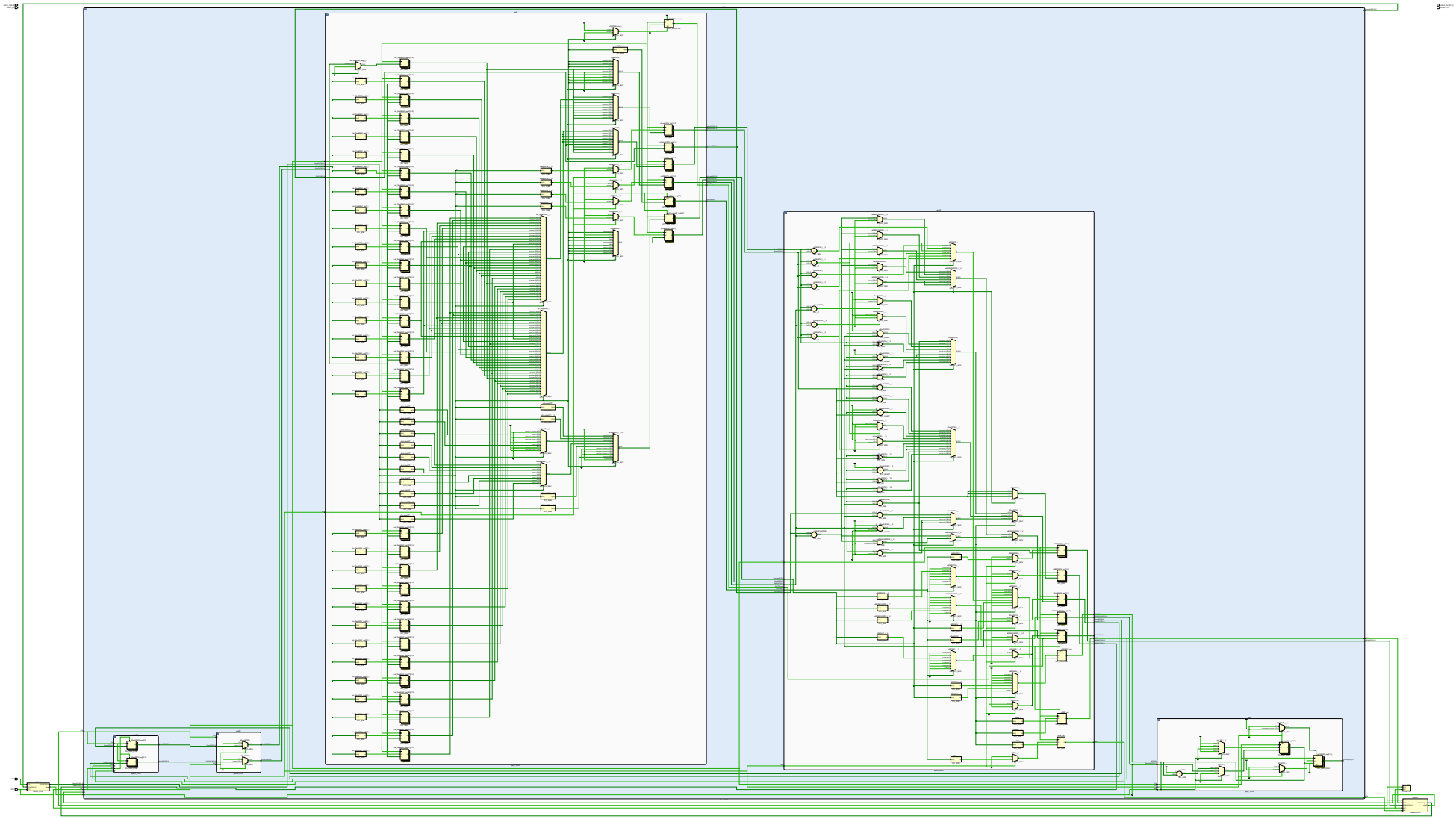

iGPIO_IN[31:0]
iUART_RX
iCLK
iRST
CacheI
iCLK
iPCADDR[31:0]
iRST
oPCDATA[31:0]
oStallI
CacheI_RV32
Core
iCLK
iCacheDATA[31:0]
iMEMDATA[31:0]
iRST
iStallD
iStallI
oCacheADDR[31:0]
oMEM
oMEMADDR[31:0]
oRW
Core_RV32
CacheCTRL
iCLK
iRST
CacheCTRL
CacheD
iCLK
iMEM
iMEMADDR[31:0]
iRST
iRW
oMEMDATA[31:0]
oStallD
CacheD_RV32
oGPIO_OUT[31:0]
oUART_TX


iGPIO_IN[31:0]
iUART_RX
iCLK
iRST
Cachel
CLK
iPCADDR[31:0]
iRST
oPCDATA[31:0]
oStall
Cachel_RV32
CacheCTRL
CLK
iRST
CacheCTRL
oGPIO_OUT[31:0]
oUART_TX
CacheD
CLK
iMEM
MEMADDR[31:0]
iRST
iRW
oMEMDATA[31:0]
oStallD
CacheD_RV32
Core
iCLK
iCacheDATA[31:0]
iMEMDATA[31:0]
iRST
iStallD
iStall
oCacheADDR[31:0]
oMEM
oMEMADDR[31:0]
oRW
pipMA
iCLK
iDreqADDR[4:0]
iDreqDATA[31:0]
iMEM
iRST
iRW
oDreqADDR[4:0]
oDreqDATA[31:0]
pipMA_RV32
pipWB
iCLK
iDreqADDR[4:0]
iDreqDATA[31:0]
iRST
oDreqADDR[4:0]
oDreqDATA[31:0]
pipWB_RV32
pipID
iCLK
iCacheDATA[31:0]
iDreqADDR[4:0]
iDreqDATA[31:0]
iPCADDR[31:0]
iRST
oDreqDATA[31:0]
oCacheADDR[31:0]
oDecodeOP[5:0]
oDreqADDR[4:0]
oIMMDATA[31:0]
oINSTRAligned
oOpType[5:0]
pipID_RV32
pipEX
iDreqDATA[31:0]
iDreqDATA[31:0]
iCLK
iDecodeOP[5:0]
iDreqADDR[4:0]
iIMMDATA[31:0]
iINSTRAligned
iOpType[5:0]
iPCADDR[31:0]
iRST
oBRANCH
oBRANCHADDR[31:2]
oDreqADDR[4:0]
oDreqDATA[31:0]
oINVALID[1:0]
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oMEMADDR[31:0]
oMEMDATA[31:0]
oRW
pipEX_RV32
pipIF
iBRANCH
iBranchADDR[31:0]
iCLK
iRST
iStall
oPCADDR[31:0]
pipIF_RV32
Core_RV32