



1. Description

1.1. Project

Project Name	Example project
Board Name	custom
Generated with:	STM32CubeMX 6.1.0
Date	11/03/2023

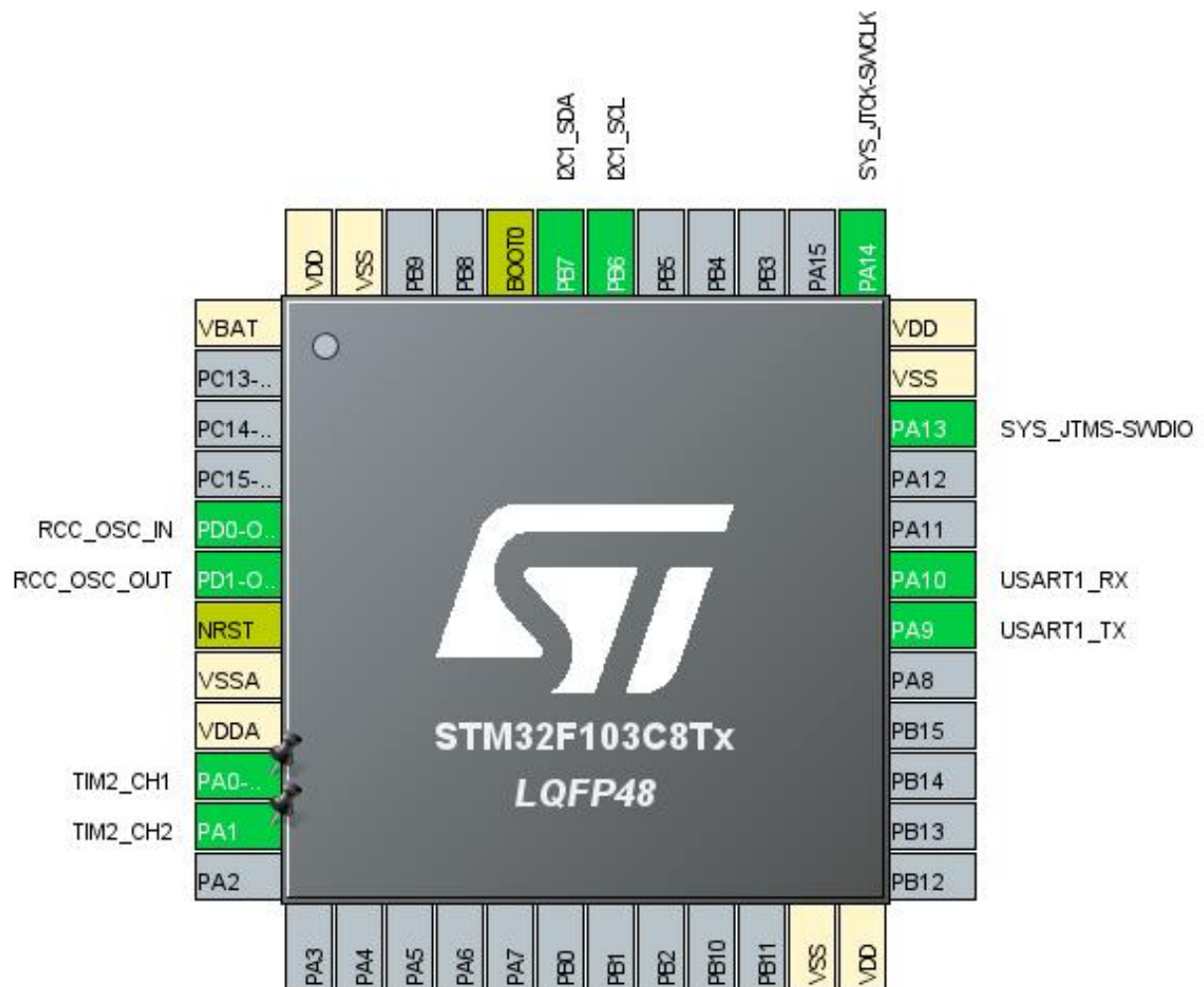
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M3
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	TIM2_CH1	
11	PA1	I/O	TIM2_CH2	
23	VSS	Power		
24	VDD	Power		
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
42	PB6	I/O	I2C1_SCL	
43	PB7	I/O	I2C1_SDA	
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Example project
Project Folder	D:\LERN_STM32\Example project
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_I2C1_Init	I2C1
5	MX_USART1_UART_Init	USART1
6	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	DS5319_Rev17

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

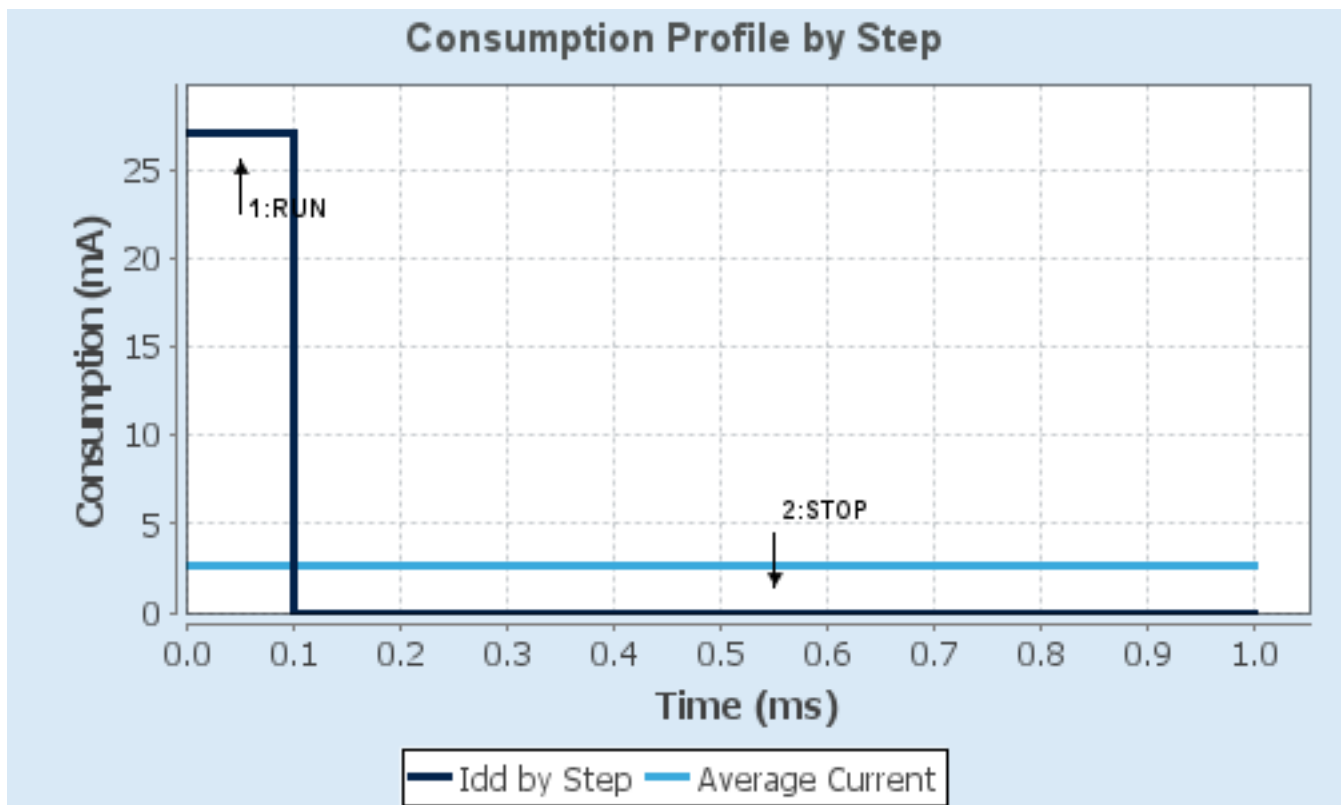
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 μ A
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days, 17 hours	Average DMIPS	61.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Master Features:

I2C Speed Mode	Fast Mode *
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	32767 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	32767 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.5. USART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
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Over Sampling

16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	n/a	High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	n/a	High *	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	n/a	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	n/a	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
USART1 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware				
System Core	Analog	Timers	Connectivity	Computing
DMA ✓		TIM2 ✓	I2C1 ✓	
GPIO ✓			USART1 ✓	
IVIC ✓				
RCC ✓				
SYS ✓				

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/CD00161566.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/CD00171190.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00228163.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00283419.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/CD00190234.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00164185.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167326.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00032987.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033267.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033344.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00052530.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00156964.pdf

Application note http://www.st.com/resource/en/application_note/DM00209695.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00296349.pdf

Application note http://www.st.com/resource/en/application_note/DM00325582.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

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