

ChipGPT: How far are we from natural language hardware design

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Abstract—As large language models (LLMs) like ChatGPT exhibited unprecedented machine intelligence, it also shows great performance in assisting hardware engineers to realize higher-efficiency logic design via natural language interaction. To estimate the potential of the hardware design process assisted by LLMs, this work attempts to demonstrate an automated design environment that explores LLMs to generate hardware logic designs from natural language specifications. To realize a more accessible and efficient chip development flow, we present a scalable four-stage zero-code logic design framework based on LLMs without retraining or finetuning. At first, the demo, ChipGPT, begins by generating prompts for the LLM, which then produces initial Verilog programs. Second, an output manager corrects and optimizes these programs before collecting them into the final design space. Eventually, ChipGPT will search through this space to select the optimal design under the target metrics. The evaluation sheds some light on whether LLMs can generate correct and complete hardware logic designs described by natural language for some specifications. It is shown that ChipGPT improves programmability, and controllability, and shows broader design optimization space compared to prior work and native LLMs alone.

Index Terms—agile hardware development, natural language programming, program synthesis

I. INTRODUCTION

While logic design plays an essential role in agile frontend chip design, existing manual methods require considerable effort and call for more agile development flow. In response, trends point toward higher-level programming interfaces like Scala and C to enhance design accessibility and efficiency. For example, Chisel[1] and Xilinx HLS[2] enable specification in common languages. However, it is believed that the ultimate goal is probably natural language logic design, where designers articulate requirements in simple sentences. This could revolutionize chip design by maximizing creativity and complexity at scale. Though still emerging, higher-level programming interfaces represent progress toward this vision.

To equip logic design with a higher programming interface, researchers in the program synthesis community provide methods that generate Verilog from formal representation[10, 11] and input-output pairs[12], such as Bony[9]. These intuitive approaches can release programmers from writing sophisticated programs. However, it still suffers from issues of correctness and completeness, to which the recent deep learning based code generation model reveals a proper solution. The input to these fundamental generative models is natural language, while the output is the target program. For example, one of SOTA models for this case is ChatGPT, which receives natural language input and potentially facilitates natural language programming.

While large language models (LLMs) show promise as universal generators, they face limitations in adapting to chip design. Their ambiguous input and output prevent seamless integration into electronic design automation (EDA) workflows. From an input perspective, prompt engineering for hardware description language (HDL) generation remains unrefined. First, LLMs lack prompt templates producing high-quality HDL code. Second, they cannot generate customized hardware modules or apply top-down design principles. From the output perspective, LLMs only generate raw programs which neither guarantee hardware-level correctness nor enable PPA exploration in the potential design space.

From the toolset perspective, large foundational models often run on cloud servers, preventing fine-tuning for logic design[13, 14]. To overcome the challenges and limitations above, we propose a natural language chip logic design method based on in-context learning, which does not modify the large model itself. As shown in Fig. 1, the core of our method is to put a prompt manager in front of the GPT model, which helps designers to improve the program quality by generating high-quality prompts. Secondly, to enable the PPA optimization process of design generation, we set an output manager behind GPT. The output manager corrects the initial programs through machine feedback and human feedback and then collects these raw programs into a potential program list. Afterward, an enumerative search stage is invoked to select the best design(*i.e.* with target PPA) from the generated program list. The evaluation results show that our framework can improve the average effect when dealing with exemplary design cases.

ChipGPT is an attempt that explores and estimates the feasibility of automatically generating logic design using natural language chip specification, and it makes use of current LLMs to ease the cost of hardware frontend design, which traditionally requires a high degree of expertise and manual labor. The contributions are listed below:

- We are the first to evaluate the ability of large language models(*i.e.* ChatGPT) to generate hardware logic design from natural language specification. To interface the LLM to hard-

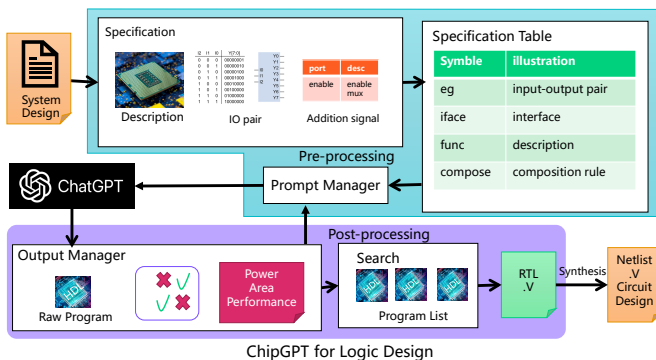


Fig. 1. Integration of our ChipGPT framework to chip design flow

TABLE I
AGILE CHIP DESIGN METHODS COMPARASION

	ChipGPT	HLS-CPP[3]	Chisel[1]	SuSy [3]	Spatial[4]	ScaleHLS[5]	TVM-VTA[6]	CIRCT[7]	XLS[8]	BoSy[9]
SD-Algorithm Simulation	Python/C++									
SD-System Design	Decomposed Document	Document	Document	Document	Document	Document/DL Model	DL Model	Document	Document	Document
SD-Specialize Field	General Digital IC	Algorithm for Digital IC	General Digital IC	Systolic Array	CGRA/FPGA	Algorithm for Digital IC/ DL Model	DL Model Accelerator	General Digital IC	General Digital IC	General Digital IC
Logic-Module Input	Prompt	C++/LLVM	Scala/FIRRTL	URE/Halide IR	Spatial-Scala	ONNX	ONNX	MLIR-Affine	Rust like	CTL Logic
Logic-Module Output	Verilog	Verilog	Verilog	HLS-C++	Verilog	Verilog	Pynq	Verilog	Verilog	Verilog
Logic verification					Verilator, ModelSIM					

ware designers, we also propose a scalable four-stage zero-code logic design framework based on GPT. This framework facilitates natural language-based chip design starting from the chip specification, thereby reducing manual design effort.

- To improve the quality of logic design, we are the first to propose a portable framework to generate Verilog program without retraining or modifying any weights in LLM(*e.g.* fine-tuning, adapter layer), which can be seamlessly integrated into the latest LLM APIs.
- We overcome the challenges brought by the power/area/performance agnostic LLMs on the chip design process through inserting a post-LLM search method with an efficient LLM output manager.
- Compared with previous agile chip logic design methods and the native ChatGPT, ChipGPT shows improvement in the programmability and scalability aspect, which shows potential to be extended to larger-scale chip design.

II. BACKGROUND AND MOTIVATION

A. Agile Hardware Design Workflow

Agile chip design approaches fall into two categories: programming language-based and program synthesis-based, as shown in Table II-A. Programming language-based methods aim to increase productivity by using higher-level languages[3]. For example, high-level synthesis (HLS) is the process of automatically generating a register-transfer level (RTL) hardware description from a high-level programming language(*e.g.* C/C++). Chisel is a Scala-embedded domain-specific language helping designers efficiently produce RTL code. However, these programming language-based agile chip design flows do not accept natural expression, which still needs hand-crafted design programming.

Program synthesis automatically generates computer programs from high-level descriptions like specifications, examples or input-output pairs. This enables faster, less error-prone program development than manual methods. Two approaches are inductive and deductive synthesis. Inductive synthesis uses input-output examples, iteratively refining a program to satisfy them[15], which is not always completely correct and rarely used in accurate hardware design. Another synthesis method is called deductive synthesis, also known as formal methods, and it is a process of synthesizing correct-by-construction hardware designs using mathematical models and formal verification techniques[9, 16]. This method has been used in Verilog generating(*e.g.* Bosy) in prior works. However, this process entails proving the correctness (soundness) of the design before implementation, thereby raising design difficulty. In general, these program synthesis-based agile workflows rely on the quality of complete examples provided or a formal specification that is hard to understand and learn.

To compare previous agile design methods with our trial of LLM-based natural language hardware design flow, ChipGPT, Tab. I lists several common agile chip design methods. Columns represent the

EDA workflow from system-level to logic design. First, algorithm simulation in Python or C++ checks design correctness. In the system design stage(*i.e.* 2th row), all methods follow design documents except TVM-VTA which uses a specialized deep learning model description format. The "specialized field"(*i.e.* 3th row) denotes whether a method is general purpose or domain-specific. In logic design, different input representations indicate unique productivities. Since the input of ChipGPT is natural language, ChipGPT is the most efficient representation compared with other methods.

TABLE II
THE DEVELOPMENT OF AGILE HARDWARE DESIGN

Agile Logic Design Method	Representative Works
Programming language based Hardware design	Chisel[1], Spatial[4], SuSy[3], ScaleHLS[5]
Program Synthesis based Hardware design	BoSy[9], Bounded Synthesis[16]

B. Agile Design Flow Comparison

To compare agile chip design productivity, we propose a 3D measurement space (Fig. 5). The first axis is soundness, indicating generated hardware description correctness. For example, BoSy uses formal methods, producing fully correct programs. ChatGPT generates correct programs probabilistically (prob-right). Methods like HLS and Chisel produce correct programs if rules are followed (rule-right). The second axis is completeness, denoting how much of the design space a method covers. For example, TVM-VTA generates domain-specific architectures (DSA generator), covering part of the space. General methods like HLS and Chisel can describe most logic structures (General HW Generators). The third axis is expressiveness, indicating input language productivity. For example, Verilog has RTL-level expression (Low RTL-level). HLS uses algorithmic languages like C (algorithm-level). ChatGPT and ChipGPT use natural language (highest expressiveness). The inputs of ChatGPT and ChipGPT are all-natural language descriptions, thus they are all at the highest expressiveness level.

C. Transfer learning

Large language models have become the foundation of code generation tasks, as Generative Pre-Trained Transformer (GPT) benefits from abundant global data (*ChatGPT*). It shows advantages in generating programs[17–20]. To apply large language models to the chip design field, we explore several common transfer learning methods(*i.e.* fine-tuning[21], adapter[22], lora[14], in-context learning[13]) and choose in-context learning as the final solution. This is because fine-tuning involves retraining pre-trained language model on task-specific data which is unrealistic since LLM serves in cloud and does not permit users' retraining. Adapter method and lora require additional layers to train, which requires repeatedly querying the LLM API, leading to inefficiency and cost. Therefore, in-context

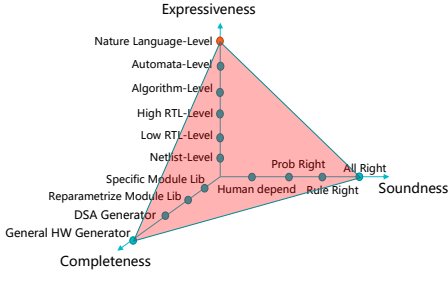


Fig. 2. Ideal Agile method productivity

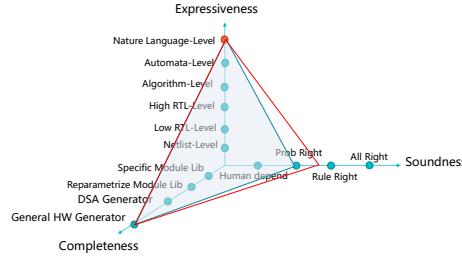


Fig. 3. ChipGPT productivity improvement

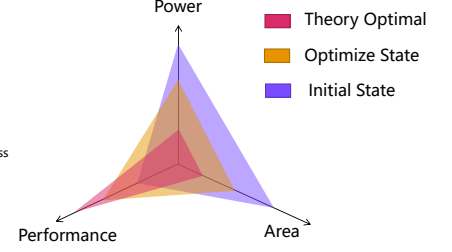


Fig. 4. ChipGPT design space exploration

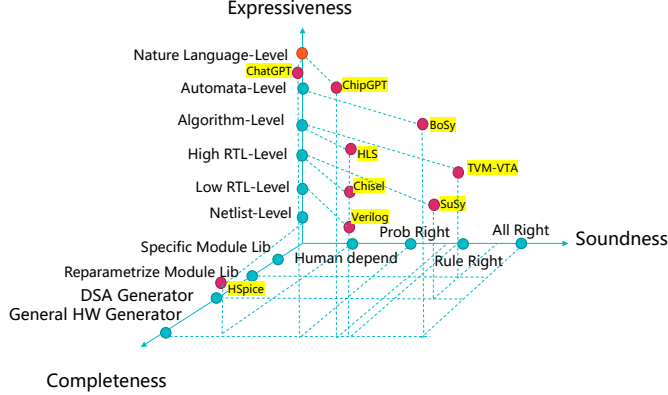


Fig. 5. Productivity Measurement of Agile Chip Design Method

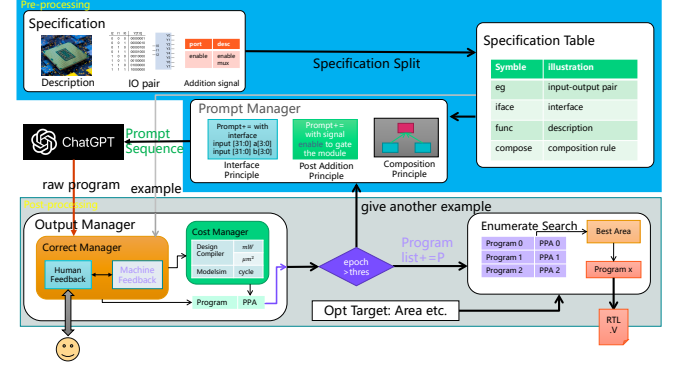


Fig. 6. The ChipGPT framework overview. Specification Split and Prompt Manager implicitly control the output (Pre-processing). Output Manager and Enumerative Search explicitly control the output (Post-processing).

learning appears as an emerging prompt tuning approach and is widely used in the natural language processing community.

In-context learning (ICL) elicits responses from a pre-trained LLM without retraining, directly predicting results based on prompts in natural language context. The key observation of ICL is that an LLM's responses depend on all preceding prompts. It incorporates a prompt manager generating prompts that guide the LLM's answers.[23]. The core of prompt manager is to generate prompts using templates, which follow several general design principles (e.g. chain-of-thought[24], least-to-most[25]). However, prompt managers differ across fields(e.g. Visual ChatGPT[26]) providing an opportunity for transfer learning in chip design.

D. Motivation

Emerging agile design workflows focus on EDA front-ends with higher-level representations. We analyzed current method productivity based on expressiveness, soundness and completeness (Sec. II-B). The ideal agile method is shown by the red triangle in Fig. 2. Ideal productivity requires: 1) Natural language expression for high abstraction and productivity. 2) A general hardware generator covering most of the design space. 3) Guaranteed correctness of all generated hardware descriptions.

Large language models (LLMs) enable natural language hardware descriptions, covering expressiveness (blue area, Fig. 3). However, LLM-generated programs may lack correctness (soundness). Enhancing correctness is key to applying LLMs for chip design, presenting three primary challenges:

a) **Challenge 1: LLM inputs are ambiguous, unable to directly integrate into chip design flows.** LLMs receive query sequences and output answer sequences. Producing HDL requires queries from specifications, which are complex with many module descriptions. Determining prompts eliciting a desired module is

difficult. Therefore, we propose a specification split method in Sec. III-A and template-based prompt manager III-B to overcome this challenge. These improve soundness from probable to nearly rule-right (red area, Fig. 3).

b) **Challenge 2: LLMs are unaware of power, area and performance (PPA), unable to generate ideal programs (red, Fig. 4).** As shown in Fig. 4, the ideal program PPA results are in the red area, but LLM-generated programs remain in the initial state (PPA-agnostic) due to their training. LLMs like InstructGPT and ChatGPT are trained using general reinforcement learning with a generic reward function to improve performance. This results in programs that are intuitively good but not optimized for PPA. Therefore, we propose an output manager in Sec. III-C to tackle this challenge and promote the PPA to the yellow area in Fig. 4.

c) **Challenge 3: It cannot expand to unlimitedly nested architecture.** LLM-generated programs consist of known modules, limiting scalability to generate top modules with customized submodules. Therefore, we propose a bottom-top method to overcome this challenge in Sec. III-B3.

III. AUTOMATIC CHIP GENERATION FRAMEWORK

ChipGPT serves as an EDA frontend framework, which aims to assist humans in compiling chip specifications to logic design. It takes chip specification as input and generates target hardware module description (i.e. Verilog program).

$$HDL = \text{ChipGPT}(\text{specification})$$

The chip specification defines the target of HDL implementation. Thus HDL should be controlled by chip specification. To control the generated HDL, there are three possible solutions in the GPT-based code generation workflow. 1) Control the context by customizing

configuration prompts(*i.e.* context). 2) Control the code query prompt by modifying the generated prompt. 3) Directly modify the generated program. Among them, 1) and 2) implicitly control output by changing the queries in the dialogue sequence S . 3) is an explicit control method via program analysis. Due to the GPT-produced program not always being accurate as well as challenging to analyze and modify, ChipGPT does not attempt to amend the generated raw program directly. Rather, it gives GPT several times of trials to generate different code versions and refine them to obtain the final output. The workflow under this design consideration is shown in Fig. 6. Specification Split and Prompt Manager implicitly control the output. Output Manager and Enumerate Search explicitly control the output.

At each iteration, ChipGPT follows these steps. At first, pre-processing occurs before the GPT model is invoked to handle descriptive and irregular information (*e.g.* the function of a module and interface descriptions). Post-processing then takes place after the GPT model. The output manager and search modules are used in post-processing to address design constraints (*e.g.* regardless of whether the raw program is correct, ChipGPT will select a version with optimized power, performance, and area).

$$\begin{aligned}
 split(spec) &= \{eg, iface, func, compose\} \\
 rawcode &= GPT(PM(iface, func, compose, fd)) \\
 code &= OM(rawcode, EM) \\
 codelist &= codelist \cup code \\
 optcode &= Search(codelist, requirements)
 \end{aligned}$$

First, to translate the specifications into a formal and unambiguous form, we propose a specification split method.

Second, to make these irregular split partitions become an available GPT input sequence, we propose a specification serialization method in PM .

Third, to improve the quality of the $code$ (raw program) generated by the GPT model, we propose an output manager OM .

Finally, the code generated in the third stage typically does not meet performance, power and area (PPA) requirements. To obtain an optimized final output program for PPA, we propose a search method compatible with the previous stages that ranks GPT-generated programs and identifies the version according to the *requirements*.

A. Specification Split

A comprehensive chip logic design specification typically comprises module, test and interface descriptions that provide the necessary information to translate into functionally verified hardware implementations. To enable hardware developers to precisely understand module functionality, specifications often provide input-output examples for the interfaces.

Based on the above specification definitions, we manually divide the specification into four parts (*i.e.* module descriptions, test descriptions, interface descriptions, input-output examples). We discard any other extraneous parts of the specifications.

$$split(spec) = \{eg, iface, func, compose\} \quad (1)$$

eg represents examples within the module specifications. This information is often provided in tables where each row lists inputs and outputs within a clock cycle. ChipGPT does not take eg as the prompt input, for the reason that this information is too complicated to fit the transformer model. Rather, we handle it in the post-processing step. The Output manager leverages this information to verify module correctness, reducing the need for manual human correction.

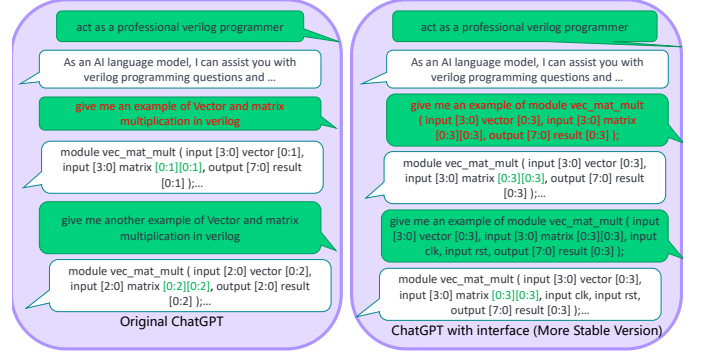


Fig. 7. An observation of interface principle in prompt manager

$iface$ represents the input and output ports definition.

$func$ represents the function of the module, which is the most crucial part of the ChipGPT workflow. The module function defines its core purpose and behavior.

$compose$ delineates how to compose the module, as designated when the module comprises the top level of the design.

B. Prompt Manager PM

Due to the context-aware feature of GPT, the prompt manager directly determines the quality of the generated code.

The goal of the prompt manager is to serialize natural language software specifications into a structured prompt format. By formatting the specifications this way, the prompts can serve as input for GPT. With well-designed prompts, GPT can produce code that successfully captures the details and purpose of the original specifications.

$$arch = \langle setup, submodule^N, compose \rangle \quad (2)$$

$$submodule = \langle \{funcdesc, iface\}, addition \rangle \quad (3)$$

To improve prompt quality, we design a template-based prompt manager where prompts are interconnected within templates. We first provide a formal representation for the prompt manager. Let $S = \{(Q_1, A_1), (Q_2, A_2), \dots, (Q_N, A_N)\}$ denote a dialogue sequence with N question-answer pairs. GPT takes queries as input and generates the final answer. We define $arch$ in Equ. 2 as a query sequence, or prompt sequence illustrated in Fig. 6. The query sequence comprises three partitions. Elements enclosed in $\langle \rangle$ represent a sequence of prompts, while elements in $\{ \}$ represent groups combined into a single prompt. The first setup prompt $\langle act as a proficient Verilog programmer \rangle$ establishes an execution environment enabling the following queries to operate in a Verilog context. Next, for the basic modules in the specification, GPT generates N modules following the interface model principle in III-B1 and post-addition principle in III-B2. Finally, there is a top module following the $compose$ rule that connects these submodules from the second step. This composition adheres to the module composition principle in III-B3.

1) *Principle for Interface Model*: An intuitive approach for generating Verilog programs is to specify the module function as the prompt only. However, omitting the module interface declaration from the prompt makes the GPT ignore chip port specifications, where the generated module cannot be integrated seamlessly into the testbench environment. Moreover, including the interface declaration within the prompt defines attributes like bit widths and array sizes that are essential for generating high-quality internal module code. This enhanced context enables GPT to produce consistent versions with the same interface, as depicted in Fig. 7.

To introduce the interface-based model principle into our template-based prompt manager PM , we examine current port definitions in specifications and hardware description languages (HDLs), such as Verilog. Port definitions comprise five elements: 1. Direction (D): Whether the port is input, output, or inout 2. Data width (W): The bit width of the port (e.g. 32 bits) 3. Variable name (VN): The name given to the port (e.g. instruction) 4. Array size (S): The number of elements in an array port 5. Port description (PD): A text description of the port's purpose.

$$iface = \{D, W, VN, S, PD\}$$

Among the port definition elements, the variable name (VN) is particularly important. Because GPT is a variable name-aware model, the names given to ports help the model infer the appropriate program structure.

No Post-Addition Principle	Post-Addition Principle
Prompt: Give me an example of on chip network with ready and valid signal	Prompt 1: Give me an example of on chip network Prompt 2: add ready and valid signal
<pre>module network(input clk, input [7:0] data_in, input valid_in, output ready_in, output [7:0] data_out, output valid_out, input ready_out); // valid is not a output signal ... (Ignore the implementation)</pre>	<pre>module network(input clk, input rst, input [4:0] src_addr, input [4:0] dst_addr, input [7:0] data, input ready, output [7:0] data_out, output valid); ... (Ignore the implementation)</pre>
	Correct

Fig. 8. An example of post-addition Principle in LLM[27].

2) *Post Addition Principle*: In a production environment, multiple cross-module handshake signals are often added to existing modules (e.g. ready-valid mode). However, composing handshake signals directly into the interface prompt reduces the accuracy of the generated raw program. GPT struggles to well understand programs created this way. The reason is that LLM's reward model always selects the highest-ranked raw program version based on both the handshake and function. It considers the weights of the handshake and function together. However, programmers prioritize function correctness.

Based on the above observations, we place additional information such as cross-module handshake signal declarations after generating the first raw program in Equ. 3. Because this supplemental information is added following the primary module details, we call this the "post-addition principle". For example, in Fig. 8, we show the effectiveness of the post-addition principle. In the left column, the handshake signals are added to the same prompt. As a result, the language model generates an incorrect implementation where valid cannot be an output port. The right column implements the post-addition principle, where the implementation is correct.

3) *Module Composition Principle*: An architecture-level chip specification includes not only component modules but also a top module to connect them. To gain a high-level overview, chip designers typically take a top-down design approach. However, if we prompt GPT to generate the top-level module directly, it lacks information about the submodules it should reference.

Based on this observation, we propose the "bottom-up composition principle" to improve the quality of the generated raw program, which is similar to least-to most principle[25]. As shown in Equation 4, this principle specifies that **submodule interfaces must be declared before the top module**. For example, < the submodule has interface ... > followed by < the top module consists of ... >. By following this sequence, when GPT generates the top module, the submodules' ports are clearly defined. As a result, GPT can connect them appropriately. Because this principle is recursive, it can be applied to a wide

No Composition Principle	Composition Principle
Prompt: Define top module and the two number add module output through FIFO to a two number minus module, where the input of minus module are two FIFO connect to two add modules. <pre>module add_module(input clk, input reset, input [31:0] a, input [31:0] b, output [31:0] sum); // Note: This is unimplement endmodule module minus_module(input clk, input reset, input [31:0] a, input [31:0] b, output [31:0] diff); // Note: This is unimplement endmodule // The top module</pre>	Prompt 1: Define minus module as a module to subtract two numbers. Prompt 2: Define add module as a module to add two numbers. Prompt 3: Define top module and the three numbers add module output through FIFO to a two number minus module, where the input of minus module are two FIFO connect to two add modules. <pre>module add_module(input clk, input reset, input [31:0] a, input [31:0] b, output [31:0] sum); reg [31:0] add; always @(posedge clk) begin if (reset) begin add <= 0; end else begin add <= a + b; end end assign sum = add; endmodule module minus_module(input clk, input reset, input [31:0] a, input [31:0] b, output [31:0] diff); reg [31:0] sub; always @(posedge clk) begin if (reset) begin sub <= 0; end else begin sub <= a - b; end end assign diff = sub; endmodule // The top module is the same as left</pre>

Fig. 9. An example of composition principle in LLM[27].

range of architectural design scenarios. For example, in Fig. 9, we want to design a complex module. On the left, the add module and minus module are defined in the same prompt, where the LLM cannot output the correct implementation of the submodules. However, when applying the composition principle, the LLM can generate correct implementations of the submodules.

$$compose : submodule^N \longrightarrow topmodule \quad (4)$$

C. Output Manager OM

The programs GPT generates (referred to as "raw" programs) may not adhere to specifications. To address this issue, an additional correct model is needed to improve accuracy. A cost model can then optimize the raw program for power, performance, area (PPA) and other metrics based on human-specified targets. The workflow incorporating these models is as follows:

$$OM = Correct \hookrightarrow Cost \quad (5)$$

1) *Correction Manager*: In order to correct raw program output from GPT, programmers often fix them manually. However, we found the examples provided in the specification facilitate machine-based feedback. Thus we propose a two-stage correction manager. The first stage is to use a compiler and simulator to check its correctness. If the machine feedback is correct, then the program does not need human feedback. The second stage is to manually check the raw program. After these steps, the raw program is corrected.

$$Correct = Machine_correct \hookrightarrow Human_correct \quad (6)$$

a) *Machine Feedback*: Machine feedback checks the correctness of the raw program generated by GPT. We can use machine feedback models because specifications provide sound examples (the examples are guaranteed to be correct).

$$Machine_correct = simulator(synthesis(raw), eg) \quad (7)$$

Raw programs and the corresponding examples are fed into the simulator to test if modules are functional right.

b) *Human Feedback*: Human feedback follows machine feedback for two reasons. First, the machine feedback stage may become stuck at a compile error it cannot address. Second, the examples provided by only the machine feedback stage are not complete. Due to the above observations, programmers need to correct the program manually. Note that this stage serves as an auxiliary for the composition principle to reduce incorrect generation errors. However, it has little effect within the ChipGPT automatic framework discussed further in Section IV regarding Research Question 5.

<pre> module matrix_multiplier (input signed [15:0] A [0:3][0:3], input signed [15:0] B [0:3][0:3], output reg signed [31:0] C [0:3][0:3]; integer i, j, k; always @ (*) begin for (i = 0; i < 4; i = i + 1) begin for (j = 0; j < 4; j = j + 1) begin C[i][j] = 0; for (k = 0; k < 4; k = k + 1) begin C[i][j] = C[i][j] + A[i][k] * B[k][j]; end end end end endmodule </pre>			
Power:	105.2380	Area	179679.995125
<pre> module matrix_multiplier (input signed [15:0] A [0:3][0:3], input signed [15:0] B [0:3][0:3], input clk, output reg signed [31:0] C [0:3][0:3]; reg signed [31:0] M [0:3][0:3]; always@(posedge clk) begin for (i = 0; i < 4; i = i + 1) begin for (j = 0; j < 4; j = j + 1) begin M[i][j] <= A[i][0] * B[0][j] + A[i][1] * B[1][j] + A[i][2] * B[2][j] + A[i][3] * B[3][j]; end end end end endmodule </pre>			
Power:	122.3770	Area	198511.994667
<pre> module matrix_multiplier (input [15:0] A [0:3][0:3], input [15:0] B [0:3][0:3], output [31:0] C [0:3][0:3]; wire [31:0] P [0:15]; assign P[0] = {A[0][0], A[0][1]} * {B[0][0], B[1][0]}; assign C[0][0] = P[0][15:8] + P[8][15:8] + P[4][15:8] + P[12][15:8]; endmodule </pre>			
Power:	13.1363	Area	21743.999433

Fig. 10. Matrix Multiply Verilog Program list, where power is measured in milliwatts (mW), area is measured in micrometers squared (μm^2)

TABLE III
CHATGPT PROGRAM RANKING MODEL ON BUTTON COUNT DESCRIPTION

Program	Power (mW)	Area (μm^2)	Latency (Cycle)	Rank Model
Raw Program 0	4.2900e-02	139.199999	1	5
Raw Program 1	1.3593e-02	265.200006	1	4
Raw Program 2	1.0704e-02	193.600004	1	3
Raw Program 3	9.7253e-03	187.200004	1	2
Raw Program 4	1.0283e-02	196.000003	1	1

2) *Cost Manager*: As discussed in Section II-D, power, performance, and area (PPA) are crucial metrics in chip logic design. However, GPT lacks comparable PPA configurations. In GPT model, the reward model only provides general ranking. Therefore, ChipGPT proposes a cost manager to optimize PPA following the GPT model.

This stage uses design tools to test the PPA of each program, appending the results to the program list (Equ. 8) until it completes an enumerated search to select the target version. For example, in Fig. 10, GPT generates different versions, they have different PPAs. Therefore, the cost manager tries to use EDA tools to output their PPAs and search for the optimal one.

D. Enumerative Search

The key question is whether the search stage is necessary. As shown in Table III-D, the GPT model's ranking does not consistently match the PPA rank. For example, searching the button count module programs produces the results in Table III-D. This shows that if we choose different targets, the selected final program depends highly on the chosen target, as highlighted in yellow. Therefore, adding a search algorithm to the output manager is necessary. We use design space exploration to obtain better results from the program list. The

TABLE IV
SEARCH RESULT

Select by Power	Select by Area	Select by Performance	Direct Select
P3	P0	P0	P4
P4	P3	P1	P1
P2	P2	P2	P2
P1	P4	P3	P3
P0	P1	P4	P4

number of correct programs GPT generates is limited, typically less than 10. As a result, we use enumerate search to select the optimal result.

$$program_list = \{\{p_1, PPA_1\}, \dots, \{p_n, PPA_n\}\} \quad (8)$$

where p denotes a program. Enumerate search selects the best program in the program list of performance, area and power, which relies on the programmers' target.

IV. EVALUATION

To explore the LLM ability in natural language hardware design and evaluate our method's effectiveness, we list several key questions below(RQ) and try to answer them with proofs.

a) *RQ1*: Compare with other agile developing method(e.g. Chisel, HLS), what advantages do natural language based method have?

b) *RQ2*: Does our method(ChipGPT) takes effect compare with original ChatGPT in both PPA results and programmability perspective?

c) *RQ3*: Does our framework sensitive to workloads?

d) *RQ4*: Does the prompt principles (i.e. ablation study of composition module, interface model, and post-addition principle) really take effect to enhance the soundness(i.e. code quality) of our method?

e) *RQ5*: To automate the design flow, does the human feedback really takes a heavy effect on our LLM-based framework?

A. Experimental Setup

1) *Experimental Environment*: We use the ChatGPT model from OpenAI's website, which is a GPT-3.5 model. The raw programs of input are in SystemVerilog format. We use Design Compiler and 65nm technology to evaluate the power and area of output designs. The performance cycle numbers of the designs produced through different approaches are obtained by simulation with common hand-written testbeds. For line of code measurement, the cloc tool is used.

2) *Programmability measurement*: Traditional programmability evaluation in EDA uses lines of code (LOC) as the measurement metric[1]. This LOC subtraction method cannot directly measure natural language code generation for two reasons: 1) The LOC of natural language is undefined. 2) Natural language-based zero-code programming frameworks use neural networks, which cannot ensure output programs strictly follow specifications. To address these challenges, we define LOC subtraction as Equation 9 to evaluate GPT code generation under the prompt manager:

$$quality = raw + correct - prompt \quad (9)$$

Where $quality$ represents code generation algorithm efficiency, raw is the number of lines in the generated program, $correct$ is the number of lines modified by humans to correct the raw program, and $prompt$ is the number of prompt queries.

TABLE V
WORKLOAD DETAIL

Workload	Type	Brief Illustration
matmul	CSM	Multiplying two matrices 4x4 with 16 bits
mux	SSM	A 4x1 Multiplexer
3-8decoder	SSM	Select one of the eight lines in a 3-to-8 decoder
button	CSM	Counts the number of button presses
vecmat	CSM	Vector matrix multiply with 4-bits element
addmulti tree	CM	Add multiply tree with 8-bit operand
accumulator	CSM	Sum an array of 8-bits elements
simple CPU	CM	A simple CPU implementation

3) *Benchmarks*: The benchmarks include several typical hardware structures and algorithm accelerator implementations as shown in Table IV-A3. Simple CPU implements the instruction set in Tab. IV-A3. GPT exhibits different performance on different workloads. Therefore, we classify them into three parts based on complexity: 1) Composition (CM): The most complex architecture, requiring module composition. 2) Complex single module (CSM): More complex individual modules. 3) Simple single module (SSM): The simplest modules, with identical program lists and PPA.

4) *Baseline*: To validate our workflow works with ChatGPT, we compare it to the baseline ChatGPT model. The naive code ChatGPT generates uses only the module description as the prompt. To analyze improvement over traditional agile workflows, we compare with Chisel and high-level synthesis (Xilinx Vivado HLS). **For a fair comparison, 1) we add unroll directive to pipeline the HLS design and used Synopsys Design Compiler to measure power and area, as with our approach. 2) The HLS and Chisel implementations follow the same specification and were developed by the same 2-year graduate student and evaluated with a coverage identical testbed suite.**

Vector Multiply (Version 1)	Vector Multiply (Version 2)	Vector Multiply (Version 3)
<pre> module vec_mat_mult { input [3:0] vector [0:3], input [3:0] matrix [0:3][0:3], input clk, input rst, output [7:0] result [0:3] }; --(ignore) reg [7:0] temp_result [0:3]; reg signed [1:0] temp_result; temp_result <= 0; temp_result[i] <= temp_result[i] + vector[j] * matrix[j][i]; end //result[i] <= temp_result[i];delete endmodule temp_result; endmodule </pre>	<pre> module vec_mat_mult { input [3:0] vector [0:3], input [3:0] matrix [0:3][0:3], input clk, input rst, output [7:0] result [0:3] }; reg [7:0] temp [0:3]; integer i, j; always @(posedge clk, posedge rst) begin if (rst) begin for (i = 0; i < 4; i = i + 1) temp[i] <= 0; end else begin --(ignore) temp[i] <= temp[i] + vector[j] * matrix[j][i]; end end end endmodule assign result = temp; endmodule </pre>	<pre> module vec_mat_mult{ input [3:0] vector [0:3], input [3:0] matrix [0:3][0:3], input clk, input rst, output [7:0] result [0:3] }; reg [7:0] temp [0:3]; reg signed [1:0] temp; temp <= 0; always @(posedge clk) begin if (rst) begin temp <= {8'h0, 8'h0, 8'h0, 8'h0}; end else begin temp[0] <= vector[0] * matrix[0][0] + vector[1] * matrix[1][0] + vector[2] * matrix[2][0] + vector[3] * matrix[3][0]; --(ignore) end end endmodule assign result = temp; endmodule </pre>

Fig. 11. Human Correct Implementation of Vector Multiply

B. Experimental Results

To answer the above questions, we analyze our framework under different workloads. Tab. IV-A4 shows the power, performance, and area (PPA) results compared to other agile methods when optimizing for the area. As the HLS compiler prefers to use state machines rather than pipeline for scheduling, sometimes resulting in areas smaller than the Chisel counterparts and also longer latencies than that of Chisel. The static power consumption is directly related to the total area. For example, in the matrix multiplication workload, our HLS solution has lower area and power consumption compared to Chisel, but exhibits much higher latency.

We found several interesting findings during our generation process, which helps us understand natural language digital design

deeply. These findings and insights provide answers to our five research questions.

Finding 1: Natural language methods could achieve higher programmability than conventional agile hardware design techniques. (Answer RQ1)

Evidence: Fig. 12 compares the number of code lines generated for the same designs by our language model ChipGPT, high-level synthesis (HLS) tools, and the Chisel hardware design framework. On average, ChipGPT decreased the code volume by 9.25 times compared to HLS and 5.32 times compared to Chisel. This substantial reduction clearly demonstrates the enhanced programmability enabled by natural language techniques.

Finding 2: Our four-stage framework optimizes PPA metrics while also improving code quality versus the original ChatGPT model. (Answer RQ2)

Evidence: Fig. 13 illustrates the improved program generation efficiency enabled by our framework under the programmability metrics defined in Sec. IV-A2. Maximum quality improvement corresponds to a 2.01 times reduction in the number of incorrect code lines required, demonstrating a more compact, higher-quality final design.

Finding 3: Our framework improves program quality across workloads while also primarily optimizing PPA for complicated designs. On simple workloads, it shows limited PPA benefits due to the small pool of raw candidates and lack of opportunity for optimization. (Answer RQ3)

Evidence: Fig. 13 demonstrates our framework brings program generation quality improvement to all the evaluated workloads. However, Tab. IV-A4 shows that for simple (SSM) workload, PPA results exhibit no significant optimization relative to the baseline, as the limited number of raw program candidates provides little room for improvement. In contrast, for complex workloads like the CMS and CM tasks, our framework's targeted optimization at the search stage reduced average area by 47% (0.53x) and overall average area by 35% (0.65x) compared to the original ChatGPT model. By jointly optimizing PPA objectives and program coherence for complex designs with ample raw candidates, our framework achieved substantial optimization.

Finding 4: Our composition, interface, and post-addition principles improve raw program coherence with natural language specifications, enabling high code quality at a large scale. (Answer RQ4)

Evidence: Fig. 13 show that a 2.01× average increase in code quality is brought by the three principles in the prompt manager to our framework. They can enhance single-module generation quality and consistency for complex, large-scale designs.

Finding 5: Our framework requires minimal human feedback for module generation and single large-scale modules due to the effect of prompt management principles. (Answer RQ5)

Evidence: Fig. 14 shows less than 10 lines of code needing correction for all workloads. Simple modules like the 4x1 multiplexer required no feedback, demonstrating autonomous generation. For complex modules and integrated accelerators up to 100 lines of code, only minor corrections were needed. For some cases, fewer than 10

TABLE VI
SIMPLE CPU ISA IMPLEMENTATION

Instruction	Description	Opcode	Bit Function	Opcode length(bit)
Computing Instructions				
add	Add reg[op2] to reg[op1]	00000	12b'x+5bop1+5b'op2+10b'x	32
mul	Mul reg[op2] to reg[op1]	00001	12b'x+5bop1+5b'op2+10b'x	32
cmp	Determine the equality of reg[op1] and reg[op2].	00011	12b'x+5bop1+5b'op2+10b'x	32
Control Instructions				
beq	Determine if reg[op1] is greater than or equal to reg[op2].	00100	12b'x+5bop1+5b'op2+10b'x	32
ble	Determine if reg[op1] is less than or equal to reg[op2]	00101	12b'x+5bop1+5b'op2+10b'x	32
blt	Determine if reg[op1] is less than reg[op2].	00110	12b'x+5bop1+5b'op2+10b'x	32
bge	Determine if reg[op1] is greater than or equal to reg[op2].	00111	12b'x+5bop1+5b'op2+10b'x	32
br	PC Jump to reg[31:0]	00010	32b'M	32
Memory Instructions				
store	Store data_in to reg[op1].	01000	12b'x+5bop1+15b'x	32
load	Load the value from reg[op1] into data_out.	01001	12b'x+5bop1+15b'x	32

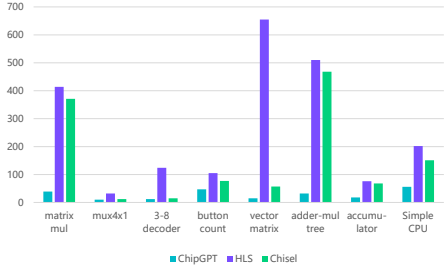


Fig. 12. Generated code line number

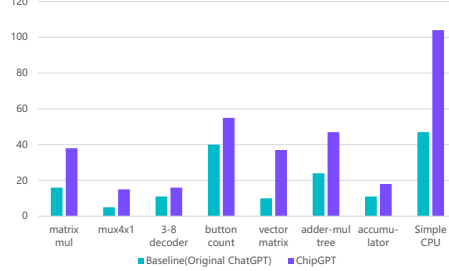


Fig. 13. Code quality

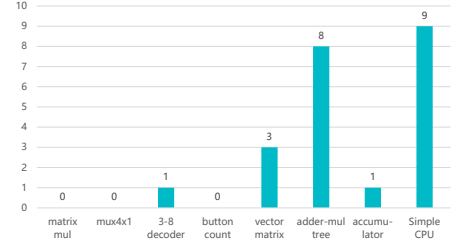


Fig. 14. Human correction effort measured in line number of code

TABLE VII

PPA COMPARISON TO SHOW THE EFFICIENCY OF OUR METHOD UNDER THE AREA OPTIMIZATION TARGET, WHERE POWER IS MEASURED IN MILLIWATTS (mW), AREA IS MEASURED IN MICROMETERS SQUARED (μm^2) AND LATENCY MEASURES THE NUMBER OF RUNNING CYCLES

Workload	Configuration	Power	Area	Latency
matrix mul	ChatGPT(Baseline)	105.24	179680.0	1
	HLS	0.1946	2592.79	169
	Chisel	28.5361	55983.6	1
	Ours(ChipGPT)	13.14	952.4	1
mux4x1	ChatGPT(Baseline)	2.62E-03	11.2	1
	HLS	2.62E-03	11.2	1
	Chisel	2.62E-03	11.2	1
	Ours(ChipGPT)	2.62E-03	11.2	1
3-8decoder	ChatGPT(Baseline)	2.60E-03	22.8	1
	HLS	7.03E-03	156.4	9
	Chisel	3.27E-03	24.4	1
	Ours(ChipGPT)	2.60E-03	22.8	1
button-count	ChatGPT(Baseline)	0.01	265.2	1
	HLS	7.80E-03	200.4	9
	Chisel	8.34E-03	146.8	1
	Ours(ChipGPT)	4.29E-02	139.2	1
vector-matrix	ChatGPT(Baseline)	1.30	3451.2	2
	HLS	0.03	428.8	191
	Chisel	1.27	3400.0	1
	Ours(ChipGPT)	1.15	3144.0	1
adder-multi tree	ChatGPT(Baseline)	28.50	60070.4	1
	HLS	0.09	1784.4	73
	Chisel	28.54	55983.6	1
	Ours(ChipGPT)	27.79	50498.8	1
accumulator	ChatGPT(Baseline)	0.02	174.0	1
	HLS	1.10E-02	204.0	17
	Chisel	2.57E-02	136.4	1
	Ours(ChipGPT)	0.03	136.0	1
Simple CPU	ChatGPT(Baseline)	2.57	23138.4	5
	HLS	0.10	2780.0	38
	Chisel	1.48	25346.0	3
	Ours(ChipGPT)	0.48	3240.8	5

lines of code need to be corrected. As an example, we analyze the vector matrix multiplication in Figure 11. The lines highlighted in blue indicate incorrect code that requires correction. The comments following these highlighted lines provide the appropriate fixes to yield the correct implementation. In each program, the number of highlighted lines that require corrections is fewer than three.

V. CONCLUSION

This paper explores natural language hardware design and proposes ChipGPT, a framework that uses natural language specifications for automatic chip logic design. It integrates language models into EDA tools without retraining. This could enable natural language chip design flows, reducing code volume by 5.32-9.25 compared to traditional agile methods. By harnessing language, ChipGPT significantly accelerates chip development. ChipGPT is an interface for GPT to address natural language hardware design and PPA optimization, which has an area reduction of 47% compared with the original ChatGPT in area target optimization mode. It also improves the correctness of LLM from probable right to rule right.

REFERENCES

- [1] J. Bachrach, H. Vo, B. Richards, Y. Lee, A. Waterman, R. Avižienis, J. Wawrzynek, and K. Asanović, "Chisel: constructing hardware in a scala embedded language," *Design Automation Conference*, pp. 1216–1225, 2012.
- [2] G. Martin and G. Smith, "High-level synthesis: Past, present, and future," *IEEE Design & Test of Computers*, vol. 26, no. 4, pp. 18–25, 2009.
- [3] Y.-H. Lai, H. Rong, S. Zheng, W. Zhang, X. Cui, Y. Jia, J. Wang, B. Sullivan, Z. Zhang, Y. Liang, *et al.*, "Susy: A programming model for productive construction of high-performance systolic arrays on fpgas," *International Conference on Computer-Aided Design*, pp. 1–9, 2020.

- [4] D. Koeplinger, M. Feldman, R. Prabhakar, Y. Zhang, S. Hadjis, R. Fiszal, T. Zhao, L. Nardi, A. Pedram, C. Kozyrakis, and K. Olukotun, "Spatial: A language and compiler for application accelerators," *SIGPLAN Not.*, vol. 53, p. 296–311, jun 2018.
- [5] H. Ye, C. Hao, J. Cheng, H. Jeong, J. Huang, S. Neuendorffer, and D. Chen, "Scalehls: A new scalable high-level synthesis framework on multi-level intermediate representation," *IEEE International Symposium on High-Performance Computer Architecture*, pp. 741–755, 2022.
- [6] T. Chen, T. Moreau, Z. Jiang, L. Zheng, E. Yan, H. Shen, M. Cowan, L. Wang, Y. Hu, L. Ceze, C. Guestrin, and A. Krishnamurthy, "TVM: An automated End-to-End optimizing compiler for deep learning," *USENIX Symposium on Operating Systems Design and Implementation*, pp. 578–594, 2018.
- [7] L. community, "Circuit ir compilers and tools." <https://github.com/lvm/circt>, 2023.
- [8] A. Magyar, A. Kalantar, B. Christian, Blaok, and B. J. et al., "Xls: Accelerated hw synthesis." <https://github.com/google/xls/>, 2023.
- [9] P. Faymonville, B. Finkbeiner, and L. Tentrup, "Bosy: An experimentation framework for bounded synthesis," *Computer Aided Verification: 29th International Conference*, pp. 325–332, 2017.
- [10] P.-M. Osera and S. Zdancewic, "Type-and-example-directed program synthesis," *SIGPLAN Not.*, vol. 50, p. 619–630, jun 2015.
- [11] Z. Manna and R. Waldinger, "Synthesis: Dreams \rightarrow programs," *IEEE Transactions on Software Engineering*, vol. SE-5, no. 4, pp. 294–328, 1979.
- [12] R. Alur, R. Bodik, G. Juniwal, M. M. K. Martin, M. Raghothaman, S. A. Seshia, R. Singh, A. Solar-Lezama, E. Torlak, and A. Udupa, "Syntax-guided synthesis," *Formal Methods in Computer-Aided Design*, pp. 1–8, 2013.
- [13] Q. Dong, L. Li, D. Dai, C. Zheng, Z. Wu, B. Chang, X. Sun, J. Xu, and Z. Sui, "A survey for in-context learning," *arXiv preprint arXiv:2301.00234*, 2022.
- [14] E. J. Hu, yelong shen, P. Wallis, Z. Allen-Zhu, Y. Li, S. Wang, L. Wang, and W. Chen, "LoRA: Low-rank adaptation of large language models," *International Conference on Learning Representations*, pp. 1–13, 2022.
- [15] J. K. Feser, S. Chaudhuri, and I. Dillig, "Synthesizing data structure transformations from input-output examples," *ACM SIGPLAN Conference on Programming Language Design and Implementation*, p. 229–239, 2015.
- [16] B. Finkbeiner and S. Schewe, "Bounded synthesis," *International Journal on Software Tools for Technology Transfer*, vol. 15, p. 519–539, oct 2013.
- [17] Z. Feng, D. Guo, D. Tang, N. Duan, X. Feng, M. Gong, L. Shou, B. Qin, T. Liu, D. Jiang, et al., "Codebert: A pre-trained model for programming and natural languages," *Conference on Empirical Methods in Natural Language Processing*, pp. 1536–1547, 2020.
- [18] Y. Wang, W. Wang, S. Joty, and S. C. Hoi, "Codet5: Identifier-aware unified pre-trained encoder-decoder models for code understanding and generation," *Conference on Empirical Methods in Natural Language Processing*, pp. 8696–8708, 2021.
- [19] D. Guo, S. Ren, S. Lu, Z. Feng, D. Tang, S. LIU, L. Zhou, N. Duan, A. Svyatkovskiy, S. Fu, M. Tufano, S. K. Deng, C. Clement, D. Drain, N. Sundaresan, J. Yin, D. Jiang, and M. Zhou, "Graphcodebert: Pre-training code representations with data flow," *International Conference on Learning Representations*, pp. 1–18, 2021.
- [20] D. Guo, S. Lu, N. Duan, Y. Wang, M. Zhou, and J. Yin, "Unixcoder: Unified cross-modal pre-training for code representation," *Annual Meeting of the Association for Computational Linguistics*, pp. 7212–7225, 2022.
- [21] J. Yosinski, J. Clune, Y. Bengio, and H. Lipson, "How transferable are features in deep neural networks?," *Advances in neural information processing systems*, vol. 27, pp. 1–9, 2014.
- [22] N. Houlsby, A. Giurghi, S. Jastrzebski, B. Morrone, Q. De Laroussilhe, A. Gesmundo, M. Attariyan, and S. Gelly, "Parameter-efficient transfer learning for nlp," *International Conference on Machine Learning*, pp. 2790–2799, 2019.
- [23] Y. Zhou, A. I. Muresanu, Z. Han, K. Paster, S. Pitis, H. Chan, and J. Ba, "Large language models are human-level prompt engineers," *International Conference on Learning Representations*, pp. 1–43, 2023.
- [24] J. Wei, X. Wang, D. Schuurmans, M. Bosma, brian ichter, F. Xia, E. H. Chi, Q. V. Le, and D. Zhou, "Chain of thought prompting elicits reasoning in large language models," *Advances in Neural Information Processing Systems*, pp. 1–14, 2022.
- [25] D. Zhou, N. Schärli, L. Hou, J. Wei, N. Scales, X. Wang, D. Schuurmans, C. Cui, O. Bousquet, Q. V. Le, and E. H. Chi, "Least-to-most prompting enables complex reasoning in large language models," *International Conference on Learning Representations*, pp. 1–61, 2023.
- [26] C. Wu, S. Yin, W. Qi, X. Wang, Z. Tang, and N. Duan, "Visual chatgpt: Talking, drawing and editing with visual foundation models," *arXiv preprint arXiv:2303.04671*, 2023.
- [27] Anthropic, "Claude in slack." <https://www.anthropic.com/claude-in-slack>, 2023.