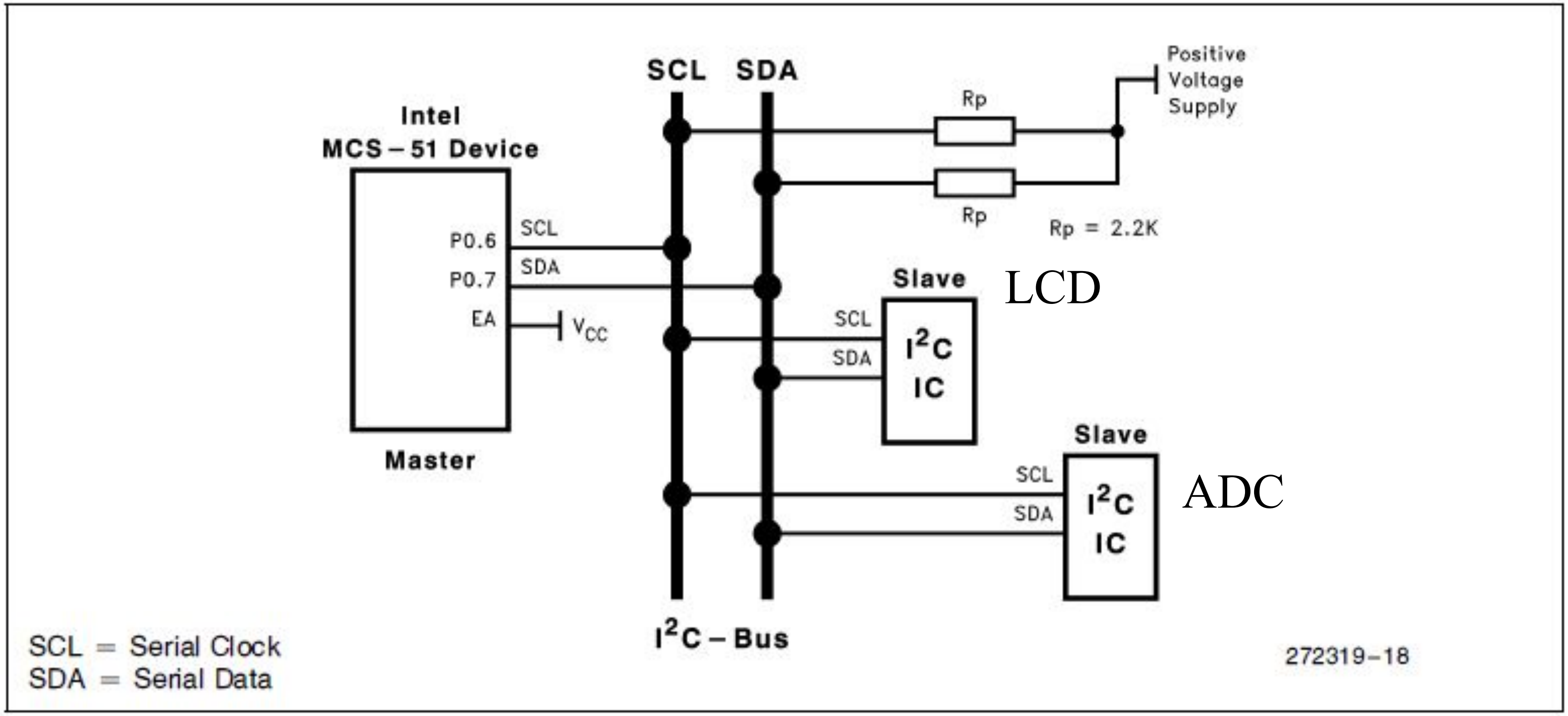
I2C Bus Protocol

Basic Characteristics

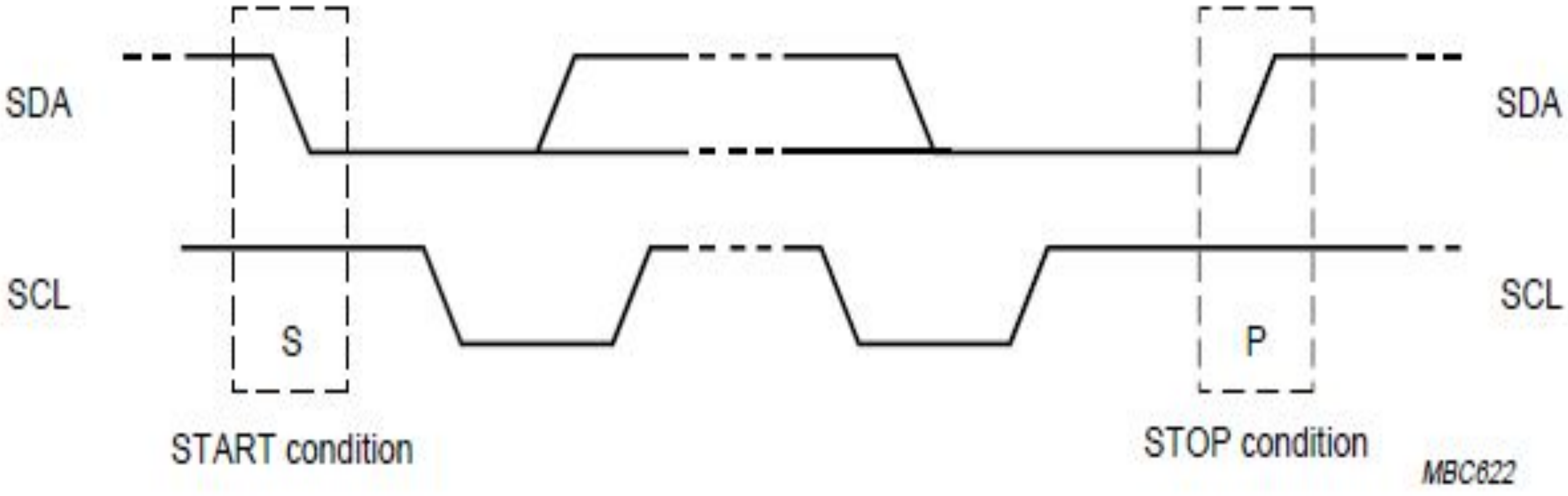
- two-wired bus
- originally to interact within small number of devices
- speeds:
  - 100 kbps (standard mode)
  - 400 kbps (fast mode)
  - 3.4 Mbps (high-speed mode)
- data transfers: serial, 8-bit oriented, bi-directional
- master/slave relationships with multi-master option (arbitration)
- master can operate as transmitter or receiver
- addressing: 7bit or 10bit unique addresses

I2C Master/Slave Bus system

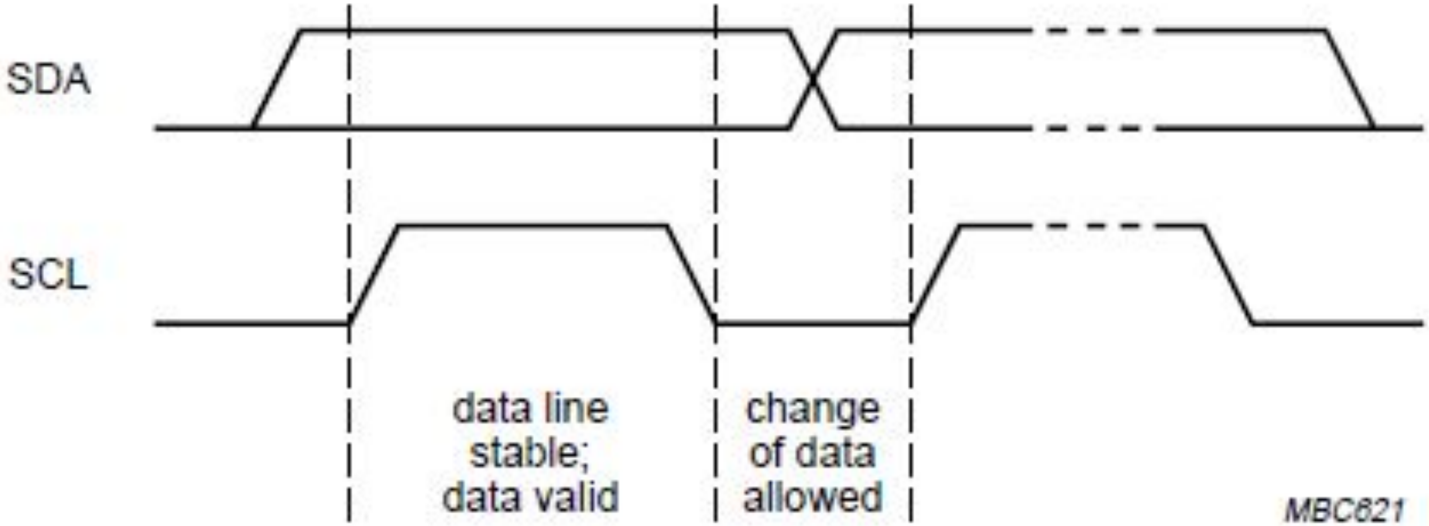


LCD

ADC

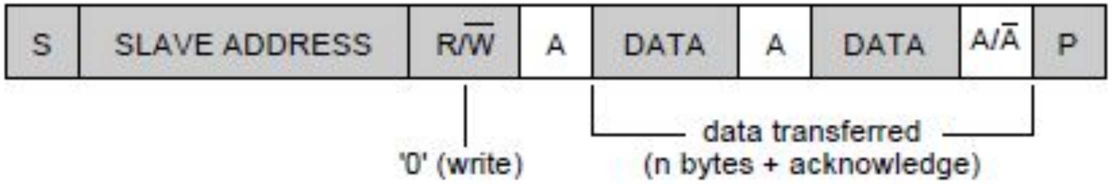

SDA
SCL
S
START condition
SDA
SCL
P
STOP condition
MBC622

Bit Transfer

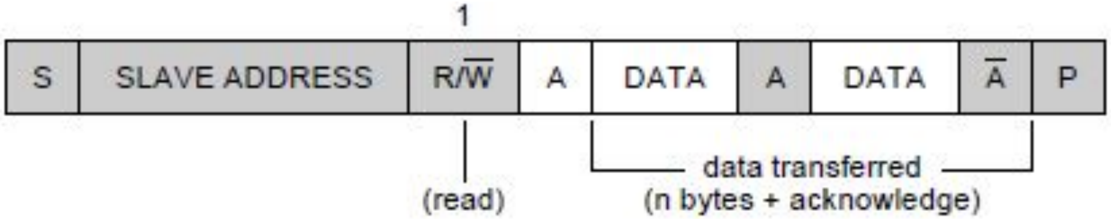


Frame Format

master-transmitter



master-receiver



▨ from master to slave

□ from slave to master

A = acknowledge (SDA LOW)

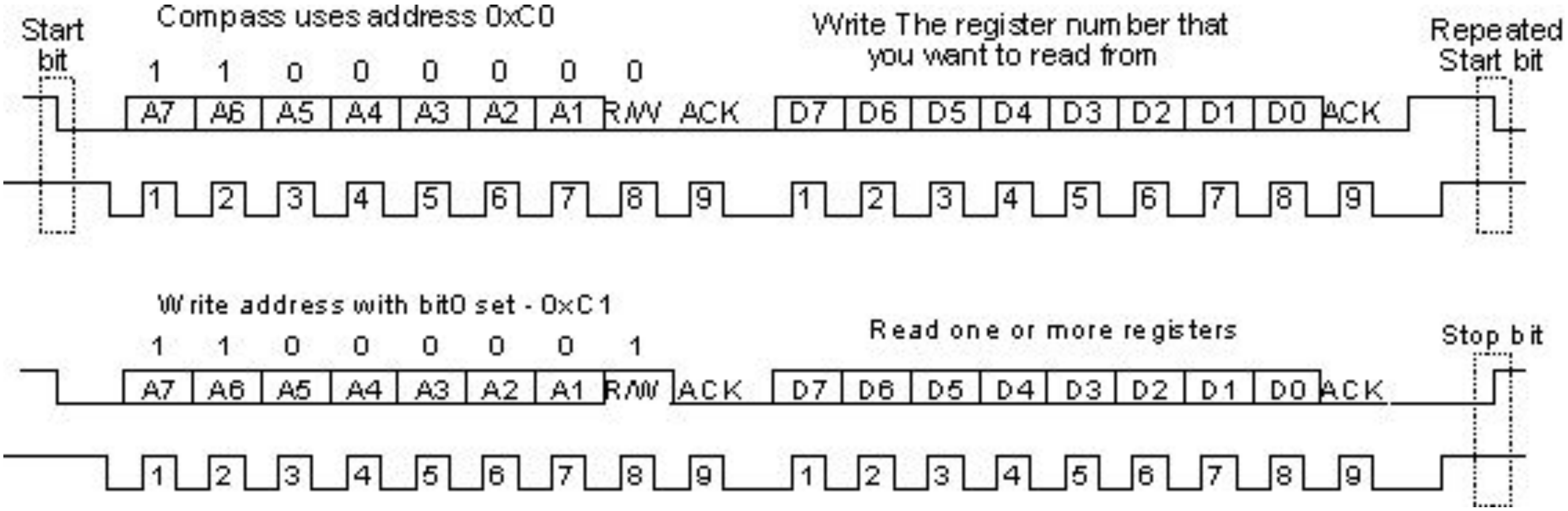
$\overline{A}$ = not acknowledge (SDA HIGH)

S = START condition

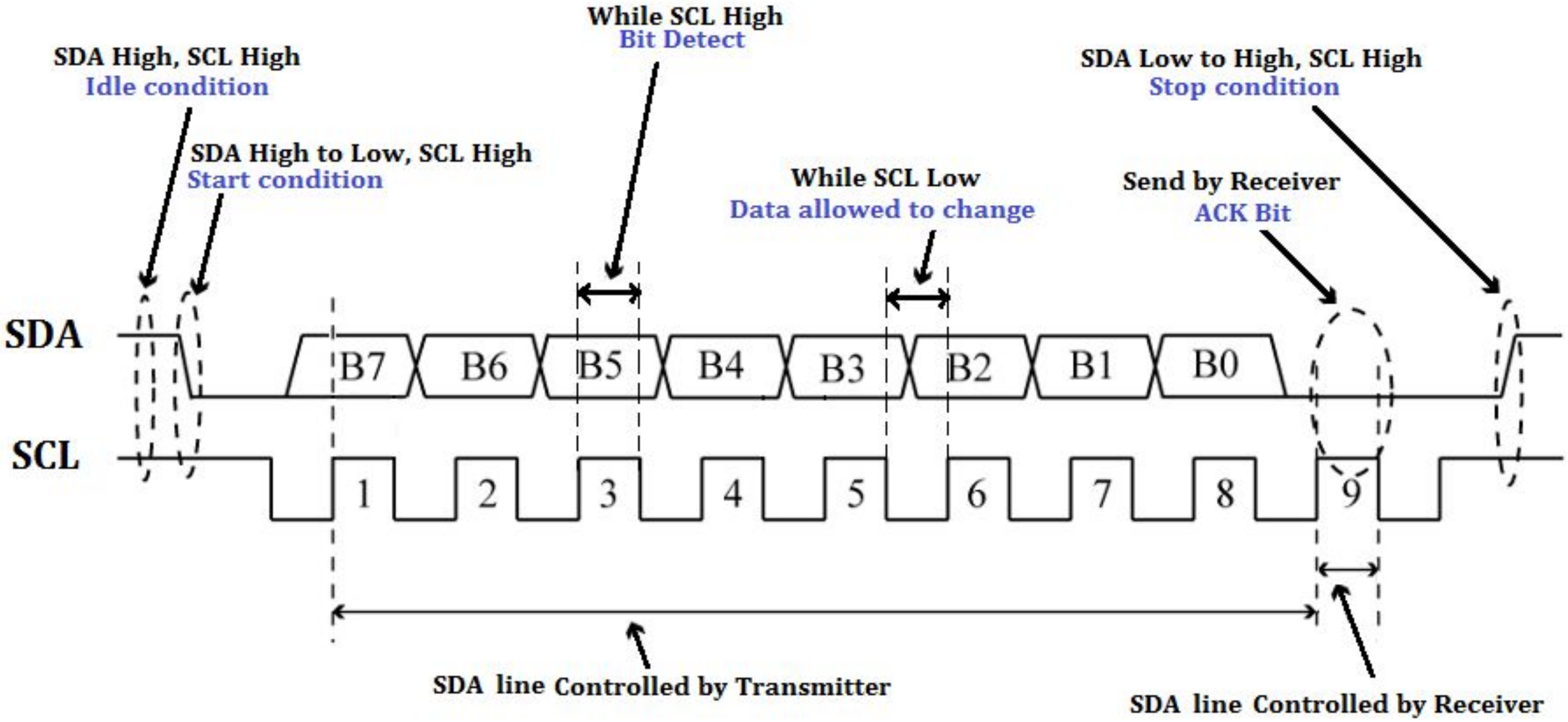
P = STOP condition

mbc605

Frame Format


Start bit
Compass uses address 0xC0
1 1 0 0 0 0 0 0
A7 A6 A5 A4 A3 A2 A1 R/W ACK
Write The register number that you want to read from
D7 D6 D5 D4 D3 D2 D1 D0 ACK
Repeated Start bit
1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9
Write address with bit0 set - 0xC1
1 1 0 0 0 0 0 1
A7 A6 A5 A4 A3 A2 A1 R/W ACK
Read one or more registers
D7 D6 D5 D4 D3 D2 D1 D0 ACK
Stop bit
1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9

I2C – Single Byte Transfer



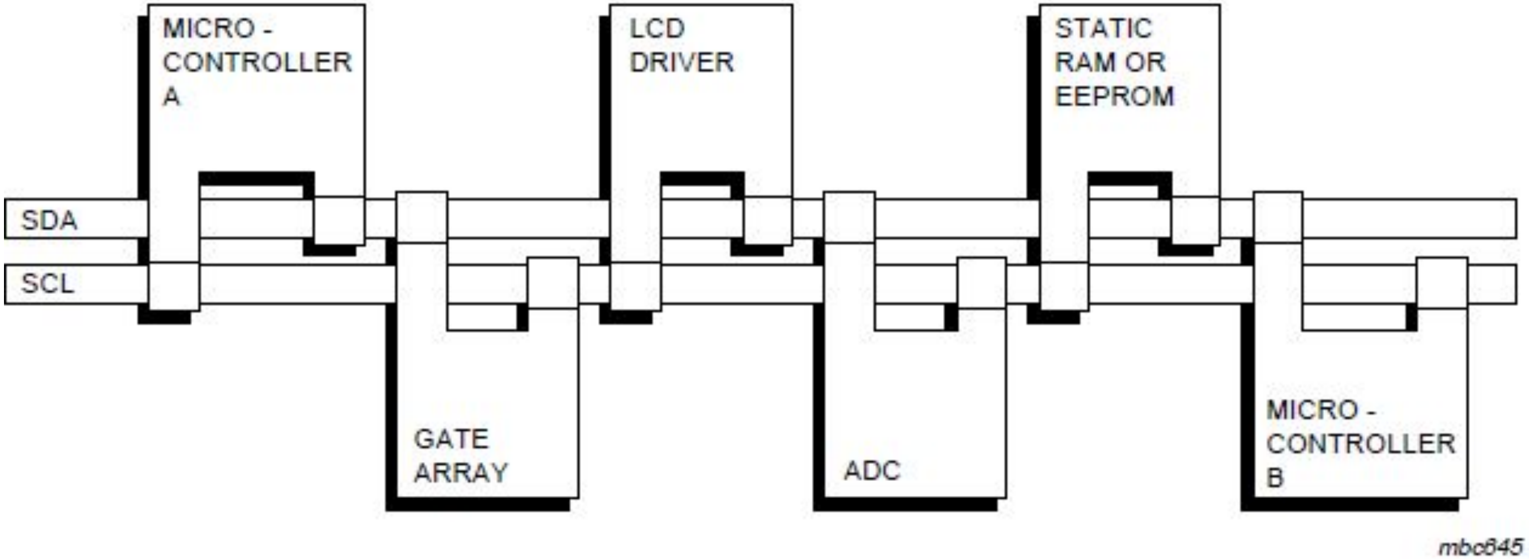
Masters and Slaves

- Master device
  - controls the SCL
  - starts and stops data transfer
  - controls addressing of other devices

- Slave device
  - device addressed by master

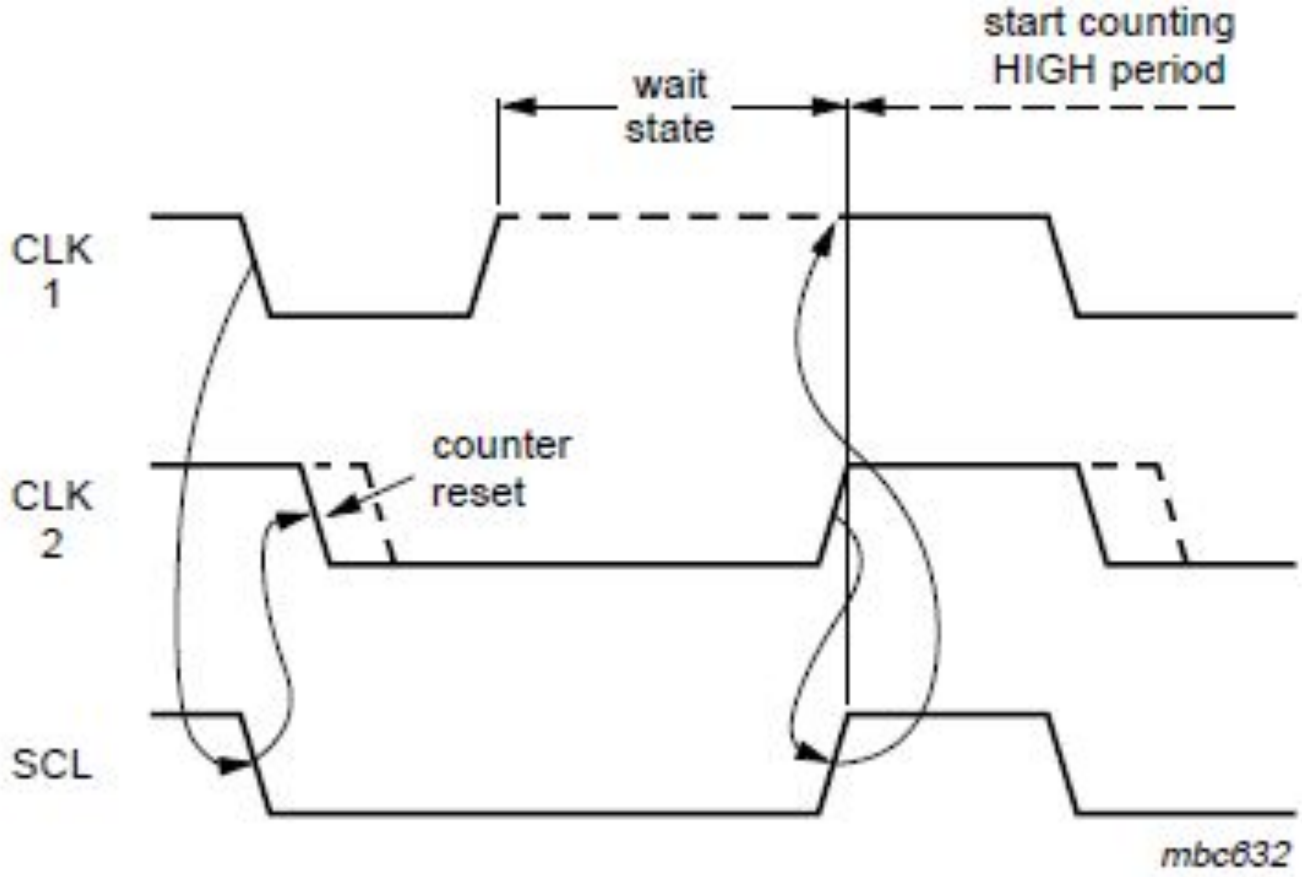
- Transmitter/Receiver
  - master or slave
  - master-transmitter sends data to slave-receiver
  - master-receiver requires data from slave-transmitter

Multiple Masters

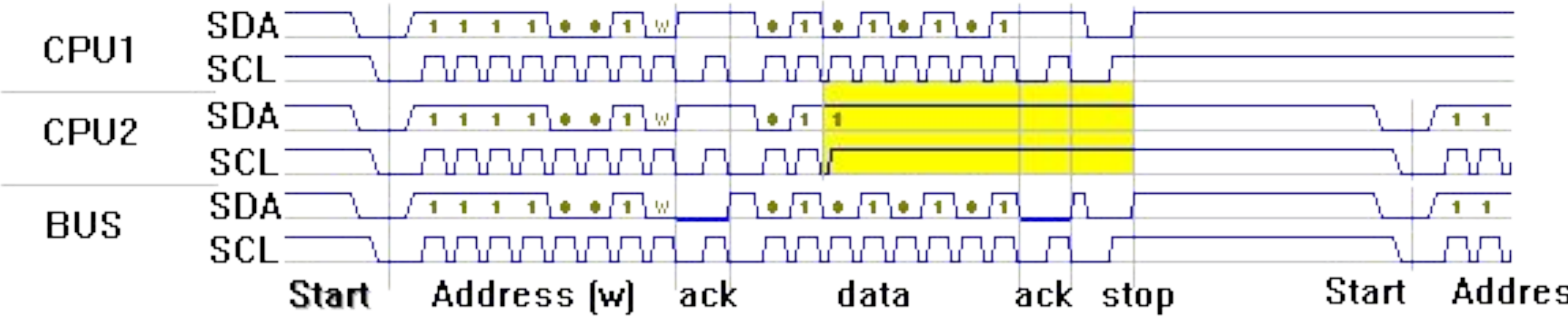


- more bus controllers can be connected
- several masters can start frame at once
- synchronization needed on SCL
- arbitration needed on SDA

Clock Stretching



I2C Bus Arbitration



Applications of I^{2}C

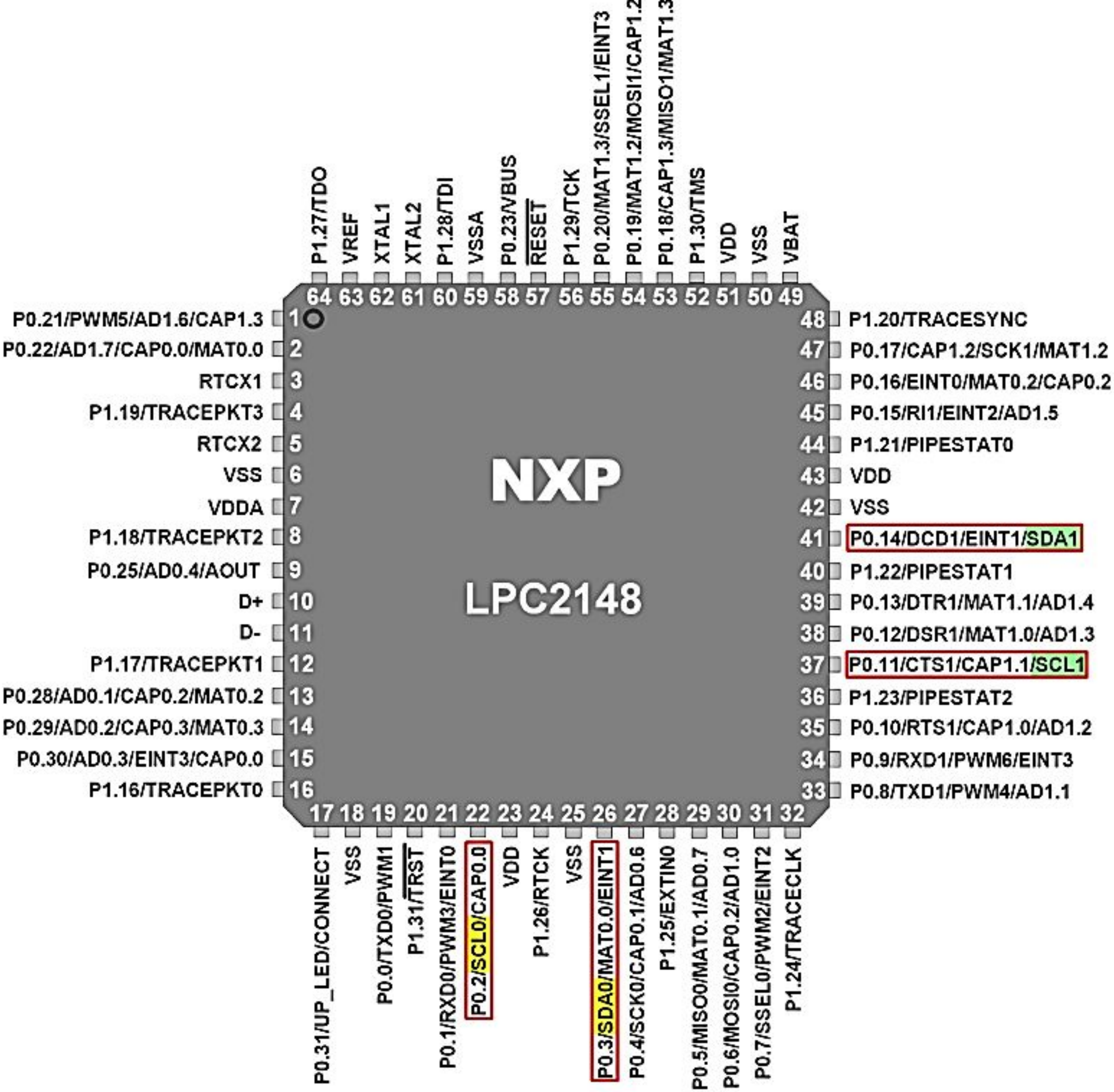
I²C is appropriate for peripherals where simplicity and low manufacturing cost are more important than speed. Common applications of the I^{2}C bus are:

- Reading configuration data from SPD EEPROMs on SDRAM, DDR SDRAM, DDR2 SDRAM memory sticks (DIMM) and other stacked PC boards.
- Supporting systems management for PCI cards.
- Accessing NVRAM chips that keep user settings.
- Accessing low speed DACs and ADCs.
- Changing contrast, hue, and color balance settings in monitors (Display Data Channel).
- Changing sound volume in intelligent speakers.
- Controlling OLED/LCD displays, like in a cellphone.
- Reading hardware monitors and diagnostic sensors, like a CPU thermostat and fan speed.
- Reading real time clocks.
- Turning on and turning off the power supply of system components.

LPC21xx/22xx I2C interface

Features

- LPC2148 has two I2C interfaces. i.e. I2C0 & I2C1
- Standard I2C compliant bus interfaces that may be configured as Master, Slave, or Master/Slave.
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock to allow adjustment of I2C transfer rates.
- Bidirectional data transfer between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I2C-bus may be used for test and diagnostic purposes.


NXP
LPC2148
1 P0.21/PWM5/AD1.6/CAP1.3
2 P0.22/AD1.7/CAP0.0/MAT0.0
3 RTCX1
4 P1.19/TRACEPKT3
5 RTCX2
6 VSS
7 VDDA
8 P1.18/TRACEPKT2
9 P0.25/AD0.4/AOUT
10 D+
11 D-
12 P1.17/TRACEPKT1
13 P0.28/AD0.1/CAP0.2/MAT0.2
14 P0.29/AD0.2/CAP0.3/MAT0.3
15 P0.30/AD0.3/EINT3/CAP0.0
16 P1.16/TRACEPKT0
17 P0.31/UP_LED/CONNECT
18 VSS
19 P0.0/TXD0/PWM1
20 P1.31/TRST
21 P0.1/RXD0/PWM3/EINT0
22 P0.2/SCL0/CAP0.0
23 VDD
24 P1.26/RTCK
25 VSS
26 P0.3/SDA0/MAT0.0/EINT1
27 P0.4/SCK0/CAP0.1/AD0.6
28 P1.25/EXTIN0
29 P0.5/MISO0/MAT0.1/AD0.7
30 P0.6/MOSI0/CAP0.2/AD1.0
31 P0.7/SSEL0/PWM2/EINT2
32 P1.24/TRACECLK
33 P0.8/TXD1/PWM4/AD1.1
34 P0.9/RXD1/PWM6/EINT3
35 P0.10/RTS1/CAP1.0/AD1.2
36 P1.23/PIPESTAT2
37 P0.11/CTS1/CAP1.1/SCL1
38 P0.12/DSR1/MAT1.0/AD1.3
39 P0.13/DTR1/MAT1.1/AD1.4
40 P1.22/PIPESTAT1
41 P0.14/DCD1/EINT1/SDA1
42 VSS
43 VDD
44 P1.21/PIPESTAT0
45 P0.15/RI1/EINT2/AD1.5
46 P0.16/EINT0/MAT0.2/CAP0.2
47 P0.17/CAP1.2/SCK1/MAT1.2
48 P1.20/TRACESYNC
49 VBAT
50 VSS
51 VDD
52 P1.30/TMS
53 P0.18/CAP1.3/MISO1/MAT1.3
54 P0.19/MAT1.2/MOSI1/CAP1.2
55 P0.20/MAT1.3/SSEL1/EINT3
56 P1.29/TCK
57 RESET
58 P0.23/VBUS
59 VSSA
60 P1.28/TDI
61 XTAL2
62 XTAL1
63 VREF
64 P1.27/TDO

PIN FUNCTION SELECT REGISTER (PINSEL0)

- 5:4 P0.2 00 GPIO Port 0.2
  01 SCL0 (I2C0)
  10 Capture 0.0 (Timer 0)
  11 Reserved

- 7:6 P0.3 00 GPIO Port 0.3
  01 SDA0 (I2C0)
  10 Match 0.0 (Timer 0)
  11 EINT1

For I2C, PINSEL_____ = _________________

PIN FUNCTION SELECT REGISTER (PINSEL0)

5:4	P0.2	00	GPIO Port 0.2
		01	SCL0 (I2C0)
		10	Capture 0.0 (Timer 0)
		11	Reserved
7:6	P0.3	00	GPIO Port 0.3
		01	SDA0 (I2C0)
		10	Match 0.0 (Timer 0)
		11	EINT1

For I2C, PINSEL0 = 0x00000050

I2C Registers

I2C0CONSET (I2C0 Configuration Set Register)

- It is an 8-bit read-write register.
- It is used to control the operation of the I2C0 interface.

7	6	5	4	3	2	1	0
RESERVED	I2CEN	STA	STO	SI	AA	RESERVED	

•Writing a 1 to a bit in this register causes corresponding bit in the I2C control register to set.
•Writing a 0 has no effect.

•**Bit 2 – AA (Assert Acknowledge Flag)**
When set to 1, Acknowledge (SDA LOW) is returned during acknowledge clock pulse on SCL. Otherwise, Not acknowledge (SDA HIGH) is returned.

•**Bit 3 – SI (I2C Interrupt Flag)**
This bit is set when the I2C state changes. Else it remains reset.

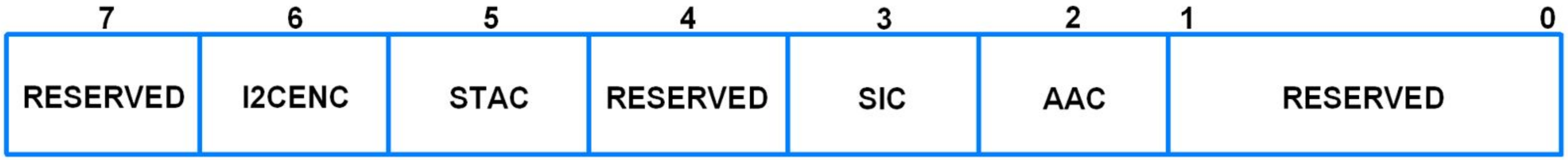
•**Bit 4 – STO (Stop Flag)**
In Master Mode, setting this bit causes the I2C interface to transmit a STOP condition. In Slave Mode, setting this bit causes recover from an error condition if any.
This bit is cleared by hardware automatically.

•**Bit 5 – STA (Start Flag)**
Setting this bit causes the I2C interface to enter in master mode and transmit a START condition or transmit a repeated START condition if it is already in master mode.

•**Bit 6 – I2CEN (I2C Interface Enable)**
Set this bit to enable I2C interface.

I2C0CONCLR (I2C0 Configuration Clear Register)

- It is an 8-bit write only register.



7	6	5	4	3	2	1	0
RESERVED	I2CENC	STAC	RESERVED	SIC	AAC	RESERVED	

- Writing a 1 to a bit in this register causes corresponding bit in the I2C control register to clear.
- Writing a 0 has no effect.

- **Bit 2 – AAC (Assert Acknowledge Flag Clear)**
  Setting this bit clears the AA bit in I2C0CONSET register.

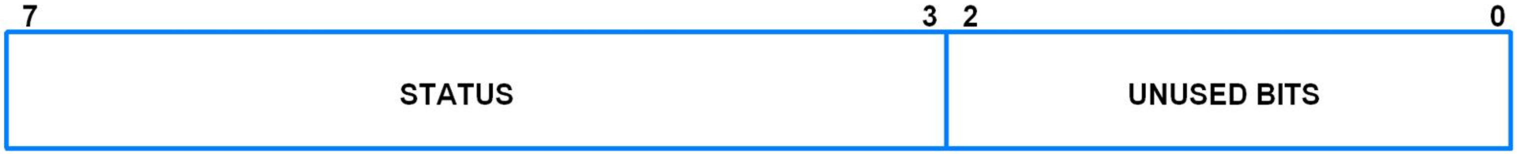
- **Bit 3 – SIC (I2C Interrupt Flag Clear)**
  Setting this bit clears the SI bit in I2C0CONSET register.

- **Bit 5 – STAC (Start Flag Clear)**
  Setting this bit clears the STA bit in I2C0CONSET register.

- **Bit 6 – I2CENC (I2C Interface Disable)**
  Setting this bit clears the I2CEN bit in I2C0CONSET register.

I2C0STAT (I2C0 Status Register)

- It is an 8-bit read only register.
- It reflects the present status of the I2C interface.



•**Bit 2:0 – Unused bits**
These are unused bits and are always 0.

•**Bit 7:3 – Status**
These are status bits which provide the status of the current event on I2C bus.
There are 26 possible status codes.

•Example, I2C0STAT = 0x08. This code indicates that a start condition has been transmitted.

Status Codes

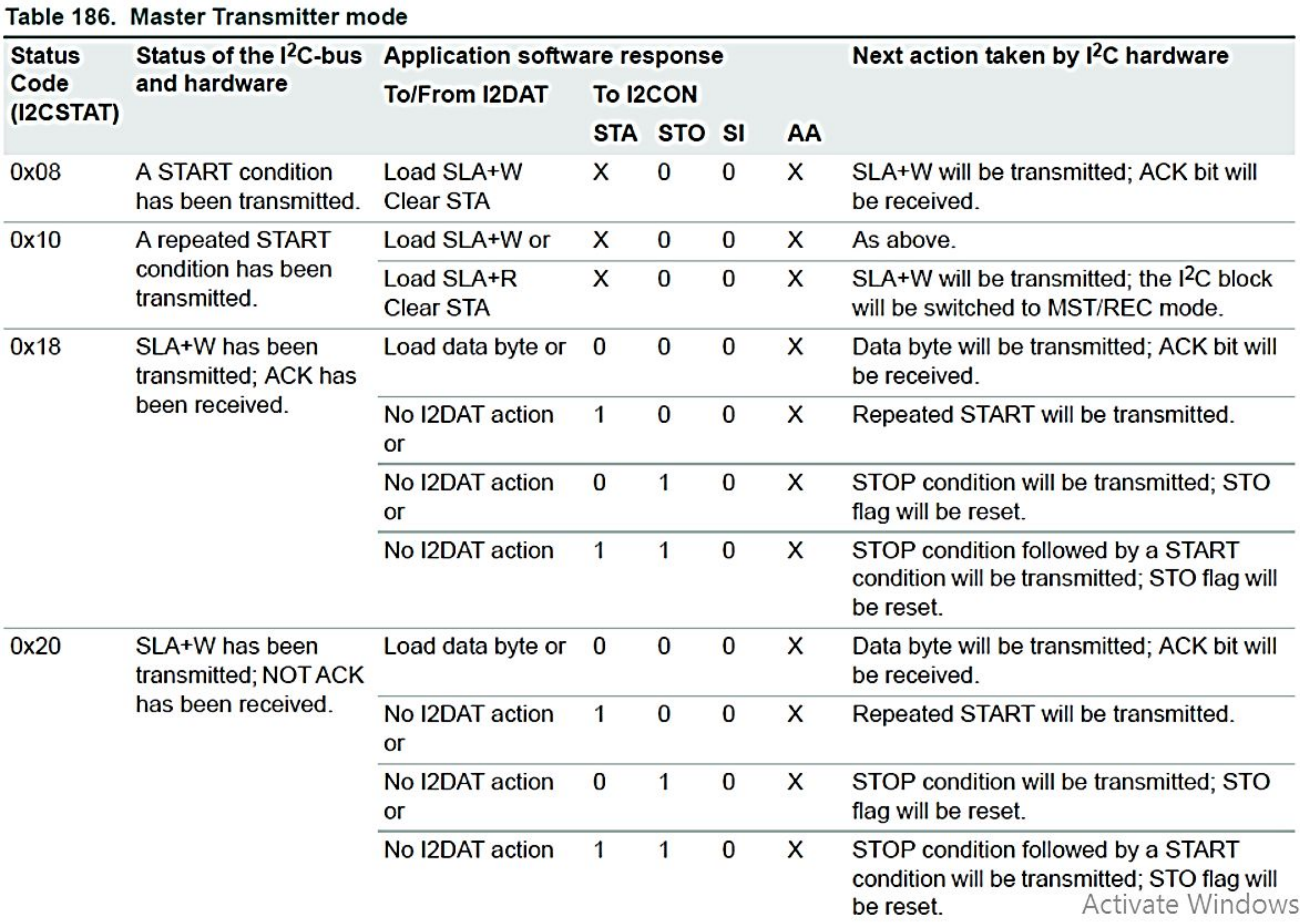
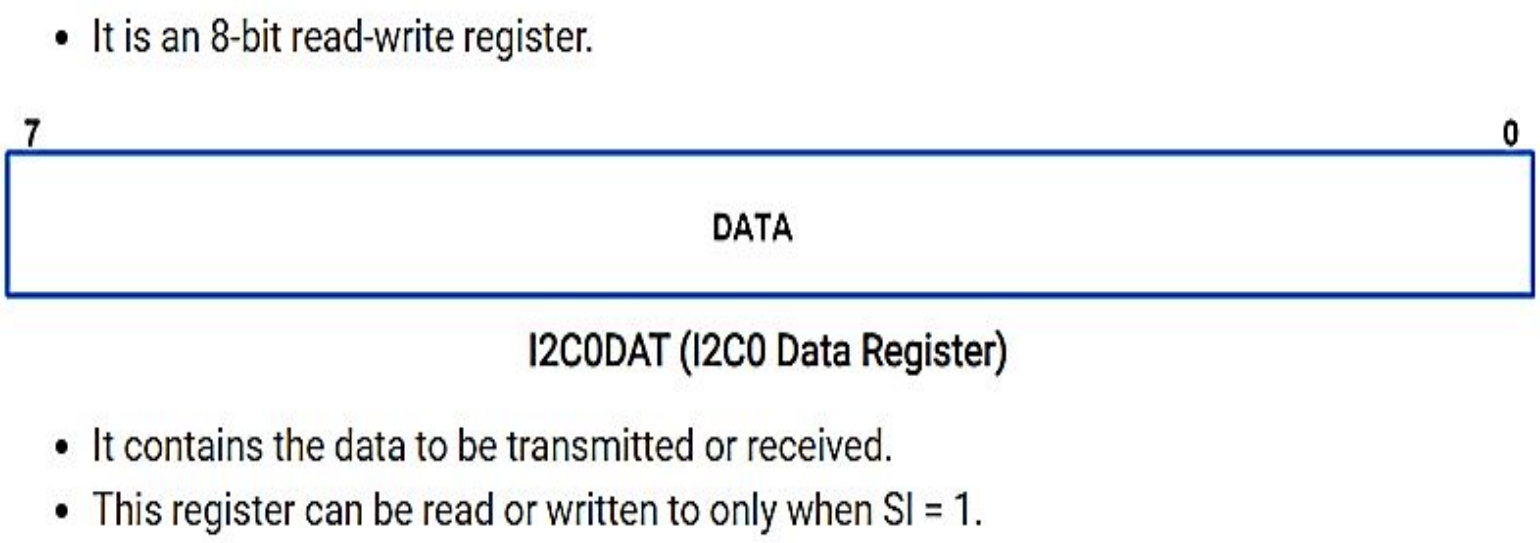


Table 186. Master Transmitter mode

Status Code (I2CSTAT)	Status of the I^{2}C-bus and hardware	Application software response					Next action taken by I^{2}C hardware
		To/From I2DAT	To I2CON				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Load SLA+W Clear STA	X	0	0	X	SLA+W will be transmitted; ACK bit will be received.
0x10	A repeated START condition has been transmitted.	Load SLA+W or	X	0	0	X	As above.
		Load SLA+R Clear STA	X	0	0	X	SLA+W will be transmitted; the I^{2}C block will be switched to MST/REC mode.
0x18	SLA+W has been transmitted; ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No I2DAT action or	1	0	0	X	Repeated START will be transmitted.
		No I2DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No I2DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x20	SLA+W has been transmitted; NOT ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No I2DAT action or	1	0	0	X	Repeated START will be transmitted.
		No I2DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No I2DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.

I2C0DAT (I2C0 Data Register)

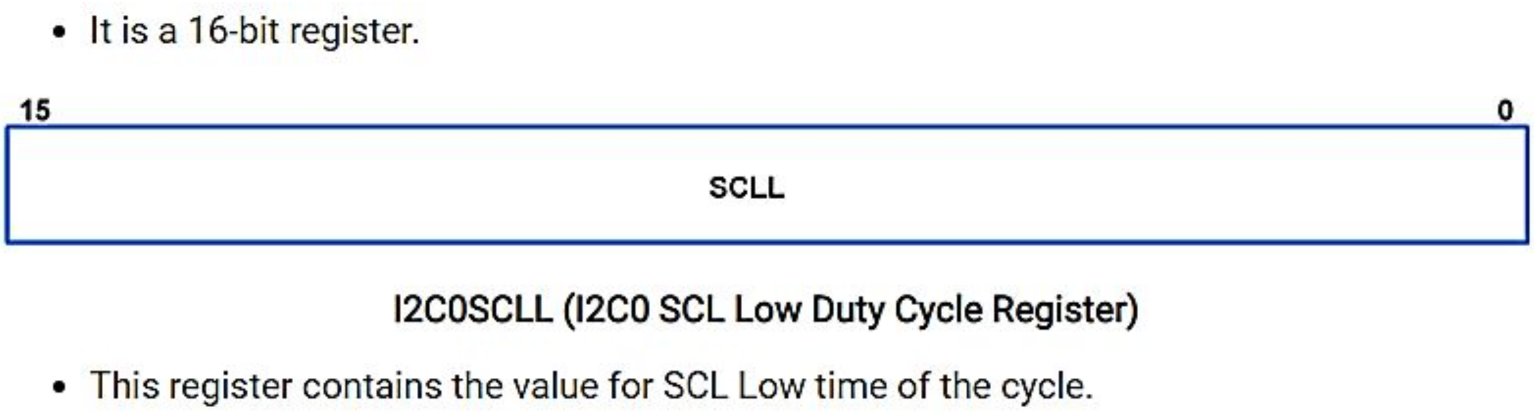


- It is an 8-bit read-write register.

I2C0DAT (I2C0 Data Register)

- It contains the data to be transmitted or received.
- This register can be read or written to only when SI = 1.

I2C0SCLL (I2C0 SCL Low Duty Cycle Register)



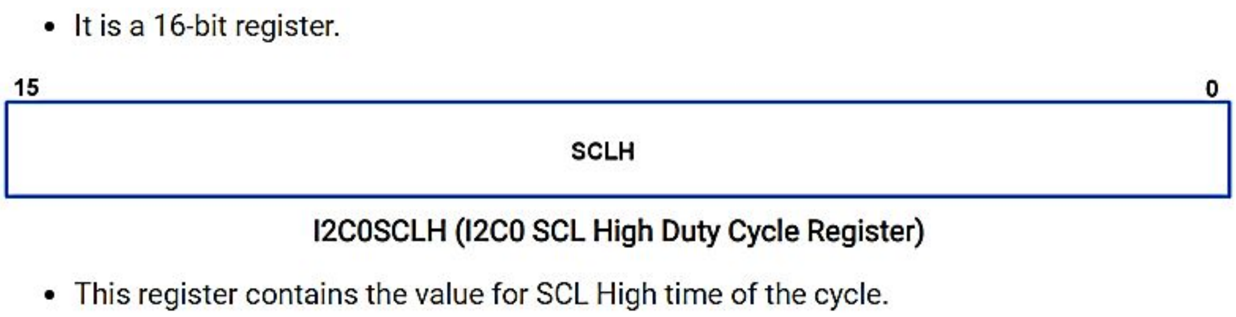
- It is a 16-bit register.

15 … 0
SCLL

I2C0SCLL (I2C0 SCL Low Duty Cycle Register)

- This register contains the value for SCL Low time of the cycle.

I2C0SCLH (I2C0 SCL High Duty Cycle Register)



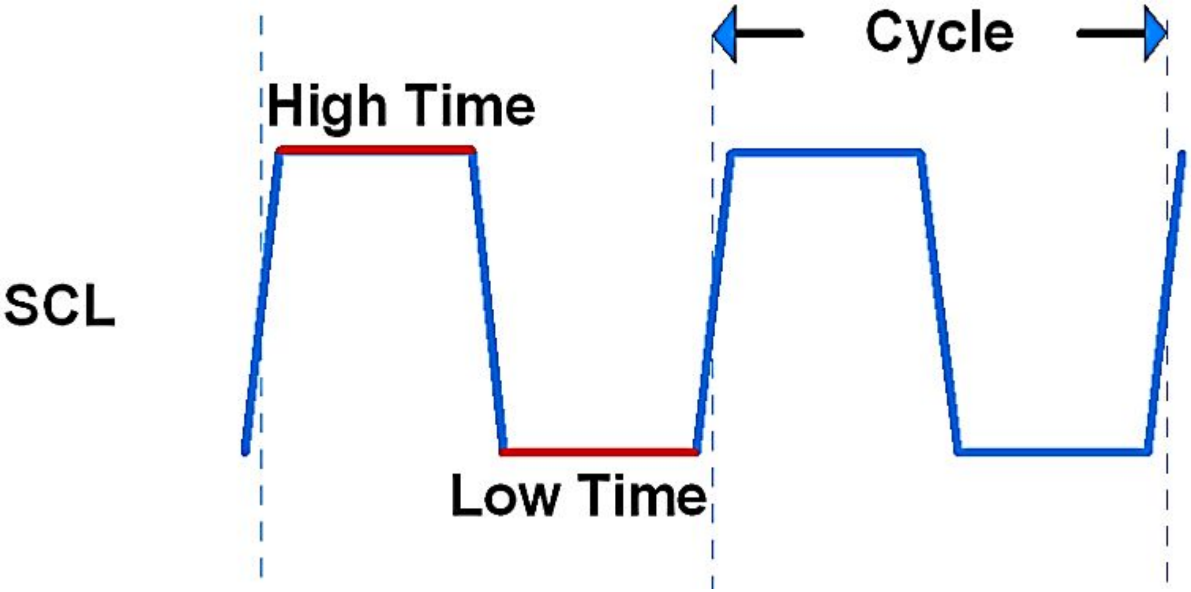
- It is a 16-bit register.

15 0

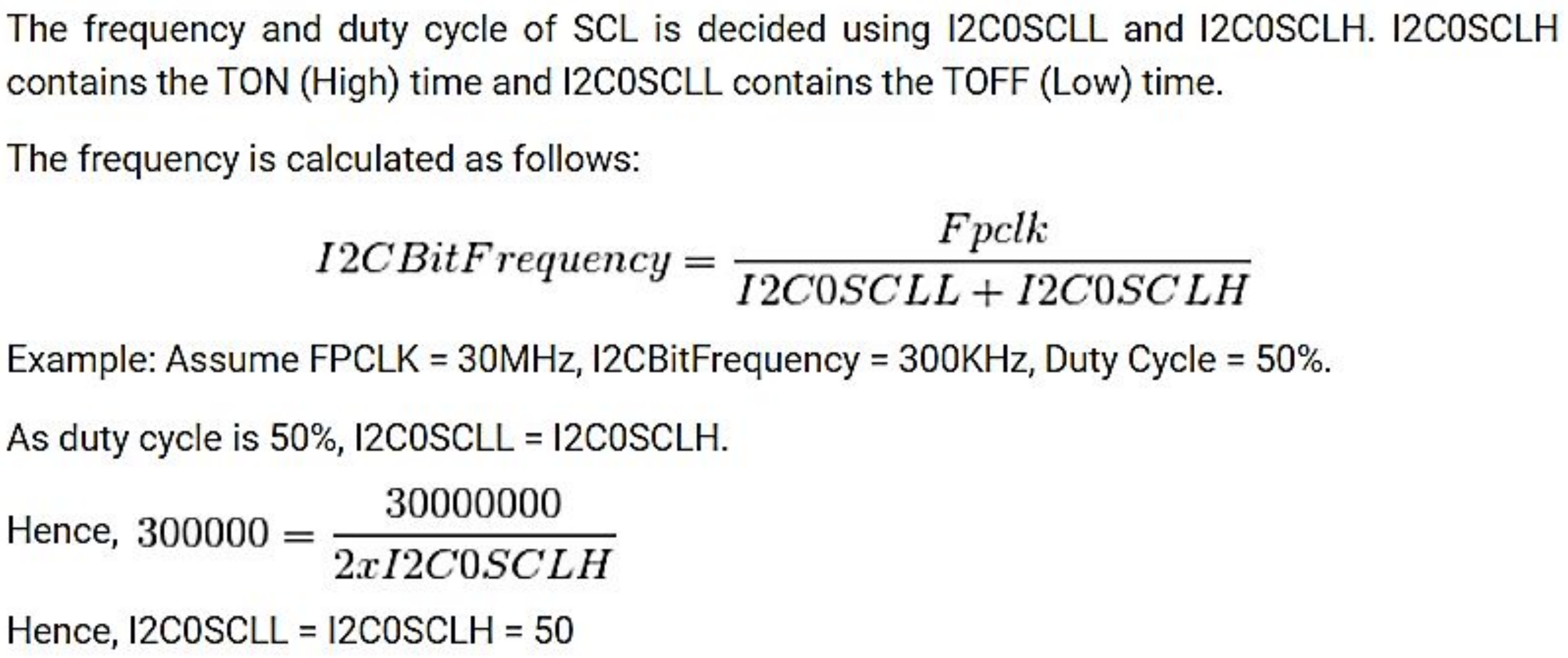
SCLH

I2C0SCLH (I2C0 SCL High Duty Cycle Register)

- This register contains the value for SCL High time of the cycle.



I2C Bit Frequency



The frequency and duty cycle of SCL is decided using I2C0SCLL and I2C0SCLH. I2C0SCLH contains the TON (High) time and I2C0SCLL contains the TOFF (Low) time.

The frequency is calculated as follows:

$$I2CBitFrequency = \frac{Fpclk}{I2C0SCLL + I2C0SCLH}$$

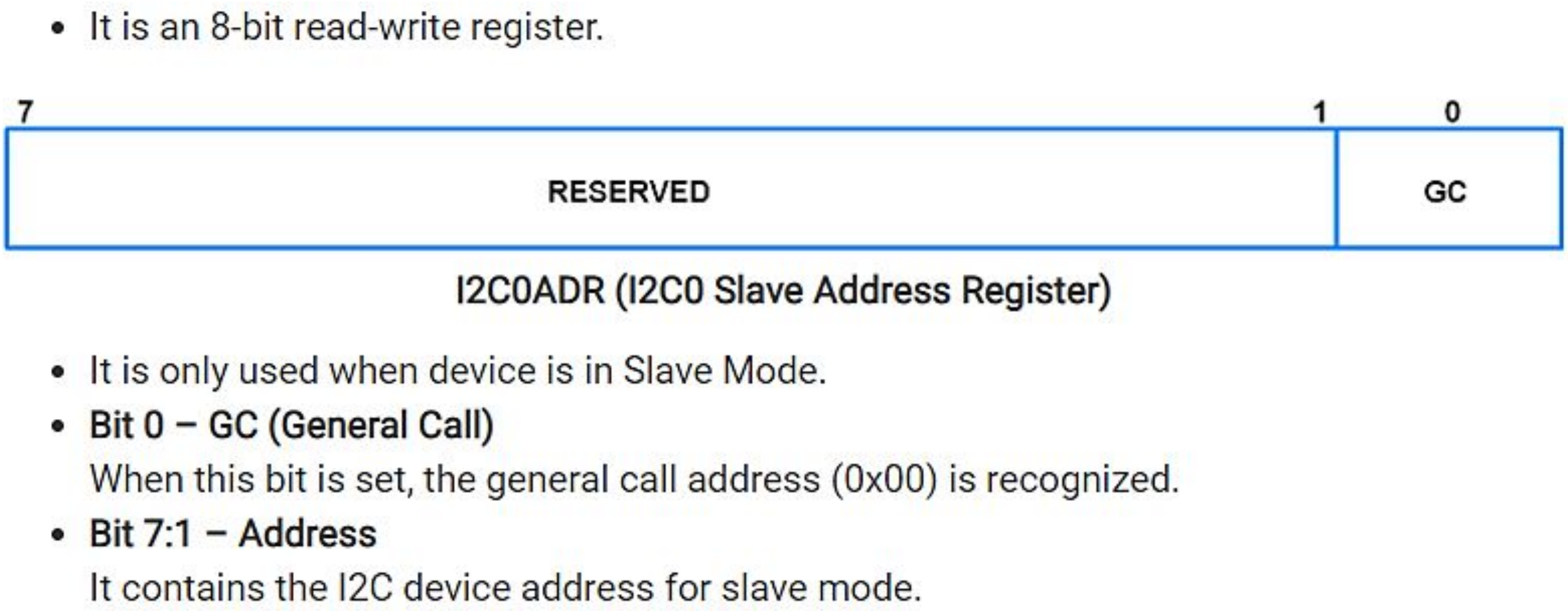
Example: Assume FPCLK = 30MHz, I2CBitFrequency = 300KHz, Duty Cycle = 50%.

As duty cycle is 50%, I2C0SCLL = I2C0SCLH.

Hence, $300000 = \frac{30000000}{2xI2C0SCLH}$

Hence, I2C0SCLL = I2C0SCLH = 50

I2C0ADR (I2C0 Slave Address Register)



- It is an 8-bit read-write register.

7 … 1	0
RESERVED	GC

I2C0ADR (I2C0 Slave Address Register)

- It is only used when device is in Slave Mode.
- **Bit 0 – GC (General Call)**
  When this bit is set, the general call address (0x00) is recognized.
- **Bit 7:1 – Address**
  It contains the I2C device address for slave mode.

Interfacing ST24C16 EEPROM with LPC2148

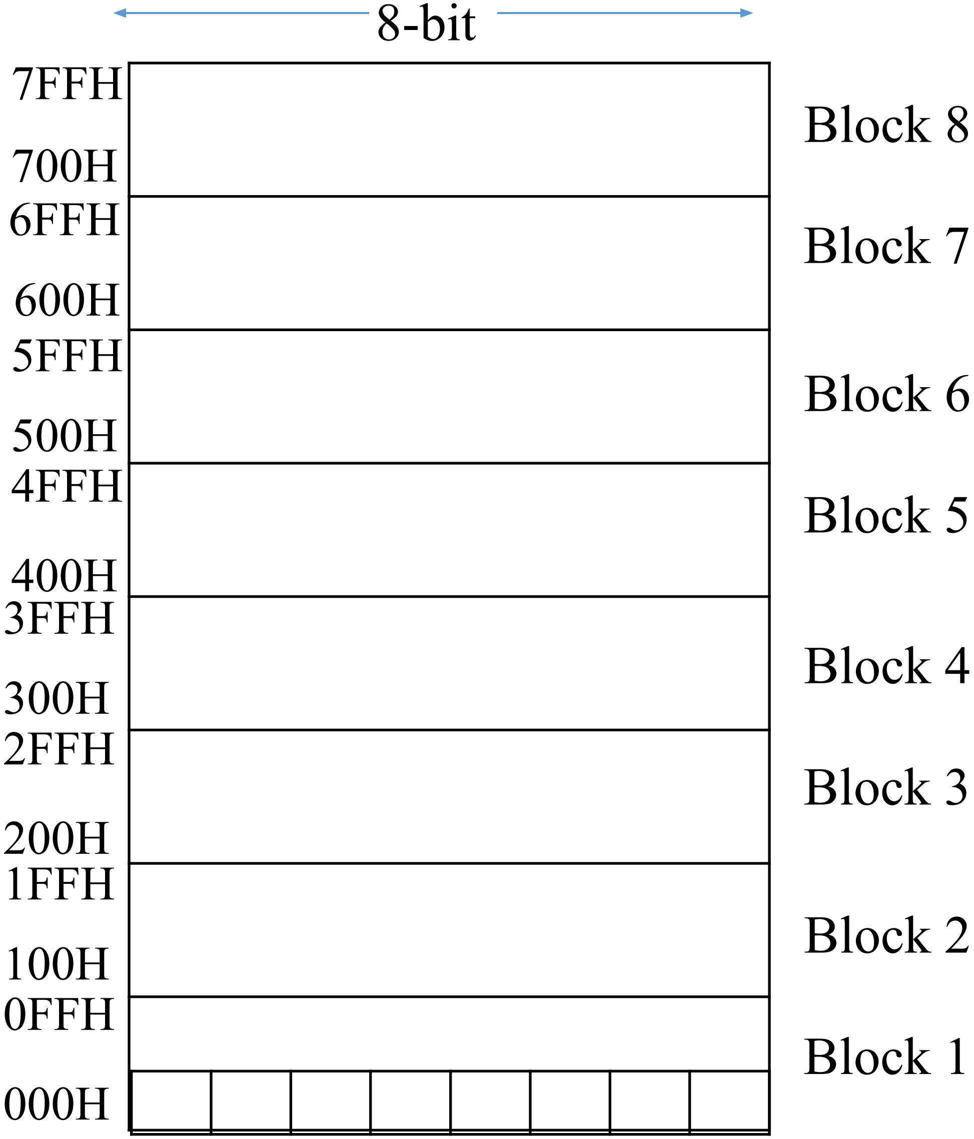
Features of ST24C16

- The ST24C16 is a 16 Kbit electrically erasable programmable memory (EEPROM), organized as 8 blocks of 256 x8 bits.

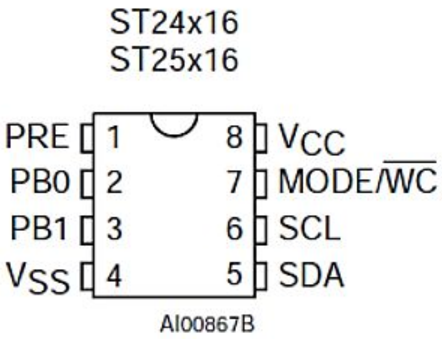
- 1 million erase/write cycles, with 40 years data retention.

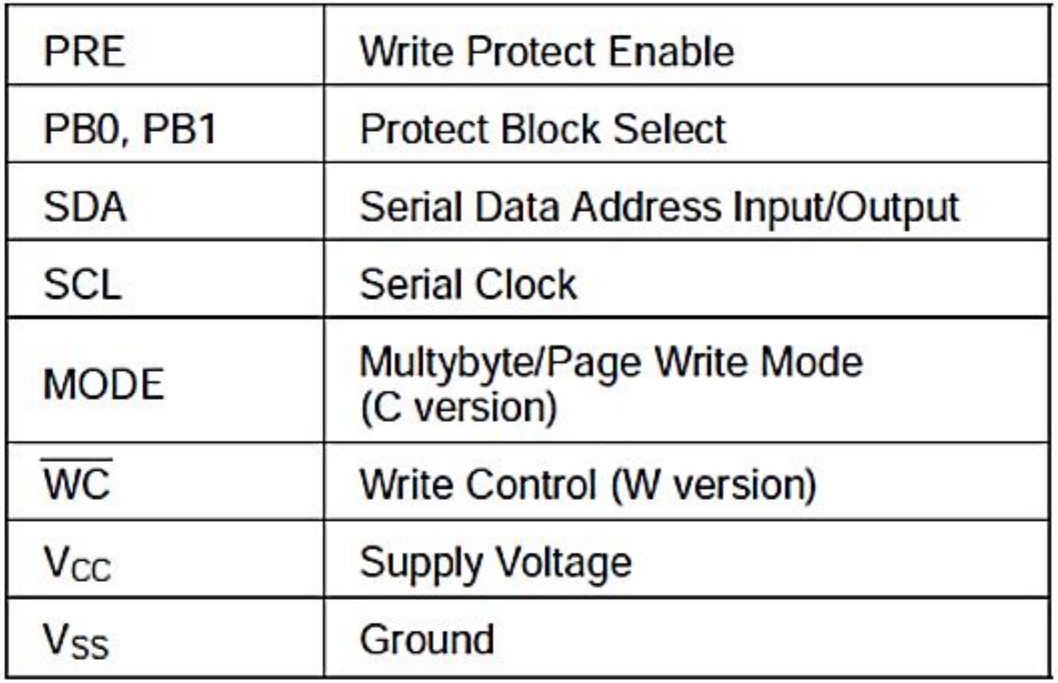
- Two wire serial interface, fully i2c bus compatible

ST24C16 EEPROM Memory Structure



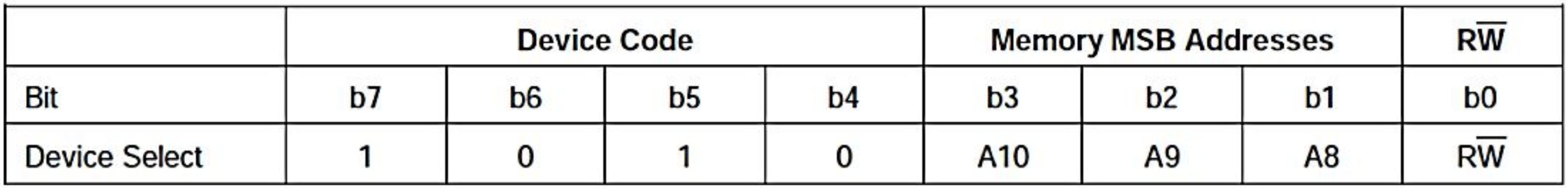
Pin Description of ST24C16





PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

EEPROM Select Code

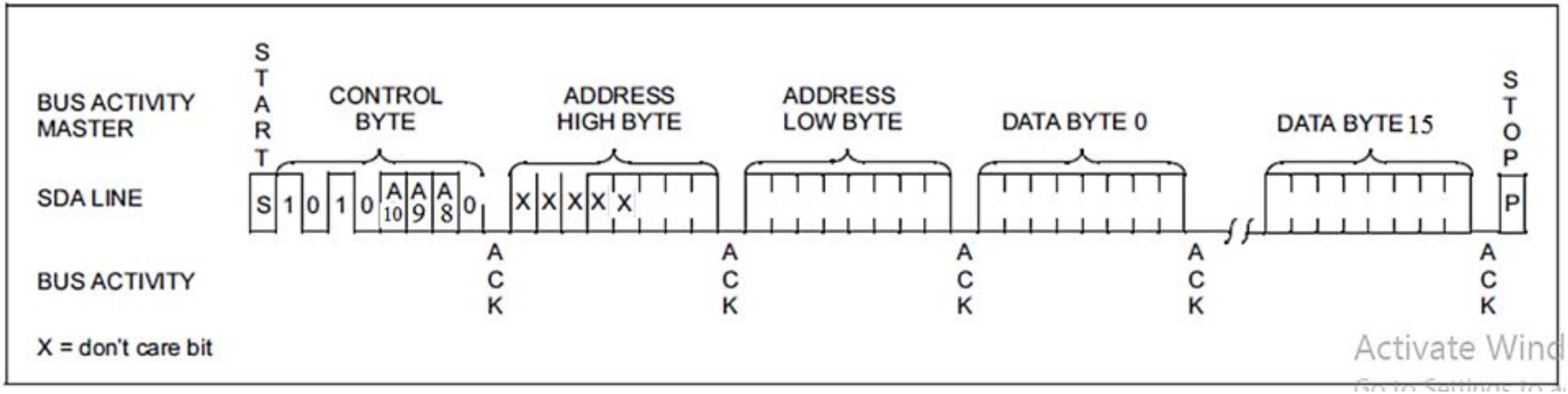


	Device Code				Memory MSB Addresses			R$\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	A10	A9	A8	R$\overline{W}$

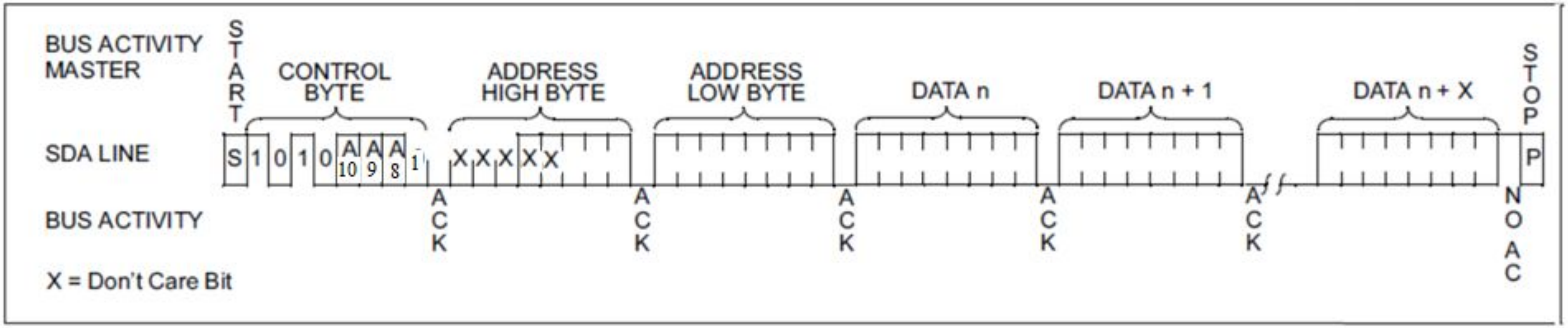
To perform a write operation – 0xA0

To perform a read operation – 0xA1

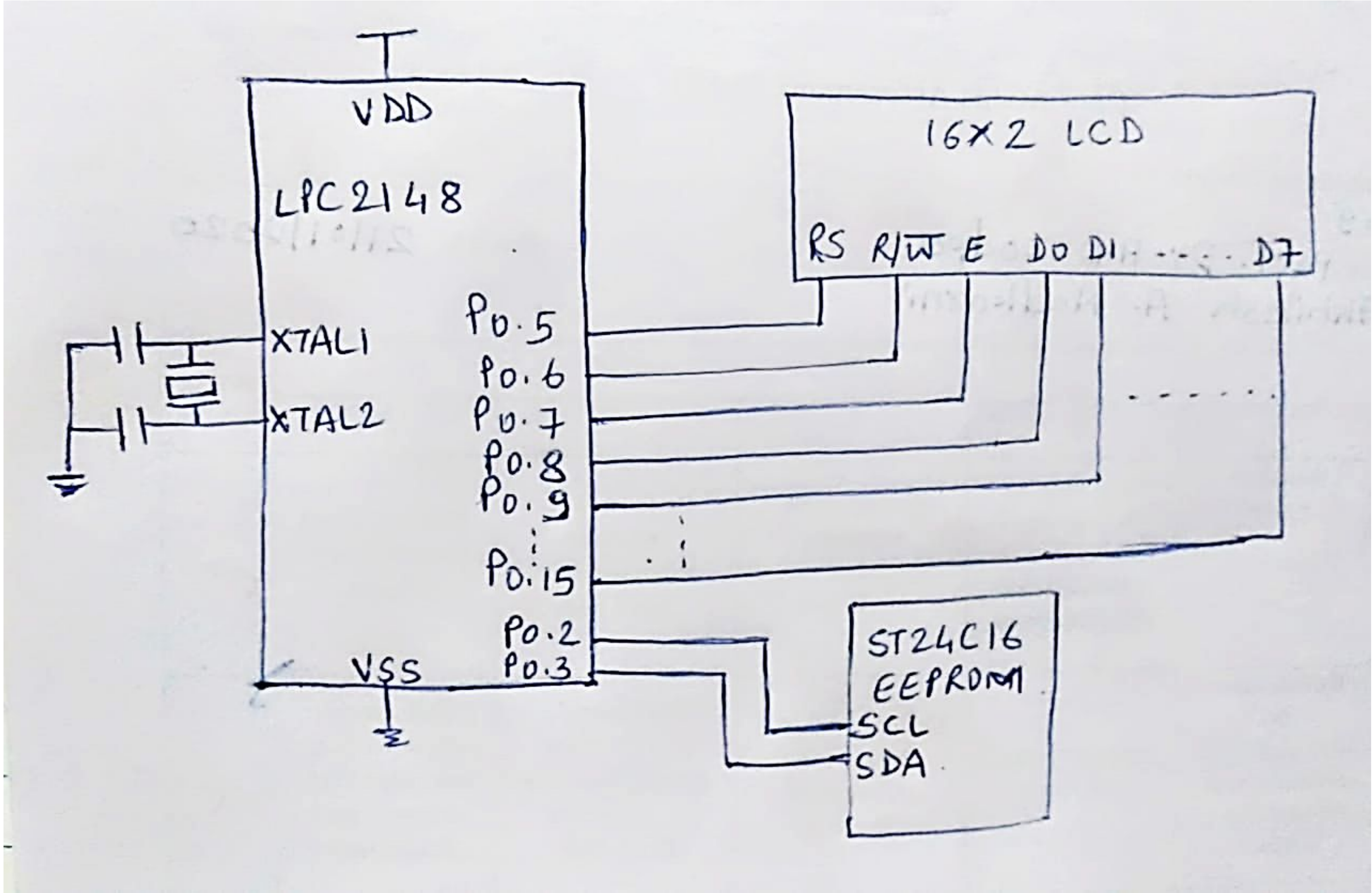
I2C Write Cycle



I2C Read Cycle



Interfacing Diagram


VDD
LPC2148
XTAL1
XTAL2
P0.5
P0.6
P0.7
P0.8
P0.9
P0.15
P0.2
P0.3
VSS
16X2 LCD
RS
R/W
E
D0
D1
D7
ST24C16
EEPROM
SCL
SDA