

ALE

Address Latch Enable. This signal is used by the microprocessor to lock the 16 lower address bus in a latch during a memory or port input/output operation.

IOW

The microprocessor makes this line LOW while doing WRITE TO PORT.

IOR

The microprocessor makes this line LOW while doing READ FROM PORT.

The three 74LS138 ICs handle the address decoding part. We have connected the address lines in a way such that there is short pulse (CLOCK) in the wires whenever the address lines contains the address and port output (IOW) is requested.

Whenever the 74LS374 get a CLOCK PULSE it latches-in the 8-Bit data present in the data bus. 74LS245 is a 3-STATE Octal Bus Transceiver. It reduces DC loading on the data bus and allows isolation of data bus when required.