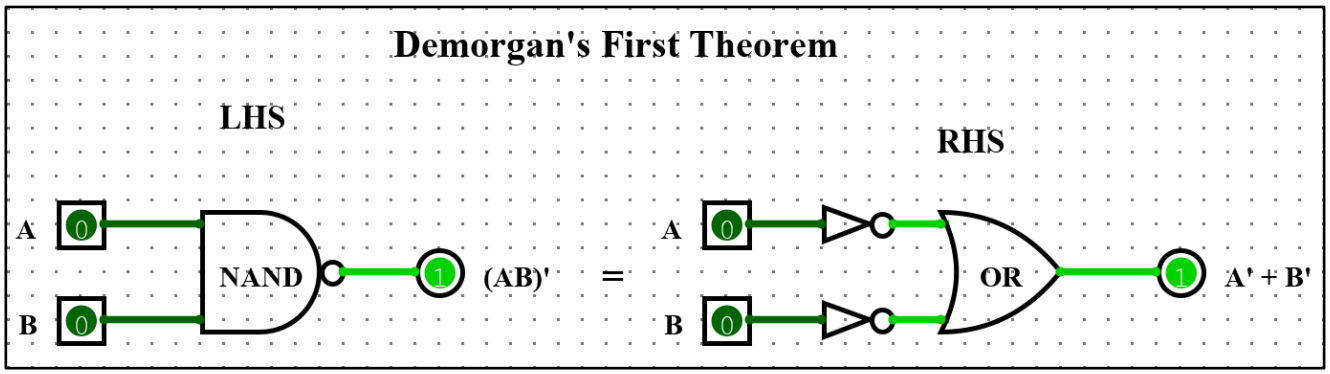
EXPT. NO: 01 DATE:	VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES

Demorgan's First Theorem → $\overline{AB} = \overline{A} + \overline{B}$

Truth Table:

A	B	AB	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Circuit Diagram:

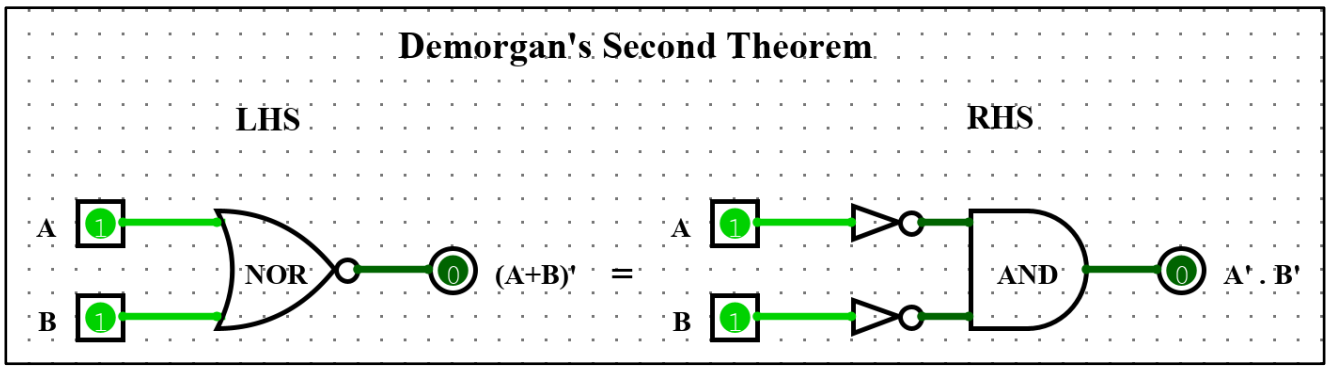


Demorgan's Second Theorem → $\overline{A + B} = \overline{A} \cdot \overline{B}$

Truth Table:

A	B	A + B	$\overline{A + B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Circuit Diagram:



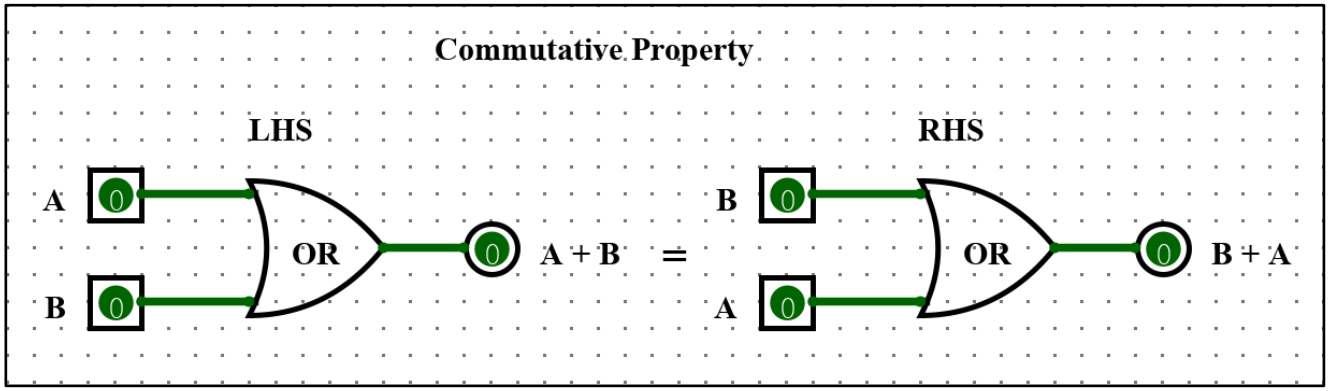
EXPT. NO: 01 DATE:	VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES

(1) Commutative Property: A + B = B + A

Truth Table:

A	B	A + B	B + A
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

Circuit Diagram:

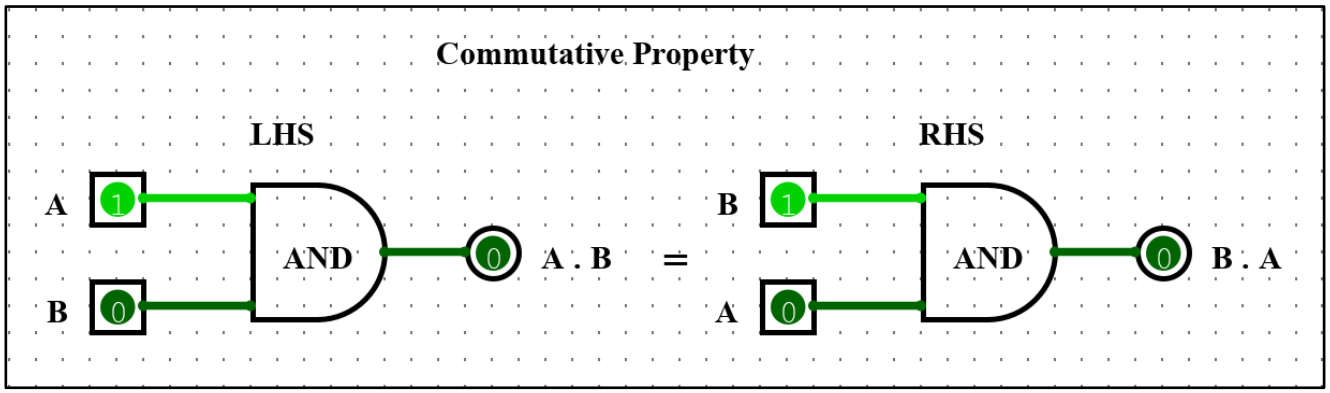


(2) Commutative Property: A . B = B . A

Truth Table:

A	B	A . B	B . A
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

Circuit Diagram:



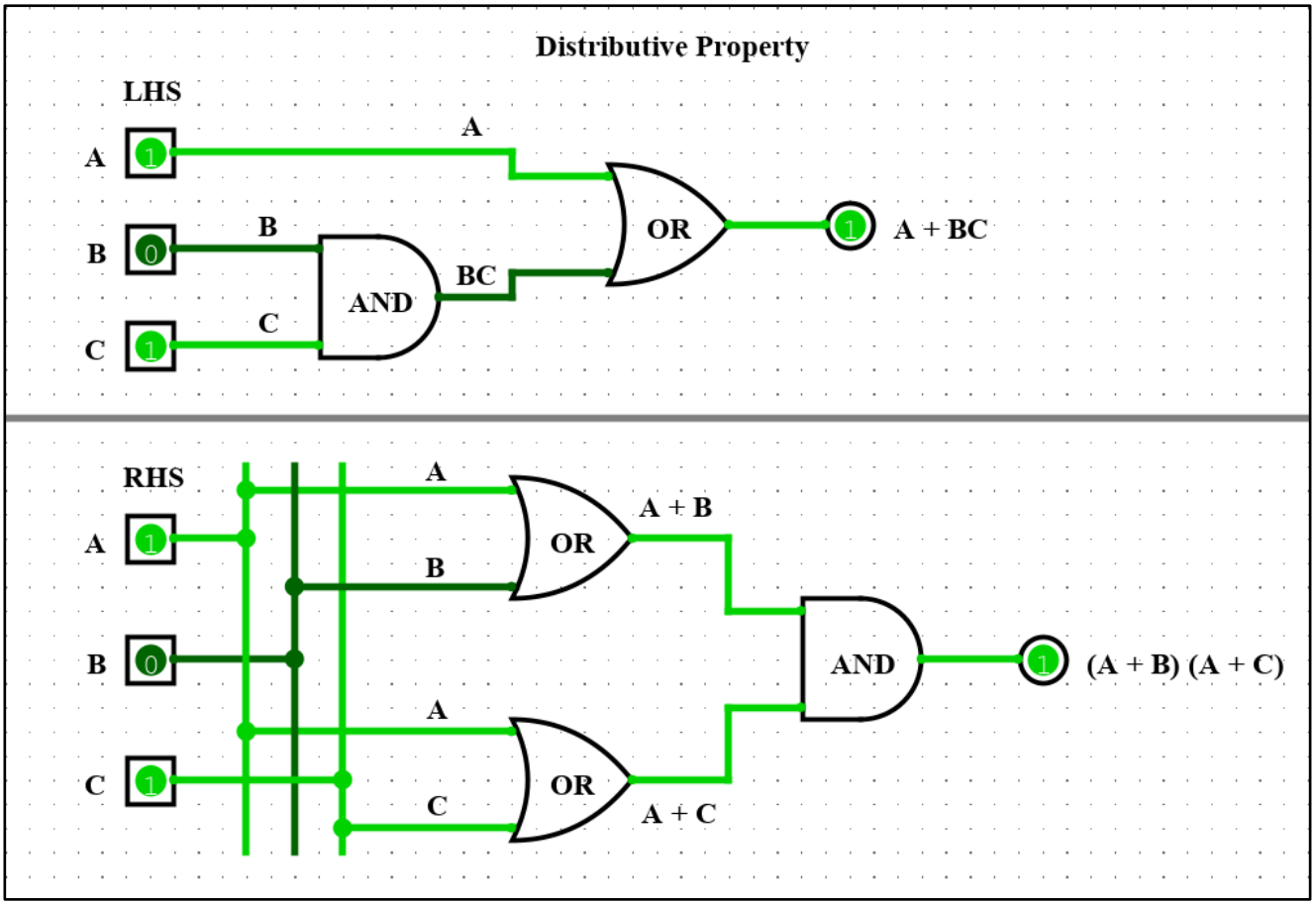
EXPT. NO: 01	VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES
DATE:	

(1) Distributive Property: A + BC = (A + B) (A + C)

Truth Table:

A	B	C	BC	A + BC	A + B	A + C	(A + B) . (A + C)
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

Circuit Diagram:



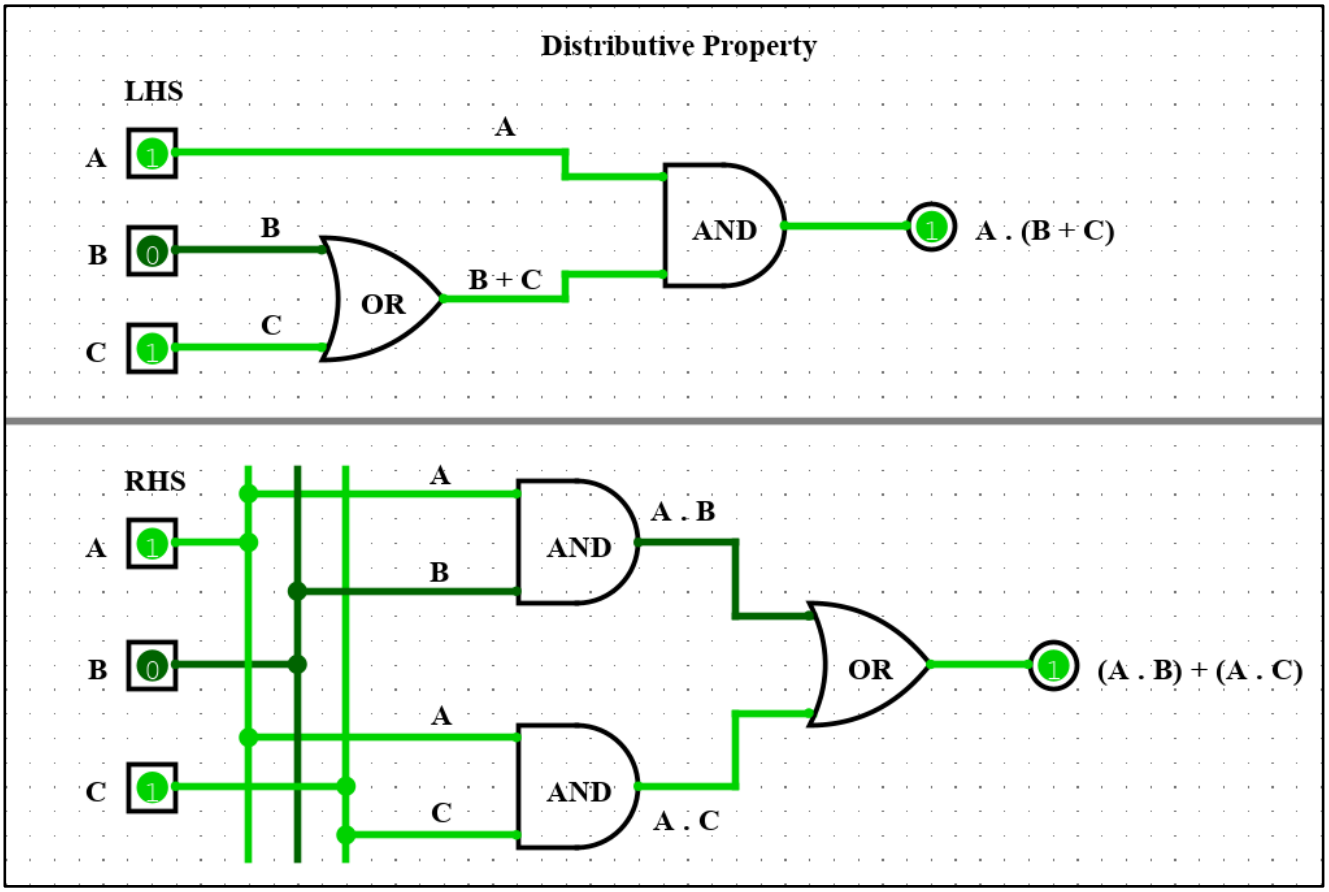
EXPT. NO: 01	VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES
DATE:	

(2) Distributive Property: A . (B + C) = (A . B) + (A . C)

Truth Table:

A	B	C	B + C	A . (B + C)	A . B	A . C	(A . B) + (A . C)
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

Circuit Diagram:



EXPT. NO: 02 DATE:	IMPLEMENTATION OF HALF – ADDER AND FULL – ADDER USING LOGIC GATES

(1) Half – Adder:

Truth Table:

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

K – Map:

SUM

B \ A	0	1
0	0	1
1	1	0

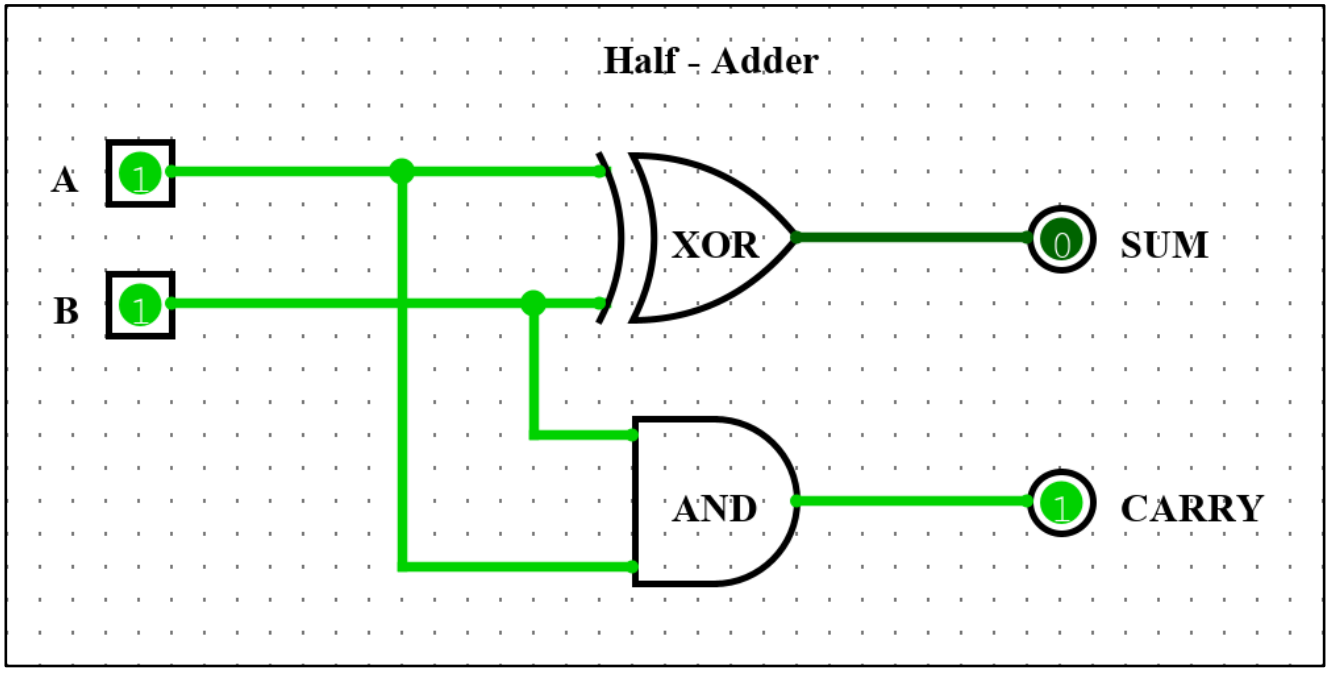
Sum = $A\overline{B} + \overline{A}B = A \oplus B$

CARRY

B \ A	0	1
0	0	0
1	0	1

Carry = AB

Circuit Diagram:



EXPT. NO: 02 DATE:	IMPLEMENTATION OF HALF – ADDER AND FULL – ADDER USING LOGIC GATES

(2) Full – Adder:

Truth Table:

A	B	C_{in}	SUM	$CARRY_{out}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K – Map:

SUM

A \ BC_{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

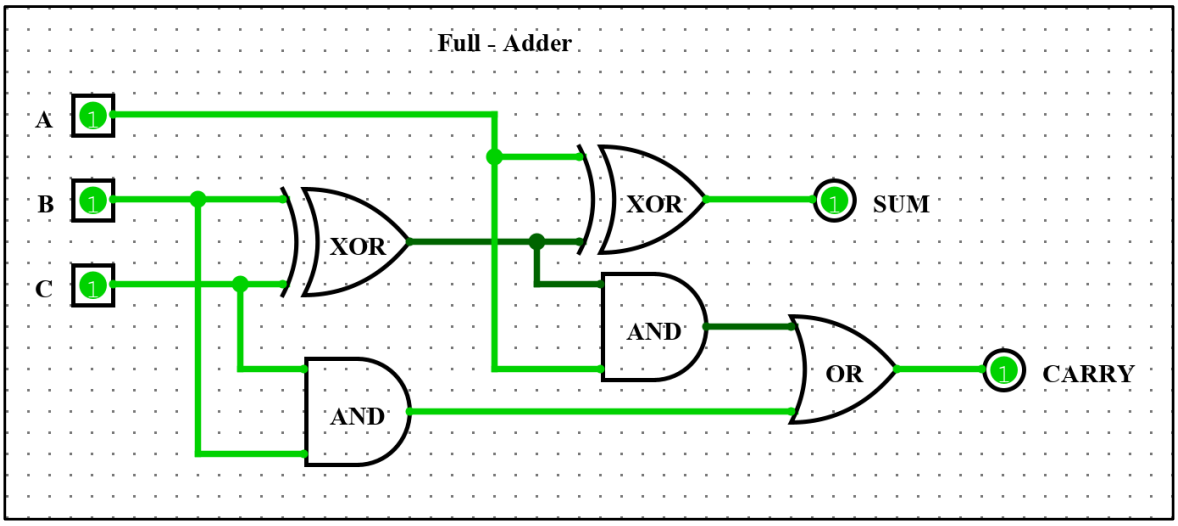
$CARRY_{out}$

A \ BC_{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$Carry_{out} = AB + AC_{in} + BCin$$

Circuit Diagram:



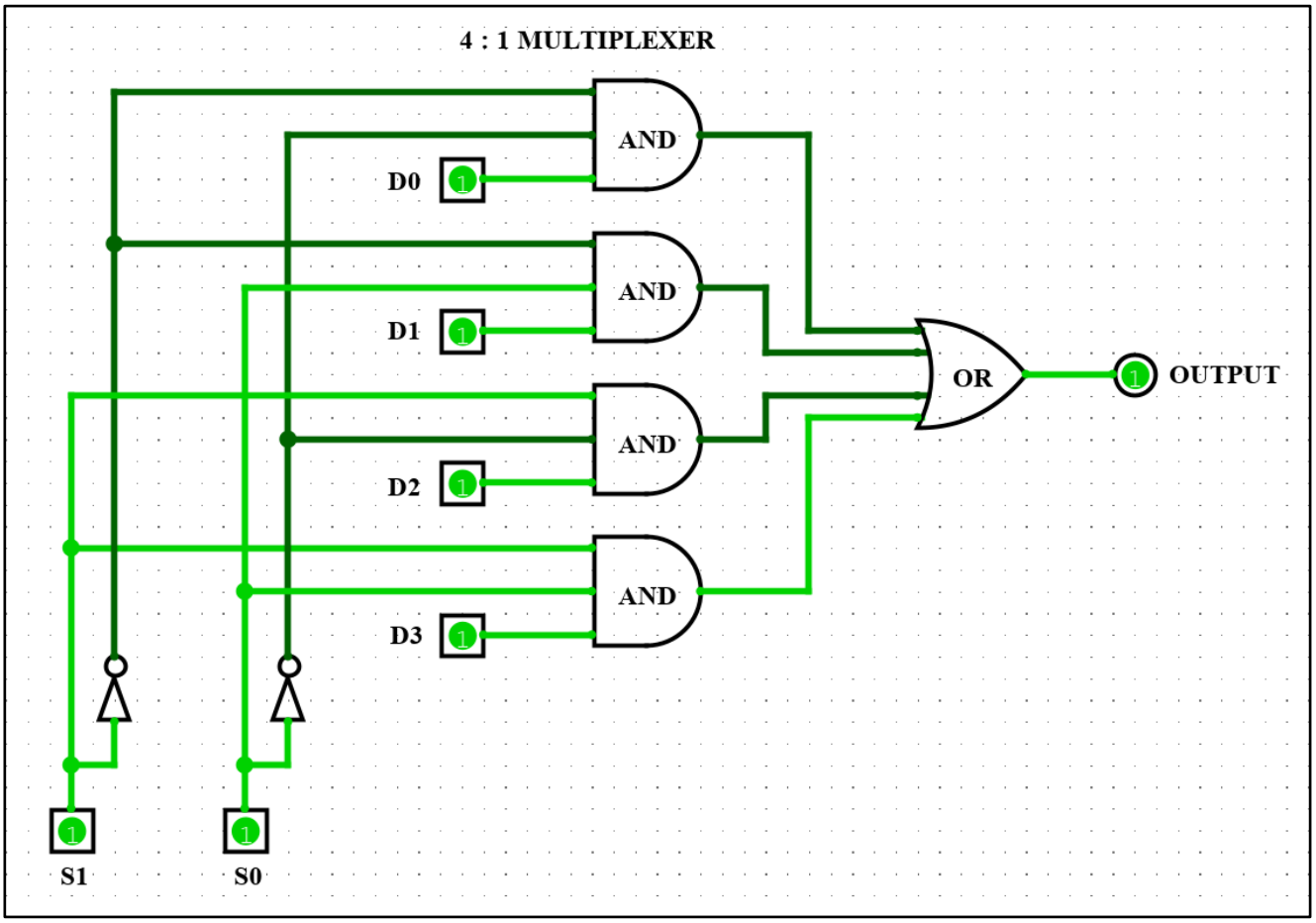
EXPT. NO: 03	IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER
DATE:	

(1) 4 : 1 MULTIPLEXER:

Truth Table:

S1	S0	OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Circuit Diagram:



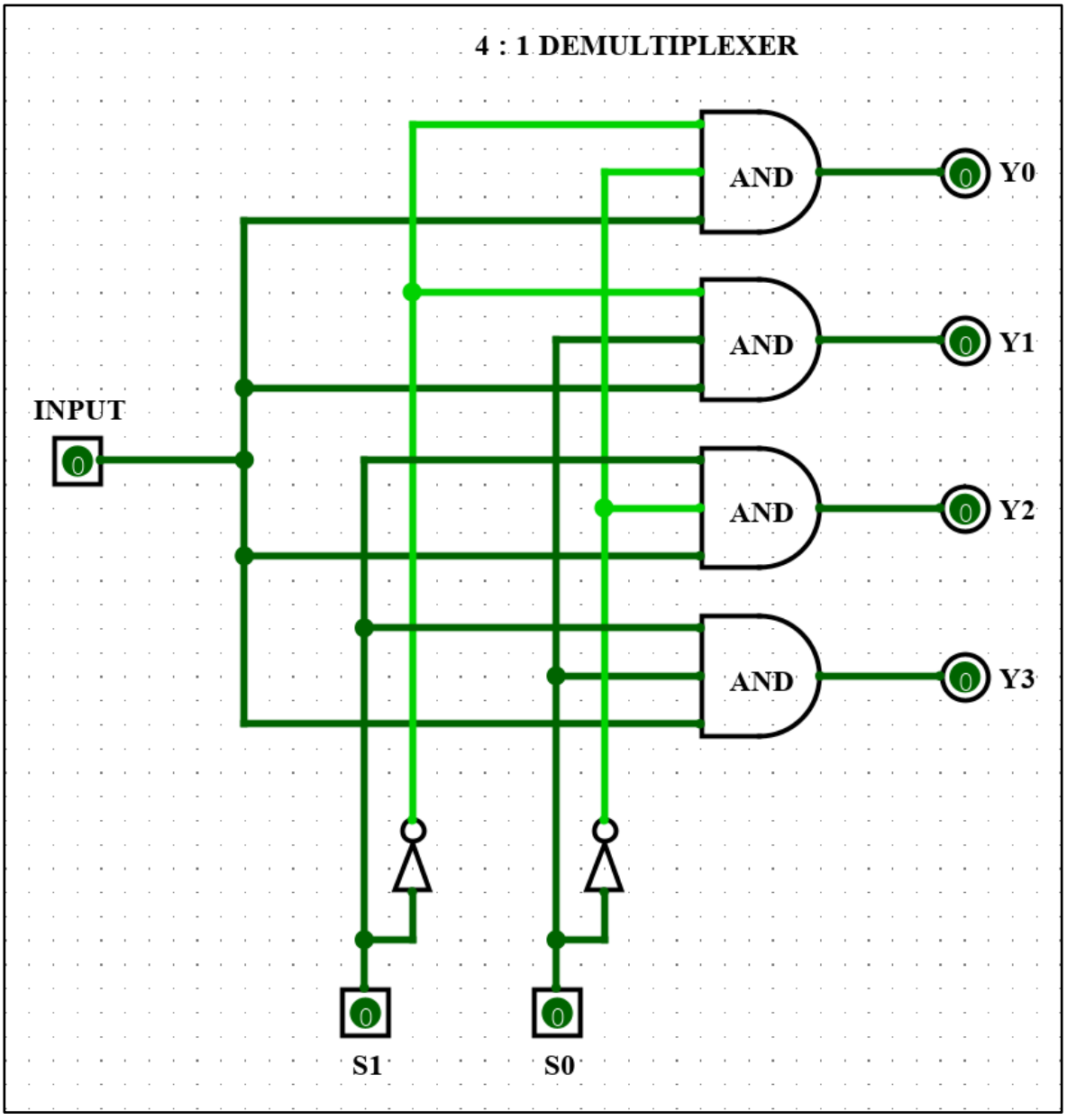
EXPT. NO: 03 DATE:	IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER

(2) 1 : 4 DEMULTIPLEXER:

Truth Table:

SELECTOR LINES		OUTPUT			
S0	**S1**	**Y0**	**Y1**	**Y2**	**Y3**
0	0	**D**	0	0	0
0	1	0	**D**	0	0
1	0	0	0	**D**	0
1	1	0	0	0	**D**

Circuit Diagram:



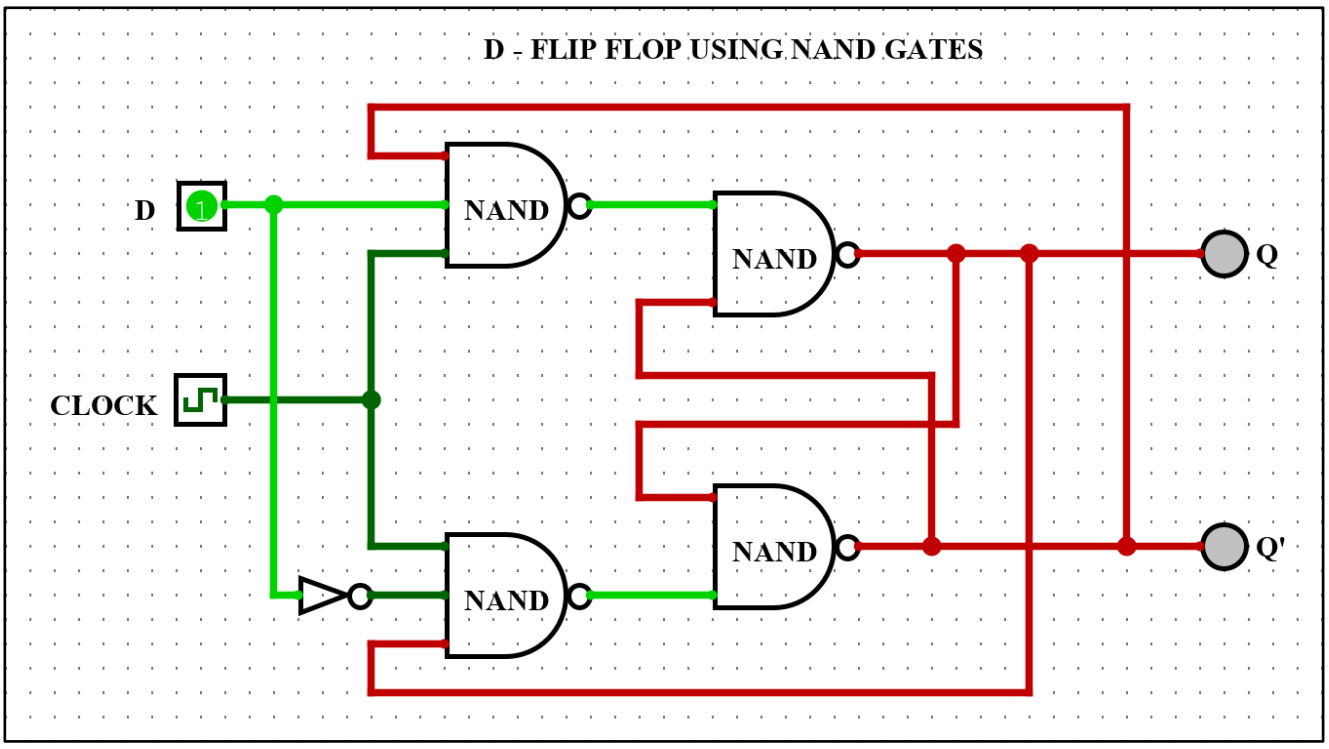
EXPT. NO: 04	DESIGN OF D AND JK FLIP FLOPS USING NAND GATES
DATE:	

(1) D FLIP – FLOP:

Truth Table:

CLOCK	D	Q_n	Q_{n+1}
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Circuit Diagram:



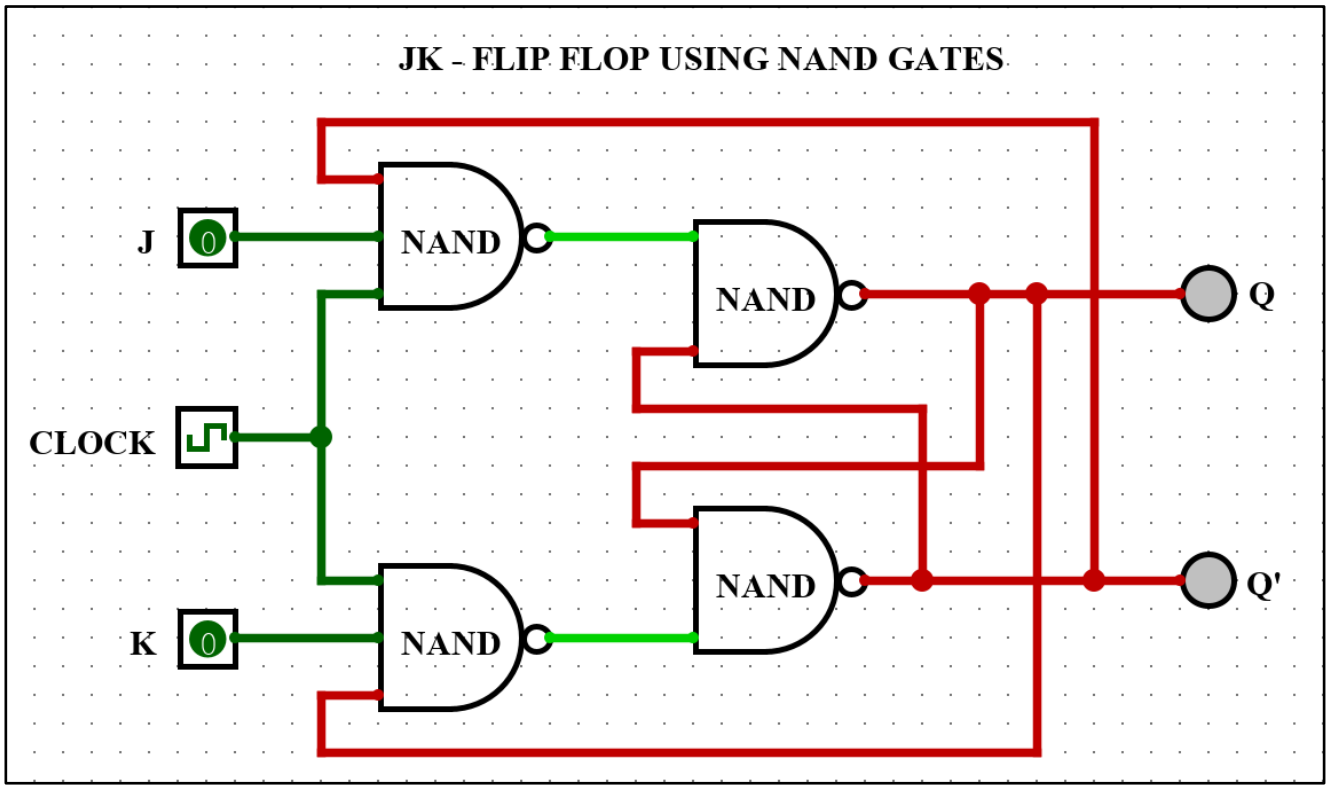
EXPT. NO: 04 DATE:	DESIGN OF D AND JK FLIP FLOPS USING NAND GATES

(2) JK FLIP – FLOP:

Truth Table:

CLOCK	J	K	Q_{n+1}	STATE
1	0	0	Q_n	No Change
1	0	1	0	Reset (0)
1	1	0	1	Set (1)
1	1	1	$\overline{Q}_n$	Toggle

Circuit Diagram:



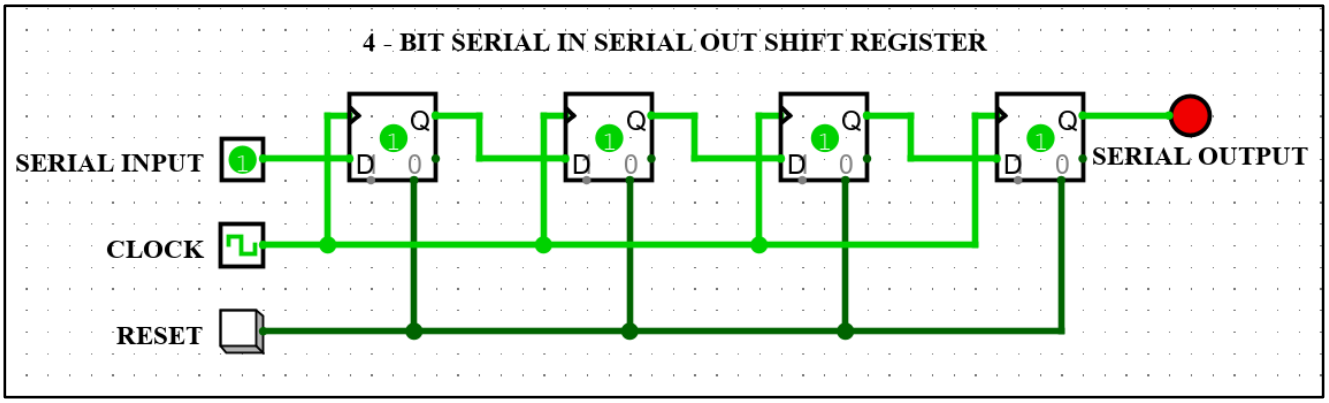
EXPT. NO: 05	IMPLEMENTATION OF SISO AND PIPO SHIFT REGISTER USING FLIP - FLOPS
DATE:	

(1) SISO SHIFT REGISTER USING D FLIP – FLOP:

Truth Table:

CLOCK	Q_0	Q_1	Q_2	Q_3
Initially	0	0	0	0
1st falling edge	1	0	0	0
2nd falling edge	1	1	0	0
3rd falling edge	1	1	1	0
4th falling edge	1	1	1	1

Circuit Diagram:



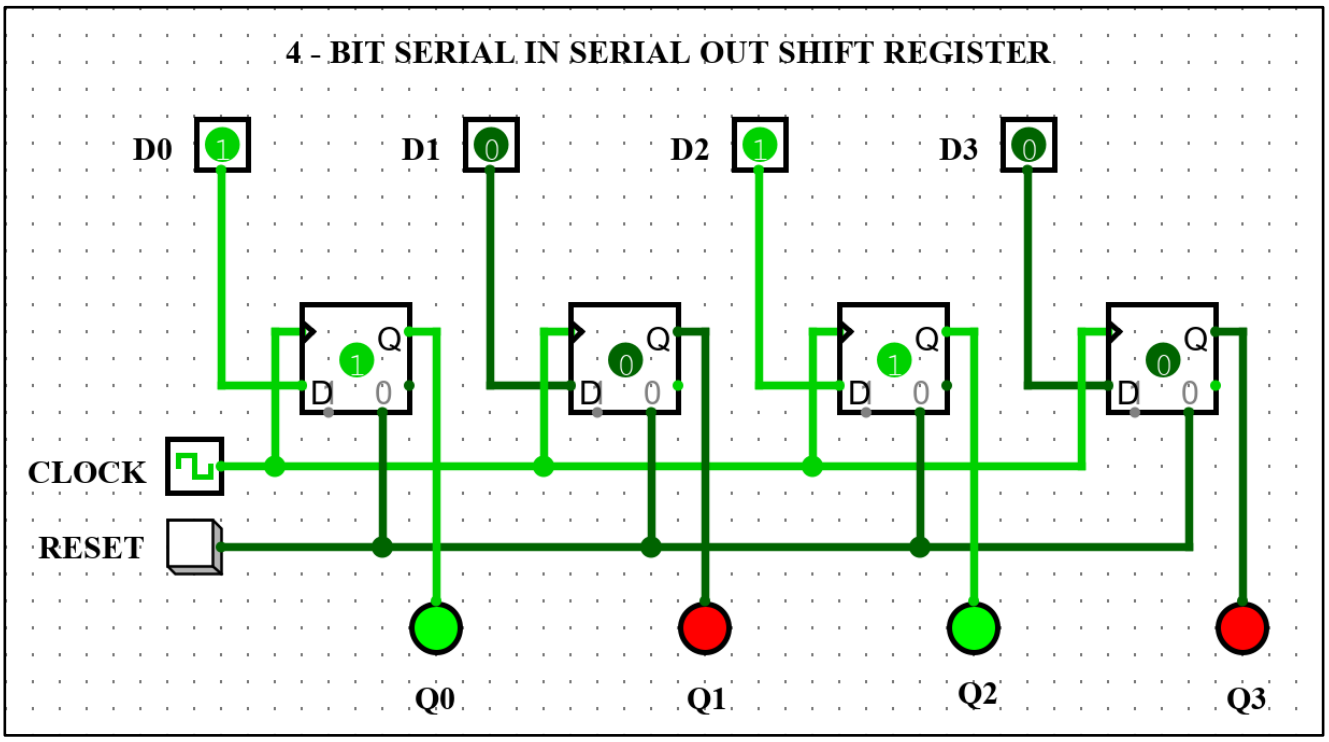
EXPT. NO: 05	IMPLEMENTATION OF SISO AND PIPO SHIFT REGISTER USING FLIP - FLOPS
DATE:	

(2) PIPO SHIFT REGISTER USING D FLIP – FLOP:

Truth Table:

CLOCK	DATA INPUT				OUTPUT			
	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

Circuit Diagram:



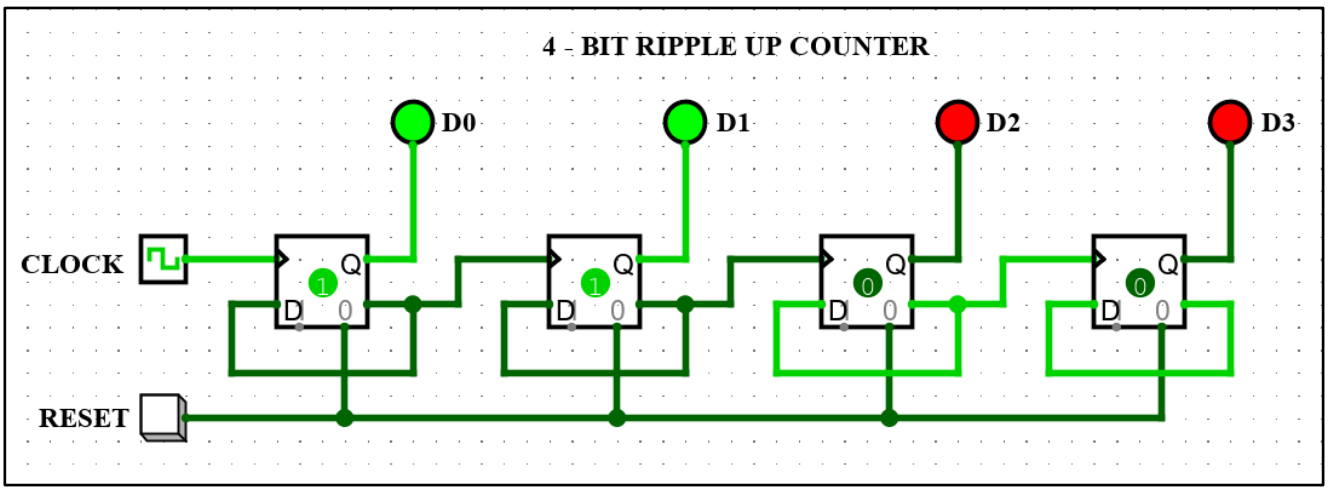
EXPT. NO: 06	CONSTRUCTION AND VERIFICATION OF 4 – BIT RIPPLE COUNTER
DATE:	

(1) 4 – BIT RIPPLE UP COUNTER:

Truth Table:

CLOCK PULSES	D_3	D_2	D_1	D_0
Initially (0)	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Circuit Diagram:



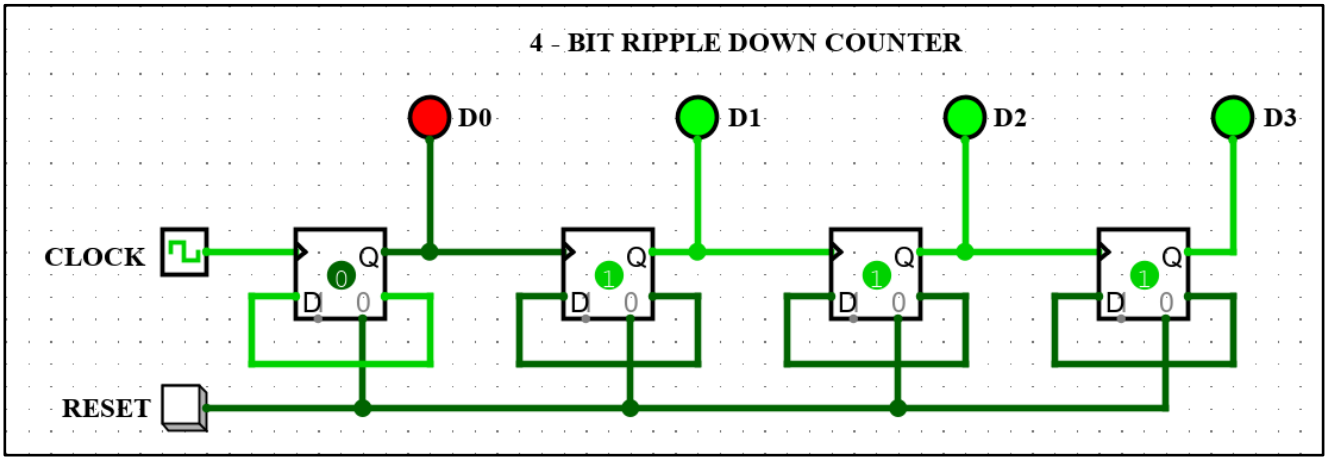
EXPT. NO: 06 DATE:	CONSTRUCTION AND VERIFICATION OF 4 – BIT RIPPLE COUNTER

(2) 4 – BIT RIPPLE DOWN COUNTER:

Truth Table:

CLOCK PULSES	D_3	D_2	D_1	D_0
Initially	0	0	0	0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1

Circuit Diagram:



EXPT. NO: 07	DESIGN AND IMPLEMENTATION OF 2 - BIT ALU USING VARIOUS COMBINATIONAL CIRCUITS
DATE:	

2 – BIT ARITHMETIC LOGIC UNIT:

Circuit Diagram: