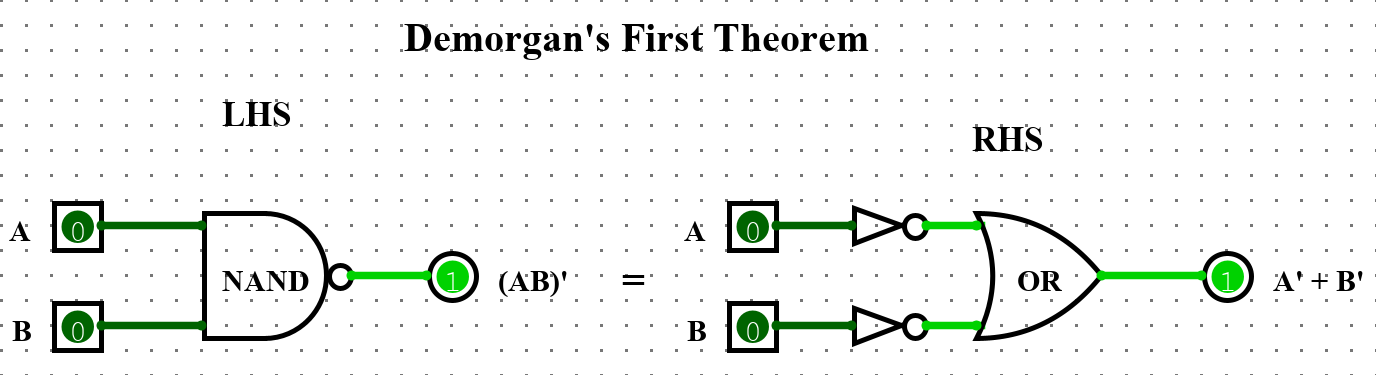
|  |  |
| --- | --- |
| **EXPT. NO: 01** | **VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES** |
| **DATE:** |

**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **AB** |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |

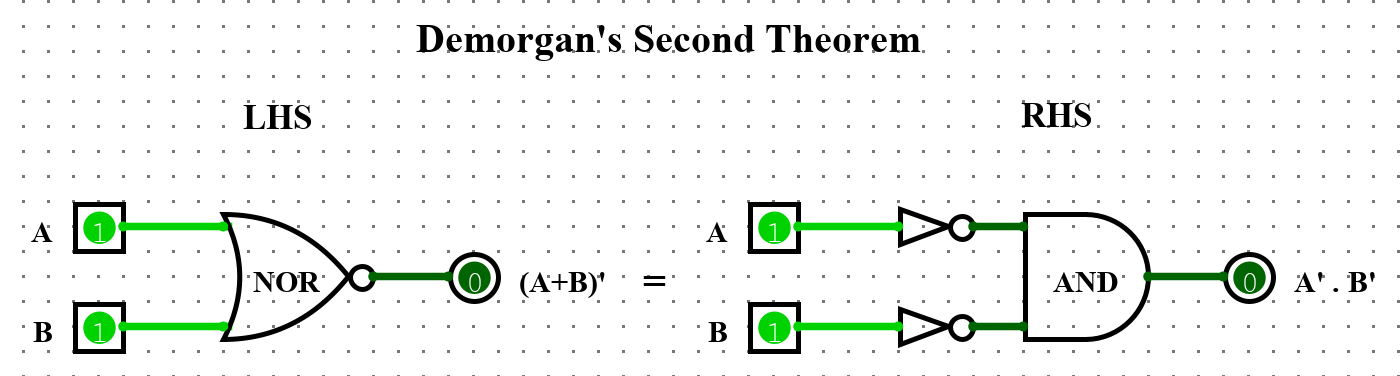
**Circuit Diagram:**



**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **A + B** |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |

**Circuit Diagram:**



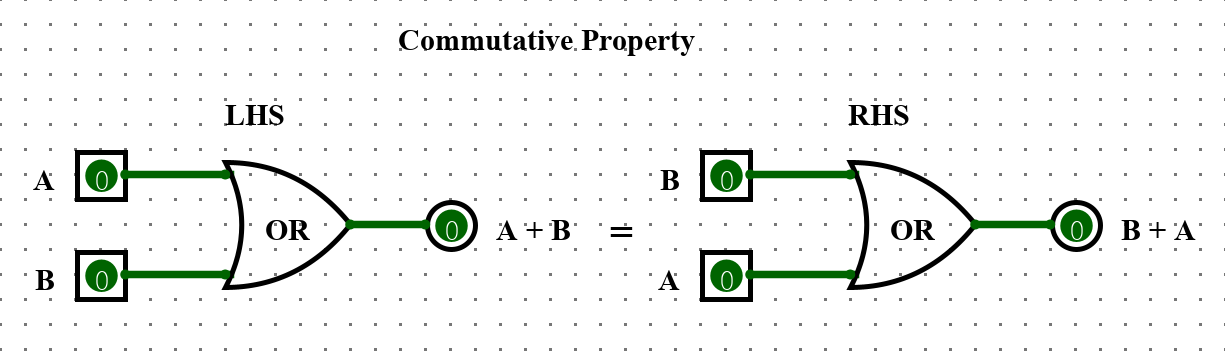
|  |  |
| --- | --- |
| **EXPT. NO: 01** | **VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES** |
| **DATE:** |

1. **A + B = B + A**

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **A + B** | **B + A** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

**Circuit Diagram:**

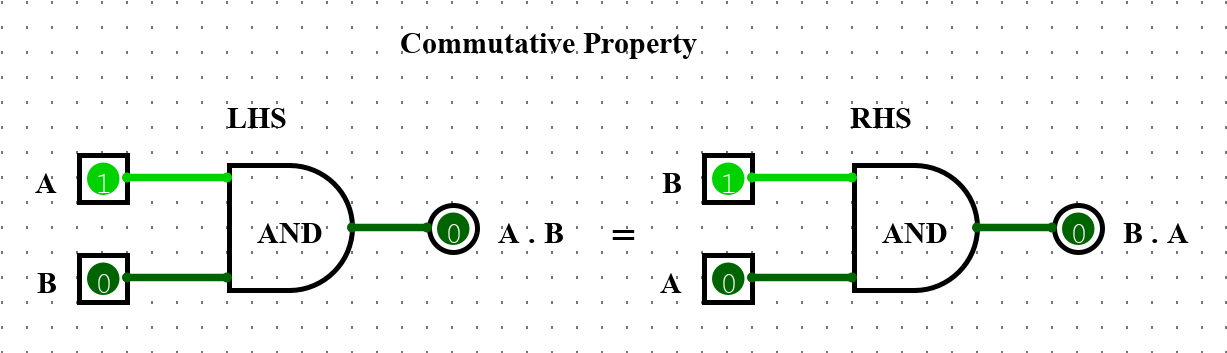
****

1. **A . B = B . A**

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **A . B** | **B . A** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Circuit Diagram:**



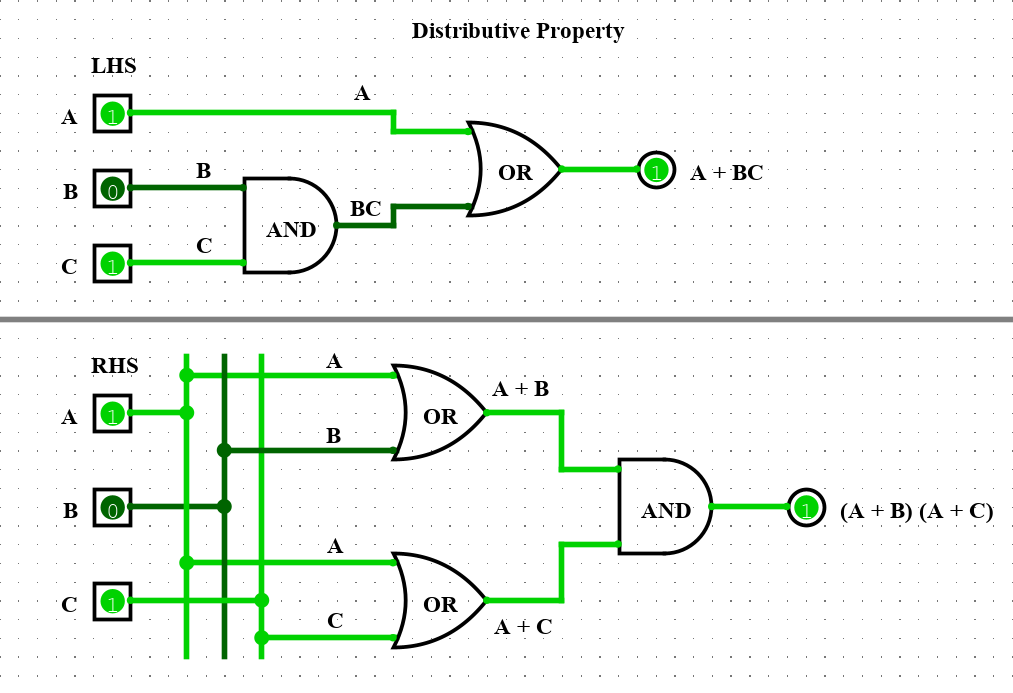
|  |  |
| --- | --- |
| **EXPT. NO: 01** | **VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES** |
| **DATE:** |

1. **A + BC = (A + B) (A + C)**

**Truth Table:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **BC** | **A + BC** | **A + B** | **A + C** | **(A + B) . (A + C)** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Circuit Diagram:**



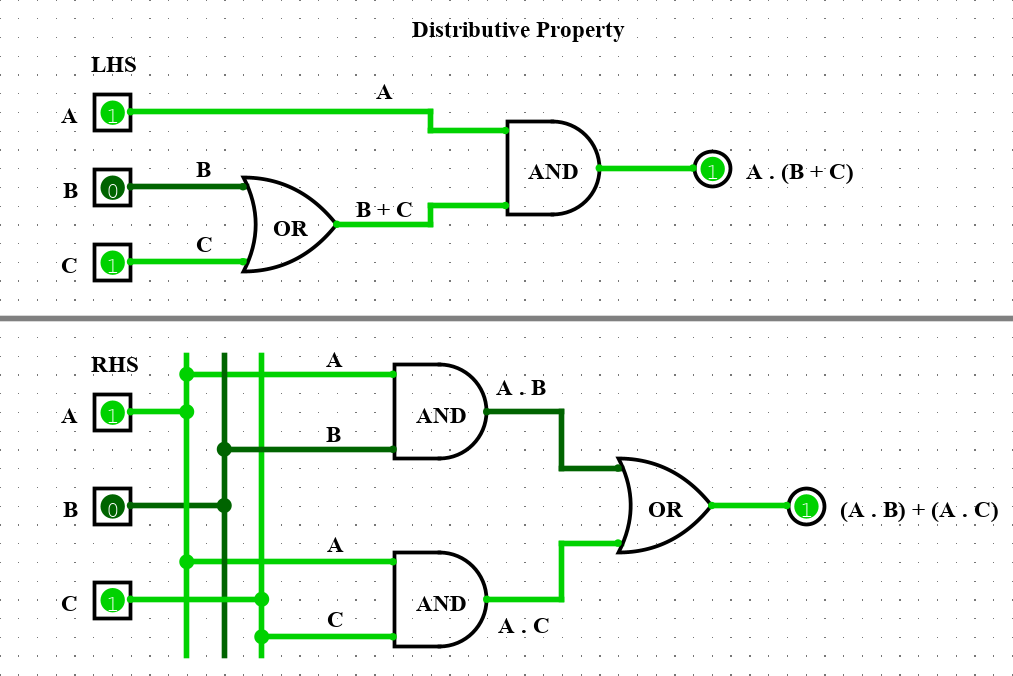
|  |  |
| --- | --- |
| **EXPT. NO: 01** | **VERIFICATION OF BOOLEAN THEOREMS USING LOGIC GATES** |
| **DATE:** |

1. **A . (B + C) = (A . B) + (A . C)**

**Truth Table:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **B + C** | **A . (B + C)** | **A . B** | **A . C** | **(A . B) + (A . C)** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Circuit Diagram:**



|  |  |
| --- | --- |
| **EXPT. NO: 02** | **IMPLEMENTATION OF HALF – ADDER AND FULL – ADDER USING LOGIC GATES** |
| **DATE:** |



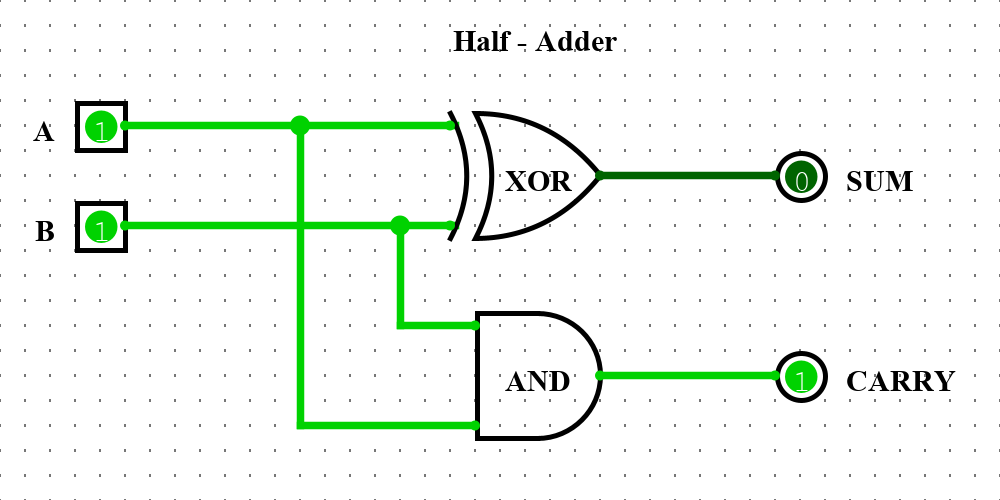
**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **SUM** | **CARRY** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**K – Map:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **SUM**   |  |  |  | | --- | --- | --- | | **A**  **B** | **0** | **1** | | **0** | 0 | 1 | | **1** | 1 | 0 |   Sum = A + B = A B | **CARRY**   |  |  |  | | --- | --- | --- | | **A**  **B** | **0** | **1** | | **0** | 0 | 0 | | **1** | 0 | 1 |   Carry = AB |

**Circuit Diagram:**

****

|  |  |
| --- | --- |
| **EXPT. NO: 02** | **IMPLEMENTATION OF HALF – ADDER AND FULL – ADDER USING LOGIC GATES** |
| **DATE:** |



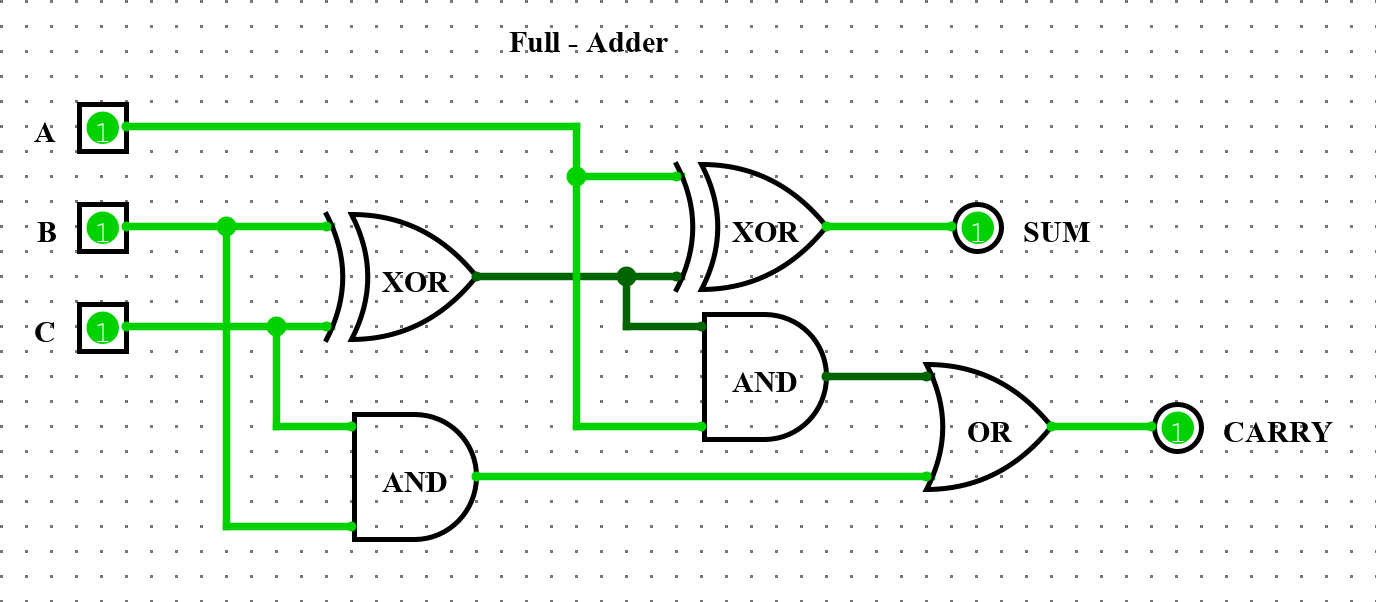
**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Cin** | **SUM** | **CARRYout** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**K – Map:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **SUM**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **BCin**  **A** | **00** | **01** | **11** | **10** | | **0** | 0 | 1 | 0 | 1 | | **1** | 1 | 0 | 1 | 0 |   Sum = | **CARRYout**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **BCin**  **A** | **00** | **01** | **11** | **10** | | **0** | 0 | 0 | 1 | 0 | | **1** | 0 | 1 | 1 | 1 |   Carryout = AB + ACin + BCin |

**Circuit Diagram:**

****

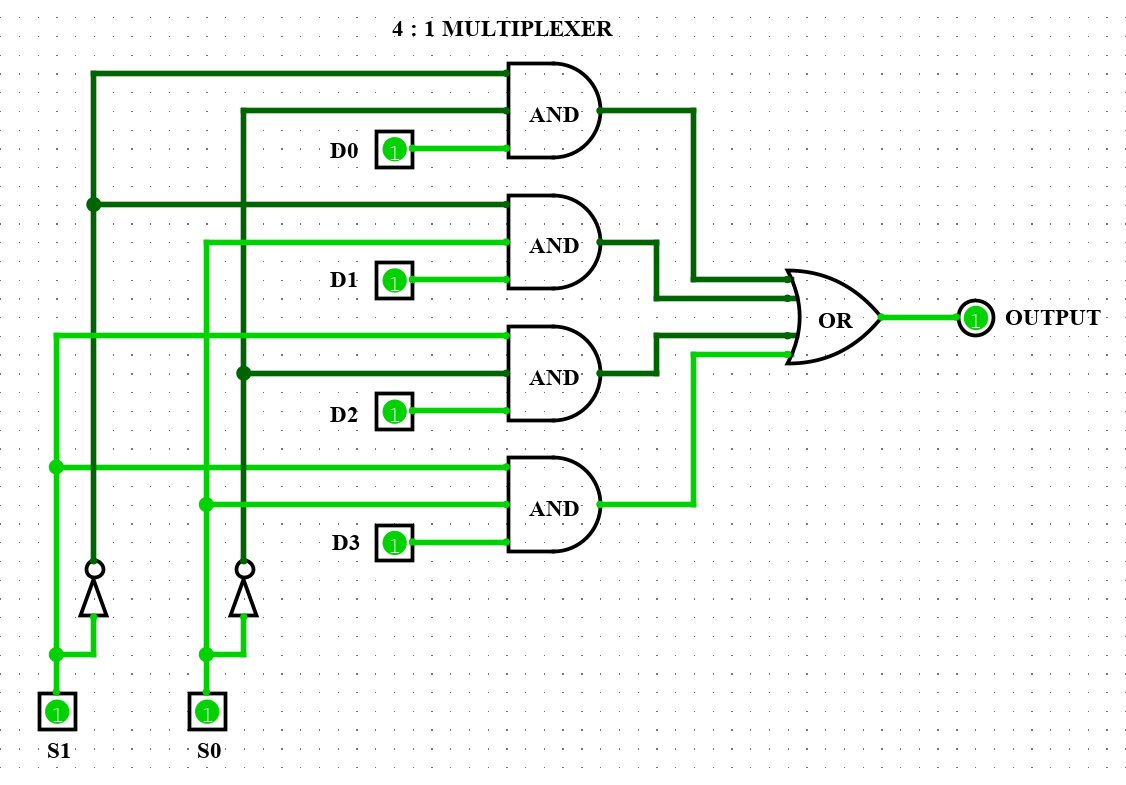
|  |  |
| --- | --- |
| **EXPT. NO: 03** | **IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER** |
| **DATE:** |



**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **S1** | **S0** | **OUTPUT** |
| 0 | 0 | D0 |
| 0 | 1 | D1 |
| 1 | 0 | D2 |
| 1 | 1 | D3 |

**Circuit Diagram:**

****

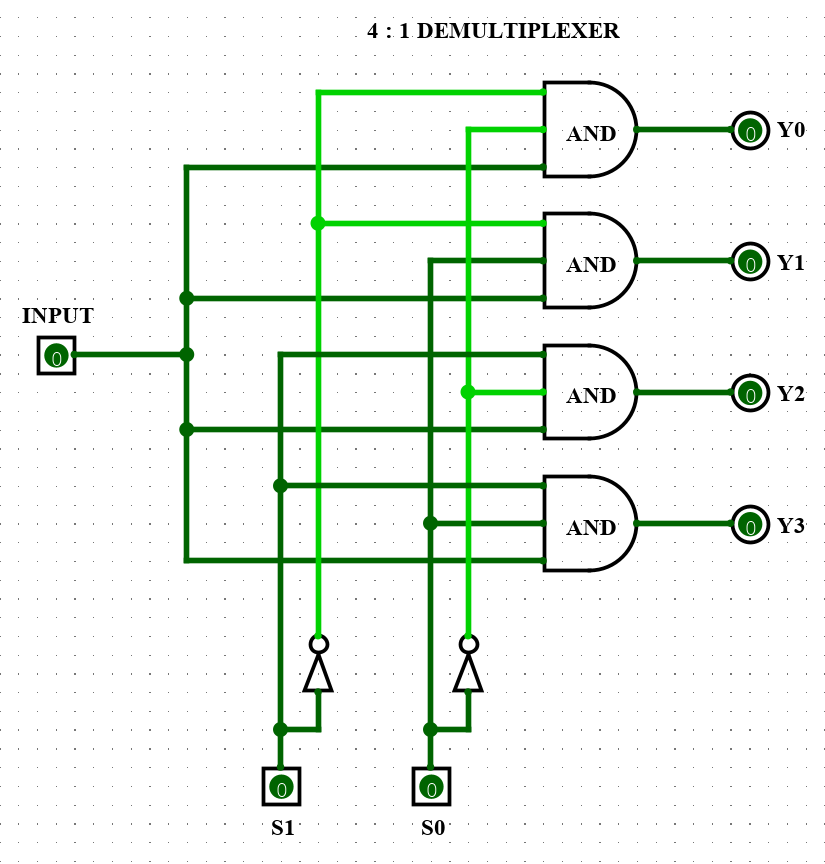
|  |  |
| --- | --- |
| **EXPT. NO: 03** | **IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER** |
| **DATE:** |



**Truth Table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SELECTOR LINES** | | **OUTPUT** | | | |
| **S0** | **S1** | **Y0** | **Y1** | **Y2** | **Y3** |
| 0 | 0 | **D** | 0 | 0 | 0 |
| 0 | 1 | 0 | **D** | 0 | 0 |
| 1 | 0 | 0 | 0 | **D** | 0 |
| 1 | 1 | 0 | 0 | 0 | **D** |

**Circuit Diagram:**

****

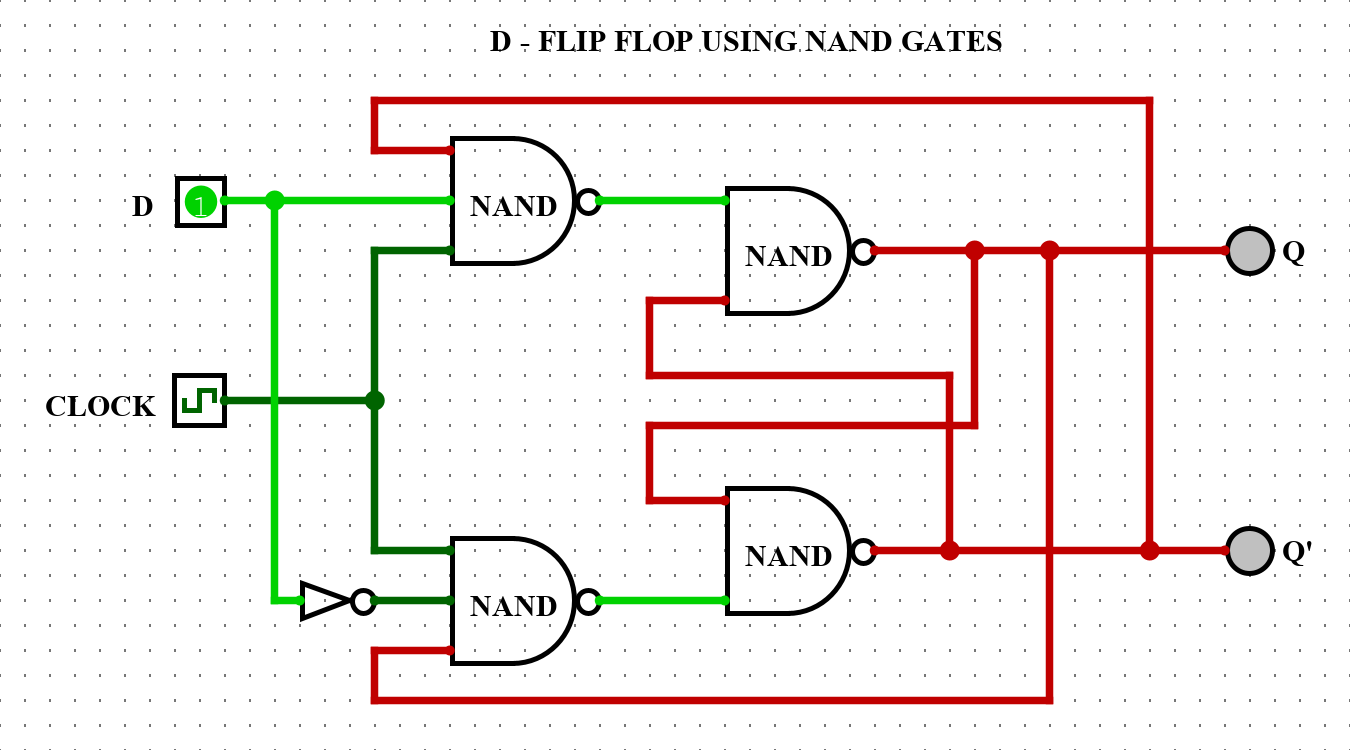
|  |  |
| --- | --- |
| **EXPT. NO: 04** | **DESIGN OF D AND JK FLIP FLOPS USING NAND GATES** |
| **DATE:** |



**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLOCK** | **D** | **Qn** | **Qn+1** |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Circuit Diagram:**

****

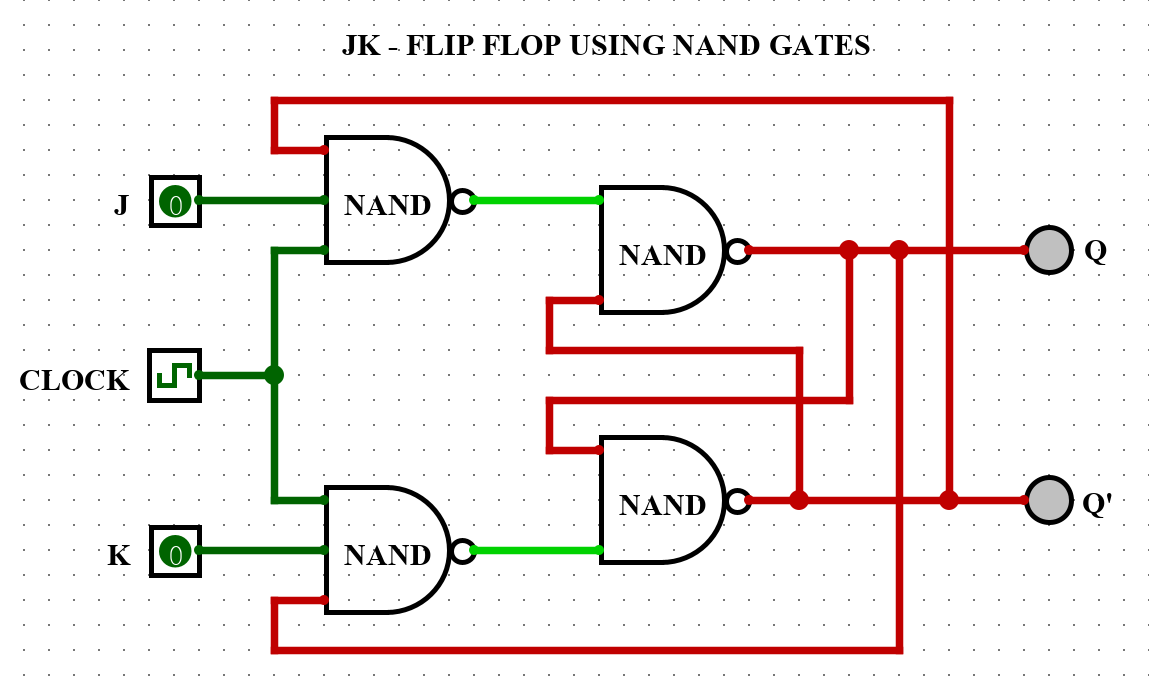
|  |  |
| --- | --- |
| **EXPT. NO: 04** | **DESIGN OF D AND JK FLIP FLOPS USING NAND GATES** |
| **DATE:** |



**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLOCK** | **J** | **K** | **Qn+1** | **STATE** |
| 1 | 0 | 0 | Qn | No Change |
| 1 | 0 | 1 | 0 | Reset (0) |
| 1 | 1 | 0 | 1 | Set (1) |
| 1 | 1 | 1 |  | Toggle |

**Circuit Diagram:**

****

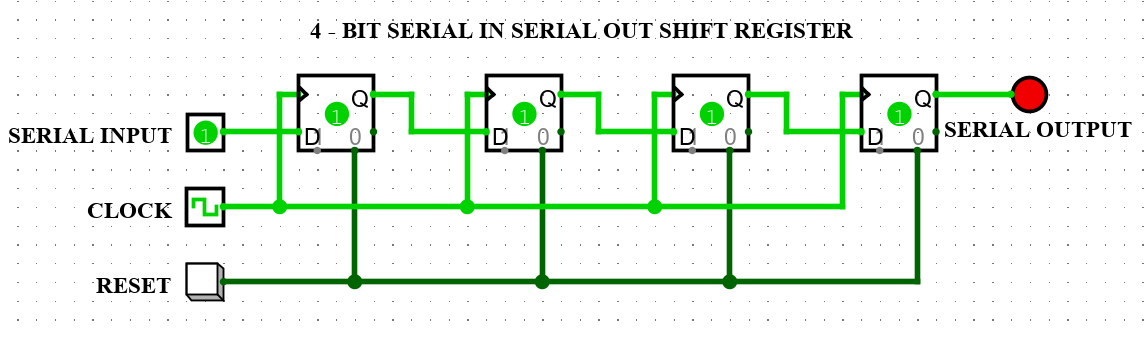
|  |  |
| --- | --- |
| **EXPT. NO: 05** | **IMPLEMENTATION OF SISO AND PIPO SHIFT REGISTER**  **USING FLIP - FLOPS** |
| **DATE:** |



**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLOCK** | **Q0** | **Q1** | **Q2** | **Q3** |
| Initially | 0 | 0 | 0 | 0 |
| 1st falling edge | 1 | 0 | 0 | 0 |
| 2nd falling edge | 1 | 1 | 0 | 0 |
| 3rd falling edge | 1 | 1 | 1 | 0 |
| 4th falling edge | 1 | 1 | 1 | 1 |

**Circuit Diagram:**

****

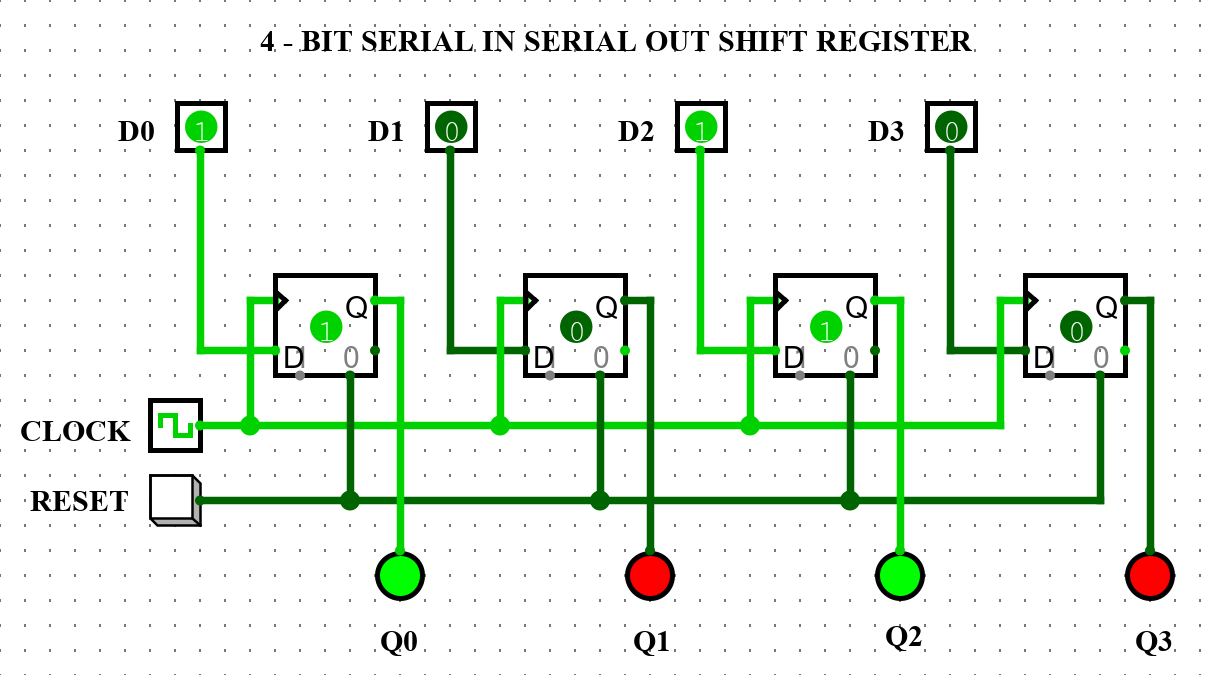
|  |  |
| --- | --- |
| **EXPT. NO: 05** | **IMPLEMENTATION OF SISO AND PIPO SHIFT REGISTER**  **USING FLIP - FLOPS** |
| **DATE:** |



**Truth Table:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **CLOCK** | **DATA INPUT** | | | | **OUTPUT** | | | |
| **D0** | **D1** | **D2** | **D3** | **Q0** | **Q1** | **Q2** | **Q3** |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 2 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

**Circuit Diagram:**

****

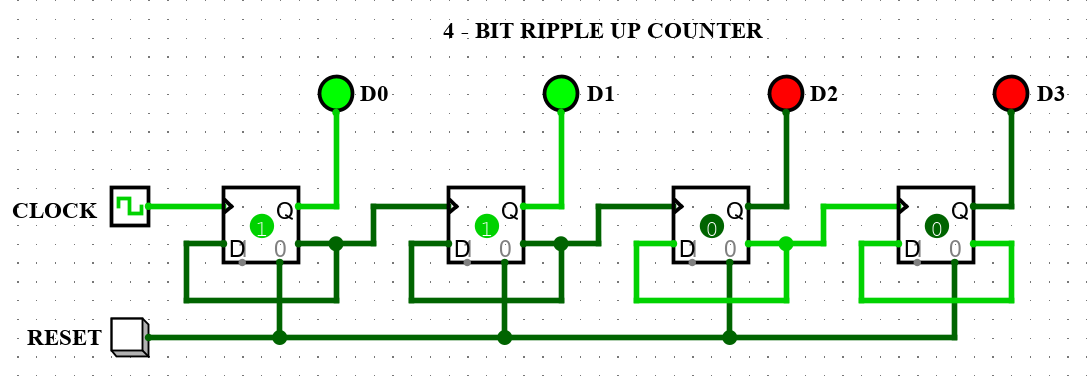
|  |  |
| --- | --- |
| **EXPT. NO: 06** | **CONSTRUCTION AND VERIFICATION OF 4 – BIT RIPPLE COUNTER** |
| **DATE:** |



**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLOCK PULSES** | **D3** | **D2** | **D1** | **D0** |
| **Initially (0)** | 0 | 0 | 0 | 0 |
| **1** | 0 | 0 | 0 | 1 |
| **2** | 0 | 0 | 1 | 0 |
| **3** | 0 | 0 | 1 | 1 |
| **4** | 0 | 1 | 0 | 0 |
| **5** | 0 | 1 | 0 | 1 |
| **6** | 0 | 1 | 1 | 0 |
| **7** | 0 | 1 | 1 | 1 |
| **8** | 1 | 0 | 0 | 0 |
| **9** | 1 | 0 | 0 | 1 |
| **10** | 1 | 0 | 1 | 0 |
| **11** | 1 | 0 | 1 | 1 |
| **12** | 1 | 1 | 0 | 0 |
| **13** | 1 | 1 | 0 | 1 |
| **14** | 1 | 1 | 1 | 0 |
| **15** | 1 | 1 | 1 | 1 |

**Circuit Diagram:**

****

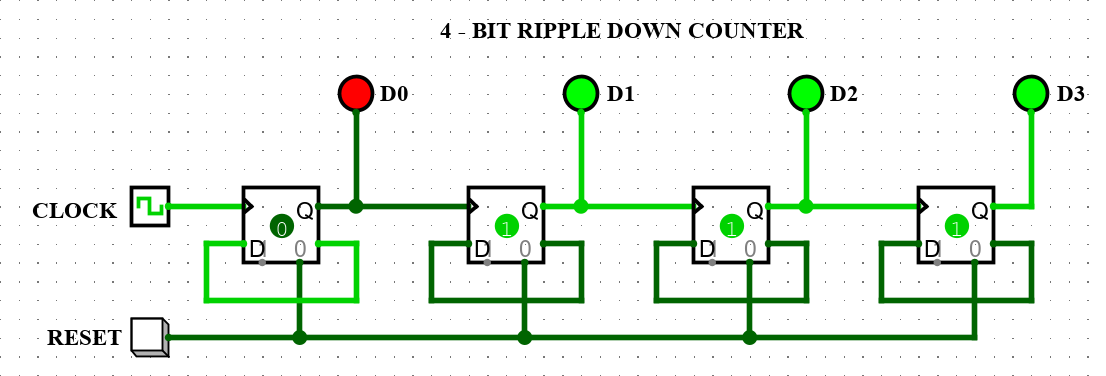
|  |  |
| --- | --- |
| **EXPT. NO: 06** | **CONSTRUCTION AND VERIFICATION OF 4 – BIT RIPPLE COUNTER** |
| **DATE:** |



**Truth Table:**

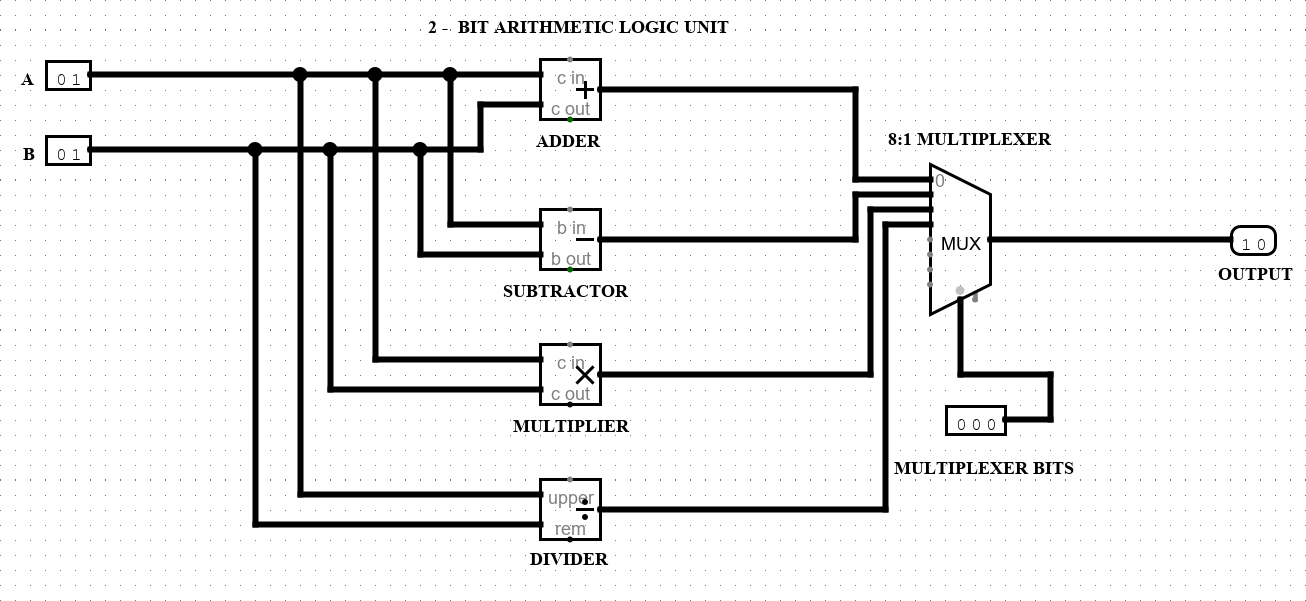
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLOCK PULSES** | **D3** | **D2** | **D1** | **D0** |
| **Initially** | 0 | 0 | 0 | 0 |
| **1** | 1 | 1 | 1 | 1 |
| **2** | 1 | 1 | 1 | 0 |
| **3** | 1 | 1 | 0 | 1 |
| **4** | 1 | 1 | 0 | 0 |
| **5** | 1 | 0 | 1 | 1 |
| **6** | 1 | 0 | 1 | 0 |
| **7** | 1 | 0 | 0 | 1 |
| **8** | 1 | 0 | 0 | 0 |
| **9** | 0 | 1 | 1 | 1 |
| **10** | 0 | 1 | 1 | 0 |
| **11** | 0 | 1 | 0 | 1 |
| **12** | 0 | 1 | 0 | 0 |
| **13** | 0 | 0 | 1 | 1 |
| **14** | 0 | 0 | 1 | 0 |
| **15** | 0 | 0 | 0 | 1 |

**Circuit Diagram:**

****

|  |  |
| --- | --- |
| **EXPT. NO: 07** | **DESIGN AND IMPLEMENTATION OF 2 - BIT ALU USING**  **VARIOUS COMBINATIONAL CIRCUITS** |
| **DATE:** |

**Circuit Diagram:**

****