

Lab 6 Report

Sathvik Kanuri

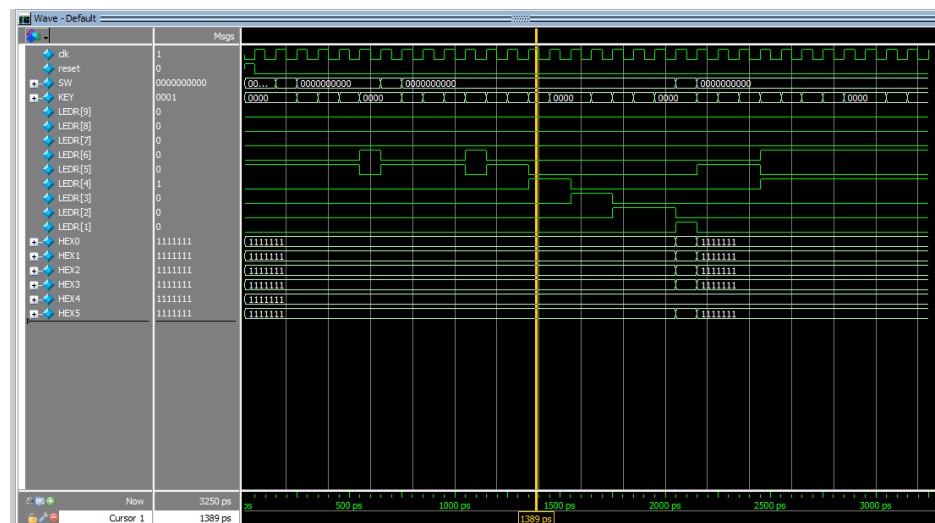
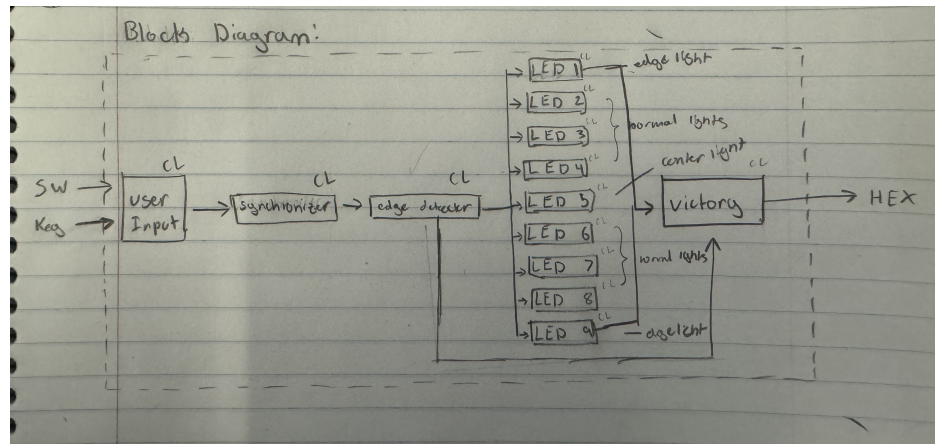
CSE 369: Intro to Digital Design

November 13 2024

Top-Level Block Diagram

Question:

The top-level block diagram, showing the major modules and how they are interconnected.

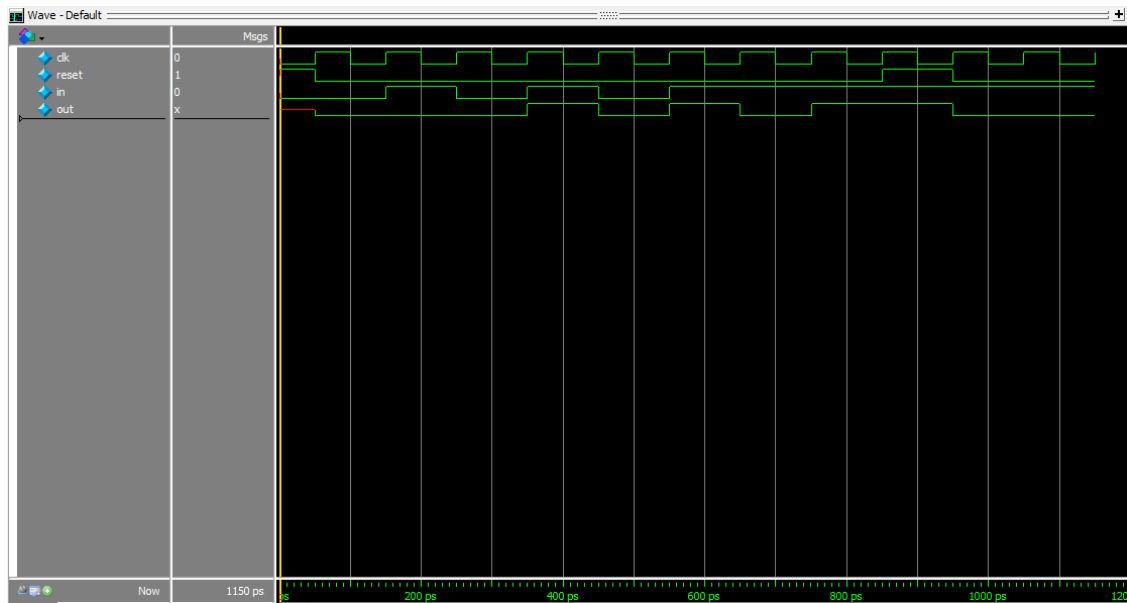


The block diagram and ModelSim for the top-level module, tug of war. The module takes in the reset switch, and the values of key 0 and key 3 as inputs. It runs the input through a synchronizer and then an edge detector to deal with metastability in user input, and then to limit button presses to one clock cycle. It then sends this input to each of 9 light modules which update according to the input and the value of the other LEDs. Finally, the victory module checks if either of the edge lights are true, and displays the value on the HEX display.

Synchronizer

Question:

The state diagram and modelsim for the synchronizer module.

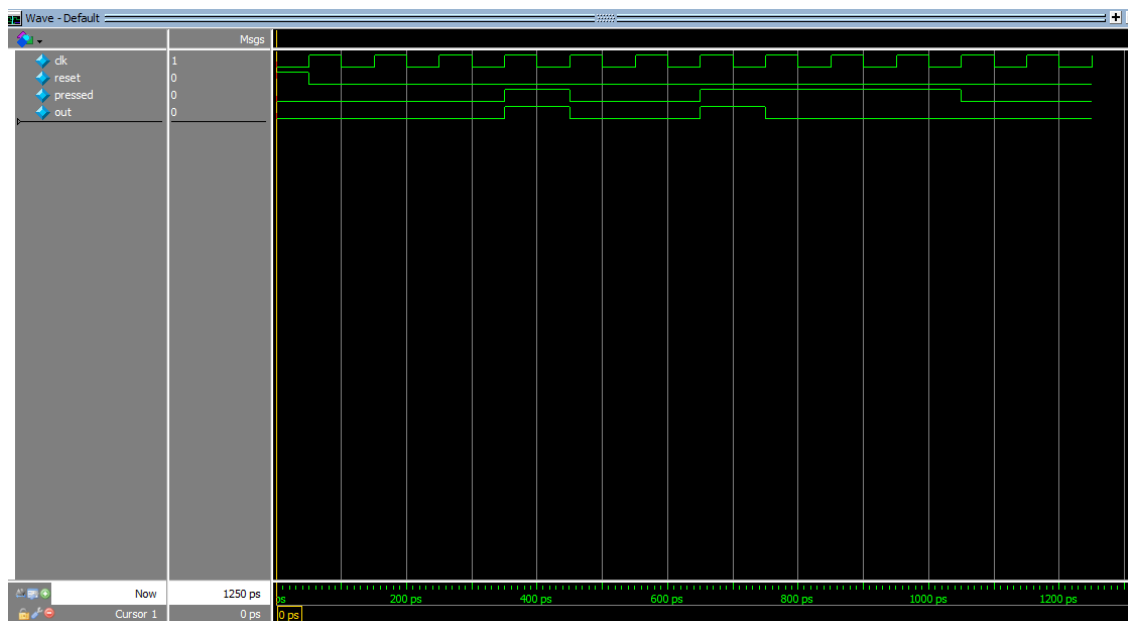
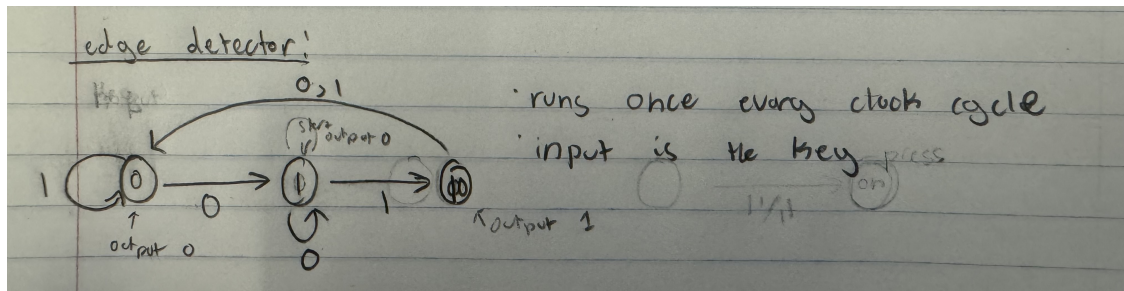


The ModelSim for the synchronizer module. The module is used to deal with metastability in user input. Runs the input through a dual flip flop to synchronize.

Edge Detector

Question:

The state diagram and modelsim for the edge detector module.

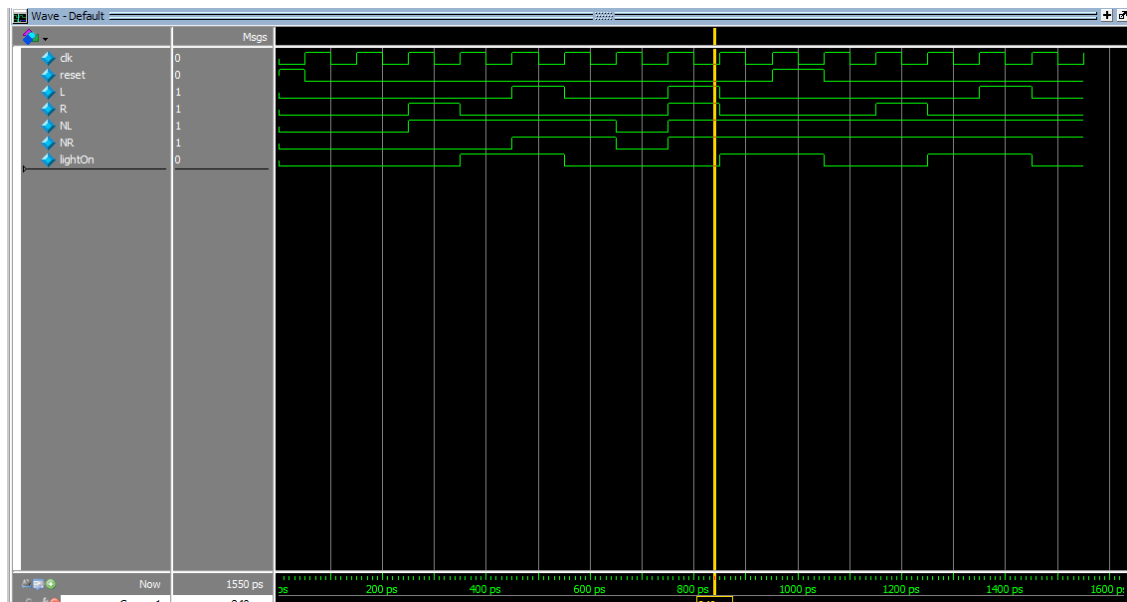
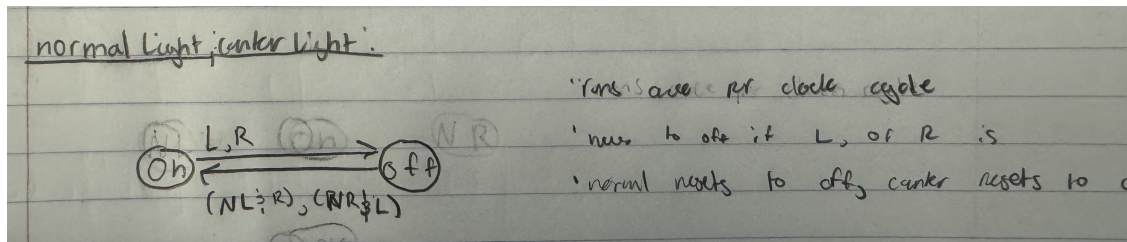


The ModelSim and FSM for the Center Light module. If the button is pressed at the time of a positive edge on the clock cycle, it goes to a state of true for one clock cycle, and then goes back to off. There are 3 states, one for being on, one for off but the button is still pressed, and one for off but the button is not pressed.

Normal Light

Question:

The state diagram and modelsim for a normal light module.

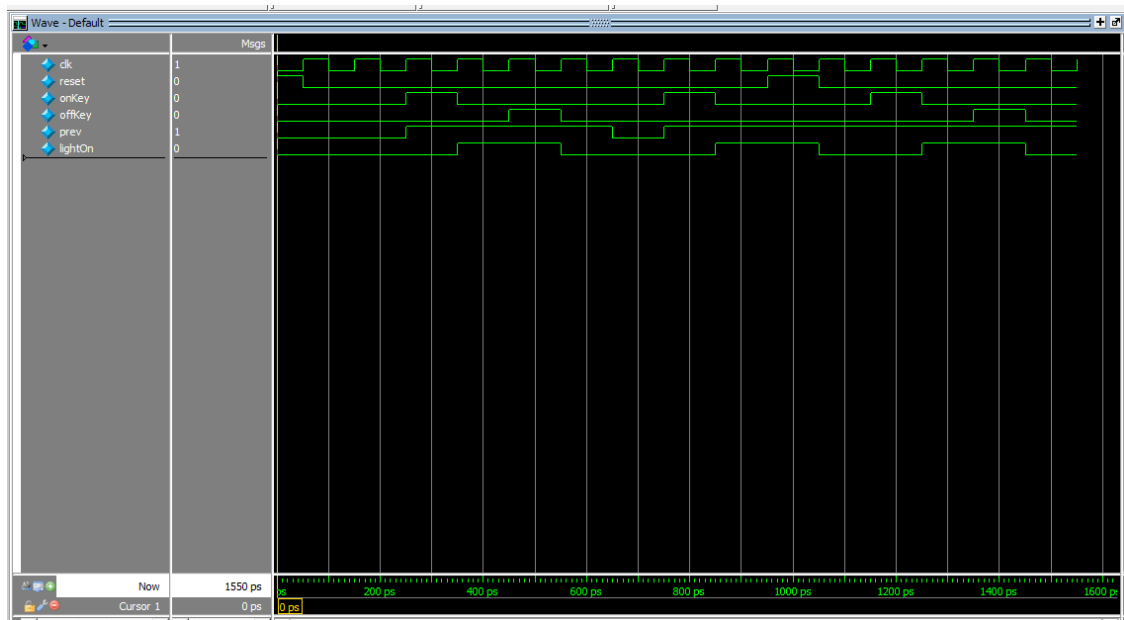
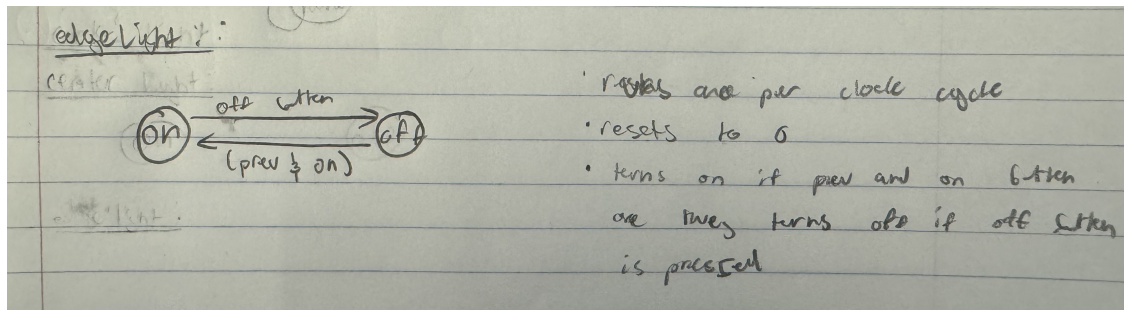


The ModelSim and FSM for the Normal Light module. If the left light and right button is true, it sets the light to on. If the right light and left button are true, it sets the light to on. If the light is on and left or right is pressed the light is set to off. It resets back to a state of false.

Edge Light

Question:

The state diagram and modelsim for a edge light module.

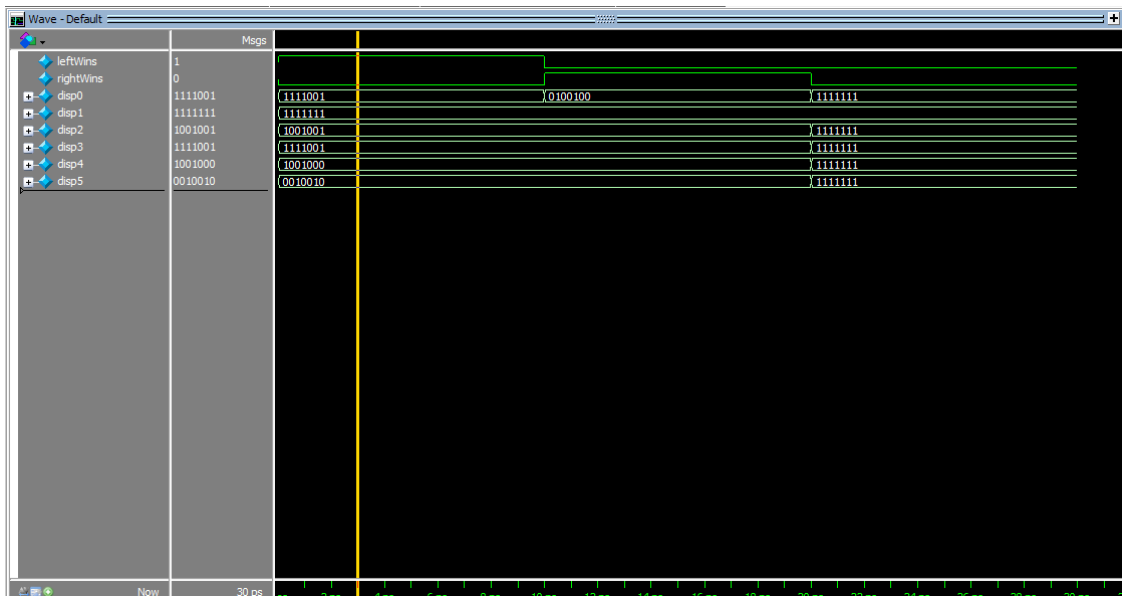
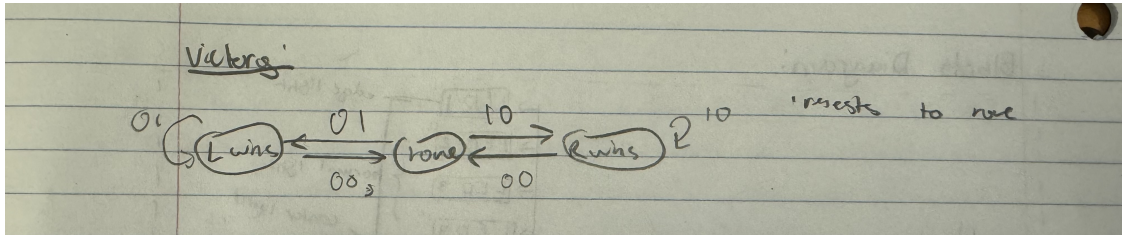


The ModelSim and FSM for the edge Light module. If the prev light and on button is true, it sets the light to on. If the light is on and the off button is pressed the light is set to off. It resets back to a state of off.

Victory

Question:

The state diagram and modelsim for the victory module.



This is the modelsim for my victory module. It takes in two inputs, leftWins and rightWins, given usually by the values of LEDR[9] and LEDR[1] respectively. It display "1 Wins" if leftWins is true, and "2 Wins" if rightWins is true. If they are both false, or reset is pressed it defaultd back to a blank dsiplay.

Resource Utilization

Question:

The resource utilization page for the module.

Analysis & Synthesis Resource Utilization by Entity										
<<Filter>>										
	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	▼ tugOfWar	19 (0)	15 (0)	0	0	67	0	tugOfWar	tugOfWar	work
1	centerLightI5	1 (1)	1 (1)	0	0	0	0	tugOfWar centerLightI5	centerLight	work
2	edgeDetector.edl	2 (2)	1 (1)	0	0	0	0	tugOfWar edgeDetector.edl	edgeDetector	work
3	edgeDetector.edr	2 (2)	1 (1)	0	0	0	0	tugOfWar edgeDetector.edr	edgeDetector	work
4	edgeLightI1	1 (1)	1 (1)	0	0	0	0	tugOfWar edgeLightI1	edgeLight	work
5	edgeLightI9	1 (1)	1 (1)	0	0	0	0	tugOfWar edgeLightI9	edgeLight	work
6	normalLightI2	1 (1)	1 (1)	0	0	0	0	tugOfWar normalLightI2	normalLight	work
7	normalLightI3	1 (1)	1 (1)	0	0	0	0	tugOfWar normalLightI3	normalLight	work
8	normalLightI4	1 (1)	1 (1)	0	0	0	0	tugOfWar normalLightI4	normalLight	work
9	normalLightI6	1 (1)	1 (1)	0	0	0	0	tugOfWar normalLightI6	normalLight	work
10	normalLightI7	1 (1)	1 (1)	0	0	0	0	tugOfWar normalLightI7	normalLight	work
11	normalLightI8	1 (1)	1 (1)	0	0	0	0	tugOfWar normalLightI8	normalLight	work
12	synch:sL	2 (2)	2 (2)	0	0	0	0	tugOfWar synch:sL	synch	work
13	synch:sR	2 (2)	2 (2)	0	0	0	0	tugOfWar synch:sR	synch	work
14	victory.vic	2 (2)	0 (0)	0	0	0	0	tugOfWar victory.vic	victory	work

My total resource utilization for the top-level module, tugOfWar.

Reflection

Question:

How many hours (estimated) it took to complete this lab in total, including reading, planning, designing, coding, debugging, and testing.

It took me around 3-3.5 hours to complete all of the lab.