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CPU Architecture Comparison Chart

Architecture	Key Features	Instruction Set	Typical Bit Width	Example CPUs / Vendors	Use Cases / Profiles
Von Neumann	Shared memory for data & code	Varies	8, 16, 32, 64	Early computers, general-purpose	PCs, servers, embedded
Harvard	Separate memory for data & code	Varies	8, 16, 32	Microcontrollers, DSPs	Embedded, real-time, signal processing
CISC	Complex instructions, fewer lines	x86, x86-64	32, 64	Intel, AMD (desktop/server CPUs)	PCs, servers, laptops
RISC	Simple instructions, faster cycles	ARM, RISC-V	32, 64	ARM, Apple, many embedded CPUs	Smartphones, tablets, embedded, IoT
SIMD	Parallel data processing	SSE, AVX, NEON	128, 256, 512	Intel, AMD, ARM	Multimedia, scientific, AI workloads
Multicore	Multiple CPU cores on one chip	Any	32, 64	Intel, AMD, ARM, Apple	Multitasking, servers, high performance
Stack-based	Uses stack for operations	Varies	8, 16, 32	Early calculators, JVM	Embedded, virtual machines
Register-based	Uses registers for operations	Varies	8, 16, 32, 64	Most modern CPUs	All general-purpose computing

Major CPU Architecture Types Explained

- **CISC (Complex Instruction Set Computer):**
  - Large, complex instructions can execute multi-step operations with a single instruction.
  - Fewer instructions per program, but each instruction may take more cycles.
  - Example: Intel x86 family.
- **RISC (Reduced Instruction Set Computer):**
  - Simple, uniform instructions designed for fast execution.

- More instructions per program, but each instruction is executed quickly.
- Example: ARM, RISC-V, PowerPC.

- **Harvard vs. Von Neumann:**
  - Harvard: Separate pathways and storage for instructions and data, often used in microcontrollers and DSPs.
  - Von Neumann: Shared pathways and storage, common in general-purpose computers.
- **SIMD (Single Instruction, Multiple Data):**
  - Executes the same operation on multiple data points simultaneously, boosting performance for vector and matrix operations.
  - Used in multimedia, scientific computing, and AI.
- **Multicore:**
  - Multiple processing cores in a single CPU, enabling parallel execution of tasks for improved multitasking and performance.

Bit Widths and Compatibility

- **32-bit vs. 64-bit:**
  - 64-bit processors handle larger data and address more memory than 32-bit.
  - Most modern CPUs are 64-bit, but many retain compatibility with 32-bit software for legacy support.
  - 64-bit operating systems and applications are required to fully utilize 64-bit CPUs.

Popular CPU Vendors and Architectures

Vendor	Architecture Type	Notable Models / Series	Typical Use Cases
Intel	CISC, Multicore	Core i3/i5/i7/i9, Xeon	PCs, servers, laptops
AMD	CISC, Multicore	Ryzen, EPYC	PCs, servers
ARM	RISC, Multicore	Cortex-A/R/M, Neoverse, Apple Silicon	Mobile, IoT, servers
IBM	RISC	PowerPC, POWER	Enterprise, servers

Open Source	RISC	RISC-V	Research, embedded, IoT

Summary Table: CISC vs. RISC

Feature	CISC (e.g., x86)	RISC (e.g., ARM, RISC-V)
Instruction Length	Variable	Fixed
Instruction Count	Large	Small
Execution Speed	Slower per instruction	Faster per instruction
Code Size	Smaller	Larger
Power Efficiency	Lower	Higher
Typical Devices	PCs, servers	Mobile, embedded, IoT

This chart provides a foundational overview for students and educators to compare major CPU architectures, their features, and typical use cases in modern computing.