KONERU LAKSHMAIAH EDUCATION FOUNDATION
(Deemed to be University estd, u/s, 3 of the UGC Act, 1956)
(NAAC Accredited "A++" Grade University)
Green Fields, Guntur District, A.P., India – 522502
Department of Basic Engineering Science - II

I B.Tech. II Semester – CSE / AI & DS / ECE / EEE / CS & IT / IOT

A.Y.2024-25 - EVEN SEMESTER

Digital Design and Computer Architecture (23EC1202)

CO – 1: Combinational Digital Logic Circuits

Session 5: Multiplexers & Demultiplexers

1. Course Description (Description of the subject):

The course on "Digital Design and Computer Architecture" provides a comprehensive exploration of the foundational principles in digital design process and computer organization. Students explore the concepts of combinational and sequential circuits, memory circuits. The curriculum extends to the Basic computer architecture concepts, memory hierarchies, and input/output fundamentals, fostering a deep understanding of computer organization. Through practical projects and simulations, students develop the skills to design and implement digital circuits. Graduates emerge with a robust skill set, ready to embark on careers in hardware design, computer architecture, and related fields, equipped to contribute to the ever-evolving landscape of digital technology.

2. Aim of the Course:

The course aims to equip students with the knowledge and skills related to:

i. Proficiency in designing and optimizing Combinational and Sequential Circuits using Boolean algebra and programmable logic devices with a solid foundation in digital design.

ii. Skill development using hands-on experience in designing digital circuits which includes latches, flip-flops, and counters in combination with memory, registers, and timing and sequence control modules using hardware & modeling tools.

iii. Explore the architecture of modern computers, including the organization and structure of central processing units, memory systems, and input/output interfaces.

iv. Bridge theoretical concepts with real-world applications by examining case studies and examples of digital design and computer architecture in modern computing systems.

Overall, the aim of the course is to prepare the student well-equipped to apply their knowledge to the design and analysis of digital systems and computer architectures, preparing them for careers in areas such as hardware design, computer engineering, and embedded systems development.

3. Instructional Objectives (Course Objectives):

The course objectives for "Digital Design and Computer Architecture" typically include:

i. To Understand and apply foundational concepts in digital design which results in proficiency over designing and analyzing combinational and sequential logic circuits.

ii. To Gain hands-on experience with industry-standard simulation and modeling tools, for verifying and testing digital designs.

iii. To analyze the architecture of a computer system, including the organization and operation of the CPU, memory hierarchy, and input/output subsystems.

iv. To apply digital design and computer architecture principles to solve real-world engineering problems and challenges by reinforcing theoretical knowledge with hands-on experience.

4. Learning Outcomes (Course Outcomes):

i. Able to build the combinational and programmable digital logic circuits using logic gates and optimization methods.

ii. Able to construct the sequential and memory circuits using flip-flops, demonstrating a comprehensive understanding of the principles governing clocked sequential logic.

iii. Able to organize computer architecture and instructions sequence through a grasp of the foundational principles that govern the organization and functioning of a computer system.

iv. Capable of modeling Memory Architecture and I/O Organization modules proficiently.

v. Able to develop and analyze the computer architecture modules using basic combinational, sequential and memory logics.

5. Module Description (CO - 1 Description):

The module covers essential topics in digital electronics, starting with Boolean algebra and progressing to the representation and optimization techniques of digital logic using SOP/POS forms. Students will delve into the design of key components such as adders, subtractors, multiplexers, de-multiplexers, decoders, and encoders. The module introduces the concept of reversible gates, exploring their unique properties. Additionally, students will gain insights into Programmable Logic Devices (PLDs) like PROM, PAL, and PLA, understanding their design principles. The implementation of Complex Programmable Logic Devices (CPLDs) with macrocells and Field-Programmable Gate Arrays (FPGAs) featuring Configurable Logic Blocks (CLBs) and Look-Up Tables (LUTs) will be covered. Practical applications of these digital logic modules in various scenarios will be emphasized, providing students with a comprehensive understanding of digital electronics and its real-world applications.

6. Session Introduction:

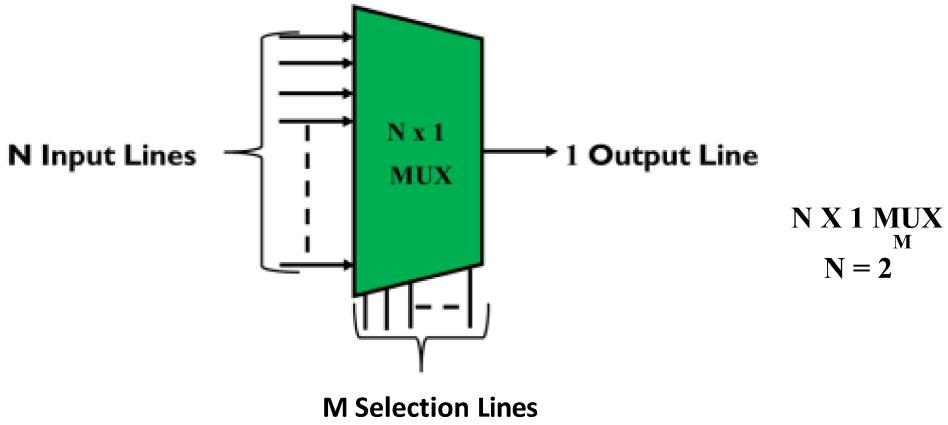
In digital circuits, multiplexers and demultiplexers are crucial components used for data routing and selection. A multiplexer, often referred to as a "mux," is a device that selects one of several input signals and forwards it to a single output line based on control signals. This allows for the transmission of multiple data streams over a single communication channel or the consolidation of various inputs into a single output. On the other hand, a demultiplexer, or "demux," performs the opposite function by taking a single input signal and routing it to one of several output lines based on control signals. Demultiplexers are commonly used for data distribution, channel selection, or signal routing in digital systems. Together, multiplexers and demultiplexers play essential roles in data transmission, signal processing, and resource sharing within digital circuits, contributing to efficient and flexible data management.

7. Session Description:

7.1 Multiplexers:

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from any of many input lines and directs it to a single output line. The selection of a particular input lie is controlled by a set of selection lines. Generally, there

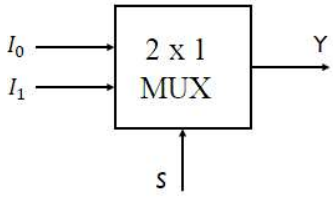
are 2^n input lines and n selection lines whose bit combinations determine which input is selected.



2 × 1 Multiplexer:

A 2:1 multiplexer, often abbreviated as "2-to-1 mux," is a digital circuit that selects one of two input signals and forwards it to a single output line based on a control signal. It consists of two data inputs (A and B), one select input (S), and one output (Y). When the select input (S) is low (0), the output (Y) connects to the first input (A), and when the select input is high (1), the output connects to the second input (B). This allows the multiplexer to choose between the two input signals and pass the selected signal to the output, effectively performing a data selection or routing function.

a) Block Diagram

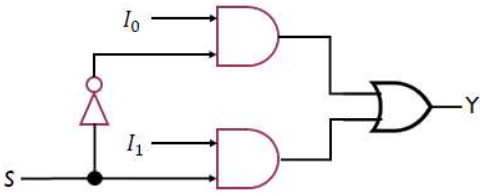


b) Truth Table

S	Y
0	I_0
1	I_1

Boolean Expression,
$Y = I_0\overline{S} + I_1 S$

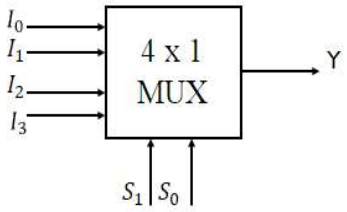
c) Logic Diagram



4 × 1 Multiplexer:

A 4 × 1 Multiplexer shown, similar working as 2: 1 multiplexer, consists of four input lines I_0 to I_3, two select lines S_1 and S_0.

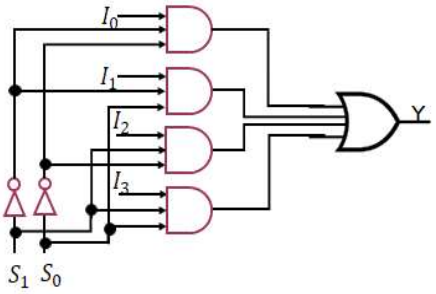
a) Block Diagram



b) Truth Table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

c) Logic Diagram

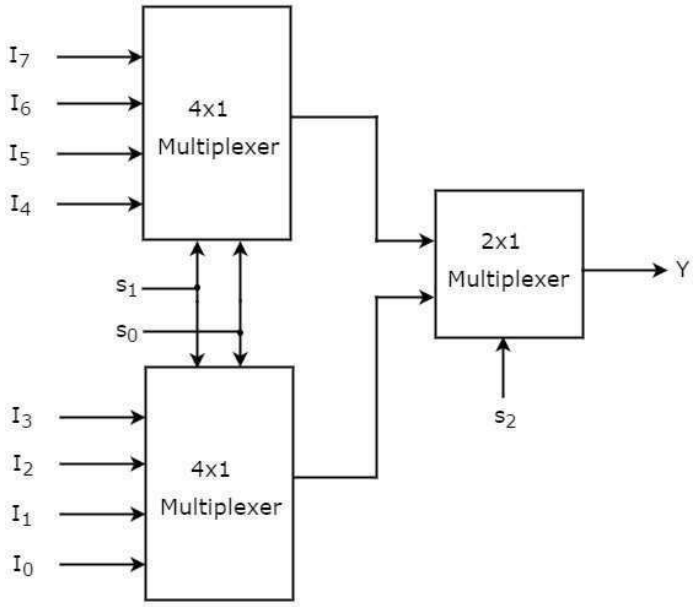


Boolean Expression,

$$Y = \overline{S_1}\,\overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

Cascading of Multiplexers:

Implement an 8 × 1 Multiplexer using two 4 × 1 multiplexers.



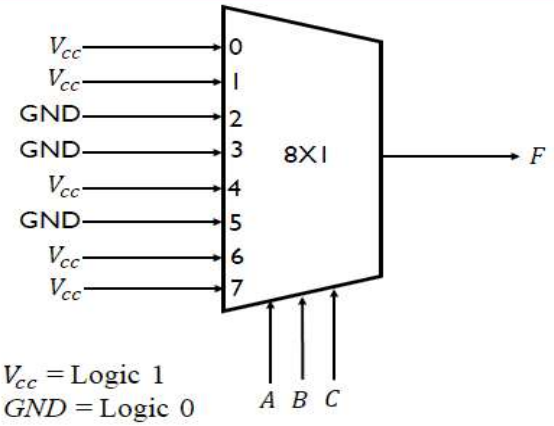
Combinational Logic Implementation:

One of the most common applications of a multiplexer is its use for implementation of combinational logic Boolean functions. The simplest technique for doing so is to employ a 2n-to-1 MUX to implement an n-variable Boolean function. The input lines corresponding to

each of the minterms present in the Boolean function are made equal to logic '1' state. The remaining minterms that are absent in the Boolean function are disabled by making their corresponding input lines equal to logic '0'.

1. Implement $F(A, B, C) = \sum(0, 1, 4, 6, 7)$ using a 8×1 Multiplexer.

A	B	C	F (A,B,C)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

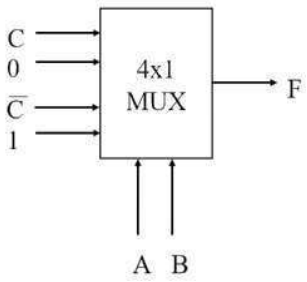


2. Implement $F(A, B, C) = \sum(0,4,6,7)$ using a 4×1 Multiplexer.

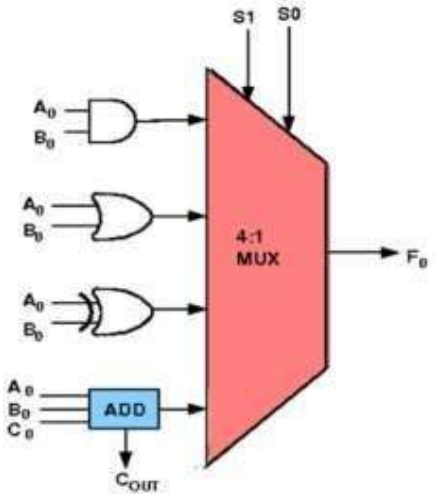
a) Implementation Table

	I_0	I_1	I_2	I_3
	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$	0	2	(4)	(6)
C	(1)	3	5	(7)
	c	0	c'	1

b) Logic Diagram



3. Develop an Arithmetic Logic Unit (ALU) by using a 4-to-1 Multiplexer.



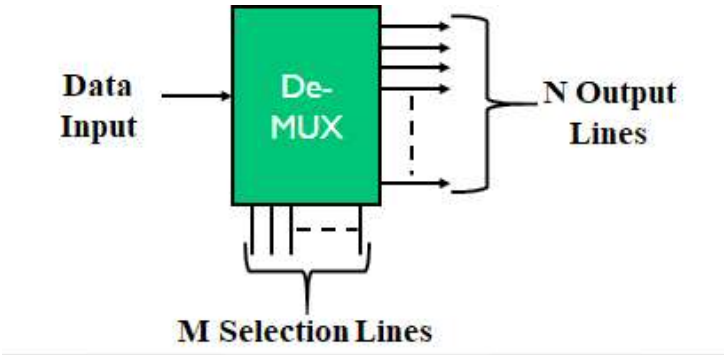
Applications of Multiplexer:

Multiplexers find numerous applications across various fields due to their ability to efficiently route and select data signals. Some common applications include:

- Digital Communication Systems: Used for combining multiple data streams onto a single transmission medium.
- Analog-to-Digital Conversion: Employed in ADCs to select different analog input signals for conversion.
- Data Acquisition Systems: Selecting sensor inputs for measurement and monitoring in instrumentation.
- Memory Address Decoding: Decoding memory addresses to select specific memory locations for read or write operations.
- Control and Routing in Digital Systems: Selecting between different control signals and routing data between components.
- Display Systems: Selecting segments or pixels in display systems like LED and LCD displays.
- Test and Measurement Equipment: Switching between different input signals for analysis and measurement in test equipment.

7.2 Demultiplexer:

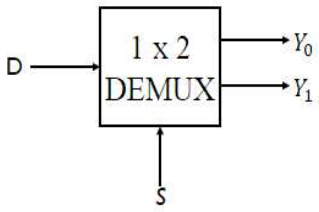
A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of a specific output line is controlled by the bit values of n selection lines.



1 × 2 Demultiplexer:

A 1:2 demultiplexer, also known as a "1-to-2 demux," is a digital circuit that takes a single input signal and routes it to one of two output lines based on a control signal. It consists of one input line, one control input, and two output lines. When the control input is low (0), the input signal is routed to the first output line, and when the control input is high (1), the input signal is routed to the second output line. Demultiplexers are commonly used in digital systems for data distribution, channel selection, and signal routing applications.

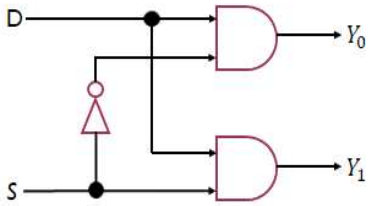
a) Block Diagram



b) Truth Table

Input	S	Y_0	Y_1
D	0	D	0
D	1	0	D

c) Logic Diagram



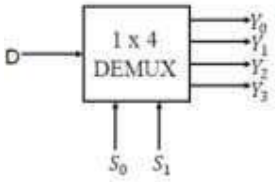
Boolean Expression,

$$Y_0 = D\overline{S}$$
$$Y_1 = DS$$

1 × 4 Demultiplexer:

A 1:4 demultiplexer, also referred to as a "1-to-4 demux," is a digital circuit that takes a single input signal and routes it to one of four output lines based on a control signal. It typically consists of one input line, two control inputs, and four output lines. The control inputs determine which of the four output lines the input signal is directed to. The combination of control signals selects the desired output line. 1:4 demultiplexers are widely used in digital systems for data distribution, channel selection, and signal routing tasks.

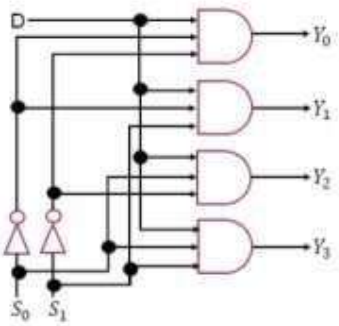
a) Block Diagram



b) Truth Table

Input	S_0	S_1	Y_0	Y_1	Y_2	Y_3
D	0	0	D	0	0	0
D	0	1	0	D	0	0
D	1	0	0	0	D	0
D	1	1	0	0	0	D

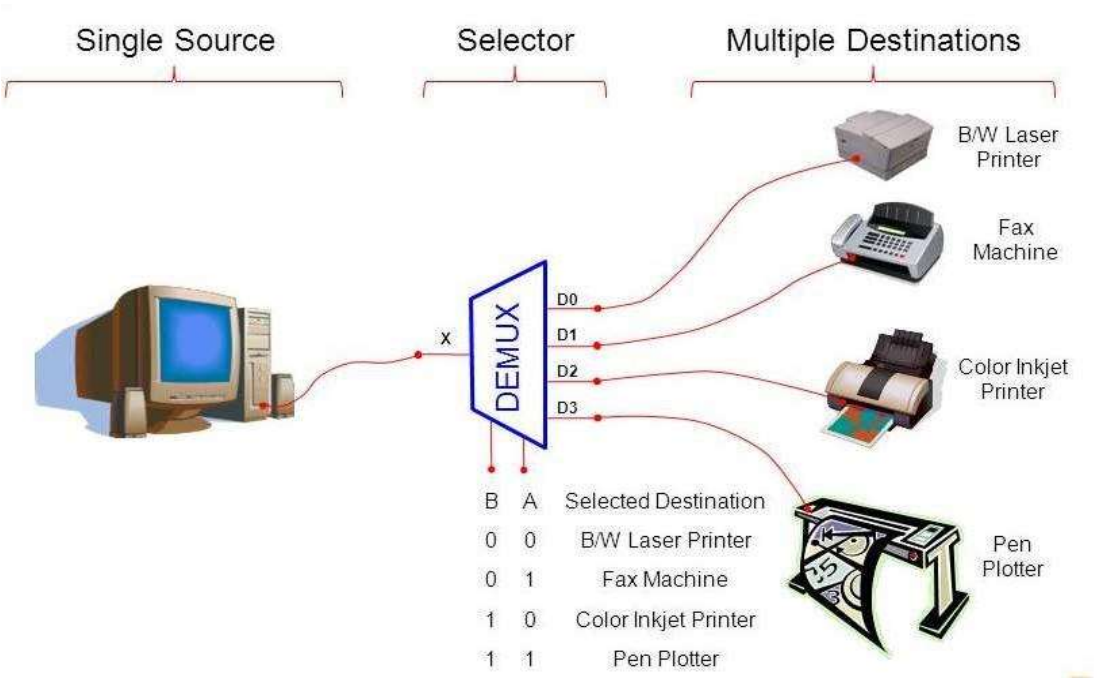
c) Logic Diagram



Boolean Expressions,

$$Y_0 = D\overline{S_0}\,\overline{S_1}$$
$$Y_1 = D\overline{S_0}S_1$$
$$Y_2 = DS_0\overline{S_1}$$
$$Y_3 = DS_0S_1$$

Application of Demultiplexer:



8. SAQ's – Self Assessment Questions:

1. What is a multiplexer?
    a) It is a type of decoder which decodes several inputs and gives one output
    b) A multiplexer is a device which converts many signals into one
    c) It takes one input and results into many output
    d) It is a type of encoder which decodes several inputs and gives one output

2. A 4-to-1 MUX has _____input lines and _____select lines.

    a) 2, 1
    b) 4, 2
    c) 8, 2
    d) 1, 4

3. What is the output configuration of a Demultiplexer (DEMUX)?

a) **One input, multiple outputs**

b) Multiple inputs, one output

c) Multiple inputs, multiple outputs

d) One input, one output

4. In a 4-to-1 MUX, if the select lines are 01, which input line will be selected?

a) Input 0

b) Input 1

c) Input 2

d) Input 3

9. Terminal Questions:

- Provide the symbol and truth table for a 4-to-1 multiplexer.
- In a 2-to-1 multiplexer, how many input lines are there, and how many control lines are required to select one of the inputs?
- Design the function F(A,B,C)=∑m(1,4,5,7) using 4X1 MUX considering "A" as Input line and B, C as selection lines.
- Describe and draw how 8:1 multiplexer can be designed using 4:1 mux and 2:1 mux.
- Design an Arithmetic Logic Unit (ALU) by using a 4-to-1 Multiplexer.
- Design the function F(A,B,C)=∑m(1,4,5,7) using 4X1 MUX considering "A" as Input line and B, C as selection lines.
- Provide a thorough description of the architecture of a 1:4 de-multiplexer, including its input lines, control lines, and output.

10. Glossary:

Multiplexer (MUX): A multiplexer is a digital circuit that selects one of several input signals and forwards it to a single output line based on control signals. It typically consists of multiple data inputs, one or more select inputs, and a single output. The select inputs determine which input signal is transmitted to the output. Multiplexers are used for data routing, signal switching, and channel selection in various digital systems.

Demultiplexer (DEMUX): A demultiplexer is the inverse of a multiplexer, taking a single input signal and routing it to one of several output lines based on control signals. It usually

consists of one data input, one or more select inputs, and multiple output lines. The select inputs determine which output line the input signal is directed to. Demultiplexers are commonly used for data distribution, channel demultiplexing, and signal routing in digital circuits.

11. References books:

- Computer System Architecture by M. Moris Mano
- Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic

12. Sites and Web links:

- https://unacademy.com/content/jee/difference-between/multiplexer-and-demultiplexer/
- https://www.electronicshub.org/multiplexer-and-demultiplexer/