KONERU LAKSHMAIAH EDUCATION FOUNDATION
(Deemed to be University estd, u/s, 3 of the UGC Act, 1956)
(NAAC Accredited "A++" Grade University)
Green Fields, Guntur District, A.P., India – 522502
**Department of Basic Engineering Science - II**

**I B.Tech. II Semester – CSE / AI & DS / ECE / EEE / CS & IT / IOT**

**A.Y.2024-25 - EVEN SEMESTER**

**Digital Design and Computer Architecture (23EC1202)**

**CO – 1: Combinational Digital Logic Circuits**

**Session 7: PLD's and PROM**

## 1. Course Description (Description of the subject):

The course on "Digital Design and Computer Architecture" provides a comprehensive exploration of the foundational principles in digital design process and computer organization. Students explore the concepts of combinational and sequential circuits, memory circuits. The curriculum extends to the Basic computer architecture concepts, memory hierarchies, and input/output fundamentals, fostering a deep understanding of computer organization. Through practical projects and simulations, students develop the skills to design and implement digital circuits. Graduates emerge with a robust skill set, ready to embark on careers in hardware design, computer architecture, and related fields, equipped to contribute to the ever-evolving landscape of digital technology.

## 2. Aim of the Course:

The course aims to equip students with the knowledge and skills related to:

i. Proficiency in designing and optimizing Combinational and Sequential Circuits using Boolean algebra and programmable logic devices with a solid foundation in digital design.

ii. Skill development using hands-on experience in designing digital circuits which includes latches, flip-flops, and counters in combination with memory, registers, and timing and sequence control modules using hardware & modeling tools.

iii. Explore the architecture of modern computers, including the organization and structure of central processing units, memory systems, and input/output interfaces.

iv. Bridge theoretical concepts with real-world applications by examining case studies and examples of digital design and computer architecture in modern computing systems.

Overall, the aim of the course is to prepare the student well-equipped to apply their knowledge to the design and analysis of digital systems and computer architectures, preparing them for careers in areas such as hardware design, computer engineering, and embedded systems development.

**3. Instructional Objectives (Course Objectives):**

The course objectives for "Digital Design and Computer Architecture" typically include:

i. To Understand and apply foundational concepts in digital design which results in proficiency over designing and analyzing combinational and sequential logic circuits.

ii. To Gain hands-on experience with industry-standard simulation and modeling tools, for verifying and testing digital designs.

iii. To analyze the architecture of a computer system, including the organization and operation of the CPU, memory hierarchy, and input/output subsystems.

iv. To apply digital design and computer architecture principles to solve real-world engineering problems and challenges by reinforcing theoretical knowledge with hands-on experience.

**4. Learning Outcomes (Course Outcomes):**

i. Able to build the combinational and programmable digital logic circuits using logic gates and optimization methods.

ii. Able to construct the sequential and memory circuits using flip-flops, demonstrating a comprehensive understanding of the principles governing clocked sequential logic.

iii. Able to organize computer architecture and instructions sequence through a grasp of the foundational principles that govern the organization and functioning of a computer system.

iv. Capable of modeling Memory Architecture and I/O Organization modules proficiently.

v. Able to develop and analyze the computer architecture modules using basic combinational, sequential and memory logics.

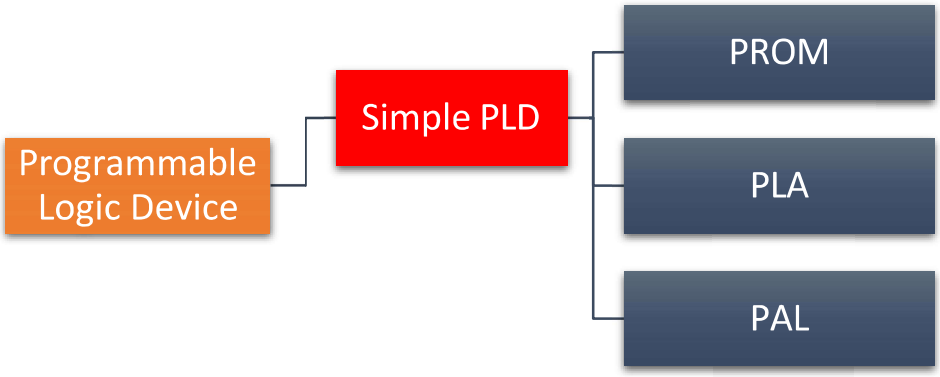
## 5. Module Description (CO - 1 Description):

The module covers essential topics in digital electronics, starting with Boolean algebra and progressing to the representation and optimization techniques of digital logic using SOP/POS forms. Students will delve into the design of key components such as adders, subtractors, multiplexers, de-multiplexers, decoders, and encoders. The module introduces the concept of reversible gates, exploring their unique properties. Additionally, students will gain insights into Programmable Logic Devices (PLDs) like PROM, PAL, and PLA, understanding their design principles. The implementation of Complex Programmable Logic Devices (CPLDs) with macrocells and Field-Programmable Gate Arrays (FPGAs) featuring Configurable Logic Blocks (CLBs) and Look-Up Tables (LUTs) will be covered. Practical applications of these digital logic modules in various scenarios will be emphasized, providing students with a comprehensive understanding of digital electronics and its real-world applications.

## 6. Session Introduction:

Programmable Logic Devices (PLDs) are key components in digital design that allow designers to implement custom digital logic circuits without the need for custom silicon. PLDs are programmable at the logical or routing level, providing flexibility in creating digital circuits tailored to specific applications.

The classification of PLDs given in the fig.



7. **Session Description:**

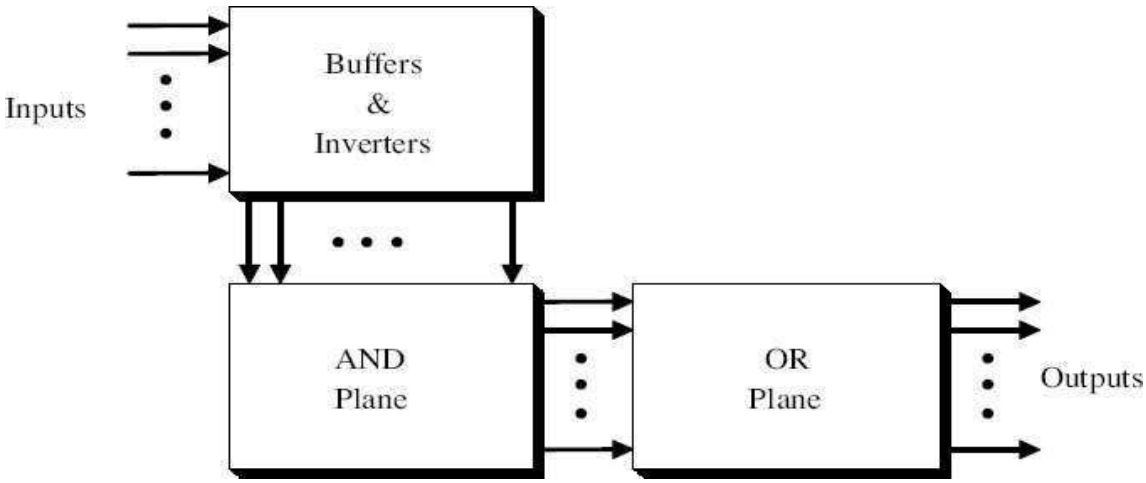
**Simple Programmable Logic Device (SPLD):**

Overview: SPLDs are a category of PLDs with relatively simple architectures, designed for implementing straightforward digital logic circuits.

Examples: PAL (Programmable Array Logic) devices and PLA (Programmable Logic Array) devices fall under the SPLD category.

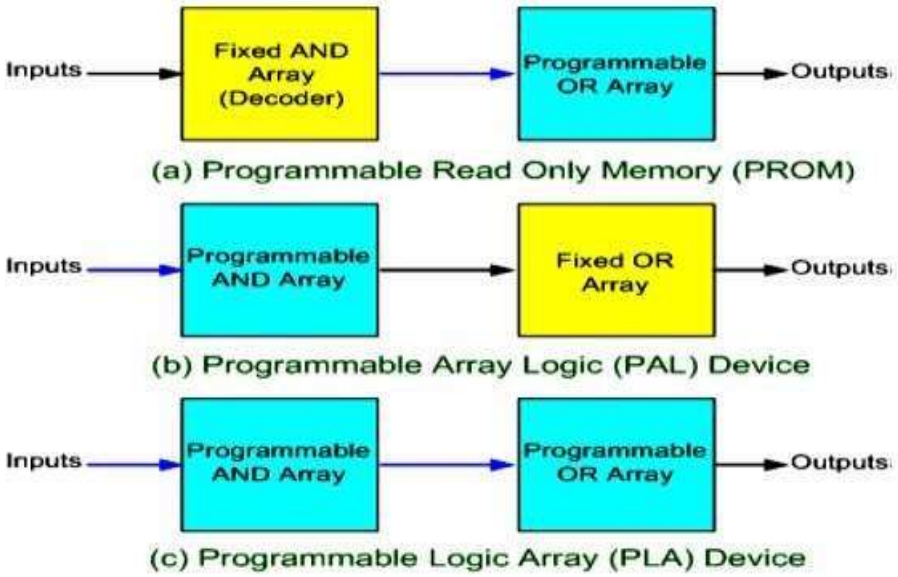
Architecture: SPLDs typically consist of fixed OR arrays and programmable AND arrays (PAL), or both programmable AND and OR arrays (PLA). These devices are suitable for applications with relatively simple combinational logic requirements.

Programming: SPLDs are programmed at the manufacturing stage using technologies like fuse blowing or antifuse programming. The programming is typically one-time and irreversible.



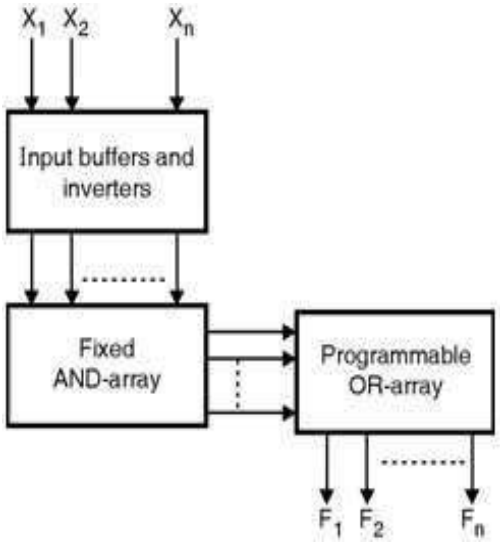

There are three kinds of SPLDs based on the type of arrays, which has programmable feature.

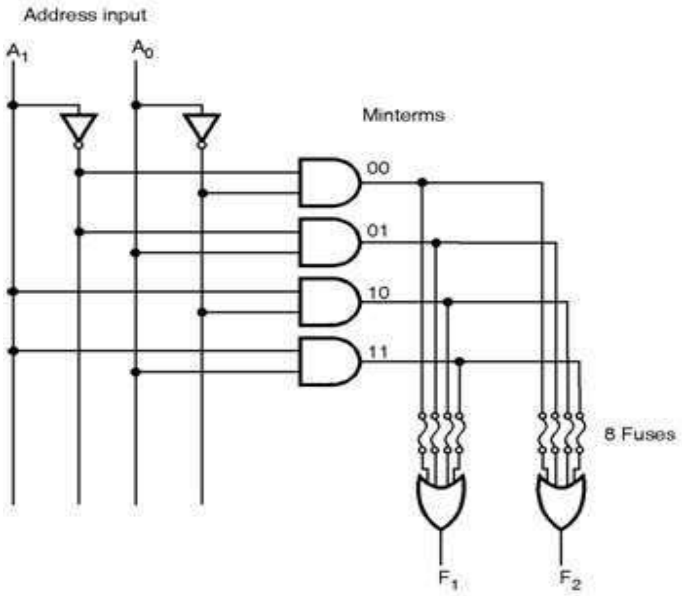
1. Programmable Read Only Memory (PROM)
2. Programmable Array Logic (PAL)
3. Programmable Logic Array (PLA)




**Programmable Read Only Memory (PROM):**

PROM is a type of PLD that is primarily used for implementing combinational logic. PROM devices consist of an array of AND gates feeding into a fixed OR array. The programming is done by selectively burning fuses or antifuses to establish connections between the AND gates and the OR array. PROMs are programmed after manufacturing by the user. The programming is typically irreversible, but some modern variants allow for multiple programming cycles. PROMs are commonly used for applications requiring fixed logic functions, such as address decoding and small combinational logic circuits.






**Applications of PLDs in Digital Design:**

PLDs find applications in various digital design scenarios, including:

- Combinational Logic: Implementing custom combinational logic functions to perform specific tasks.
- Control Logic: Designing control circuits for systems and devices.
- Glue Logic: Connecting different components or interfaces in a larger digital system.
- Arithmetic Logic: Performing arithmetic and logic operations in digital computations.
- Memory Decoding: Generating address decoding logic for memory devices.

**Applications of PROMs in Digital Design:**

- Look-Up Tables (LUTs)
- Custom Logic Functions
- Multiplexers and Decoders
- Digital Calibration
- Security Key Storage
- Data and Configuration Storage
- Bootloader Programs
- Table-Based Algorithms

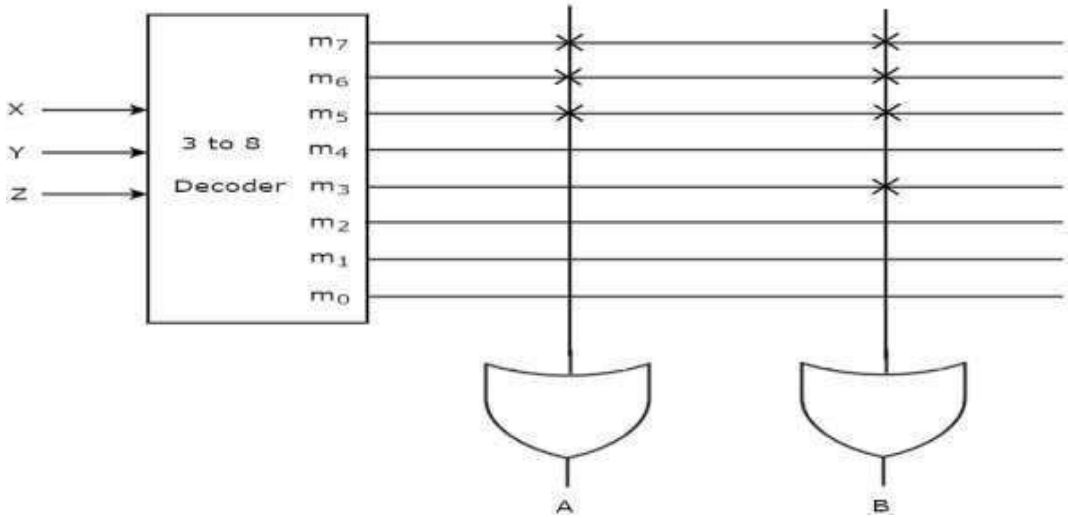
8. **Activities/ Case studies/ Important facts:**

***Problem: I*mplement the following Boolean functions using PROM.**

**A(X,Y,Z)=∑m(5,6,7)**

**B(X,Y,Z)=∑m(3,5,6,7)**

***Solution:*** The given two functions are in sum of min terms form and each function is having three variables X, Y & Z. So, we require a 3 to 8 decoder and two programmable OR gates for producing these two functions.



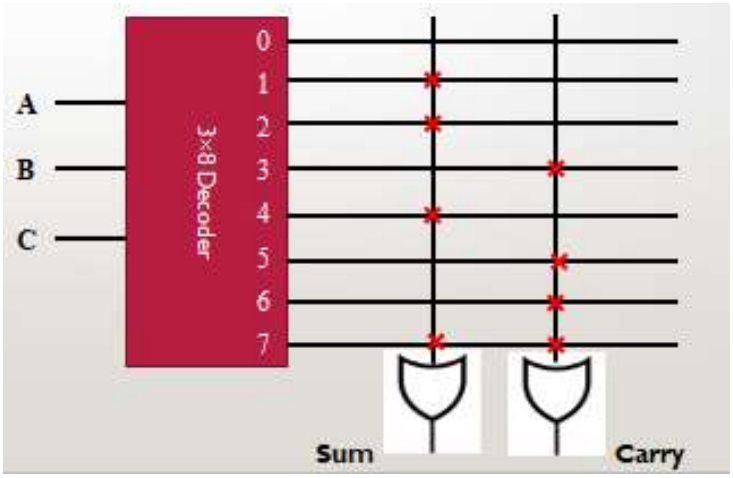

9. **Examples and contemporary extracts of articles or practices to convey the idea of the module:**

**Implement Full Adder by using PROM:**

Full adder output logic function:

Sum = ∑ m (1,2,4,7)

Carry = ∑ m (3,5,6,7)



## 10. SAQ's – Self Assessment Questions:

1. **Which of the following is a type of PLD?**
    a) CPU
    **b) FPGA**
    c) RAM
    d) ROM
2. **What is the main advantage of using PLDs in digital circuit design?**
    a) Lower cost
    b) Faster development time
    c) Higher power efficiency
    **d) All of the above**
3. **How is the programming of a PROM different from that of a ROM (Read-Only Memory)?**
    a) PROMs are read-only and cannot be programmed.
    b) ROMs are programmable multiple times, while PROMs are programmed only once.
    **c) PROMs are programmed once, and the data is permanent.**
    d) ROMs require a special programming voltage, unlike PROMs.
4. **Which component is typically used for implementing combinational logic functions in a PLD?**
    a) Flip-flop
    **b) AND gate**
    c) OR gate
    d) Inverter

## 11. Summary:

PLDs play a crucial role in digital design by providing a flexible and programmable platform for implementing custom digital circuits. SPLDs, including PALs and PLAs, are suitable for simpler applications, while PROMs are often used for fixed combinational logic functions. These devices enable designers to customize digital logic based on specific requirements, making them versatile components in the field of digital electronics.

**12. Terminal Questions:**

- Draw the classification diagram of Programmable Logic Devices (PLDs).
- List the applications of PROM in digital circuit design, considering factors such as flexibility and reprogrammability.
- Design the following Boolean functions using PROM.

  i) A (X,Y,Z) = ∑m (2,5,6)  ii) B (X,Y,Z) = ∑m (0,2,4,7)
- Design the following Boolean functions using PROM.

  i) A (X,Y,Z) = ∑m (2,4,6)  ii) B (X,Y,Z) = ∑m (4,5,6,7)
- Design the following Boolean functions using PROM.

  A (X,Y,Z) = ∑m (5,6,7)  B (X,Y,Z) = ∑m (3,5,6,7)
- How can the outputs of a full adder be designed using a Programmable Read-Only Memory (PROM) along with the appropriate decoder?

**13. References books:**

1. Computer System Architecture by M. Moris Mano

2. Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic

**14. Sites and Web links:**

1. https://www.tutorialspoint.com/digital_circuits/digital_circuits_programmable_logic_devices.htm
2. https://www.geeksforgeeks.org/programming-array-logic/
3. https://www.electrically4u.com/programmable-array-logic/