

## **EE517: ANALOG VLSI LAB LAB PROJECT**

**Design a 2-stage Op-amp in 180 nm technology  
targeting different target specifications by  
gm/Id methodology**



*Submitted by,*

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**EEE - VLSI & NANO ELECTRONICS**

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# 1 OBJECTIVE OF THE EXPERIMENT

Group 3 Specifications (Refer Fig. 1)

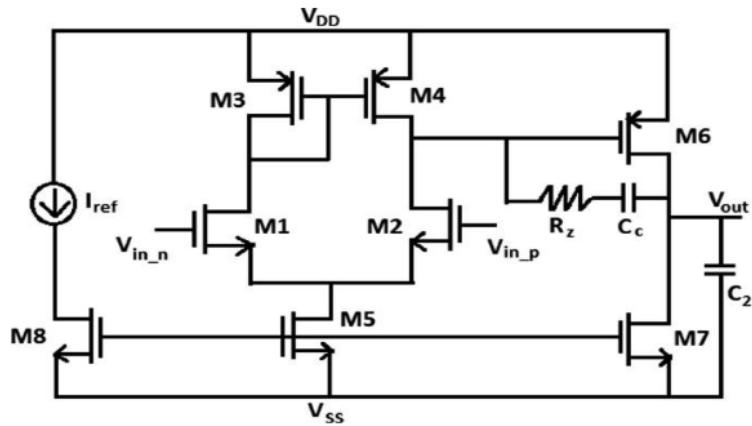
## General Specifications:

- Supply Voltage ( $V_{DD}$ ): 1.8V
- Slew Rate: 5V/
- Phase Margin:  $\geq 60^\circ$
- Load Capacitance ( $C_L$ ): 1pF

**Target: High GBW with Low Power**

## Design Requirements:

- Gain:  $\geq 50dB$
- Common Mode Gain: At least  $-10dB$
- Gain Bandwidth Product (GBW):  $\geq 150MHz$
- Output Voltage Swing (Differential Peak-to-Peak): At least 800mV<sub>pp</sub>
- Power Consumption:  $< 1mW$



## 2 gm / Id METHOD

### 2.1 Drawbacks of traditional design process

Traditional methods of analog circuit design are predominantly based on the square law expression relating the drain current ( $I_d$ ) of MOSFET with the gate overdrive voltage ( $V_{gs} - V_{th}$ ). The shortcomings of this method include neglecting several other second-order effects as enlisted below:

- Drain induced barrier lowering, reverse drain induced barrier lowering.
- Dependence on VT H of a MOSFET on its dimensions.
- Channel length modulation

and many more. As a result, there is significant departure of the simulation results from the hand calculations at sub-micron process nodes.

The gm/Id method aims to address this issue and arrive at better correspondence of hand calculations and simulation results. The method involves detailed characterization of the MOSFET and prepare lookup tables to aid hand-calculation.

### 2.2 Motivation of gm/ID

- gm/ID is a measure of the efficiency to translate current (i.e., power) into gm (i.e., gain).
- gm/Id is a simulation-based, technology-aware method that accurately reflects the real behavior of transistors in scaled CMOS.
- gm/Id directly relates transconductance efficiency (how much gain you get per unit of current), which is key for:
  - \*Low-power design
  - \*High-speed operation
  - \*Noise-performance optimization.
- gm/Id works from weak inversion (subthreshold), through moderate, to strong inversion. This is crucial for low-power or ultra-low-power analog/mixed-signal circuits.
- You select a target gm/Id value based on your design goals (e.g., noise, power, speed)
- Then you extract the corresponding  $V_{ov}$ ,  $I_d$ , and  $(W/L)$  from pre-characterized plots or lookup tables.
- This approach is modular and reusable—makes it easier to iterate and optimize.

### 2.3 Preparation of gm/Id charts

The gm/Id method is based on the following figures of merit:

- Transit frequency  $f_T = \frac{g_m}{2\pi C_{gs}}$ . This figure is an indication of the device bandwidth.
- Intrinsic Gain :  $gm^*ro$  or  $gm/gds$ . This figure is an indication of the maximum voltage gain that can be obtained from the device.
- transconductance efficiency :  $gm/Id$ . This indicates the transconductance obtained per unit drain current.

In this method, the MOSFET is characterized to obtain the following plots

1.  $g_m$  versus  $V_g$
2.  $I_d$  versus  $V_{gs}$
3.  $g_m/I_d$  versus  $V_{gs}$
4.  $f_T$  versus  $V_{gs}$
5.  $g_m/gds$  versus  $V_{gs}$

From the above plots, the plots of  $f_T$ ,  $gm/gds$ ,  $Id/W$  versus  $gm/Id$  need to be obtained.

## 2.4 USING GM/ID CHARTS FOR CIRCUIT DESIGN

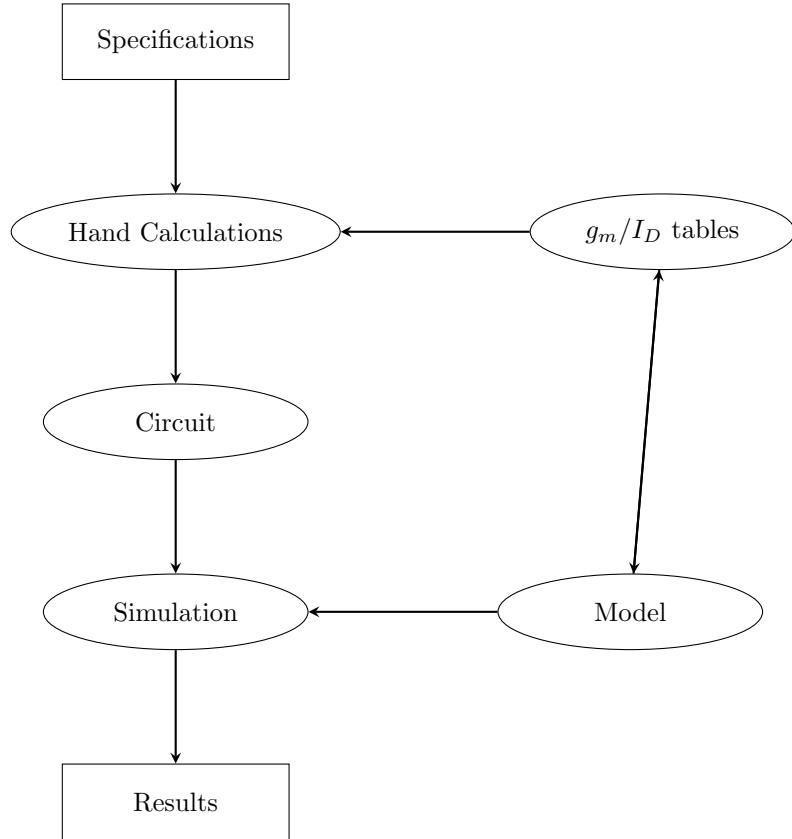


Figure 1: Flowchart of  $g_m/I_D$  based design process

## 2.5 Using gm/Id charts for circuit design

$g_m/I_d$  of a MOS transistor is nearly independent of its aspect ratio (fig. 2.8, 2.7) when the gate overdrive voltage  $V_{ov}$  ( $V_{gs} - V_{th}$ )  $\geq 0$ . Also, its variation is less significant from one technology to another. The typical range of  $g_m/I_d$  is 5 to 25. While choosing the  $g_m/I_d$  of each device, the following guidelines may be followed:

1. A small  $g_m/I_d$  can be chosen for the devices whose transconductance doesn't contribute to gain (e.g. active loads) or in cases where small area and high speed is desired.
2. A large  $g_m/I_d$  can be chosen for devices whose transconductance contributes to the gain (e.g. input stage of an amplifier) or in cases where low flicker noise, less mismatch and large voltage swings are desired.

After choosing the  $g_m/I_d$  for a device,  $I_d$  has to be chosen as per the power budget, and  $L$  has to be chosen such that the intrinsic gain  $g_m/g_{ds}$  is enough to meet the gain requirement. Choosing a very large  $g_m/g_{ds}$  might lead to a low  $f_T$  resulting in a low bandwidth: this tradeoff has to be taken care of properly. After choosing  $I_d$ , the width  $W$  can be obtained from the  $I_d/W$  versus  $g_m/I_d$  chart. Lastly, The DC operating voltage of the device should be chosen from the  $g_m/I_d$  versus  $V_{ov}$  chart so that it operates at the chosen  $g_m/I_d$ .

### 3 Design of Two-Stage Op-Amp using $g_m/I_d$ Method

#### 3.1 Miller Compensation Capacitor and Input Transconductance Calculation

To ensure sufficient phase margin and to implement pole splitting for frequency compensation, the compensation capacitor  $C_c$  must satisfy:

$$C_c > 0.22 \cdot C_L$$

Where:

- $C_L = 1 \text{ pF}$  is the load capacitance.

Substituting the values:

$$C_c > 0.22 \cdot 1 \text{ pF} = 0.22 \text{ pF} = 220 \text{ fF}$$

To provide margin, we select:

$$C_c = 350 \text{ fF}$$

#### 3.2 Input Transconductance $g_m$

The gain-bandwidth product (GBW) constraint dictates the minimum required input stage transconductance:

$$\text{GBW} = \frac{g_m}{2\pi C_c}$$

Given that the required gain bandwidth is:

$$\text{GBW} \geq 150 \text{ MHz}$$

Substituting  $C_c = 350 \text{ fF}$ :

$$\begin{aligned} g_m &\geq 2\pi \cdot C_c \cdot \text{GBW} \\ g_m &\geq 2\pi \cdot 350 \times 10^{-15} \cdot 150 \times 10^6 \\ g_m &\geq 2\pi \cdot 52.5 \times 10^{-9} \approx 300 \mu\text{S} \end{aligned}$$

I selected less  $g_m$  than theoretical value, because we have to use resistor to get GBW in my design,

$$g_m = 300 \mu\text{S}$$

This  $g_m$  value corresponds to the input differential pair formed by transistors M1 and M2.

### 3.3 Summary

- Load Capacitance  $C_L = 1 \text{ pF}$
- Selected Miller Cap  $C_c = 350 \text{ fF}$
- Gain Bandwidth Requirement  $\text{GBW} \geq 150 \text{ MHz}$
- Required Transconductance  $g_m = 240 \mu\text{S}$

### 3.4 Selection of $g_m/I_D$ for Different Transistors

The design of a two-stage operational amplifier using the  $g_m/I_D$  methodology begins with selecting appropriate  $g_m/I_D$  values for the transistors based on their functional requirements.

Transistors that require a large signal swing must operate in a region of higher intrinsic gain, which corresponds to a larger  $g_m/I_D$  value. On the other hand, transistors primarily used for biasing or current mirroring can function efficiently with a smaller  $g_m/I_D$ , prioritizing speed and area.

- **Input NMOS transistors (M1, M2):** A large  $g_m/I_D$  value of **11** is chosen for M1 and M2 because their transconductance contributes directly to the gain of the differential pair. A higher  $g_m/I_D$  is desirable in this case to ensure low flicker noise, less mismatch, and larger voltage swings, all of which improve the overall performance of the amplifier.
- **Current Mirror and Load Transistors (M3, M4, M5, M6):** A smaller  $g_m/I_D$  value of **10** is chosen for these transistors. Since their transconductance does not significantly contribute to the gain and their primary function is current copying or load operations, a lower  $g_m/I_D$  is sufficient. This choice helps in reducing area and improving speed without sacrificing performance.

The selected values are summarized below:

Transistors	Selected $g_m/I_D$
M1, M2	11
M3, M4, M5, M6	10

### 3.5 Preparation for Plotting: Saving Operating Points for NMOS and PMOS

To perform accurate analysis and plotting of the  $g_m/I_D$  characteristics, we must first extract the operating points for both NMOS and PMOS transistors. This section outlines the steps for setting up the NMOS device in Cadence for extracting the required data.

### 3.6 Setting Up the NMOS Schematic in Cadence

1. Create a testbench with an NMOS transistor connected appropriately for a DC sweep simulation.
2. Perform a **DC sweep of  $I_D$  vs  $V_{GS}$**  to cover the range of interest.
3. Ensure that operating points of the transistor are saved during the simulation.

### 3.7 Creating the Save File for Operating Points

1. In the server terminal, create a new save file with the **.scs** extension. For example:

```
touch nmos_1.scs
```

2. Edit the file using a text editor like **nano**:

```
nano nmos_1.scs
```

3. Inside the file, add the following line to save all operating points for the NMOS device (assuming the instance name is **NM0**):

```
save NM0:all
```

4. Save and exit the file.

### 3.8 Linking the Save File in ADE\_XL

1. Open **ADE\_XL** and load your simulation setup.
2. Navigate to **Setup→Simulation Files**.
3. Under **Definition Files**, click **Add** and select the previously created **nmos\_1.scs** file.
4. Click **Apply** to include the save file in the simulation setup.

This process ensures that all necessary NMOS operating point data will be available for plotting and further calculations such as  $g_m/I_D$ ,  $V_{ov}$ , and intrinsic gain.

### 3.9 Fixing the Channel Length using $g_m/g_{ds}$ vs $g_m/I_D$

After running the DC sweep and saving all operating points, open the **Results Browser** in Cadence. Click on the DC analysis result to view all the saved signal quantities.

To fix the length  $L$  of the transistor, we use the plot of  $g_m/g_{ds}$  versus  $g_m/I_D$ . The quantity  $g_m/g_{ds}$  is representative of the intrinsic gain of the device, combining both transconductance and output resistance:

$$\frac{g_m}{g_{ds}} = \text{gain}$$

For this design, a total gain of approximately 50 dB is required, which corresponds to a linear gain of around 316. To ensure margin, we target a gain of 400.

### 3.10 Stage-wise Gain Allocation

Since this is a two-stage operational amplifier, the total gain will be split across both stages. Due to the parallel combination of output resistances, we aim for:

- Stage 1 Gain: 20
- Stage 2 Gain: 20

This leads us to select individual transistor gain values of approximately:

$$\frac{g_m}{g_{ds}} = 40$$

### 3.11 Plotting in Cadence

1. In the Results Browser, select the signals: `gm`, `gds`, and `gmoverid`.
2. Send each of these to the calculator.
3. In the calculator, use the expression:

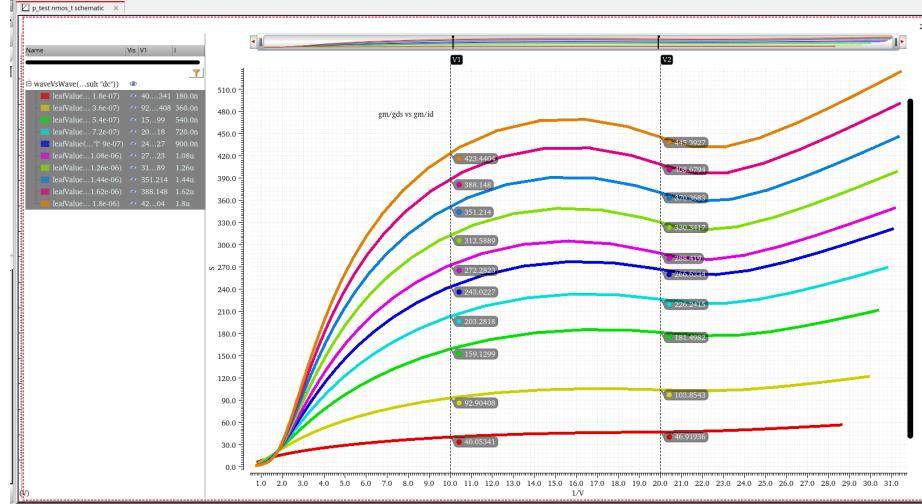
$$\frac{g_m}{g_{ds}} \text{ vs } \frac{g_m}{I_D}$$

using the `waveform vs waveform` function.

4. Parametrically vary the channel length  $L$  and generate the plot.

### 3.12 NMOS Length Selection

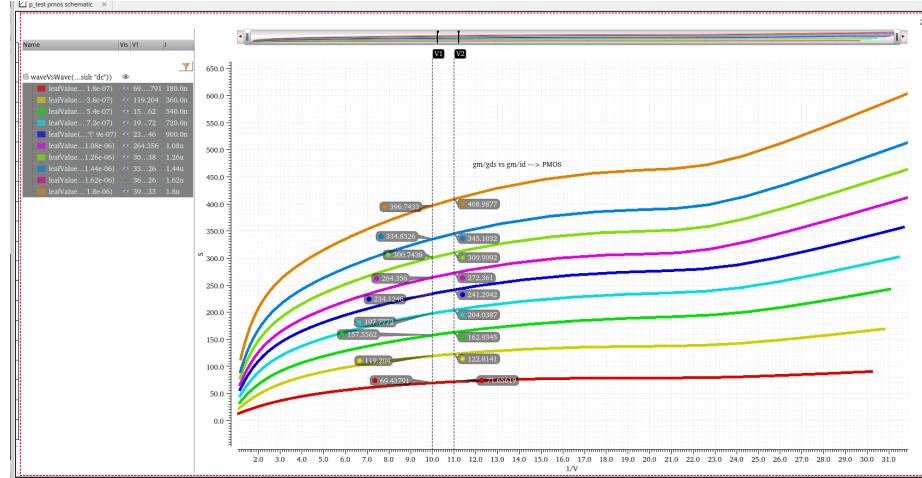
From the plot for NMOS transistors:



We observe that for  $g_m/g_{ds} = 40$  and  $g_m/I_D = 11$ , the required channel length is approximately **180 nm**. Here For  $g_m/g_{ds} = 40$  we are getting  $g_m/i_{ds} = 10$  Where  $g_m = 300\mu S$  we get  $I_d = 30\mu A$ .

### 3.13 PMOS Length Selection

Repeat the same procedure for PMOS transistors.



For  $g_m/g_{ds} = 40$  and  $g_m/I_D = 10$ , the suitable channel length is also **180 nm**.

### 3.14 Final Length Assignments

- Input NMOS transistors M1, M2:  $L = 180 \text{ nm}$
- Load and current mirror transistors M3, M4, M5, M6:  $L = 180 \text{ nm}$

### 3.15 Current Distribution Based on Power and Slew Rate Constraints

In this section, we determine the current allocation in the operational amplifier based on the overall power budget and dynamic performance requirements.

### 3.16 Power Constraint

The total power consumption is constrained by:

$$P \leq 1 \text{ mW}$$

Since power is related to the supply voltage and current as:

$$P = V_{DD} \cdot I_D$$

Given  $V_{DD} = 1.8 \text{ V}$ , we can calculate the maximum allowable current:

$$I_D \leq \frac{1 \text{ mW}}{1.8 \text{ V}} \approx 555 \mu\text{A}$$

### 3.17 Slew Rate Constraint

To ensure fast dynamic response, the required slew rate is considered:

$$\text{Slew Rate} \geq 5 \frac{\text{V}}{\mu\text{s}}$$

We conservatively select:

$$\text{Slew Rate} = 10 \frac{\text{V}}{\mu\text{s}}$$

The slew rate in a Miller compensated two-stage op-amp is determined by:

$$\frac{I_D}{C_c} \geq \text{Slew Rate}$$

Assuming compensation capacitance:

$$C_c = 350 \text{ fF}$$

Then the minimum required current is:

$$I_D \geq 10 \cdot 350 \text{ fF} = 3.5 \mu\text{A}$$

### 3.18 Selected Tail Current and Branch Currents

To balance between power efficiency and dynamic performance, we choose a practical value:

$$I_D = 30 \mu\text{A}$$

This current flows through the tail current source transistor  $M_7$ .

As a result, the current through each half of the differential pair is:

$$i_1 = i_2 = \frac{I_D}{2} = 15 \mu\text{A}$$

This also applies to current mirror and active load branches:

$$i_3 = i_4 = 15 \mu\text{A}$$

### 3.19 Summary of Current Distribution

Transistor(s)	Current ( $\mu\text{A}$ )
$M_7$ (Tail Current Source)	30
$M_1, M_2$ (Input Pair)	15 each
$M_3, M_4$ (Current Mirrors)	15 each

#### 3.19.1 Calculating Current in the Second Stage ( $I_6$ )

The current in the second stage ( $I_6$ ) is calculated using the formula:

$$I_6 = I_{SS} \left( 1 + \frac{C_L}{C_C} \right)$$

Given:

$$I_{SS} = 30 \mu\text{A}, \quad C_L = 1 \text{ pF}, \quad C_C = 0.35 \text{ pF}$$

Substituting the values:

$$I_6 = 30 \times 10^{-6} \left( 1 + \frac{1 \times 10^{-12}}{0.35 \times 10^{-12}} \right)$$

$$I_6 = 30 \times 10^{-6} (1 + 2.857)$$

$$I_6 = 30 \times 10^{-6} \times 3.857$$

$$I_6 \approx 115.14 \mu\text{A}$$

Approximating to a practical value:

$$I_6 \approx 120 \mu\text{A}$$

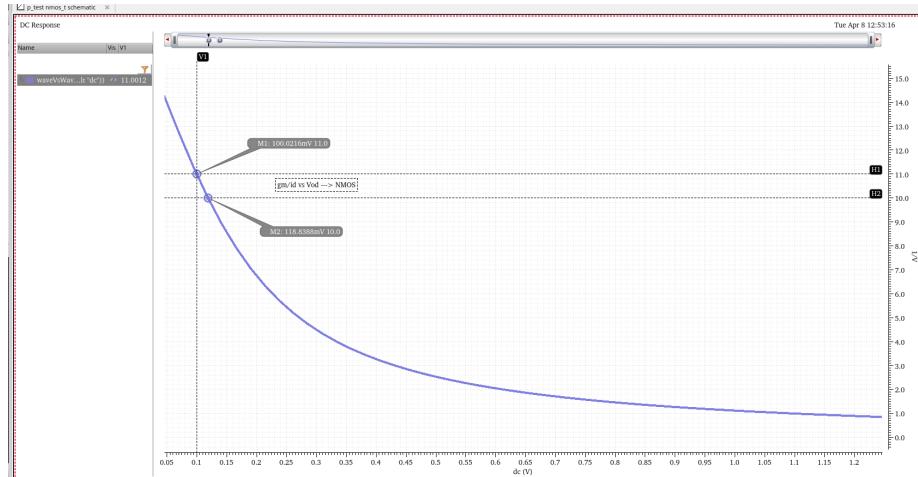
### 3.20 Overdrive Voltage Calculation Using $g_m/I_D$ vs $V_{ov}$

To size the transistors correctly using the  $g_m/I_D$  method, we extract the required overdrive voltages  $V_{ov}$  for the corresponding  $g_m/I_D$  values from simulation data.

### 3.21 Procedure

1. From the results browser, send the signals `gmoverid` and `vod` (overdrive voltage) to the calculator.
2. Use the `waveform vs waveform` function to plot  $g_m/I_D$  vs  $V_{ov}$ .
3. Identify the  $V_{ov}$  corresponding to the selected  $g_m/I_D$  for each transistor.

### 3.22 NMOS Overdrive Extraction



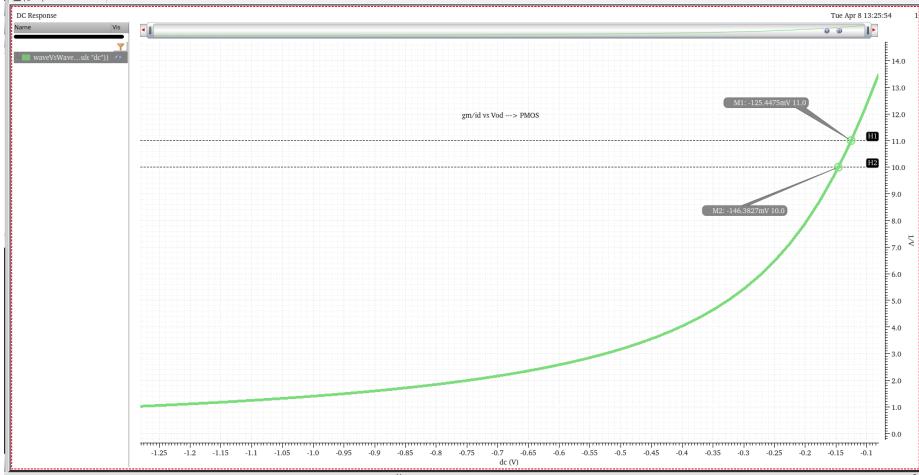
From the plot above:

- For  $g_m/I_D = 11$ ,  $V_{ov} \approx 100 \text{ mV}$
- For  $g_m/I_D = 10$ ,  $V_{ov} \approx 118 \text{ mV}$

Thus, the overdrive voltages for NMOS transistors are:

- M1, M2 (Input Pair):  $V_{ov} = 0.1 \text{ V}$

### 3.23 PMOS Overdrive Extraction



From the plot:

- For  $g_m/I_D = 10$ ,  $V_{ov} \approx 146 \text{ mV}$
- For  $g_m/I_D = 11$ ,  $V_{ov} \approx 125 \text{ mV}$

### 3.24 Summary of Overdrive Voltages

Transistor	$g_m/I_D$	$V_{ov} (\text{V})$
M1, M2 (NMOS Input)	11	0.1
M3, M4, M5, M6 (PMOS)	10	0.143

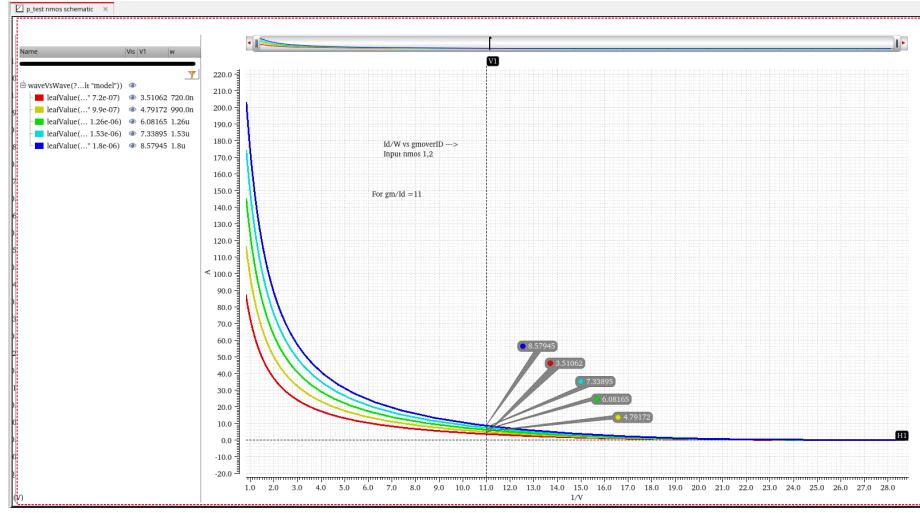
### 3.25 Transistor Width Calculation using $I_D/W$ vs $g_m/I_D$

To size the transistor widths  $W$ , we use the simulated plots of drain current per unit width  $I_D/W$  vs. transconductance efficiency  $g_m/I_D$ . From the chosen  $g_m/I_D$  and required  $I_D$ , we determine the width as:

$$W = \frac{I_D}{(I_D/W)}$$

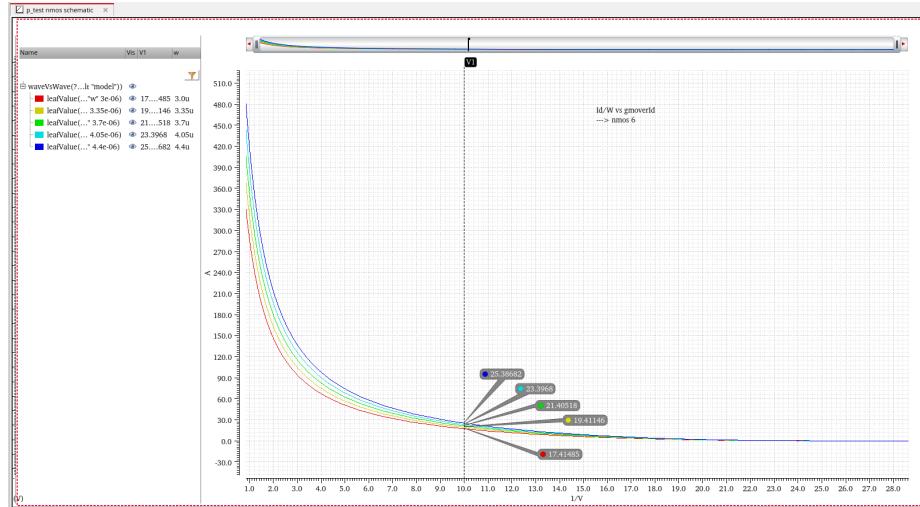
### 3.26 NMOS Input Transistors (M1, M2)

- $g_m/I_D = 11$
- $I_D = 15 \mu\text{A}$
- From plot:  $I_D/W \approx 8.57 \text{ A/m} \Rightarrow W \approx \frac{15 \times 10^{-6}}{8.57} \approx 1.2 \mu\text{m}$



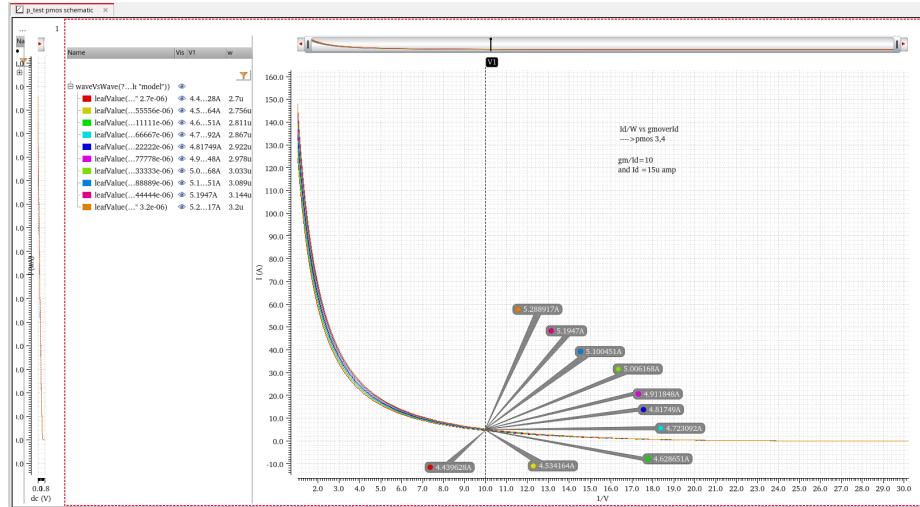
### 3.27 NMOS SECOND STAGE (M6)

- $g_m/I_D = 10$
- $I_D = 120 \mu\text{A}$
- From plot:  $I_D/W \approx 6.08 \times 10^{-6} \text{ A/m} \Rightarrow W \approx \frac{120 \times 10^{-6}}{6.08 \times 10^{-6}} \approx 5.5 \text{ um} = 5.5 \mu\text{m}$



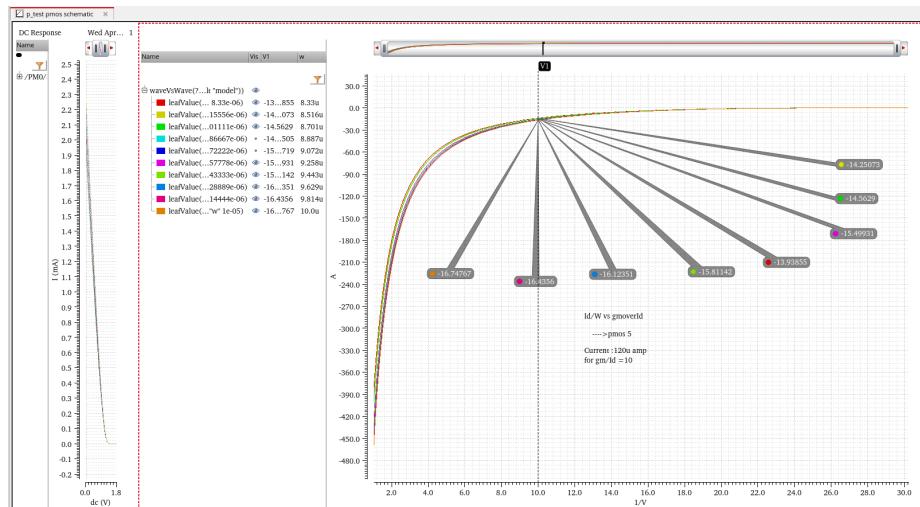
### 3.28 PMOS Transistors (M3, M4)

- $g_m/I_D = 10$
- $I_D = 15 \mu\text{A}$
- From plot:  $I_D/W \approx 3.00616 \text{ A/m} \Rightarrow W \approx \frac{15 \times 10^{-6}}{3.00618} \approx 3.0003 \text{ um} = 3 \mu\text{m}$



### 3.29 PMOS Second Stage (M5)

- $g_m/I_D = 10$
- $I_D = 120 \mu\text{A}$
- From plot:  $I_D/W \approx 14.56 \text{ A/m} \Rightarrow W \approx \frac{120 \times 10^{-6}}{14.56} \approx 8.56 \text{ um} = 8.5 \mu\text{m}$



### 3.30 NMOS Tail transistor (M7)

- $g_m/I_D = 10$
- $I_D = 30 \mu\text{A}$
- From plot:  $I_D/W \approx 30 \text{ A/m} \Rightarrow W \approx \frac{30 \times 10^{-6}}{30} \approx 1 \text{ um} = 1 \mu\text{m}$

### 3.31 Summary of Transistor Widths

Transistor	$g_m/I_D$	$I_D (\mu\text{A})$	Width $W (\mu\text{m})$
M1, M2 (NMOS Input)	11	15	1.8
M3, M4 (PMOS Load)	10	15	3.003
M5 (PMOS Second Stage)	10	120	8.516
M6 (NMOS Second Stage)	10	15	5.5
M7 (NMOS Tail Transistor)	10	30	5.5

## 4 Pole-Zero Calculation

### 4.1 Pole 1 Calculation

The first pole location ( $f_{p1}$ ) can be approximated by:

$$f_{p1} \approx \frac{1}{R_{out1} \times (G_{m6} \times R_{out2} \times C_c) \times 2\pi} \quad (1)$$

Where:

- $R_{out1}$  is the output resistance of the first stage
- $G_{m6} = 1.2 \text{ mS}$  (transconductance of the second stage)
- $R_{out2}$  is the output resistance of the second stage
- $C_c = 350 \text{ fF}$  (compensation capacitance)

#### 4.1.1 Calculating $R_{out1}$

$R_{out1}$  is the parallel combination of  $146 \text{ k}\Omega$  and  $225 \text{ k}\Omega$ :

$$R_{out1} = \frac{146 \text{ k}\Omega \times 225 \text{ k}\Omega}{146 \text{ k}\Omega + 225 \text{ k}\Omega} \approx 88.54 \text{ k}\Omega \quad (2)$$

#### 4.1.2 Calculating $R_{out2}$

$R_{out2}$  is the parallel combination of  $45 \text{ k}\Omega$  and  $24 \text{ k}\Omega$ :

$$R_{out2} = \frac{45 \text{ k}\Omega \times 24 \text{ k}\Omega}{45 \text{ k}\Omega + 24 \text{ k}\Omega} \approx 15.65 \text{ k}\Omega \quad (3)$$

#### 4.1.3 Calculating Pole Frequency

Now compute  $f_{p1}$ :

$$\begin{aligned} f_{p1} &\approx \frac{1}{2\pi \times 88.54 \text{ k}\Omega \times (1.2 \text{ mS} \times 15.65 \text{ k}\Omega \times 350 \text{ fF})} \\ &= \frac{1}{6.283 \times 88.54 \times 10^3 \times (1.2 \times 10^{-3} \times 15.65 \times 10^3 \times 350 \times 10^{-15})} \\ &= \frac{1}{6.283 \times 88.54 \times 10^3 \times 6.573 \times 10^{-12}} \\ &\approx 173.4 \text{ kHz} \end{aligned}$$

#### 4.2 Pole 2 Calculation

$$f_{p2} = \frac{G_{m6}}{2\pi C_L} = \frac{1.2 \text{ mS}}{2\pi \times 1 \text{ pF}} \approx 191 \text{ MHz} \quad (4)$$

#### 4.3 Zero Calculation

$$f_z = \frac{G_{m6}}{2\pi C_c} = \frac{1.2 \text{ mS}}{2\pi \times 350 \text{ fF}} \approx 546 \text{ MHz} \quad (5)$$

#### 4.4 LEFT HAND ZERO

To ensure a left-half-plane (LHP) zero, the following condition must be satisfied:

$$R > \frac{1}{g_{m6}} \quad (6)$$

Given:

$$g_{m6} = 1.2 \text{ mA/V} = 1.2 \times 10^{-3} \text{ S} \quad (7)$$

Therefore,

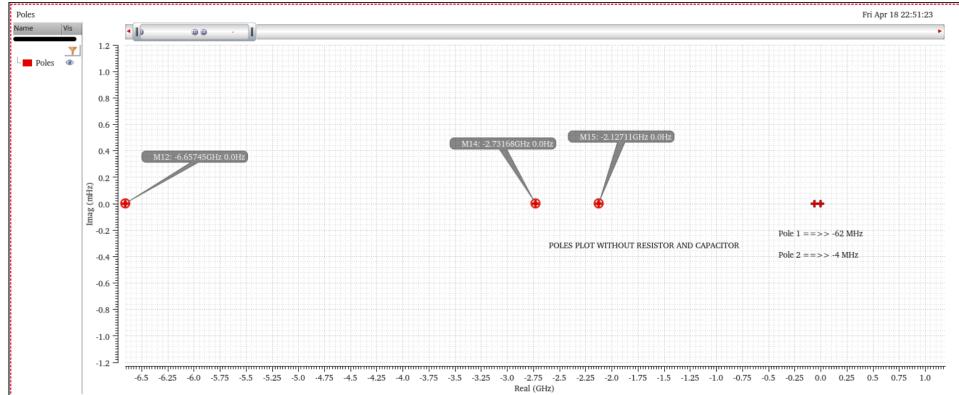
$$\frac{1}{g_{m6}} = \frac{1}{1.2 \times 10^{-3}} = 833.33 \text{ ohms} \quad (8)$$

Hence, the resistance  $R$  must satisfy:

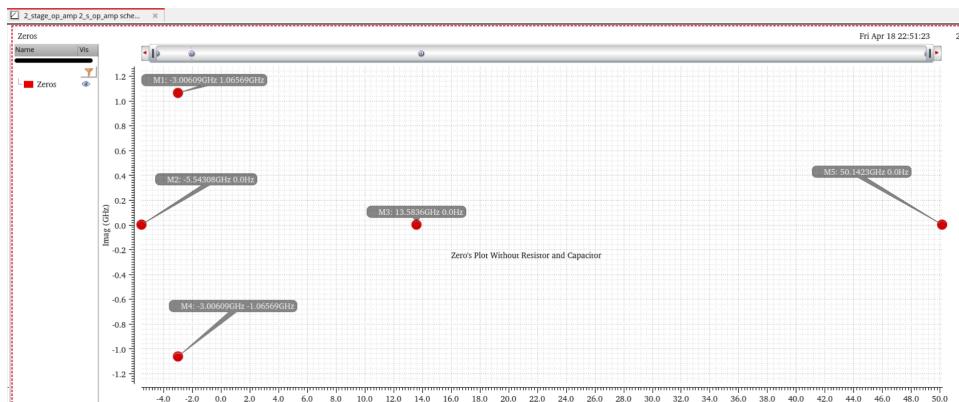
$$R \geq 1 \text{ KOHMS} \quad (9)$$

## 5 POLE ZERO ANALYSIS PLOTS

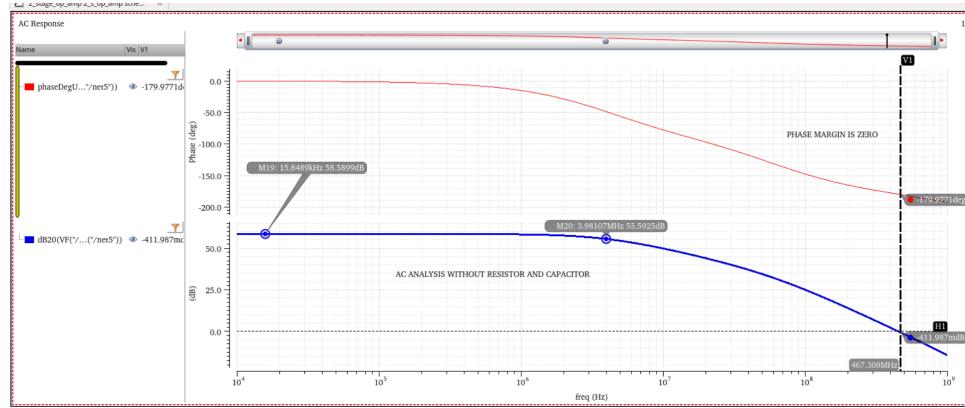
### 5.1 POLES'S PLOT WITH OUT ADDING RESISTOR AND CAPACITOR



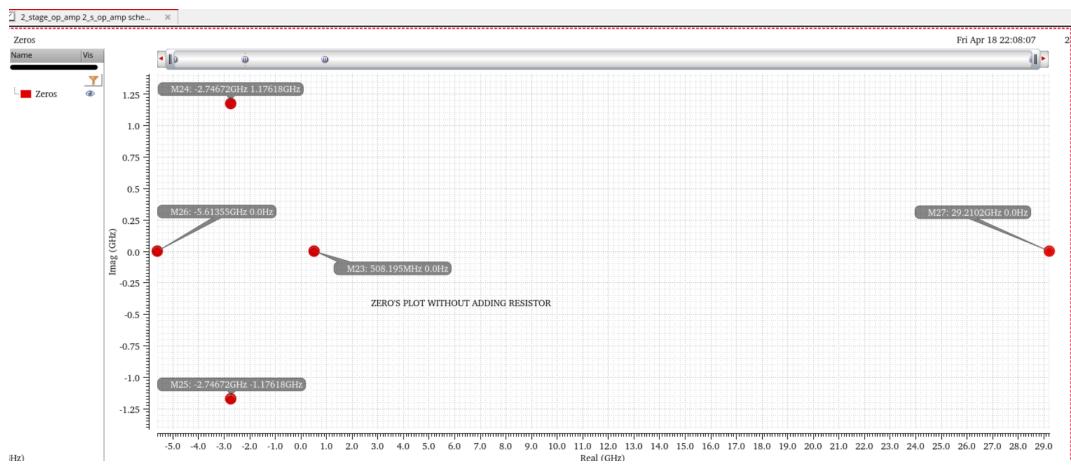
### 5.2 ZERO'S PLOT WITH OUT ADDING RESISTOR AND CAPACITOR



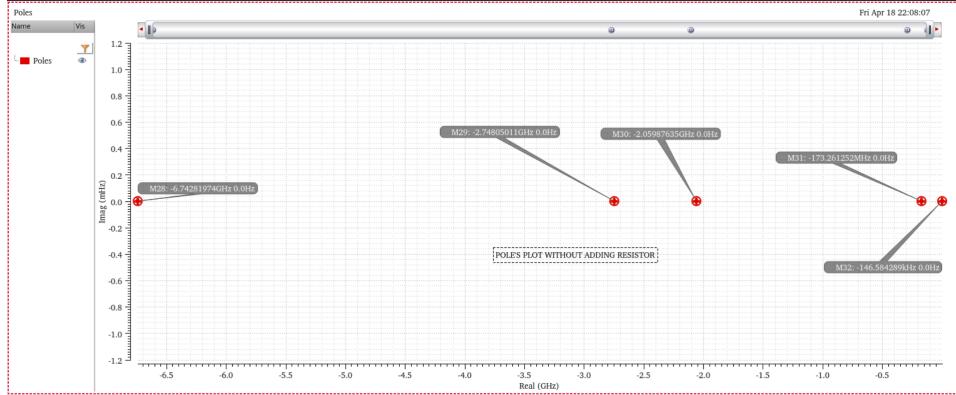
### 5.3 AC ANALYSIS PLOT WITH OUT ADDING RESISTOR AND CAPACITOR



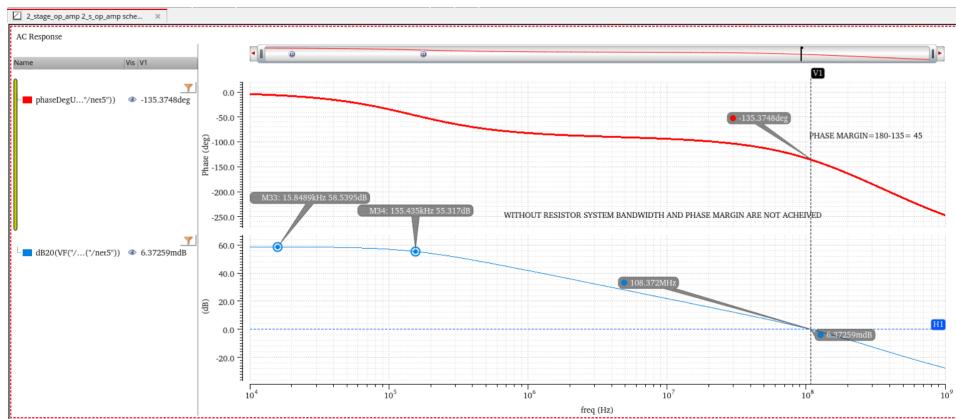
### 5.4 ZERO'S PLOT WITH OUT ADDING RESISTOR AND WITH CAPACITOR



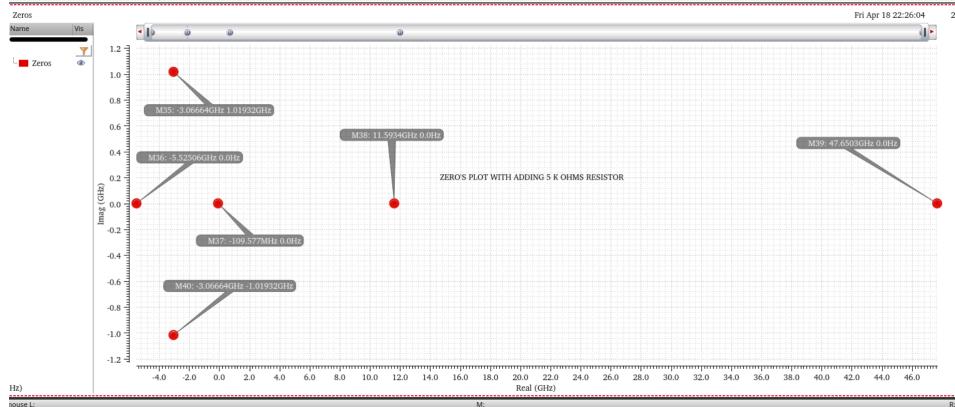
## 5.5 POLE'S PLOT WITHOUT ADDING RESISTOR AND WITH CAPACITOR



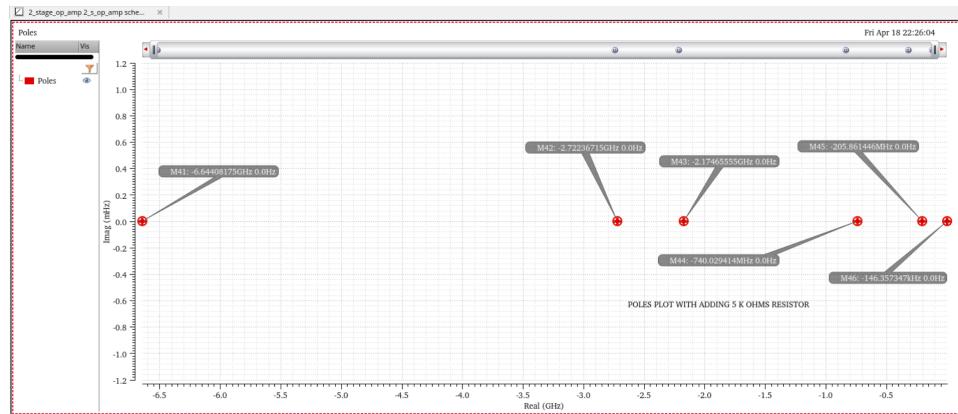
## 5.6 AC ANALYSIS WITHOUT RESISTOR AND WITH CAPACITOR



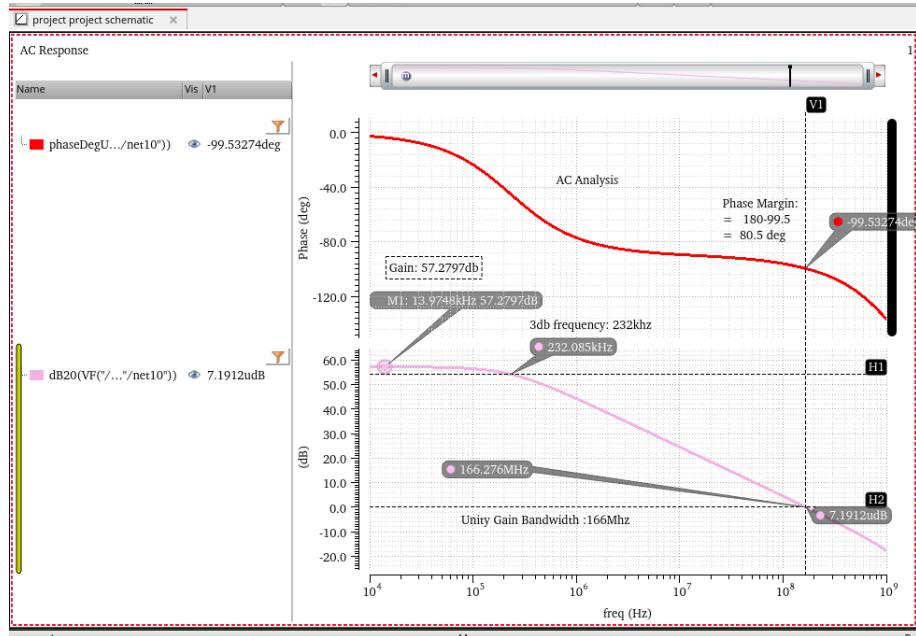
## 5.7 ZERO'S PLOT AFTER ADDING RESISTOR AND CAPACITOR



## 5.8 POLE'S PLOT AFTER ADDING RESISTOR AND CAPACITOR



## 5.9 AC ANALYSIS AFTER ADDING RESISTOR AND WITH CAPACITOR



## 6 Key Observations Pole-Zero Analysis of Compensation Techniques

### Without Compensation

- No compensation capacitor ( $C_c$ ) or resistor ( $R_z$ ) added
- Observed poles:
  - Pole 1 ( $P_1$ ) at 4 MHz
  - Pole 2 ( $P_2$ ) at 66 MHz
- Phase margin =  $0^\circ$  (system unstable)
- Conclusion: Two closely spaced poles cause instability

### With Only Compensation Capacitor

- Added  $C_c = 350 \text{ fF}$  (no  $R_z$ )
- Observed characteristics:
  - Pole 1 ( $P_1$ ) at 145 kHz
  - Pole 2 ( $P_2$ ) at 175 MHz

- RHP Zero (RHZ) at 500 MHz
- Phase margin =  $45^\circ$  (marginally stable)
- **Problem:** RHZ degrades phase margin
- **Conclusion:** Compensation helps but zero creates new issues

#### With Capacitor and Zero-Resistor

- Added both  $C_c = 350 \text{ fF}$  and  $R_z$
- Observed characteristics:
  - Pole 1 ( $P_1$ ) at 145 kHz
  - Pole 2 ( $P_2$ ) at 200 MHz
  - RHZ converted to LHZ at 109 MHz
- Phase margin =  $89^\circ$  (stable)
- **Advantages:**
  - Proper pole splitting achieved
  - Problematic zero moved to left-half plane
  - Excellent phase margin obtained
- **Conclusion:** Complete compensation network provides optimal stability
- Pole splitting effectively separates  $P_1$  and  $P_2$
- RHZ must be either:
  - Pushed to higher frequencies, or
  - Converted to LHZ using  $R_z$
- Optimal compensation requires both  $C_c$  and  $R_z$
- Final configuration achieves  $89^\circ$  phase margin (excellent stability)

## 7 Design of a Two-Stage Operational Amplifier-Hand Calculations

The design of a \*\*two-stage operational amplifier\*\* involves determining key parameters such as \*\*Miller capacitance\*\* and \*\*bias current\*\* to ensure stability, proper phase margin, and optimal slew rate.

## 7.1 Design of Transistors M1 and M2

For \*\*M1 and M2\*\*, the transconductance is chosen based on the \*\*Gain-Bandwidth Requirement\*\*:

The width-to-length ratio for \*\*M1 and M2\*\* is calculated using:

$$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{\mu_n C_{ox} I_{bias}} \quad (10)$$

Assuming:

- $\mu_n C_{ox} = 300 \text{ } \mu\text{A/V}^2$  (for NMOS)
- $I_{bias} = 15 \text{ } \mu\text{A}$

$$\left(\frac{W}{L}\right)_1 = \frac{(240 \times 10^{-6})^2}{300 \times 10^{-6} \times 15 \times 10^{-6}} \quad (11)$$

$$\left(\frac{W}{L}\right)_1 = 12.8 \quad (12)$$

Choosing  $L = 180 \text{ nm}$ :

$$W_1 = 12.8 \times 180 \text{ nm} = 2.304 \text{ } \mu\text{m} \quad (13)$$

**Conclusion:** The design of transistors  $M_1$  and  $M_2$  is completed with:

- $W/L = 12.8$
- $W = 2.304 \mu\text{m}, L = 180 \text{ nm}$

## 7.2 Design of PMOS Transistors $M_3$ and $M_4$

For the design of \*\*PMOS transistors  $M_3$  and  $M_4**$ , we follow a similar approach as in the differential amplifier.

### 7.2.1 ICMR and Saturation Condition

The design must satisfy the \*\*Input Common Mode Range (ICMR)\*\* and ensure \*\*saturation conditions\*\* for  $M_1$  and  $M_3$ . The boundary conditions are:

$$V_d > ICMR - V_{tn} \quad (14)$$

$$V_d < V_{gp} - V_{tp} \quad (15)$$

Using the expression for \*\*gate voltage of  $M_3**$ :

$$V_{gp} = \frac{2I_d}{\mu_p C_{ox} (W/L)_3} \quad (16)$$

### 7.2.2 Width-to-Length Ratio Calculation

Using the equation:

$$(W/L)_3 = \frac{2I_{d3}}{\mu_p C_{ox} (V_{DD} - ICMR - V_{th3} + V_{th1})} \quad (17)$$

Given values:

- $I_{d3} = 15 \text{ }\mu\text{A}$
- $\mu_p C_{ox} = 60 \text{ }\mu\text{A/V}^2$
- $V_{DD} = 1.8V$
- $ICMR_{max} = 1.6V$
- $|V_{th3,PMOS}| = 0.452V$
- $V_{th1,NMOS} = 0.492V$

$$(W/L)_3 = \frac{2 \times 15 \times 10^{-6}}{60 \times 10^{-6} \times (1.8 - 1.6 - 0.452 + 0.492)} \quad (18)$$

$$(W/L)_3 = 8.6 \quad (19)$$

Since  $M_3$  and  $M_4$  are symmetric, they have the same  $W/L$ .  
Choosing  $L = 500 \text{ nm}$ :

$$W_3 = 8.6 \times 180 \text{ nm} = 1.5348 \text{ }\mu\text{m} \quad (20)$$

### 7.2.3 Trans conductance Calculation

The trans conductance is given by:

$$g_{m3} = \sqrt{2I_d(W/L)_3 \mu_p C_{ox}} \quad (21)$$

Substituting values:

$$g_{m3} = \sqrt{2 \times 15 \times 10^{-6} \times 8.6 \times 60 \times 10^{-6}} \quad (22)$$

$$g_{m3} = 124 \text{ }\mu\text{S} \quad (23)$$

Since  $M_3$  and  $M_4$  are symmetric, we have:

$$g_{m4} = g_{m3} = 124 \text{ }\mu\text{S} \quad (24)$$

**Conclusion:** The design of transistors  $M_3$  and  $M_4$  is completed with:

- $W/L = 8.6$
- $W = 1.548\mu\text{m}, L = 180\text{nm}$
- Transconductance  $g_m = 124\mu\text{S}$

### 7.3 Designing Current Mirror MOSFET $M_5$

For the current mirror transistors  $M_5$  and  $M_6$ , we must ensure they remain in \*\*saturation\*\* while providing the required bias current.

#### 7.3.1 \* Minimum $V_{DS}$ Requirement for $M_5$

To keep  $M_5$  in saturation, we consider the \*\*minimum drain-source voltage\*\*:

$$V_{DS_{sat}} \geq ICMR_{\min} - \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)_1}} - V_{th1} \quad (25)$$

**Substituting values:**

- $ICMR_{\min} = 0.8V$
- $I_D = 15\mu A$
- $\mu_n C_{ox} = 300\mu A/V^2$
- $(W/L)_1 = 8.6$
- $V_{th1} = 0.492V$

$$V_{DS_{sat}} \geq 0.8 - \sqrt{\frac{2 \times (15 \times 10^{-6})}{300 \times 10^{-6} \times 8.6}} - 0.492 \quad (26)$$

$$V_{DS_{sat}} \geq 0.280V \quad (27)$$

#### 7.3.2 \* Calculating $W/L$ for $M_5$

Since  $M_5$  is a current mirror transistor, its width-to-length ratio is determined using the MOSFET current equation:

$$I_{D5} = 30\mu A \quad (28)$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{\mu_n C_{ox} V_{DS_{sat}}^2} \quad (29)$$

Substituting values:

$$\left(\frac{W}{L}\right)_5 = \frac{2 \times (30 \times 10^{-6})}{(300 \times 10^{-6}) \times (0.280)^2} \quad (30)$$

$$\left(\frac{W}{L}\right)_5 = 2.55 \quad (31)$$

Since  $M_5$  and  $M_6$  form a \*\*current mirror\*\*, they have the same \*\* $W/L$ \*\* ratio.

**Conclusion:** The design of current mirror transistors  $M_5$  and  $M_8$  is completed with:

- $W/L = 2.55$  for both  $M_5$  and  $M_8$ .
- Minimum  $V_{DS_{sat}} = 0.280V$  ensures saturation.
- $gm_5, gm_6 = 247\mu A/V$

## 7.4 Stage 2 Design Style 2

We add a resistor in series with cap and we will create a Zero their, So 10 times gm is not required.

### 7.4.1 Calculating $(W/L)_6$ for $I_6$

The  $(W/L)_6$  ratio is calculated using the equation:

$$I_6 = \frac{1}{2} \cdot \mu_p C_{ox} \cdot \left(\frac{W}{L}\right)_6 \cdot (V_{GS} - V_{TH})^2$$

Rearranging to solve for  $(W/L)_6$ :

$$\left(\frac{W}{L}\right)_6 = \frac{2I_6}{\mu_p C_{ox} \cdot (V_{GS} - V_{TH})^2}$$

Given:

$$I_6 = 120 \mu A, \quad \mu_p C_{ox} = 120 \mu A/V^2, \quad V_{GS} - V_{TH} = 0.15 V$$

Substituting the values:

$$\begin{aligned} \left(\frac{W}{L}\right)_6 &= \frac{2 \times 120 \times 10^{-6}}{120 \times 10^{-6} \times (0.15)^2} \\ \left(\frac{W}{L}\right)_6 &= \frac{240 \times 10^{-6}}{120 \times 10^{-6} \times 0.0225} \\ \left(\frac{W}{L}\right)_6 &\approx 88.88 \end{aligned}$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_6 \approx 88$$

### 7.4.2 Calculating $(W/L)_7$ Using Current Mirror Concept

To achieve the required current in the second stage, we use the current mirror concept. The  $(W/L)_7$  ratio is scaled from the golden source current ( $I_{golden} = 30 \mu A$ ) to the desired current ( $I_6 = 120 \mu A$ ).

The scaling relationship is:

$$\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_{\text{golden}}} = \frac{I_6}{I_{\text{golden}}}$$

Given:

$$I_{\text{golden}} = 30 \mu\text{A}, \quad I_6 = 120 \mu\text{A}, \quad \left(\frac{W}{L}\right)_{\text{golden}} = 10$$

Substituting the values:

$$\begin{aligned} \left(\frac{W}{L}\right)_7 &= \left(\frac{W}{L}\right)_{\text{golden}} \cdot \frac{I_6}{I_{\text{golden}}} \\ \left(\frac{W}{L}\right)_7 &= 10 \cdot \frac{120 \times 10^{-6}}{30 \times 10^{-6}} \\ \left(\frac{W}{L}\right)_7 &= 10 \cdot 4 \\ \left(\frac{W}{L}\right)_7 &\approx 40 \end{aligned}$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_7 \approx 40$$

#### 7.4.3 Calculating $g_{m6}$

The transconductance  $g_{m6}$  is calculated using the equation:

$$g_{m6} = \frac{2I_D}{V_{GS} - V_{TH}}$$

Given:

$$I_D = 120 \mu\text{A}, \quad V_{GS} - V_{TH} = 0.15 \text{ V}$$

Substituting the values:

$$\begin{aligned} g_{m6} &= \frac{2 \times 120 \times 10^{-6}}{0.15} \\ g_{m6} &= \frac{240 \times 10^{-6}}{0.15} \\ g_{m6} &\approx 1600 \mu\text{S} \end{aligned}$$

Approximating to a practical value:

$$g_{m6} \approx 1600 \mu\text{S}$$

---

Calculation of Resistor  $R$ : ““latex

#### 7.4.4 Calculating Resistor $R$

The resistor  $R$  is calculated using the formula:

$$R = \frac{1}{g_{m7}} \left( 1 + \frac{C_L}{C_C} \right)$$

Given:

$$g_{m7} = g_{m6} = 1067 \mu\text{S}, \quad C_L = 1 \text{ pF}, \quad C_C = 0.35 \text{ pF}$$

Substituting the values:

$$R = \frac{1}{1600 \times 10^{-6}} \left( 1 + \frac{1 \times 10^{-12}}{0.35 \times 10^{-12}} \right)$$

$$R = \frac{1}{1600 \times 10^{-6}} (1 + 2.857)$$

$$R = \frac{1}{1600 \times 10^{-6}} \times 3.857$$

$$R \approx 2259.375 \Omega$$

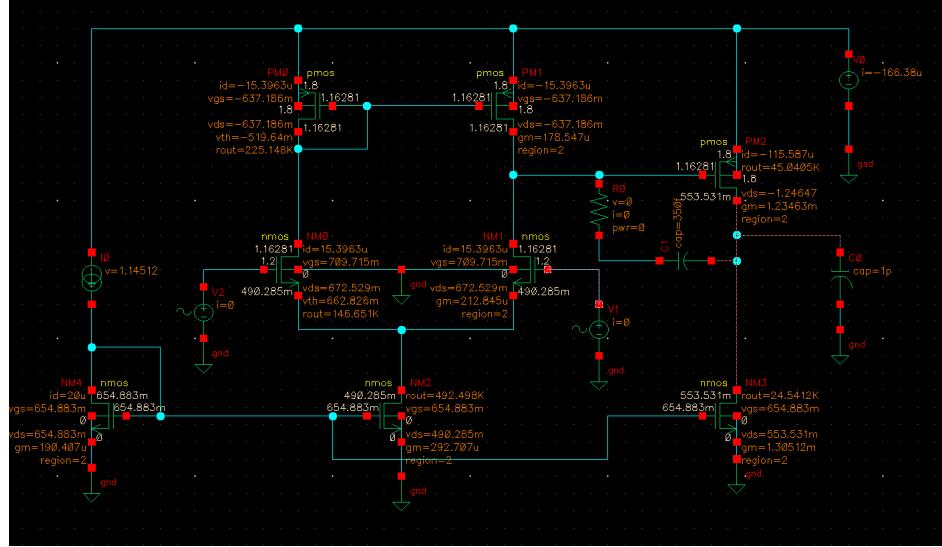
Approximating to a practical value:

$$R \approx 2.2 \text{ k}\Omega$$

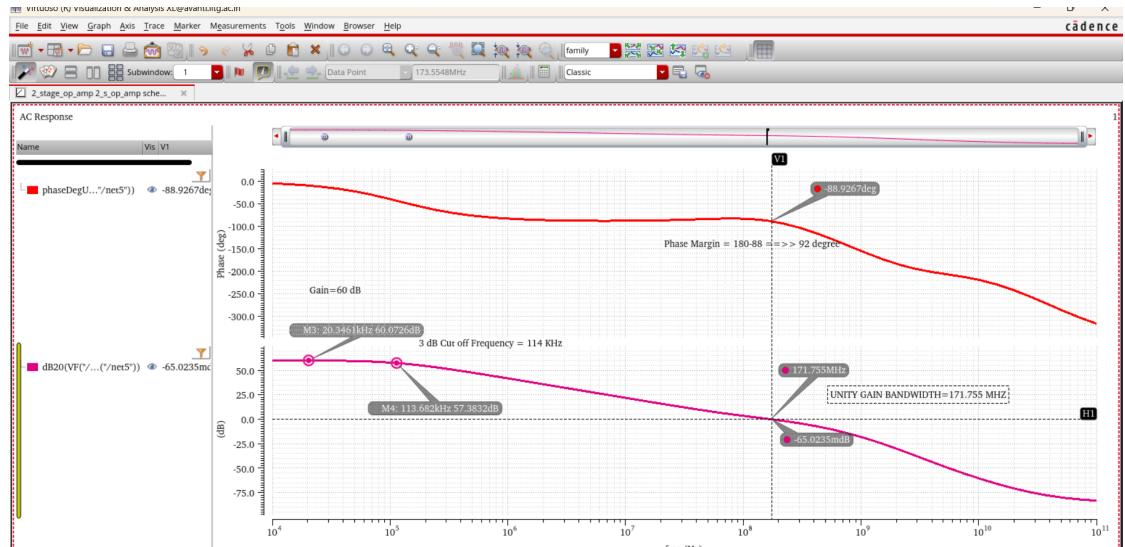
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## 8 OUTPUT RESULTS

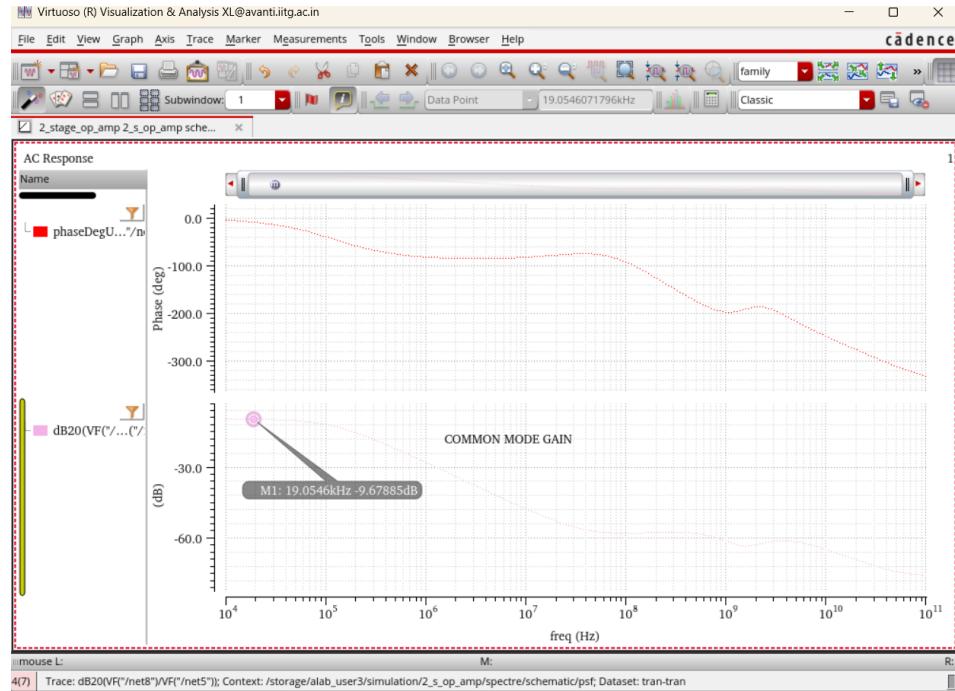
### 8.1 DC Operating Point



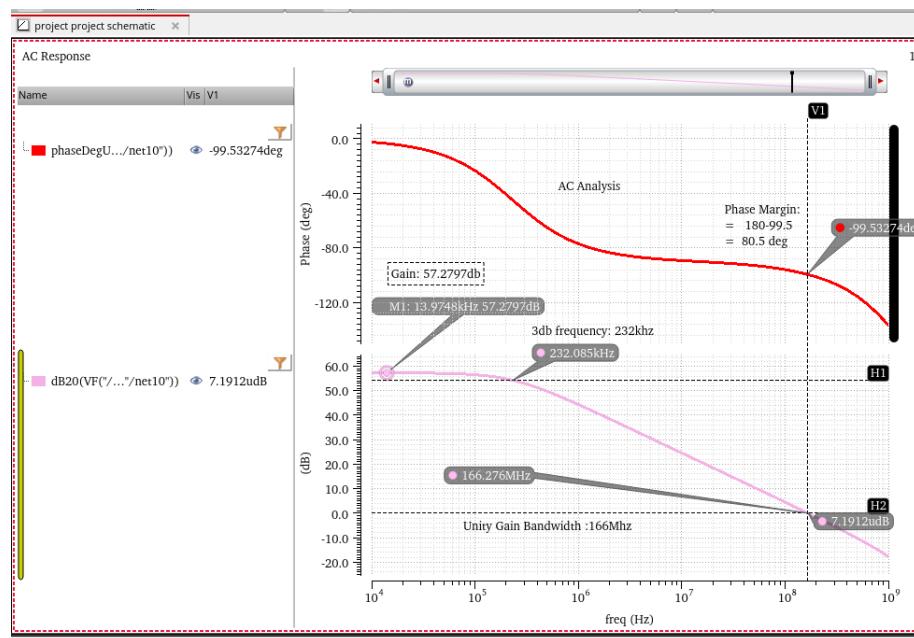
### 8.2 Gain for ICM 0.9



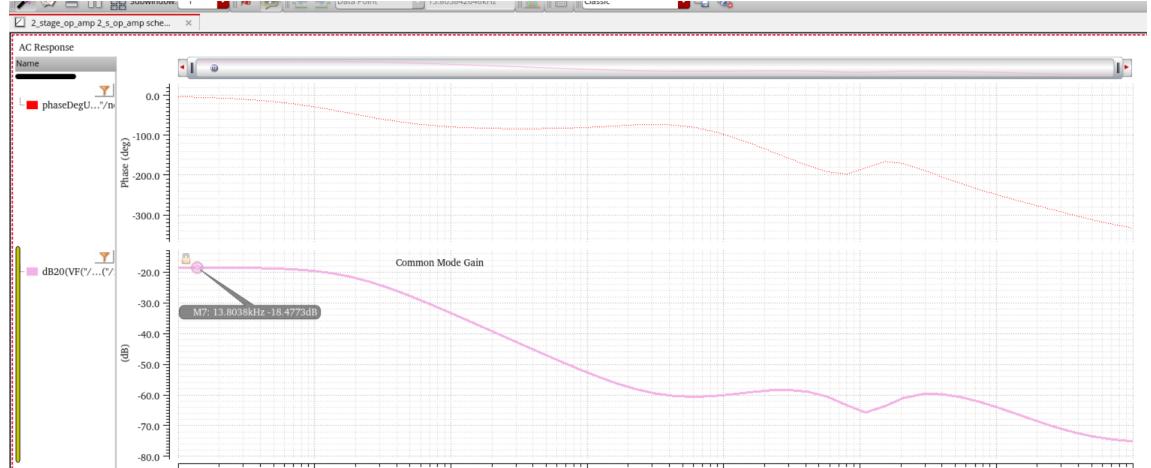
### 8.3 Common Mode Gain for ICM 0.9



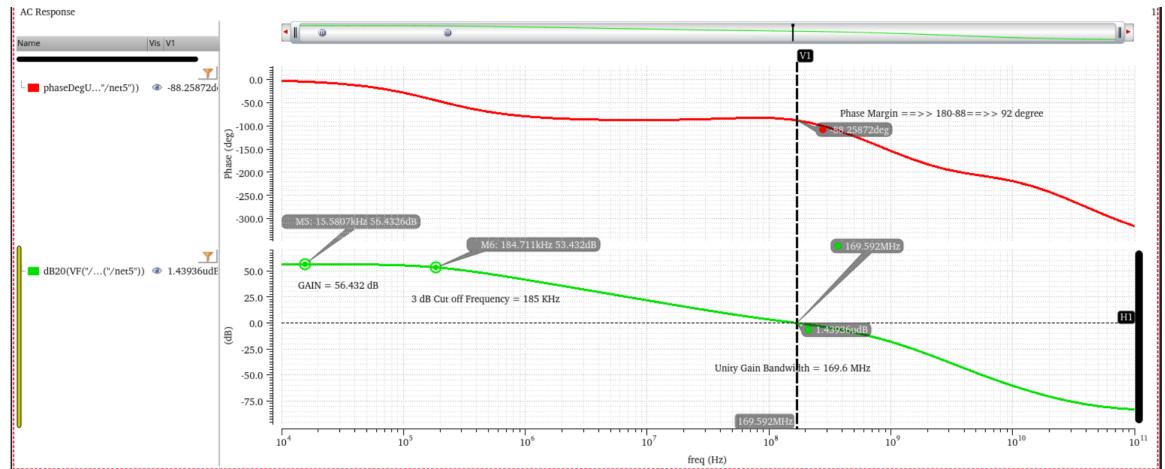
### 8.4 Gain for ICM 1.2V



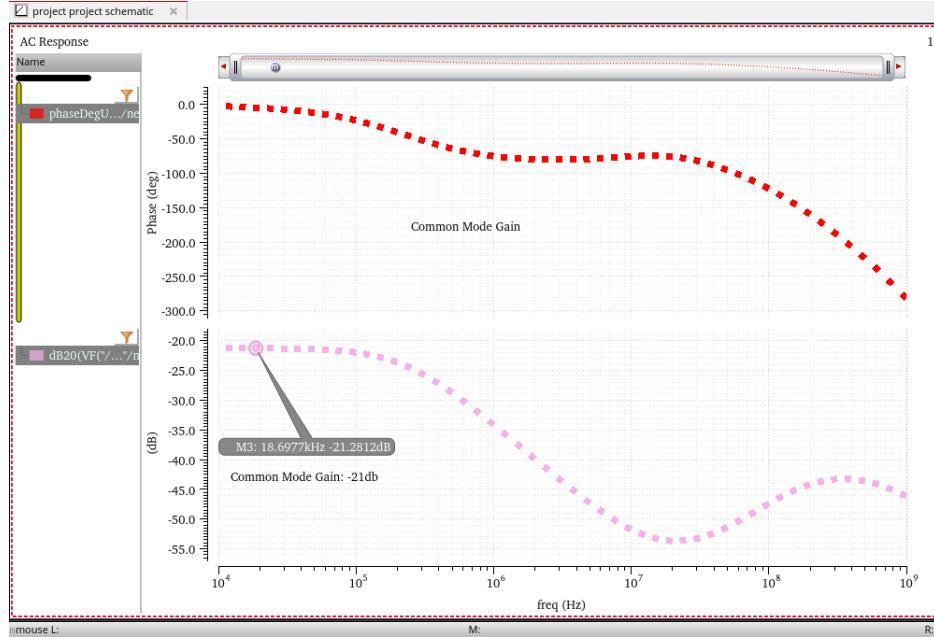
## 8.5 Common Mode Gain for ICM 1.2V



## 8.6 Gain for ICM 1.4

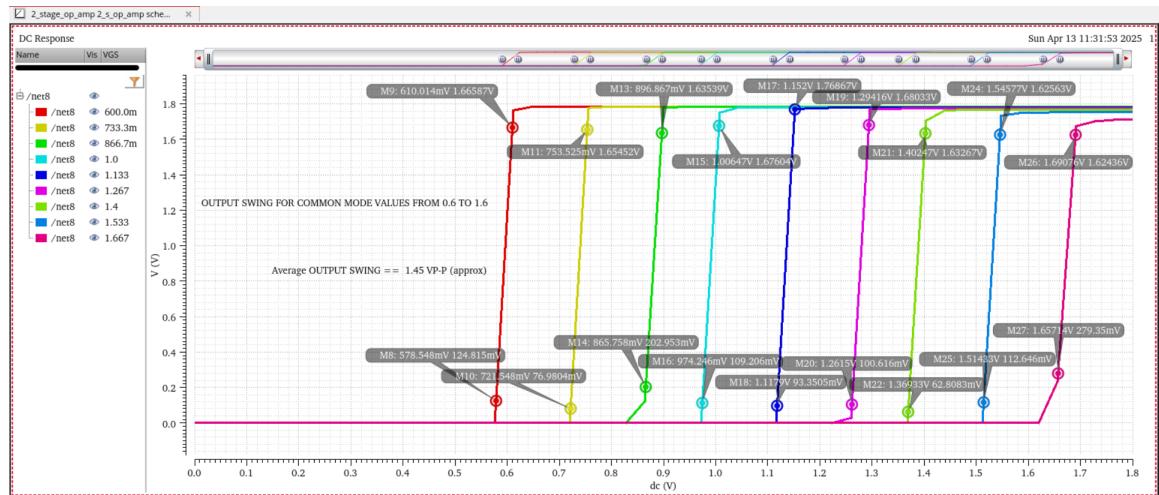


## 8.7 Common Mode Gain for ICM 1.4V



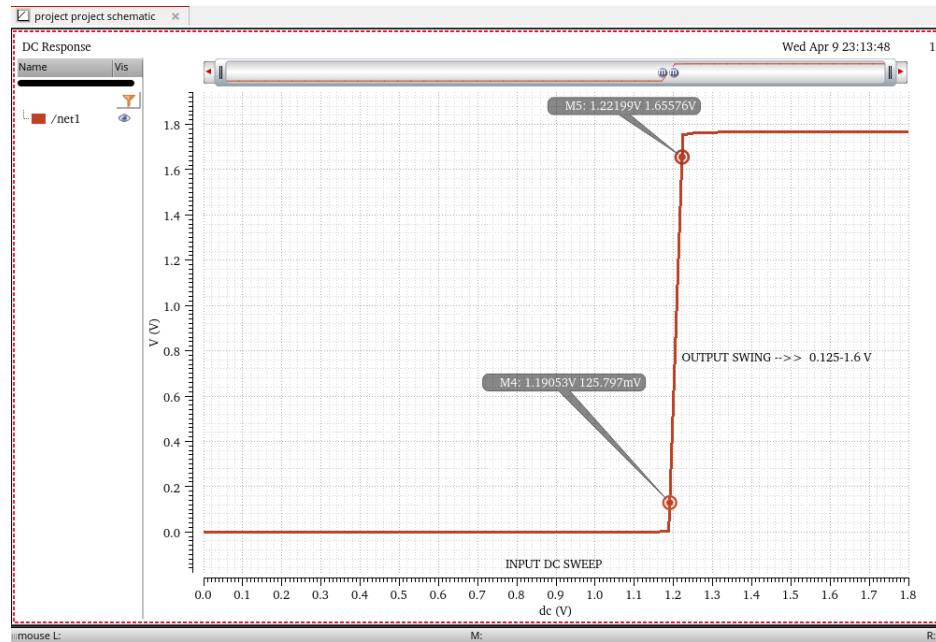
From above Plots for different Values of Input Common Mode , clearly We observed with increasing of Common Mode Values, Gain is decreasing and Common Mode Gain becoming More Negative, so based on need of application selecting common mode DC value will give desired Result, and No change GBW Phase Margin is observed ...

## 8.8 INPUT COMMON MODE RANGE



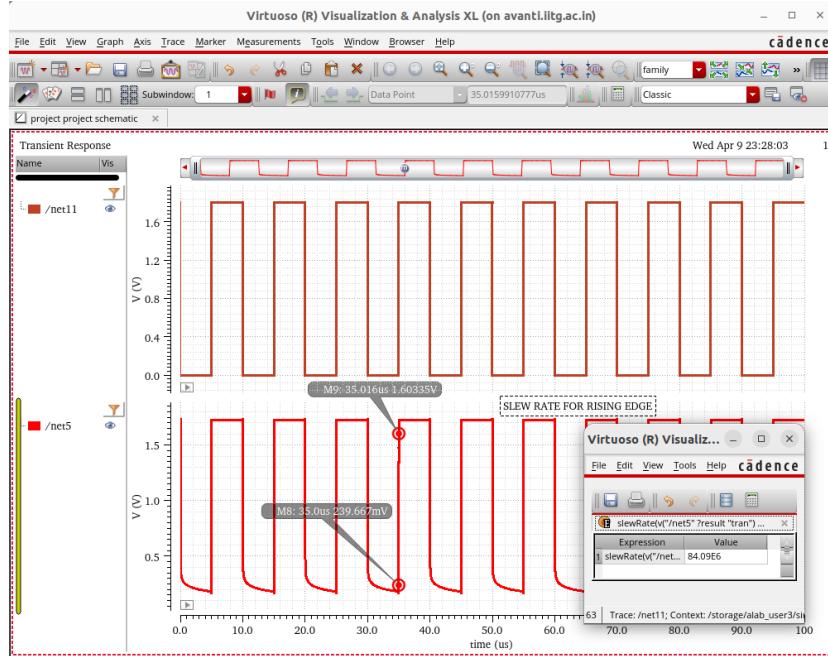
We done Parametric Analysis to find the Common Mode values of my OP-Amp, and We Observed from 0.6-1.6 It Mosfets are in saturation. and We calculated the average Output Swing

## 8.9 Output Swing for Common Mode Input 1V

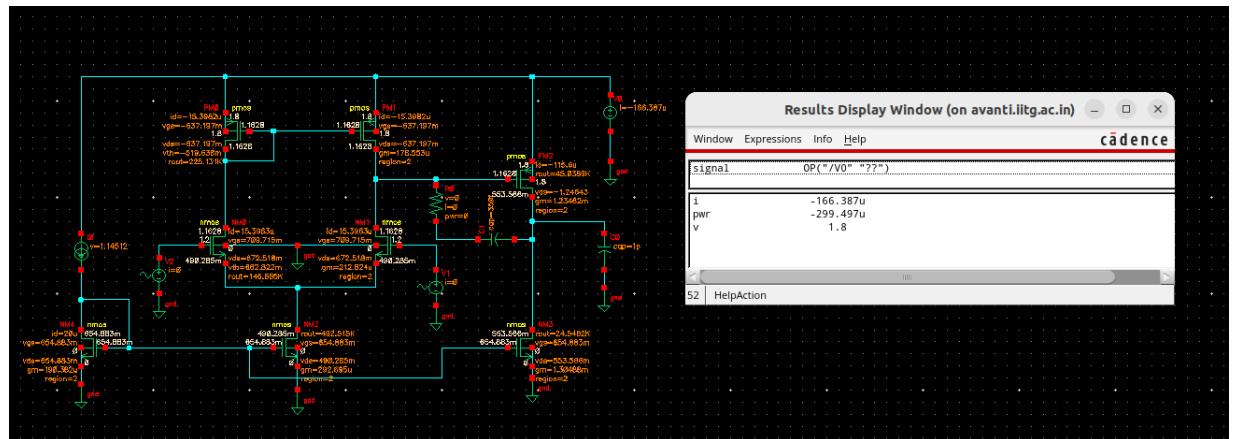


It is noted that We need to connect negative feedback to find Output swing and Slew rate

## 8.10 Slew Rate



## 8.11 POWER



## 9 Figure of Merit (FOM)

FOM :- The gain-bandwidth product (GBW), power, and area. This is especially useful when optimizing for speed, power efficiency, and silicon area, which are all critical in practical IC design.

$$\text{FoM} = \frac{\text{GBW}}{P \cdot A} = 51.4188187 \text{ } GHz/W\mu m^2$$

GBW: Gain-bandwidth product (in Hz)

P: Total power consumption (in Watts)

A: Total area of all transistors (in  $\mu m^2$ )

### \*Key Design Insights

- Higher GBW → faster response
- Lower Power → better energy efficiency
- Smaller Area → lower cost and possibly higher yield in layout

## 9.1 Final Results

Parameter	ICMR	Theoretical	Practical
Gain	0.9 V (1 kΩ)	55 dB	60.072 dB
	1.2 V (5 kΩ)	55 dB	57.279 dB
	1.4 V (5 kΩ)	55dB	56.432 dB
	1 V (Without Cap and Resistor)	55 dB	58.279 dB
Bandwidth (BW)	0.9 V (1 kΩ)	150 MHz	171.75 MHz
	1.2 V (5 kΩ)	150 MHz	166.276 MHz
	1.4 V (5 kΩ)	150 MHz	169.59 MHz
	1 V (Without CAP AND RESISTOR)	– MHz	470.276 MHz
Phase Margin	1 V (With CAP AND WITHOUT RESISTOR)	150 MHz	108.276 MHz
	0.9 V (1 kΩ)	90°	89°
	1.2 V (5 kΩ)	90°	89°
	1.4 V (5 kΩ)	90°	89°
Common Mode Gain	1 V (With CAP AND WITHOUT RESISTOR)	60°	45°
	1 V (Without CAP AND RESISTOR)	0°	1°
Slew Rate	0.9 V (1 kΩ)	–15 dB	–9.6 dB
	1.2 V (5 kΩ)	–15 dB	–18.47 dB
	1.4 V (5 kΩ)	–15 dB	–21.28 dB
Slew Rate	-	88 V/μs	84.35 V/μs
Input Swing	-	0.6V to 1.6V	0.6 V to 1.6V
Output Swing	-	0.12V to 1.62 V	0.125V to 1.65V
POWER	-	306 uW	299.5uW

Table 1: Summary of Theoretical and Practical Parameters for Different ICMR Values

While calculating the Theoretical Phase Margin, for the ideal case, the zero will come such that 90° will be the phase margin.

When calculating the swing from the DC VDS the upper MOSFET's overdrive contributes to the positive swing, and the lower MOSFET's overdrive contributes to the negative swing.

## 10 Conclusion

The design of the two-stage operational amplifier has been successfully completed, and the following conclusions can be drawn:

- **Gain and Stages:** To achieve the required gain, a two-stage op-amp structure was used. The first stage provides gain with medium transconductance ( $g_m$ ) and medium output resistance ( $r_{out}$ ), while the second stage provides additional gain with high  $g_m$  and high current, resulting in lower  $r_{ds}$ .
- **Bandwidth and Phase Margin:** The first stage primarily determines the bandwidth of the op-amp, as indicated by the design formulas. A compensator capacitor ( $C_C$ ) was used to ensure a phase margin of  $60^\circ$ .
- **Design Approaches:** The design was implemented in below ways:
  - **gm/Id:** In this method we are considering all 2nd order effects and using the simulator to design the OP AMP,SO That by this process we approach to the required results accurate .
  - **With Resistor:** By adding a  $1\text{ k}\Omega$  resistor, the required phase margin was achieved with lower current and smaller ( $W/L$ ), reducing power consumption. However, placing a resistor in an integrated circuit (IC) is challenging due to layout and process limitations.
- **Effect of Resistor on Bandwidth:** Increasing the resistor value was observed to increase the bandwidth while maintaining a constant gain. This provides flexibility in tuning the op-amp's performance.
- **ICMR and Gain Variation:** The input common-mode range (ICMR) affects the gain of the op-amp, but the variation in gain across the ICMR is not significant. This ensures stable operation across a wide range of input voltages.
- **Power and Area Trade-offs:** The design with the resistor offers better power efficiency and smaller transistor sizes, but it introduces additional complexity in the IC layout. The resistor-less design, while simpler to implement, consumes more power and area.
- **Practical Considerations:** The choice between the two design approaches depends on the specific application requirements, such as power consumption, area constraints, and the feasibility of integrating resistors in the IC.

In conclusion, the two-stage op-amp design successfully meets the specified requirements, and the trade-offs between the two design approaches have been thoroughly analyzed. The use of a compensator capacitor and resistor provides flexibility in achieving the desired phase margin and bandwidth while optimizing power and area.