EE517: ANALOG VLSI LAB
Experiment 6

Design and analysis of a 2-stage op-amp

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EEE - VLSI & Nanoelectronics

Contents

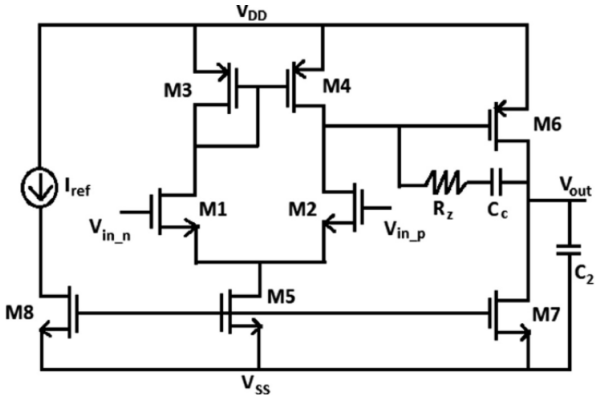
1 Objective:

Design and analyze a 2-stage op-amp with the Design specification mentioned below.

1.1 Design Specification:

- **Process Technology:** 0.18μm CMOS
- **Power Supply:**
  - $V_{DD} = 1.8$V
  - $V_{SS} = 0$V
- **Load Capacitance:** 1pF
- **Phase Margin:** Greater than or equal to 60°
- **DC Gain:** At least 1000 V/V (60 dB)
- **Common Mode Gain:** At most 0.1 V/V (-20 dB)
- **Unity Gain Frequency:** Greater than 100 MHz
- **Slew Rate:** Greater than or equal to 10 V/μs
- **Output Voltage Swing (Differential Peak-to-Peak):** At least 800 mV_{pp}
- **Power Consumption:** Minimum

1.2 Circuit Diagram:

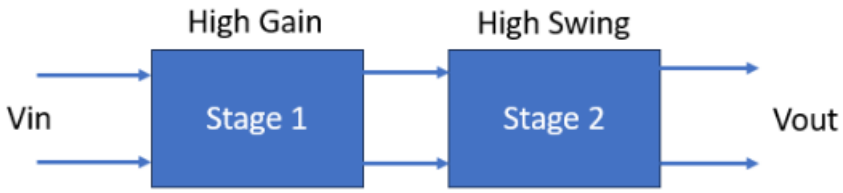


2 Theory

The two-stage circuit architecture has historically been the most popular approach to OpAmp design.
It can provide high gain and high output swing.
It is an excellent example to illustrate many important design concepts that area also directly applicable to other designs.
Typical applications of OpAmps in analog integrated circuits:

1. Amplification and filtering
2. Biasing and reguation
3. Switched-capacitor circuits

The two-stage refers to the number of gain stages in the OpAmp. The output buffer is normally present only when resistive loads needs to be driver. If the load is purely capacitive, it is not needed.



The load is assumed capacitive.
The first stage is a pMOS differential pair with nMOS current mirrors. Second stage is a common-source amplifier.
Shown in the diagram are reasonable widths in 0.18um technology (length all made 0.3um). Reasonable sizes for the lengths are usually 1.5 to 10 times of the minimum length (while digital circuits usually use the minimum).

2.1 OpAmp gain

For low-frequency applications, the gain is one of the most critical parameters. Note that compensation capacitor Cc can be treated open at low frequency.
gain of 1st stage

$$A_{V1} = -g_{m1}(r_{ds2}||r_{ds4}) \tag{1}$$

The second gain stage is simply a common stage gain stage with a pchannel active load Q6s .Its gain is given by

$$A_{V2} = -g_{m7}(r_{d6}||r_{ds7}) \tag{2}$$

$$Overallgain(A_V) = A_{V1} * A_{V2} \tag{3}$$

3 THEORETICAL ANALYSIS

For MOSFET we have several basic parameters including

$$I_D = \frac{1}{2} * Kn\frac{W}{L}(V_{gs} - V_{tn})^2 \tag{4}$$

3.1 Gain, Pole and zeros

We define the input Vin, the output voltage of the first stage i.e. the input voltage of the second stage V1, and the output voltage of the whole circuit Vout, so we can get that for two stage operational amplifier we have

$$V_{out}/V_{in} = (V_{out}/V_1) * (V_1/V_{in}) \tag{5}$$

so we can calculate the voltage gain of two stage separately and then combine together We set the output resistance of the first stage Ro2 k Ro4 as R1 and the output resistance of the second stage Ro6 k Ro7 as R2. We also se the output capacitance of the first stage as C1 and C2 CL for the second stage. So we finally get that

$$V_{out}/V_{in} = \frac{(gm1 * R1)(gm2 * R2)(1 - sCc/gm2)}{as^2 + bs + c} \tag{6}$$

$$a = R_1R_2(C_1C_2 + C_1C_L + C_2C_L) \tag{7}$$

$$b = R_2(C_c + C_2) + R_1(C_c + C_1) + Cc * gm2 * R1R2 \tag{8}$$

to find the poles and zeros, we must transform the equation into form like

$$\frac{V_{out}}{V_{in}} = \frac{A_{dc}(1 - \frac{s}{z1})}{(1 + \frac{s}{p1})(1 + \frac{s}{p2})} \tag{9}$$

here for this two stage amplifier we have the DC gain of the amplifier

$$A_{dc} = gm1R1gm2R2 \tag{10}$$

the zero point of the circuit

$$z1 = \frac{gm2}{Cc} \tag{11}$$

When it comes to the poles of the circiut, approximately we have

$$p1 = \frac{1}{b} \tag{12}$$

we can simply it to

$$p_1 = \frac{1}{C_c g_{m2} R_1 R_2} \tag{13}$$

for another pole p2 we have

$$p_2 = \frac{g_{m2}}{C_1 + C_2} \tag{14}$$

3.2 Phase Margin

The gain band with GBW is equal to $DCgainp_1 = (g_{m1}/C_c)$ For phase margin, we have

$$z = 10 * GBW \tag{15}$$

then we need

$$p_2 \geq 2.2GBW \tag{16}$$

and finally

$$C_c \geq 0.22C_L \tag{17}$$

to get more than 60∘ phase margin. Thus we also have

$$\frac{gm1}{gm2} \leq 0.22 \tag{18}$$

3.3 Slew Rate

In our design, the slew rate is just equal to

$$slewrate = \frac{I_5}{C_c} \tag{19}$$

we already have I5 = 40µA so Cc must be under 10C, with is certain to full-fill. Here we need to obtain 10MV /s slew rate under 100MHZ, so we need the voltage change more than 0.05V in one pulse, which is 5ns in width.

4 Design Steps

Design your opamp such that the specifications are met under a 0.1 variation of the supply voltage

4.1 Design Principle

The minimum size of the MOSFET we can use is 180nm in length and 400 nm in width, but normally we don't use the minimum channel length due to the increase of the λ. L ¿ 2Lmin is recommended, in this design, we use L = 1u. And after initially designed, to optimise the performance of the op-amp, we will adjust the length of some MOSFET while keep the (W/L) unchanged.
To control the systematic offset we set

$$\beta = \frac{W}{L} \tag{20}$$

$$\frac{\beta_3}{\beta_6} = \frac{\beta_4}{\beta_6} = \frac{\beta_5}{2 * \beta_7} \tag{21}$$

We also have

$$\frac{\beta_8}{\beta_5} = \frac{I_{ref}}{i_5} \tag{22}$$

and

$$\frac{\beta_8}{\beta_7} = \frac{I_{ref}}{i_7} \tag{23}$$

During the procedure of the design. we first calculate the proper value of the compensate capacitance and resistance, then we will design the first stage, finally the second stage will be designed.

4.2 Calculations and Parameter Optimization

4.2.1 Design of Cc

To satisfy the phase margin of 60 degrees we need $Cc > 0.22CL$, since we have CL = 1pF so we can use $Cc > 220fF$. To achieve slew rate 10V /—mus we need Cc = 10pf , to meet a balance between two requirement,and we choose Cc = 4pf

4.2.2 Design of M1 and M2:

We have

$$gm1 = GBW * Cc * 2\pi \tag{24}$$

and GBW is also called unity gain frequency, which is listed in the design goal with value of 100MHZ. So we need to apply that

$$gm1 = 100MHZ * 4pF * 2p = 251\mu \tag{25}$$

and for convince we choose a litter larger value 510µ. Since

$$\frac{W}{L} = \frac{g_{m1}^2}{\mu_n C_{ox} * 2I_D} \tag{26}$$

4.2.3 Design of M3 and M4

To get more than 800mV of the output range, we need to at least 800mV input common mode voltage range before the zero point, where the gain is 1. This characteristic parameter can also be used to determined the size of the MOSFET M1 and M2. We have

$$(\frac{W}{L})1,2 = \frac{2 * I_{d3}}{\mu p C_{ox}(V_{DD} - ICMR(+) - VTH1 + VTH3)^2} \tag{27}$$

we choose ICMR(+) at 1.6V

4.2.4 Design of M5 and M8

In the mean while, we also need to fit the proper value of ICMR(-) to determine the size of MOSFET M5. We have

$$(\frac{W}{L})5 = \frac{Id5}{\mu_n Cox(VDsat)^2} \tag{28}$$

with

$$VDsat = ICMR(-) - \sqrt{\frac{2I_{D1}}{\beta_1}} \tag{29}$$

4.2.5 Design of M6

And also we need $gm2 > gm1$, so we need $gm2 > 2318$, we want

$$V_{DS3} = V_{DS4} = V_{DS6} \tag{30}$$

and

$$V_{GS3} = V_{GS4} = V_{GS6} \tag{31}$$

So we need

$$\frac{\beta 6}{\beta 4} = \frac{I_6}{I_4} = \frac{g_{m2}}{g_{m4}} \tag{32}$$

4.2.6 Design of M7:

$$\frac{\beta 7}{\beta 5} = \frac{I_7}{I_5} = \frac{g_{m7}}{g_{m5}} \tag{33}$$

4.2.7 Common and differential mode gain

After initially determining the parameters of the MOSFETs, we need to check output voltage gain, than we may need to adjust the parameters to meet the requirements of common and differential mode voltage gain.

Advantage of Low Common-Mode Gain in Op-Amps A low common-mode gain in operational amplifiers is highly advantageous, especially in reducing noise and improving signal integrity. Common-mode gain refers to the amplification of signals that are present simultaneously and in-phase on both input terminals of the op-amp. In practical applications, common-mode signals often arise from external noise sources, such as electromagnetic interference (EMI) or power supply fluctuations.

By minimizing the common-mode gain (typically to values less than 0.1 V/V or -20 dB), the op-amp effectively rejects these unwanted noise signals. This is particularly important in differential amplifier configurations, where the desired signal is the difference between the two input terminals. A low common-mode gain ensures that the op-amp amplifies only the differential signal while attenuating common-mode noise, thereby enhancing the signal-to-noise ratio (SNR).

Furthermore, a low common-mode gain contributes to better overall performance in precision analog circuits, such as instrumentation amplifiers and data acquisition systems, where noise reduction is critical. This characteristic makes the op-amp more robust and reliable in environments with high levels of electrical noise.

5 Design Caluculations

5.1 Stage 1

5.1.1 Finding Compensator Capacitor (C_c)

In operational amplifier design, a compensator capacitor (C_c) is often used to ensure stability and achieve the desired phase margin. For a phase margin of 60°, the compensator capacitor should satisfy the following condition:

$$C_c > 0.22 \times C_L$$

where:

- C_c is the compensator capacitor.
- C_L is the load capacitance.

Given:

$$C_L = 1\,\text{pF}$$

Substituting the value of C_L into the equation:

$$C_c > 0.22 \times 1\,\text{pF}$$

$$C_c > 0.22\,\text{pF}$$

To ensure sufficient margin, we choose:

$$C_c = 0.3\,\text{pF}$$

Thus, the compensator capacitor (C_c) is selected as 0.3 pF to achieve a phase margin of 60°.

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5.1.2 Finding Current

The current in the operational amplifier can be determined using the slew rate (SR) and the compensator capacitor (C_c). The slew rate is defined as:

$$SR = \frac{I}{C_c}$$

$$I = 10\,\text{V}/\mu\text{s} \times 0.3\,\text{pF}$$

$$I = 10 \times 10^6\,\text{V/s} \times 0.3 \times 10^{-12}\,\text{F}$$

$$I = 3\,\mu\text{A}$$

However, to ensure proper biasing and good V_{GS} and $(W/L)_1$ values for the transistors, we choose a higher current value. Let:

$$I_D = 20\,\mu\text{A}$$

This ensures sufficient drive capability and better performance in the operational amplifier design.

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5.1.3 Gain Bandwidth Product (GBW)

The Gain Bandwidth Product (GBW) is given as 100 MHz. The transconductance (g_{m1}) of the input stage can be calculated using the formula:

$$g_{m1} = \text{GBW} \times C_c \times 2\pi$$

Substituting the given values:

$$g_{m1} = 100 \times 10^6 \,\text{Hz} \times 0.3 \times 10^{-12} \,\text{F} \times 2\pi$$

$$g_{m1} = 100 \times 10^6 \times 0.3 \times 10^{-12} \times 6.28$$

$$g_{m1} \approx 188.5 \,\mu\text{S}$$

For simplicity, we approximate g_{m1} to:

$$g_{m1} \approx 200 \,\mu\text{S}$$

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5.1.4 Finding $(W/L)_1$ Ratio

The transconductance (g_{m1}) is also related to the $(W/L)_1$ ratio of the transistor by the equation:

$$g_{m1} = \sqrt{2 \cdot I_D \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_1}$$

Rearranging to solve for $(W/L)_1$:

$$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{2 \cdot I_D \cdot \mu_n \cdot C_{ox}}$$

Given:

$$I_D = 10 \,\mu\text{A}, \quad \mu_n C_{ox} = 350 \,\mu\text{A/V}^2, \quad g_{m1} = 200 \,\mu\text{S}$$

Substituting the values:

$$\left(\frac{W}{L}\right)_1 = \frac{(200 \times 10^{-6})^2}{2 \times 10 \times 10^{-6} \times 350 \times 10^{-6}}$$

$$\left(\frac{W}{L}\right)_1 = \frac{4 \times 10^{-8}}{7 \times 10^{-9}}$$

$$\left(\frac{W}{L}\right)_1 \approx 5.71$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_{1,2} \approx 6$$

—

5.1.5 Finding $V_{GS} - V_{TH}$ and V_{GS}

The transconductance (g_{m1}) is also related to the overdrive voltage ($V_{GS} - V_{TH}$) by the equation:

$$g_{m1} = \frac{2I_D}{V_{GS} - V_{TH}}$$

Rearranging to solve for $V_{GS} - V_{TH}$:

$$V_{GS} - V_{TH} = \frac{2I_D}{g_{m1}}$$

Substituting $I_D = 10\,\mu\text{A}$ and $g_{m1} = 200\,\mu\text{S}$:

$$V_{GS} - V_{TH} = \frac{2 \times 10 \times 10^{-6}}{200 \times 10^{-6}}$$

$$V_{GS} - V_{TH} = 0.1\,\text{V}$$

$$V_{GS} = V_{TH} + (V_{GS} - V_{TH})$$

$$V_{GS} = 0.5\,\text{V} + 0.1\,\text{V}$$

$$V_{GS} = 0.6\,\text{V}$$

5.1.6 Finding $(W/L)_4$ and $(W/L)_3$ Using ICMR_max

To ensure that MOSFETs M_1 and M_2 remain in saturation, we use the maximum input common-mode range (ICMR_max). Let ICMR_max be 1.6 V.

5.1.7 Condition for M_1 and M_2 to Remain in Saturation

For M_1 and M_2 to remain in saturation, the drain voltage of M_1 (V_D) must satisfy:

$$V_D \geq V_G - V_{TH}$$

where:

- $V_D = V_X$ (drain voltage of M_1),
- V_G is the gate voltage of M_1,
- V_{TH} is the threshold voltage.

Expressing V_X in Terms of M_4 The voltage V_X is also the gate-source voltage (V_{GS}) of M_4. For M_4:

$$V_X = V_{DD} - V_{SG4}$$

where V_{SG4} is the source-gate voltage of M_4.

The source-gate voltage of M_4 is given by:

$$V_{SG4} = \sqrt{\frac{2I_D}{\beta_4}} + V_{TH}$$

where:

- $I_D = 10\,\mu\text{A}$ (drain current),
- $\beta_4 = \left(\frac{W}{L}\right)_4 \cdot \mu_p C_{ox}$,
- $\mu_p C_{ox} = 60\,\mu\text{A/V}^2$.

Substituting V_{SG4} into the equation for V_X:

$$V_X = V_{DD} - \left(\sqrt{\frac{2I_D}{\beta_4}} + V_{TH}\right)$$

Ensuring $V_D \geq V_G - V_{TH}$ For M_1 and M_2 to remain in saturation:

$$V_X \geq V_G - V_{TH}$$

Substituting V_X:

$$V_{DD} - \left(\sqrt{\frac{2I_D}{\beta_4}} + V_{TH}\right) \geq V_G - V_{TH}$$

Simplifying:

$$V_{DD} - \sqrt{\frac{2I_D}{\beta_4}} - V_{TH} \geq V_G - V_{TH}$$

$$V_{DD} - \sqrt{\frac{2I_D}{\beta_4}} \geq V_G$$

Given $V_G = \text{ICMR\_max} = 1.6\,\text{V}$ and $V_{DD} = 1.8\,\text{V}$:

$$1.8 - \sqrt{\frac{2 \times 10 \times 10^{-6}}{\beta_4}} \geq 1.6$$

$$1.8 - 1.6 \geq \sqrt{\frac{20 \times 10^{-6}}{\beta_4}}$$

$$0.2 \geq \sqrt{\frac{20 \times 10^{-6}}{\beta_4}}$$

Squaring both sides:

$$0.04 \geq \frac{20 \times 10^{-6}}{\beta_4}$$

$$\beta_4 \geq \frac{20 \times 10^{-6}}{0.04}$$

$$\beta_4 \geq 500 \times 10^{-6}$$

Calculating $(W/L)_4$

$$\left(\frac{W}{L}\right)_4 \cdot 60 \times 10^{-6} \geq 500 \times 10^{-6}$$

$$\left(\frac{W}{L}\right)_4 \geq \frac{500}{120}$$

$$\left(\frac{W}{L}\right)_4 \geq 8.34$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_{4,3} \approx 8$$

5.1.8 Finding $(W/L)_5$ and $(W/L)_8$ Using Minimum ICMR

Using the minimum input common-mode range (ICMR_min = 0.6 V), we calculate $(W/L)_5$ to ensure proper operation. Based on the design constraints and calculations, we obtain:

$$\left(\frac{W}{L}\right)_5 = 6$$

5.1.9 Finding $(W/L)_8$ for $V_{GS} = 650\,\mathbf{mV}$

For a current of 30 μA and an overdrive voltage corresponding to $V_{GS} = 650$ mV, we calculate $(W/L)_6$. Based on the design constraints and calculations, we obtain:

$$\left(\frac{W}{L}\right)_8 = 8.3$$

—

This completes the calculations for Stage one,

5.2 Stage 2 Design Style 1

5.2.1 Finding g_{m6}

To ensure a phase margin of 60°, the transconductance of M_6 (g_{m6}) must satisfy:

$$g_{m6} \geq g_{m1}$$

where $g_{m1} = 200\,\mu$S (from previous calculations).

For sufficient phase margin, we choose:

$$g_{m6} = 2000\,\mu\text{S}$$

5.2.2 Finding I_D Using g_{m6} and $V_{GS} - V_{TH}$

The transconductance g_{m6} is related to the current I_D and the overdrive voltage $(V_{GS} - V_{TH})$ by the equation:

$$g_{m6} = \frac{2I_D}{V_{GS} - V_{TH}}$$

Given:

$$g_{m6} = 2000\,\mu\text{S}, \quad V_{GS} - V_{TH} = 0.15\,\text{V}$$

Rearranging to solve for I_D:

$$I_D = \frac{g_{m6} \cdot (V_{GS} - V_{TH})}{2}$$

$$I_D = \frac{2000 \times 10^{-6} \times 0.15}{2}$$

$$I_D = 150\,\mu\text{A}$$

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This completes the calculation of I_D using $V_{GS} - V_{TH} = 0.15\,\text{V}$.

5.2.3 Calculating $(W/L)_6$

The current I_D is also related to the $(W/L)_6$ ratio by the equation:

$$I_D = \frac{1}{2} \cdot \mu_p C_{ox} \cdot \left(\frac{W}{L}\right)_6 \cdot (V_{GS} - V_{TH})^2$$

Rearranging to solve for $(W/L)_6$:

$$\left(\frac{W}{L}\right)_6 = \frac{2I_D}{\mu_p C_{ox} \cdot (V_{GS} - V_{TH})^2}$$

Given:

$$I_D = 150\,\mu\text{A}, \quad \mu_p C_{ox} = 120\,\mu\text{A/V}^2, \quad V_{GS} - V_{TH} = 0.15\,\text{V}$$

Substituting the values:

$$\left(\frac{W}{L}\right)_6 = \frac{2 \times 150 \times 10^{-6}}{120 \times 10^{-6} \times (0.15)^2}$$

$$\left(\frac{W}{L}\right)_6 = \frac{300 \times 10^{-6}}{120 \times 10^{-6} \times 0.0225}$$

$$\left(\frac{W}{L}\right)_6 = \frac{300}{2.7}$$

$$\left(\frac{W}{L}\right)_6 \approx 111.11$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_6 \approx 100$$

5.2.4 Finding $(W/L)_7$

From current mirror concepts, I can find the W/L of 7 (using W/L of 8)

$$\left(\frac{W}{L}\right)_7 \approx 30.31$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_7 \approx 30$$

5.2.5 Summary of Calculated Parameters

The following table summarizes the calculated values for transconductance (g_m), (W/L) ratios, and current (I_D) for each MOSFET in the design:

MOSFET	**Parameter**	**Value**	I_D
M_1, M_2	g_{m1}	$200\,\mu$S	$10\,\mu$A
M_1, M_2	$(W/L)_1, (W/L)_2$	6	$10\,\mu$A
M_3, M_4	$(W/L)_3, (W/L)_4$	8	$10\,\mu$A
M_5	$(W/L)_5$	6	$20\,\mu$A
M_6	g_{m6}	$2000\,\mu$S	$70\,\mu$A
M_6	$(W/L)_6$	100	$150\,\mu$A
M_7	$(W/L)_7$	16	$150\,\mu$A
M_8	$(W/L)_8$	8	$30\,\mu$A

Table 1: Summary of Calculated Parameters for MOSFETs

5.3 Stage 2 Design Style 2

We add a resistor in series with cap and we will create a Zero their, So 10 times gm is not required.

5.3.1 Calculating Current in the Second Stage (I_6)

The current in the second stage (I_6) is calculated using the formula:

$$I_6 = I_{SS}\left(1 + \frac{C_L}{C_C}\right)$$

Given:

$$I_{SS} = 20\,\mu\text{A}, \quad C_L = 1\,\text{pF}, \quad C_C = 0.35\,\text{pF}$$

Substituting the values:

$$I_6 = 20 \times 10^{-6}\left(1 + \frac{1 \times 10^{-12}}{0.35 \times 10^{-12}}\right)$$

$$I_6 = 20 \times 10^{-6}\,(1 + 2.857)$$

$$I_6 = 20 \times 10^{-6} \times 3.857$$

$$I_6 \approx 77.14\,\mu\text{A}$$

Approximating to a practical value:

$$I_6 \approx 80\,\mu\text{A}$$

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5.3.2 Calculating $(W/L)_6$ for I_6

The $(W/L)_6$ ratio is calculated using the equation:

$$I_6 = \frac{1}{2} \cdot \mu_p C_{ox} \cdot \left(\frac{W}{L}\right)_6 \cdot (V_{GS} - V_{TH})^2$$

Rearranging to solve for $(W/L)_6$:

$$\left(\frac{W}{L}\right)_6 = \frac{2I_6}{\mu_p C_{ox} \cdot (V_{GS} - V_{TH})^2}$$

Given:

$$I_6 = 80\,\mu\text{A}, \quad \mu_p C_{ox} = 120\,\mu\text{A/V}^2, \quad V_{GS} - V_{TH} = 0.15\,\text{V}$$

Substituting the values:

$$\left(\frac{W}{L}\right)_6 = \frac{2 \times 80 \times 10^{-6}}{120 \times 10^{-6} \times (0.15)^2}$$

$$\left(\frac{W}{L}\right)_6 = \frac{160 \times 10^{-6}}{120 \times 10^{-6} \times 0.0225}$$

$$\left(\frac{W}{L}\right)_6 = \frac{160}{2.7}$$

$$\left(\frac{W}{L}\right)_6 \approx 59.26$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_6 \approx 60$$

5.3.3 Calculating $(W/L)_7$ Using Current Mirror Concept

To achieve the required current in the second stage, we use the current mirror concept. The $(W/L)_7$ ratio is scaled from the golden source current ($I_{\text{golden}} = 30\,\mu\text{A}$) to the desired current ($I_6 = 80\,\mu\text{A}$).

The scaling relationship is:

$$\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_{\text{golden}}} = \frac{I_6}{I_{\text{golden}}}$$

Given:

$$I_{\text{golden}} = 30\,\mu\text{A}, \quad I_6 = 80\,\mu\text{A}, \quad \left(\frac{W}{L}\right)_{\text{golden}} = 10$$

Substituting the values:

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_{\text{golden}} \cdot \frac{I_6}{I_{\text{golden}}}$$

$$\left(\frac{W}{L}\right)_7 = 10 \cdot \frac{80 \times 10^{-6}}{30 \times 10^{-6}}$$

$$\left(\frac{W}{L}\right)_7 = 10 \cdot 2.6667$$

$$\left(\frac{W}{L}\right)_7 \approx 26.67$$

Approximating to a practical value:

$$\left(\frac{W}{L}\right)_7 \approx 23.33$$

5.3.4 Calculating g_{m6}

The transconductance g_{m6} is calculated using the equation:

$$g_{m6} = \frac{2I_D}{V_{GS} - V_{TH}}$$

Given:

$$I_D = 80\,\mu\text{A}, \quad V_{GS} - V_{TH} = 0.15\,\text{V}$$

Substituting the values:

$$g_{m6} = \frac{2 \times 80 \times 10^{-6}}{0.15}$$

$$g_{m6} = \frac{160 \times 10^{-6}}{0.15}$$

$$g_{m6} \approx 1066.67\,\mu\text{S}$$

Approximating to a practical value:

$$g_{m6} \approx 1067\,\mu\text{S}$$

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Calculation of Resistor R: “‘latex

5.3.5 Calculating Resistor R

The resistor R is calculated using the formula:

$$R = \frac{1}{g_{m7}} \left(1 + \frac{C_L}{C_C}\right)$$

Given:

$$g_{m7} = g_{m6} = 1067\,\mu\text{S}, \quad C_L = 1\,\text{pF}, \quad C_C = 0.35\,\text{pF}$$

Substituting the values:

$$R = \frac{1}{1067 \times 10^{-6}} \left(1 + \frac{1 \times 10^{-12}}{0.35 \times 10^{-12}}\right)$$

$$R = \frac{1}{1067 \times 10^{-6}} (1 + 2.857)$$

$$R = \frac{1}{1067 \times 10^{-6}} \times 3.857$$

$$R \approx 937.5\,\Omega \times 3.857$$

$$R \approx 3615\,\Omega$$

Approximating to a practical value:

$$R \approx 3.6\,\text{k}\Omega$$

—

Updated Table: Here is the updated table with the new values for g_{m6} and R:

5.4 Summary of Calculated Parameters

As I designe two design but I have put outputs of second Design. and all final caluculations and W/L table is shown below,

MOSFET	**Parameter**	**Value**	I_D
M_1, M_2	g_{m1}	$200\,\mu$S	$10\,\mu$A
M_1, M_2	$(W/L)_1, (W/L)_2$	6	$10\,\mu$A
M_3, M_4	$(W/L)_3, (W/L)_4$	8	$10\,\mu$A
M_5	$(W/L)_5$	6	$20\,\mu$A
M_6	g_{m6}	$1067\,\mu$S	$80\,\mu$A
M_6	$(W/L)_6$	60	$80\,\mu$A
M_7	$(W/L)_7$	23.33	$80\,\mu$A
M_8	$(W/L)_8$	8	$40\,\mu$A
Resistor	R	$3.6\,\text{k}\Omega$	-

Table 2: Summary of Calculated Parameters for MOSFETs and Resistor

5.5 Summary of MOSFET Dimensions

The following table summarizes the (W/L) ratios, widths (W), and lengths (L) for each MOSFET in the design:

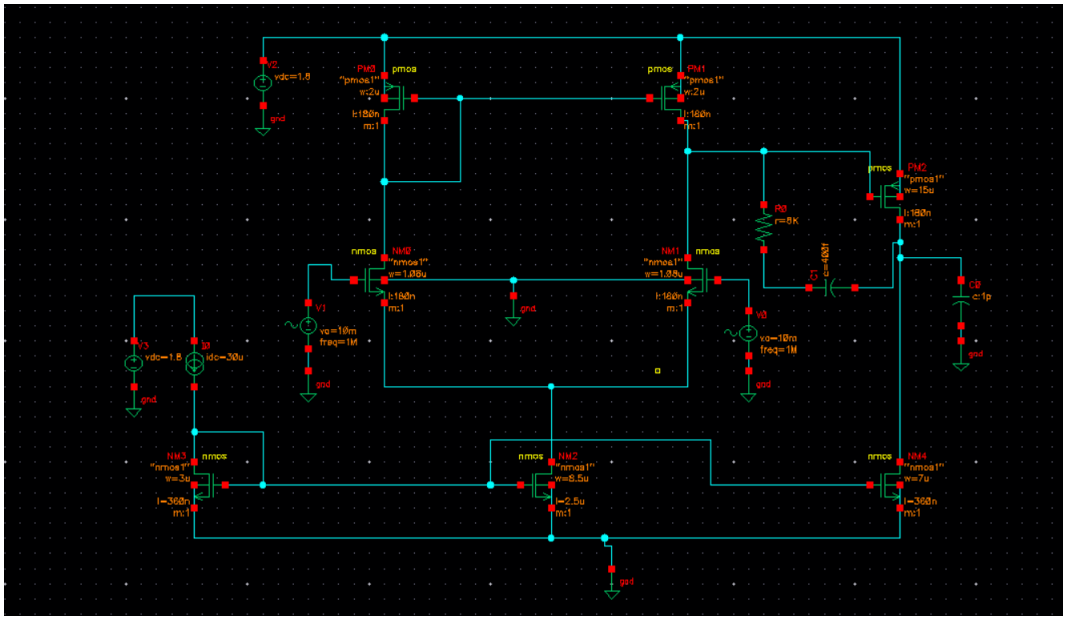
MOSFET	**W/L**	**W (Width)**	**L (Length)**
M_1, M_2	6	$1.08\,\mu$m	180 nm
M_3, M_4	8	$1.44\,\mu$m	180 nm
M_5	6	$8.4\,\mu$m	$2.5\,\mu$m
M_6	60	$11\,\mu$m	180 nm
M_7	23.33	$8.2\,\mu$m	360 nm
M_8	8	$2.88\,\mu$m	360 nm

Table 3: Summary of MOSFET Dimensions

TO get common mode gain -20dB I took length as 2.5um and made some changes for M6 ,M7 improve the swing(to drop good VDs in between without effecting the Gain much)

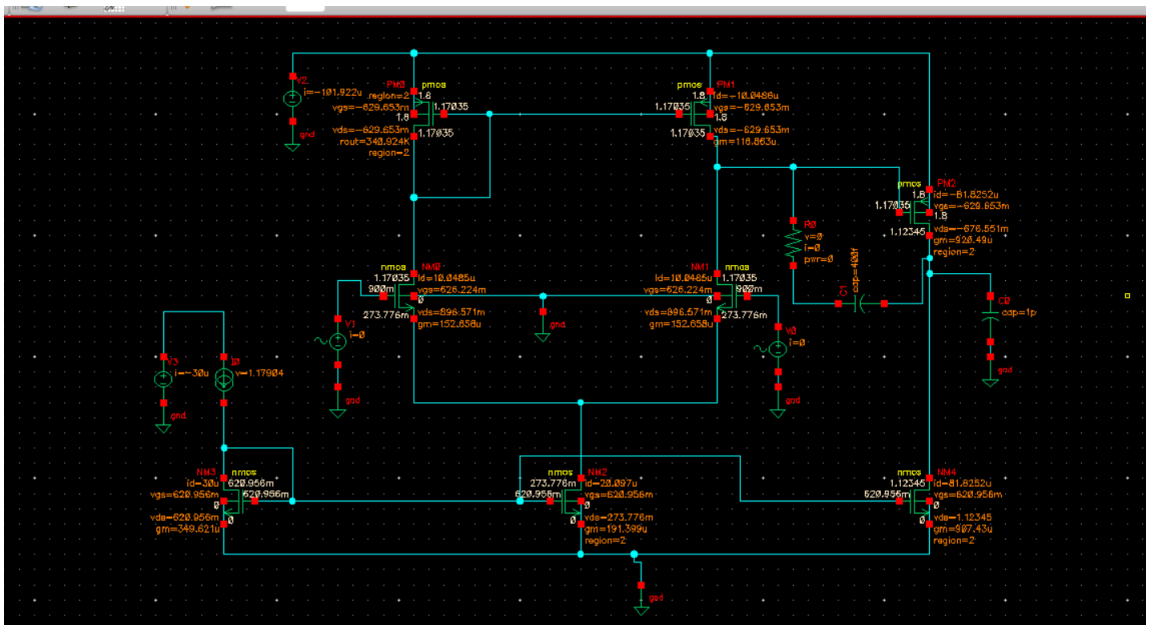
And We solved only for 1st order Vairables and I tunned the circuit based on needs, but not much and final circuit is shown below

5.6 Circuit

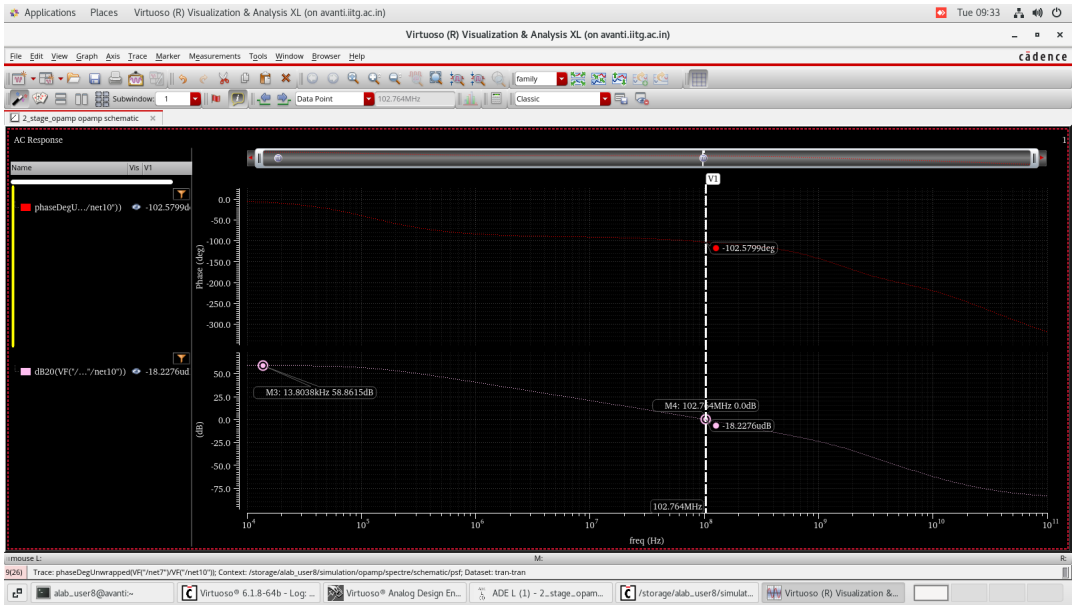


6 OUTPUT RESULTS

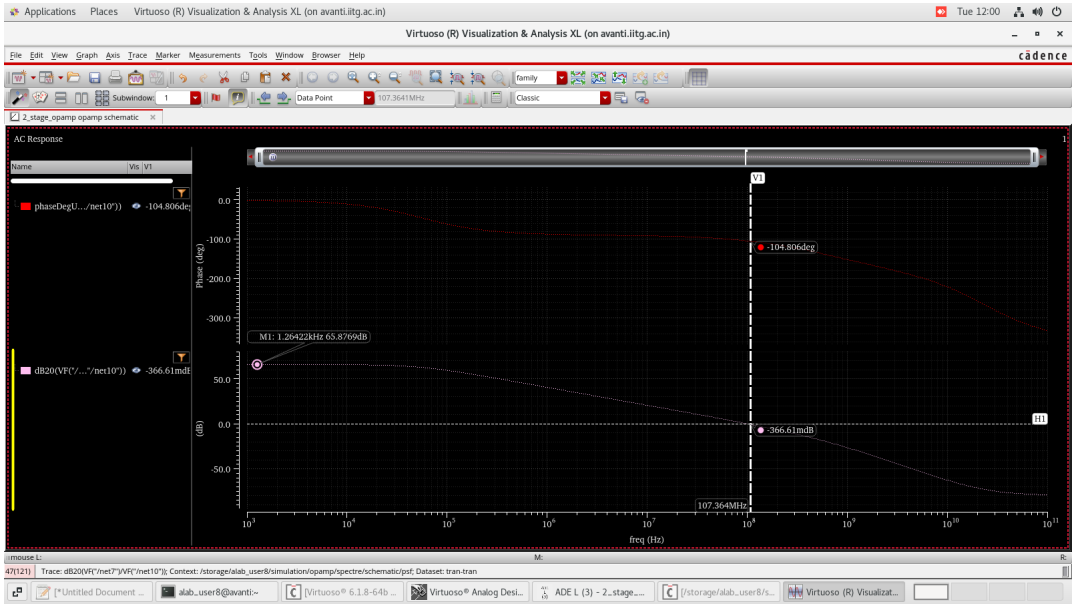
6.1 DC Operating Point



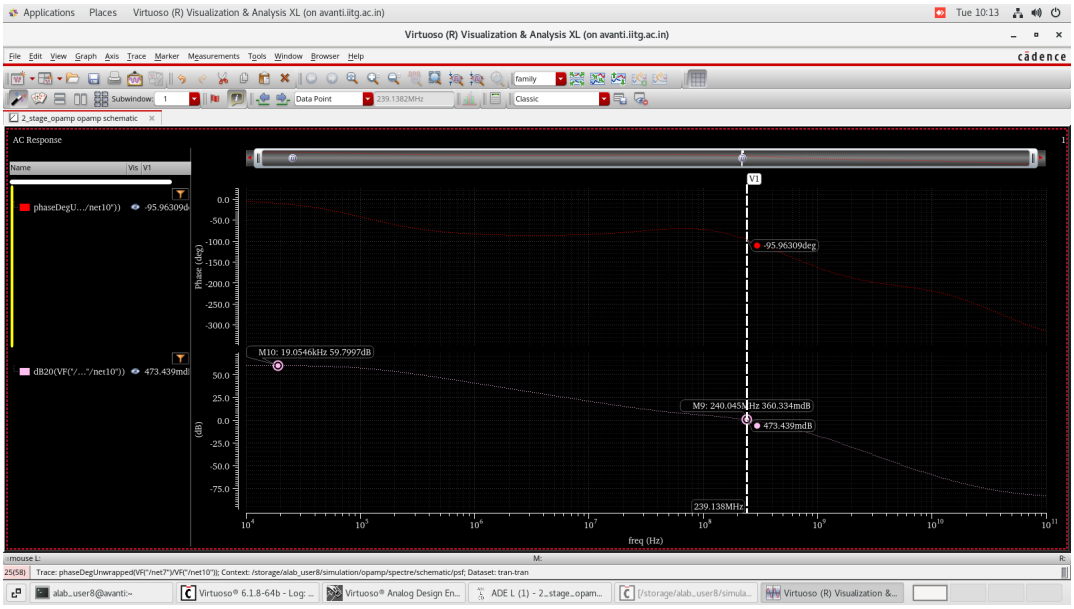
6.2 Gain for ICMR 1.2V



6.3 Gain for ICMR 0.850V

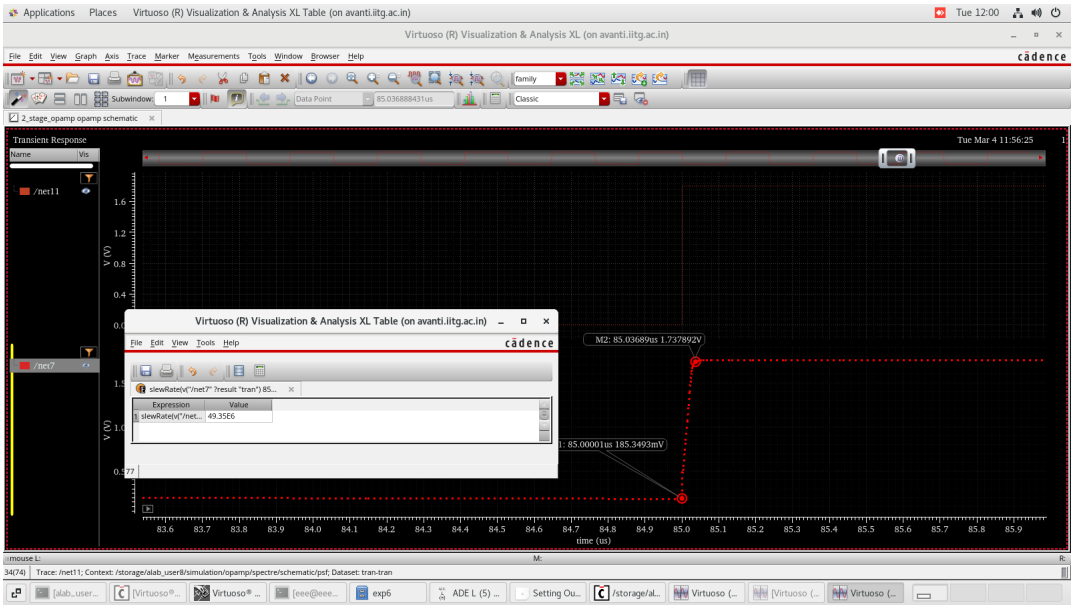


6.4 Gain for ICMR 1.1V

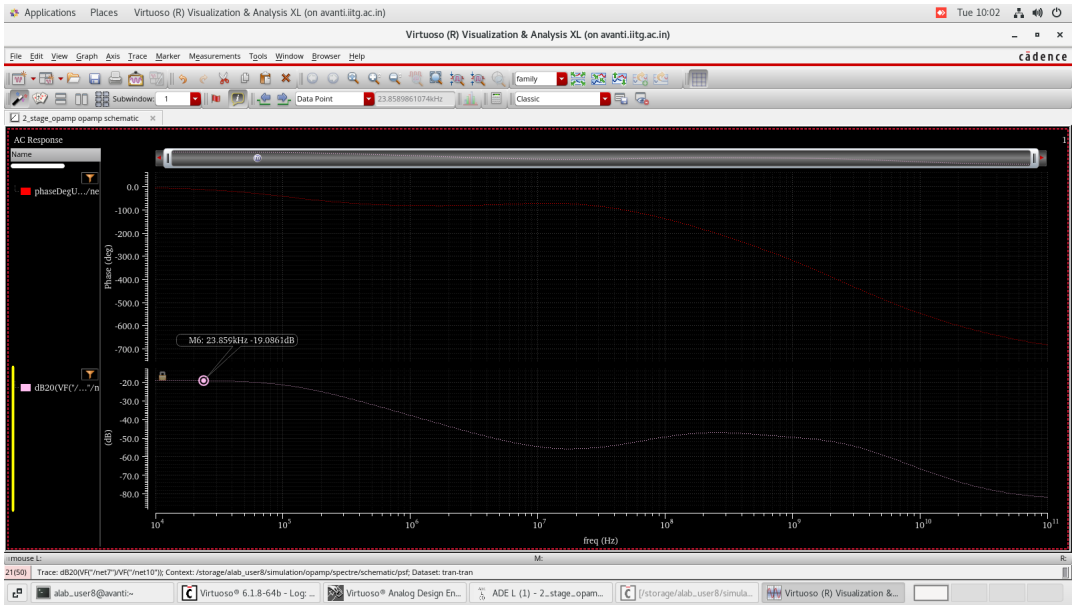


Here I have increased the resistance value to 8Kohms and bought the zero closer to Pole1, and I observed no change in Gain but Increase in Bandwidth but these cause increase in Area on IC, It will be like a Tradeoff between Area and BW

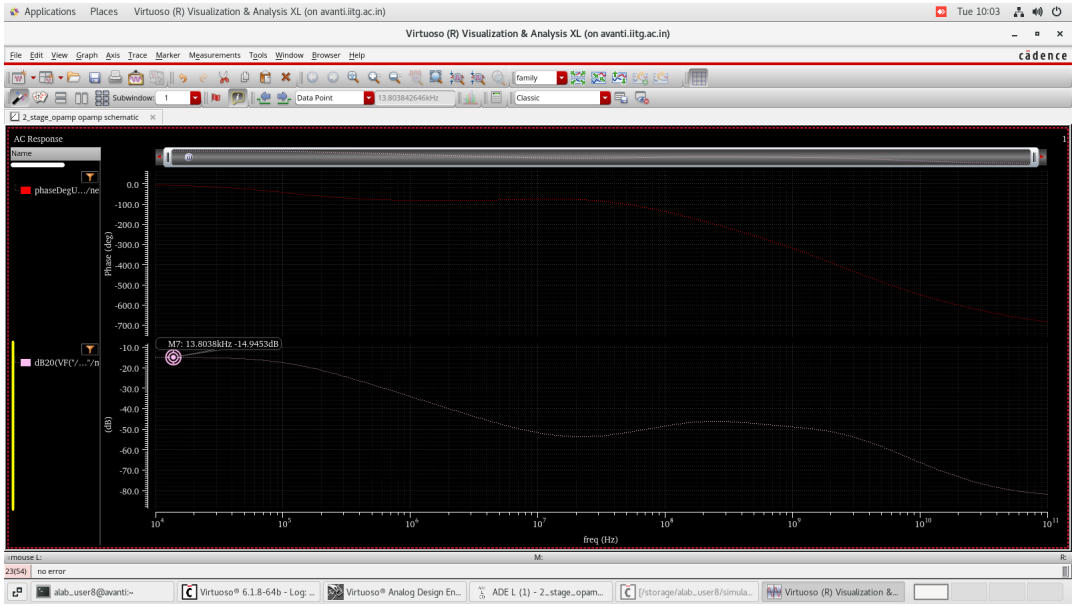
6.5 Slew Rate



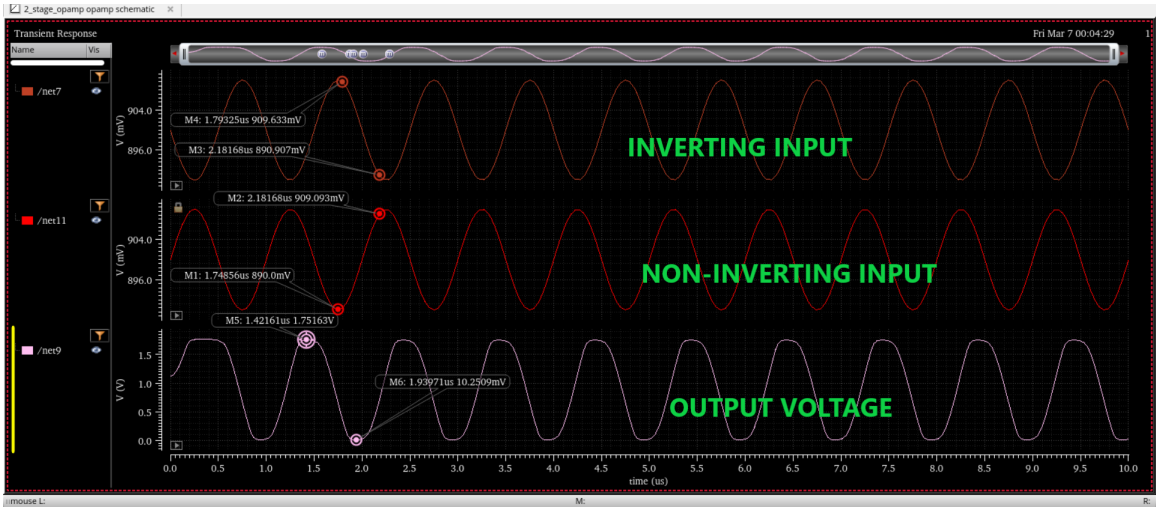
6.6 Common Mode Gain for ICMR 1.1V



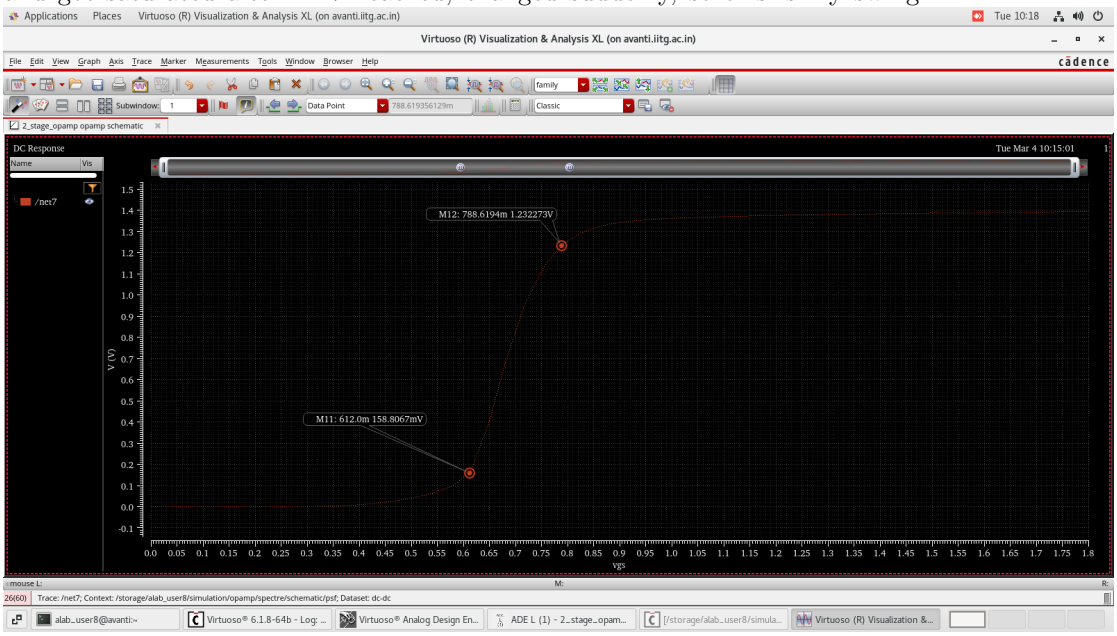
6.7 Common Mode Gain ICMR 0.850V



6.8 Output Swing



I calculated the swing by connecting to negative feedback and I observed the linearity in Output, i.e, till the output changes linearly with Input , it is the swing, once the Output changes sudden , then it act like a comparator, even in above picture, we can observe that my ouput almost hold the input and got saturated after 1.2V reached, changed suddenly, so this is my swing



6.9 Final Results

Parameter	ICMR	Theoretical	Practical
Gain	0.850 V (3 kΩ)	60 dB	65.8 dB
	1.1 V (8 kΩ)	60 dB	59.79 dB
	1.2 V (3 kΩ)	60 dB	58.8615 dB
Bandwidth (BW)	0.850 V (3 kΩ)	100 MHz	106 MHz
	1.1 V (8 kΩ)	100 MHz	240 MHz
	1.2 V (3 kΩ)	100 MHz	102 MHz
Margin	0.850 V (3 kΩ)	90°	74°
	1.1 V (8 kΩ)	90°	85°
	1.2 V (3 kΩ)	90°	76°
Common Mode Gain	1.1 V (3 kΩ)	−21 dB	−19.9 dB
	0.850 V (3 kΩ)	−21 dB	−15 dB
Slew Rate	-	57.14 V/μs	49.35 V/μs
Input Swing	0.950	0.6V to 0.8V to	612mV to 788.614mV
Output Swing	0.950	0.1 to 1.3V	0.158V to 1.23V

Table 4: Summary of Theoretical and Practical Parameters for Different ICMR Values

While calculating the Theoretical Phase Margin, for the ideal case, the zero will come such that 90° will be the phase margin.

When calculating the swing from the DC VDS the upper MOSFET's overdrive contributes to the positive swing, and the lower MOSFET's overdrive contributes to the negative swing.

7 Conclusion

The design of the two-stage operational amplifier has been successfully completed, and the following conclusions can be drawn:

- **Gain and Stages**: To achieve the required gain, a two-stage op-amp structure was used. The first stage provides gain with medium transconductance (g_m) and medium output resistance (r_{out}), while the second stage provides additional gain with high g_m and high current, resulting in lower r_{ds}.
- **Bandwidth and Phase Margin**: The first stage primarily determines the bandwidth of the op-amp, as indicated by the design formulas. A compensator capacitor (C_C) was used to ensure a phase margin of 60°.
- **Design Approaches**: The design was implemented in two ways:
  - **Without Resistor**: In this approach, high current, high (W/L), and high power consumption were required to achieve the desired phase margin.
  - **With Resistor**: By adding a 3 kΩ resistor, the required phase margin was achieved with lower current and smaller (W/L), reducing power consumption. However, placing a resistor in an integrated circuit (IC) is challenging due to layout and process limitations.
- **Effect of Resistor on Bandwidth**: Increasing the resistor value was observed to increase the bandwidth while maintaining a constant gain. This provides flexibility in tuning the op-amp's performance.
- **ICMR and Gain Variation**: The input common-mode range (ICMR) affects the gain of the op-amp, but the variation in gain across the ICMR is not significant. This ensures stable operation across a wide range of input voltages.
- **Power and Area Trade-offs**: The design with the resistor offers better power efficiency and smaller transistor sizes, but it introduces additional complexity in the IC layout. The resistor-less design, while simpler to implement, consumes more power and area.
- **Practical Considerations**: The choice between the two design approaches depends on the specific application requirements, such as power consumption, area constraints, and the feasibility of integrating resistors in the IC.

In conclusion, the two-stage op-amp design successfully meets the specified requirements, and the trade-offs between the two design approaches have been thoroughly analyzed. The use of a compensator capacitor and resistor provides flexibility in achieving the desired phase margin and bandwidth while optimizing power and area.