EE515: VLSI ARCHITECTURE COURSE PROJECT

Band Gap Refrence.



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EEE - VLSI & NANOELECTRONIC

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1 Theory of Bandgap Reference (BGR)

A Bandgap Reference (BGR) circuit is a fundamental building block in analog and mixed-signal integrated circuits, providing a precise DC reference voltage that is nearly independent of temperature, supply, and process variations. The reference voltage is designed to be stable around the silicon bandgap voltage at absolute zero ($\approx 1.205 \text{ V}$), but can be scaled to lower values (e.g., 0.5 V) for low-voltage CMOS technologies.

1.1 Basic Principle

The key concept behind a BGR is the combination of two voltages with opposite temperature coefficients (TCs):

- The base-emitter voltage of a bipolar transistor (V_{BE}) , which has a **negative TC** of approximately $-1.5 \text{ mV}/^{\circ}\text{C}$.
- A voltage proportional to absolute temperature (**PTAT**), generated from the difference between two V_{BE} values of bipolar devices operating at different current densities.

By adding a PTAT voltage to a CTAT (V_{BE}) voltage in proper proportion, the resulting output can be made nearly temperature-independent:

$$V_{\text{REF}} = V_{BE1} + k \cdot (V_{BE1} - V_{BE2})$$

where k is chosen so that the positive and negative TCs cancel.

In modern CMOS BGRs, instead of summing voltages directly, PTAT and CTAT **currents** are combined and passed through a resistor to obtain a stable reference voltage. This allows operation at lower supply voltages (e.g., sub-1V).

1.2 Core Circuit Operation

The basic BGR core consists of two bipolar junction transistors (BJTs) Q_1 and Q_2 with emitter area ratio n, biased by matched MOS transistors M_1 and M_2 under the control of an operational amplifier A_1 that enforces $V_X = V_Y$. The relation between their collector currents can be expressed as:

$$\Delta V_{BE} = V_T \ln(n) = I_{D1} R_1$$

where $V_T = \frac{kT}{q}$ is the thermal voltage. The resistor R_1 thus develops a PTAT voltage, and the currents through M_1 and M_2 become PTAT.

To generate a temperature-independent current, resistors R_2 and R_3 are connected from the transistor bases (nodes X and Y) to ground, producing:

$$|I_{D2}| = \frac{V_{BE1}}{R_3} + \frac{V_T \ln(n)}{R_1}$$

By choosing resistor ratios appropriately, the positive and negative TCs cancel, yielding a temperature-stable current. The reference voltage is then obtained by mirroring this current through another branch resistor R_L :

$$V_{\text{out}} = |I_{D2}|R_L$$

1.3 Low-Voltage Operation and Design Issues

In low-voltage designs (e.g., 0.95–1.2 V supply), headroom becomes critical since V_{BE} and MOS overdrive voltages consume most of the supply. Razavi's design overcomes this using:

- Regulated cascode structures to equalize drain voltages of current mirrors, minimizing errors due to channel-length modulation.
- A two-stage operational amplifier providing a high DC gain (> 300) to achieve ≥ 40 dB PSRR.
- A **start-up circuit** ensuring the BGR exits its zero-current metastable state at power-up.

The overall architecture combines precision, low temperature drift (< 5 mV from 0°C to 100°C), and low power (0.5 mA at 1.2 V).

2 Design Calculations and Component Selection

Based on the methodology described in Behzad Razavi's "The Design of a Low-Voltage Bandgap Reference", the following key parameters and calculations were used in the design:

2.1 Assumed Specifications

- Supply Voltage, $V_{DD} = 1 \text{ V}$
- Target Output Voltage, $V_{\text{out}} = 0.5 \text{ V}$
- Temperature Range: 0 °C to 100 °C
- Power Consumption < 1.5 mW
- $PSRR \ge 40 dB$

2.2 Resistor and Current Design

The emitter area ratio n=16 (i.e., $Q_1=4$ units and $Q_2=64$ units) was chosen to ensure manageable V_{BE} and op-amp offset sensitivity. The design equations are summarized as:

$$\Delta V_{BE} = V_T \ln(n)$$

$$I_{D1} = \frac{\Delta V_{BE}}{R_1}$$

$$I_{D2} = \frac{V_{BE}}{R_3} + \frac{V_T \ln(n)}{R_1}$$

$$V_{\text{out}} = I_{D2}R_L$$

For $T = 300 \text{ K } (V_T = 25.8 \text{ mV})$, we have:

$$\Delta V_{BE} = 25.8 \ln(16) = 71.6 \text{ mV}$$

Using $I_{D1} = I_{D2} = 35 \mu A$, the resistor values are selected as follows:

Table 1: Calculated Component Values for BGR Design

Component	Description	Calculated Value
R_1	PTAT resistor $(\Delta V_{BE}/I_{D1})$	$2.0~\mathrm{k}\Omega$
R_2	Base resistor from node X to ground	$13 \text{ k}\Omega$
R_3	Base resistor from node Y to ground	13 kΩ
R_L	Output resistor (V_{out}/I_{D2})	$5.5~\mathrm{k}\Omega$
I_{D1}, I_{D2}	Branch currents	$35 \mu A$
n	Emitter area ratio (Q_2/Q_1)	16
$(W/L)_{M1,M2}$	PMOS dimensions	$50 \ \mu \text{m} / 120 \ \text{nm}$
Op-Amp Gain (A_1)	Two-stage OTA	≥ 300
Supply Current	Total including OTA	0.5 mA

2.3 Expected Results

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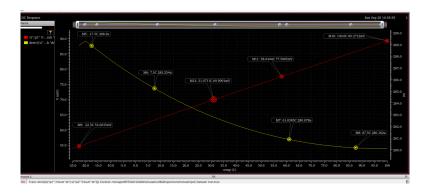


Figure 1: Generation of PTAT (Proportional To Absolute Temperature) voltage from the difference of two V_{BE} values with different current densities.

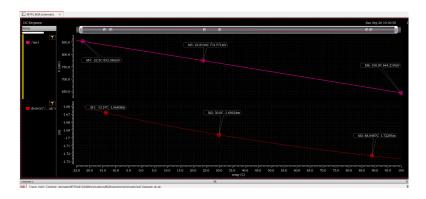


Figure 2: CTAT (Complementary To Absolute Temperature) behavior of base-emitter voltage (V_{BE}) with temperature.

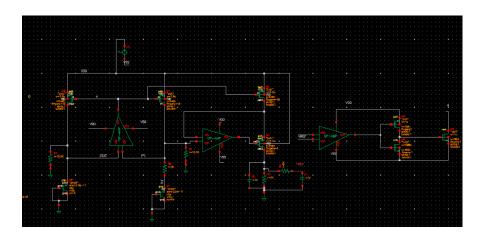


Figure 3: Complete Bandgap Reference (BGR) circuit showing PTAT and CTAT current summation, operational amplifier (A_1) , and output resistor R_L .

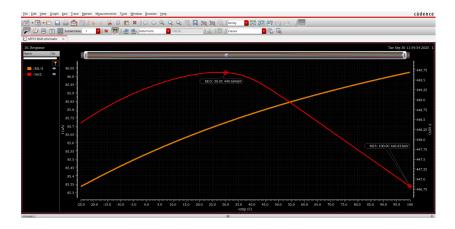


Figure 4: Simulated output reference voltage ($V_{\rm REF}$) versus temperature showing excellent temperature stability across -40°C–100°C.

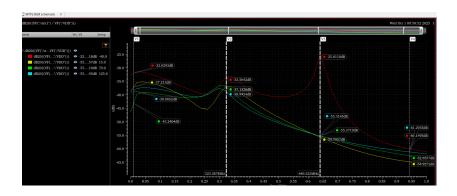


Figure 5: Power Supply Rejection Ratio (PSRR) response of the designed Bandgap Reference circuit. The circuit achieves better than 28 dB PSRR at low frequencies.