SPONSORSHIP CERTIFICATE

Certified that Mr/Ms/Dr/Prof……. is an employee of our institute and is hereby sponsored for the FDP on "Advanced VLSI Design Techniques" at GNDEC, Ludhiana during the period from 14th October to 25th October, 2013. He/ She will be permitted to attend the same, if selected.

It is also certified that our institute is an AICTE approved institute.

Name &Signature of sponsoring authority
(With Seal)

IMPORTANT INFORMATION

Selection will be on first come first serve basis as well as AICTE guidelines. *No Registration fee shall be charged.* For further details and updates visit www.gndec.ac.in.

ADDRESS FOR CORRESPONDENCE:

Dr. Sandeep Singh Gill

Professor (ECE) & Dean (Administration)

Guru Nanak Dev Engineering College

Ludhiana, Punjab-141006

Mobile: 09814801718

Phone: 0161-5064504(O)

GENERAL INFORMATION

Guru Nanak Dev Engineering College, Ludhiana, established in 1956, is one of the oldest and a premier Engineering Institution of India offering 7 UG and 15 PG courses besides being a QIP centre for Ph.D. The sprawling campus is spread over 88 acres of pristine land on Ludhiana-Malerkotla state highway within the city.

Electronics & Communication Engineering Department was established in 1981 and is currently offering B.Tech (ECE), M.Tech (ECE), M.Tech (VLSID) Part Time, and Ph.D. courses.

Ludhiana city is a well known Industrial hub in Northern India and is well connected by air, rail and road. The beautiful campus is about 10 km from the airport, 7 km from railway station and 6 km from interstate bus terminal. The weather is pleasant (20°C to 25°C) in the month of October.

TRAVEL and ACCOMODATION

Outstation participants from AICTE approved institutes will be given TA as per AICTE norms.

Boarding and Lodging shall be provided to the participants in college hostels on prior request free of cost. Hotel/ Guest house accommodation can be arranged on payment basis.

AICTE Sponsored

Two Weeks
Faculty Development Programme
On

ADVANCED VLSI DESIGN TECHNIQUES

(14th October - 25th October, 2013)

Coordinator

Dr. Sandeep Singh Gill

Organized by
Department of Electronics & Communication Engineering

GURU NANAK DEV ENGINEERING COLLEGE
An autonomous college under UGC Act-1956

Ludhiana, Punjab - 141006

INTRODUCTION

This FDP is a platform for discussion on recent trends in VLSI Design. It aims at encouraging research in the field by exposing the faculty from across the nation to experts in the field and by sharing their experience and ideas with peer group. It also focuses on the fundamentals of VLSI Design Methodology and testing and extensive lab work.

COURSE CONTENTS

- VLSI Design Basics
- Nano Devices
- Analog VLSI Design
- Digital VLSI Design
- RF VLSI Design
- Mixed Signal VLSI Design
- VLSI for Signal Processing
- Bioinspired VLSI System
- ASIC and SoC Design
- VLSI Testing and Testability
- Exposure to Cadence Tools
- Lab Work

PEDAGOGY

The pedagogy consists of lectures, interactive sessions, laboratory sessions and discussion.

RESOURCE PERSONS

Experts from IITs, NITs and other renowned academic institutions besides in house faculty will deliver expert talks.

ELIGIBILITY CRITERIA

Sponsored faculty of AICTE approved Engineering colleges in Electronics & its specializations, Electrical, Computer Science and Information Technology as well as all engineering professionals working in private, public, government organizations or industry are eligible to apply for participation.

HOW TO APPLY

Application in the specified format duly recommended/ sponsored by the competent authority should reach the coordinator on or before 4th October, 2013. Advance copy of registration form may be mailed to fdp_ece@gndec.ac.in.

REGISTRATION FORM

Name: ……

Father's Name: ……..…....

Date of Birth: …….....

Academic Qualification:……

Designation:…….

Experience (years) : ……

Mailing Address :……..

.....

Mobile No……..……..

E-Mail: ……..……....

Accommodation required: Yes/No

If yes Hostel:

Hotel/ Guest House:

Date: Signature of Applicant