SPONSORSHIP CERTIFICATE

Certified that Mr/MS/Dr/Prof…… is an employee of our institute and is hereby sponsored for the FDP on "Advanced VLSI Design Techniques" at GNDEC, Ludhiana during the period from 20th January, 2014 to 31st January, 2014. She/he will be permitted to attend the same, if selected.

It is also certified that our institute is an approved institute of AICTE.

Date:

Place: Name &Signature
(Director/Principal)

(Seal of the Institute)

IMPORTANT INFORMATION

Selection will be on first come first serve basis subjected to AICTE norms.

Last date for receipt of application: 17-01-2014

WEBSITE: www.gndec.ac.in
EMAIL : fdp_ece@gndec.ac.in

ADDRESS FOR CORRESPONDENCE:
Dr. Sandeep Singh Gill
ECE Deptt., GNDEC, Ludhiana
Mobile: +91-9814801718
Phone: 0161-5064504(O)

GENERAL INFORMATION

Guru Nanak Dev Engineering College, Ludhiana is the oldest and a premier Engineering Institution of India. The institute is setup on 88 acres of sprawling pristine land on Ludhiana-Malerkotla state highway. Ludhiana city is a well known Industrial hub in Northern India and is well connected by direct rail service with all parts of India. The beautiful campus is about 7 kms away from railway station (Auto rickshaw service available @ Rs.10/- per passenger) and around 6 km from main bus stand. The weather in the month of January in Ludhiana is cool (5°C to 15°C).

TRAVEL and ACCOMODATION

Outstation participants from AICTE approved institutes will be given TA/DA as per AICTE norms.

Lodging and boarding of selected participants will be provided in college hostels on prior request.

REGISTRATION FEES

No Registration fees.

AICTE Sponsored

Two Weeks
Faculty Development Programme
On

ADVANCED VLSI DESIGN TECHNIQUES

(20th January - 31st January, 2014)

Co-ordinator

Dr. Sandeep Singh Gill

Organized by
Department of Electronics & Communication Engineering
GURU NANAK DEV ENGINEERING COLLEGE
Ludhiana, Punjab - 141006

INTRODUCTION

This FDP is a platform for discussion on recent trends in VLSI Design in the field of Electronics and Communication Engineering. It aims to encourage the potential engineering brains across the nation by sharing their experience and innovative ideas towards technical excellence. This FDP focuses on the fundamentals of VLSI Design Methodology and testing to present how the design concepts can be applied to analyze the performance of VLSI circuits.

COURSE CONTENTS

- VLSI Design Basics
- Nano Devices
- Analog VLSI Design
- Digital VLSI Design
- RF VLSI Design
- Mixed Signal VLSI Design
- VLSI for Signal Processing
- Bioinspired VLSI System
- ASIC and SoC Design
- VLSI Testing and Testability
- Exposure to Cadence Tools
- Lab Work

PEDAGOGY

The pedagogy consists of lectures, interactive sessions, laboratory practices and discussions.

RESOURCE PERSONS

Experts from IITs, NITs and other renowned academic Institutions besides faculty from our institute will deliver expert talks.

ELIGIBILITY CRITERIA

Sponsored faculty of AICTE recognized engineering colleges, all engineering professionals working in private, public, government organization or industries are eligible to apply for participation.

HOW TO APPLY

Application in the attached format duly Recommended/sponsored by the authority concerned should reach the co-ordinator on or before 17th January, 2014.

REGISTRATION FORM

Name: ……

Father's Name: ……..…....

Date of Birth: …….....

Academic Qualification:……

Designation:…….

Address of Sponsoring Authority:……

……..……

Experience (years) : ……

Mailing Address :……..

.....

Mobile No……..……

E-Mail : ……..……....

Accommodation required : Yes/No

Date: Signature of Applicant