

# Sahaj Singh

sahajs.com | sahaj\_singh@sfu.ca | [LinkedIn](#) | [GitHub](#)

## TECHNICAL SKILLS

---

**Programming Languages:** C, C++, Python, MATLAB, Java, Assembly, HTML5/CSS3, Javascript

**Tools & Technologies:** Git VC, Visual Studio Code, PyCharm, macOS, Linux, Windows, Android

## WORK EXPERIENCE

---

### **MATLAB — SFU Student Ambassador**

**Oct 2022 — Present**

*MathWorks* (Burnaby, BC)

- Organizing and hosting numerous programming and simulation based events revolving around MATLAB and Simulink.
- Helping in the process of creating meaningful relationships between MATLAB and professors/students at SFU. Providing support for students with questions related to MATLAB and Simulink.

### **Software/Firmware Developer**

**Jan 2022 — April 2022**

*picoTera Electronics Inc.* (Richmond, BC)

- Developed advanced firmware in C/C++ for PSoC6 and ARM Cortex-M4, M0 platforms and ported the project from PSoC creator to ModusToolbox 2.4 for better compatibility.
- Constructed a unique audio dataset for a Recurrent Neural Network (RNN) model, significantly improving its noise reduction capabilities in denoising applications.
- Implemented Static Gain replacing dynamic gain, optimizing post-processing audio quality, and boosting denoising performance.
- Authored custom cmake scripts for CMSIS libraries creation, reducing memory usage in complex operations and enabled Bluetooth Low Energy (BLE) integration between PSoC6 and an Android app, facilitating real-time data transmission.

## PROJECTS

---

### **Multi-threaded Memory Allocator:** *C, Make*

**Spring 2023**

- Developed a multi-threaded memory allocator in C, supporting First Fit, Best Fit, and Worst Fit allocation algorithms.
- Implemented features such as allocator initialization, allocation/deallocation interfaces, metadata management, compaction support, statistics reporting, multi-threading support, and uninitialization.
- Designed test cases and provided usage instructions to ensure the proper functionality and efficiency.

### **FPGA UART Protocol Implementation:** *VHDL, Modelsim, Altera DE2*

**Spring 2023**

- Developed a UART protocol for the Altera DE2 FPGA, featuring baud rate generation, data framing, error detection and correction, and handshaking subsystems.
- Implemented in VHDL with comprehensive testbenches to verify the functionality of both the transmitter and receiver modules.
- Enabled synchronous data transmission between UART devices and allowed for seamless operation via onboard switches and keys for data input, baud rate selection, and module reset.

### **Drone Controller and System:** *Embedded C, Arduino (C++), Beaglebone*

**Fall 2022**

- Designed a wireless drone system using a BeagleBone Green and Arduino Nano 33 IOT drone.
- Developed multiple control modes, integrated LCD display, and implemented an ultrasonic sensor for gesture-based height control.
- Wrote a custom driver for efficient BLE communication between the controller and drone.
- Incorporated a watchdog and systemd script for automated restarts to handle any unexpected system crashes.

### **FASTrack - Reaction Time Game:** *Assembly, Embedded C, Zedboard*

**Summer 2022**

- Developed a reaction time-based game called FASTrack for the Xilinx ZedBoard, utilizing the ARM7 assembly instruction set.
- Implemented various game features such as multiple speed modes and user controls through switches. Utilized OLED display and LEDs for visual feedback.
- Demonstrated key concepts including timer interrupts, masking, OLED display usage, and Finite State Machines (FSMs).

## EDUCATION

---

**Burnaby, BC**

**Sep 2020 — Sep 2025**

*Simon Fraser University* (B.A.Sc. Computer Engineering — Honours)

## AWARDS

---

### **Innovation Award/ESSS Award: 2022**

SFU — Engineering Science Student Society

Honors contributions to the student society and Recognized for outstanding creativity, originality, and impact via my projects driving advancements in technology.