Sahaj Singh

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Education

Simon Fraser University — Burnaby, BC
B.A.Sc. Computer Engineering Honours *GPA: 3.1/4.33* — Sep 2020 - Sep 2025

Work Experience

MathWorks — Burnaby, BC
MATLAB - SFU Student Ambassador — Oct 2022 - Present

- Organizing and hosting numerous programming and simulation based events revolving around MATLAB and Simulink.
- Helping in the process of creating meaningful relationships between MATLAB and professors/students at SFU. Providing support for students with questions related to MATLAB and Simulink.

picoTera Electronics Inc. — Richmond, BC
Software/Firmware Developer — Jan 2022 - April 2022

- Developed advanced firmware features in C for communication devices operating on PSoC6 embedded platforms. Designed and implemented custom feature sets to enhance device functionality and user experience.
- Constructed tailored datasets to facilitate the training and optimization of Recurrent Neural Network (RNN) models for effective noise reduction in smart denoising applications.

Skills

Programming Languages:	C, C++, Python, MATLAB, Java, ARM Assembly, HTML5/CSS3, Javascript
Tools & Technologies:	Git VC, Visual Studio Code, PyCharm, macOS, Linux, Windows

Projects

Multi-threaded Memory Allocator *C, Make*
https://github.com/SatireSage/Multi-threaded-Memory-Allocator
Developed a multi-threaded memory allocator in C, supporting First Fit, Best Fit, and Worst Fit allocation algorithms. Implemented features such as allocator initialization, allocation/deallocation interfaces, metadata management, compaction support, statistics reporting, multi-threading support, and uninitialization. Designed test cases and provided usage instructions to ensure the allocator's functionality and efficiency.

FPGA UART Protocol Implementation *VHDL, Modelsim, Altera DE2-115*
https://github.com/SatireSage/FPGA-UART-Protocol
Developed a UART protocol for the Altera DE2-115 FPGA, featuring baud rate generation, data framing, error detection and correction, and handshaking subsystems. The project was implemented in VHDL and included comprehensive testbenches to verify the functionality of both the transmitter and receiver modules. The system enables synchronous data transmission between UART devices and allows for seamless operation via onboard switches and keys for data input, baud rate selection, and module reset.

Dronee Controller and Drone System *Embedded C, Arduino (C++), Beaglebone*
https://github.com/SatireSage/Dronee
As team and firmware lead, designed a wireless drone system using a BeagleBone Green controller and Arduino Nano 33 IOT drone. Developed multiple control modes, integrated LCD display, and implemented an ultrasonic sensor for gesture-based height control. Wrote a custom driver for efficient BLE communication between the controller and drone. Incorporated a watchdog and systemd for automated restarts, and supervised the 3D printing of the drone frame.

FASTrack - Reaction Time Game *Assembly, Embedded C, Zedboard*
https://github.com/SatireSage/FASTrack
Developed a reaction time-based game called FASTrack for the Xilinx ZedBoard, utilizing the ARM7 assembly instruction set. The game challenges users to stop their moving arrow at a randomly generated endpoint on the OLED display. Implemented various game features such as multiple speed modes and user controls through switches, as well as the OLED display and LEDs for visual feedback. Key concepts demonstrated in this project include timer interrupts, masking, OLED display usage, and Finite State Machines (FSMs).

Awards

ESSS Award and Innovation Award - 2022 — SFU Engineering Science Student Society
Honors contributions to the student society and Recognized for outstanding creativity, originality, and impact via my projects driving advancements in technology.