Sahaj Singh

Surrey, BC · sahaj_singh@sfu.ca · sahajs.com

Education

Simon Fraser University — Burnaby, BC
B.A.Sc. Computer Engineering Honours *GPA: 3.1/4.33* — Sep 2020 - Sep 2025

Skills

Programming Languages:	C, C++, Python, MATLAB, Java, ARM Assembly, HTML5/CSS3, Javascript
Tools & Technologies:	Git VC, Visual Studio Code, PyCharm, macOS, Linux, Windows

Work Experience

MathWorks — Burnaby, BC
MATLAB - SFU Student Ambassador — Oct 2022 - Present

- Organizing and hosting numerous programming and simulation based events revolving around MATLAB and Simulink.
- Helping in the process of creating meaningful relationships between MATLAB and professors/students at SFU. Providing support for students with questions related to MATLAB and Simulink.

picoTera Electronics Inc. — Richmond, BC
Software/Firmware Developer — Jan 2022 - April 2022

- Developed advanced firmware features in C for communication devices operating on PSoC6 embedded platforms. Designed and implemented custom feature sets to enhance device functionality and user experience.
- Constructed tailored datasets to facilitate the training and optimization of Recurrent Neural Network (RNN) models for effective noise reduction in smart denoising applications.

Projects

Multi-threaded Memory Allocator *C, Make*

- Developed a multi-threaded memory allocator in C, supporting First Fit, Best Fit, and Worst Fit allocation algorithms.
- Implemented features such as allocator initialization, allocation/deallocation interfaces, metadata management, compaction support, statistics reporting, multi-threading support, and uninitialization.
- Designed test cases and provided usage instructions to ensure the allocator's functionality and efficiency.

FPGA UART Protocol Implementation *VHDL, Modelsim, Altera DE2-115*

- Developed a UART protocol for the Altera DE2-115 FPGA, featuring baud rate generation, data framing, error detection and correction, and handshaking subsystems.
- Implemented in VHDL with comprehensive testbenches to verify the functionality of both the transmitter and receiver modules.
- Enabled synchronous data transmission between UART devices and allowed for seamless operation via onboard switches and keys for data input, baud rate selection, and module reset.

Drone Controller and System *VHDL, Modelsim, Altera DE2-115*

- Designed a wireless drone system using a BeagleBone Green controller and Arduino Nano 33 IOT drone.
- Developed multiple control modes, integrated LCD display, and implemented an ultrasonic sensor for gesture-based height control.
- Wrote a custom driver for efficient BLE communication between the controller and drone.
- Incorporated a watchdog and systemd script for automated restarts to handle any unexpected system crashes.

FASTrack - Reaction Time Game *VHDL, Modelsim, Altera DE2-115*

- Developed a reaction time-based game called FASTrack for the Xilinx ZedBoard, utilizing the ARM7 assembly instruction set.
- Implemented various game features such as multiple speed modes and user controls through switches. Utilized OLED display and LEDs for visual feedback.
- Demonstrated key concepts including timer interrupts, masking, OLED display usage, and Finite State Machines (FSMs).

Awards

ESSS Award and **Innovation Award - 2022** — SFU - Engineering Science Student Society
Honors contributions to the student society and Recognized for outstanding creativity, originality, and impact via my projects driving advancements in technology.