

Diagnosis

- Introduction
- Logic Diagnosis
- Scan Chain Diagnosis
- Failure Analysis *(not in exam)
- Conclusions



Physical Failure Analysis, PFA

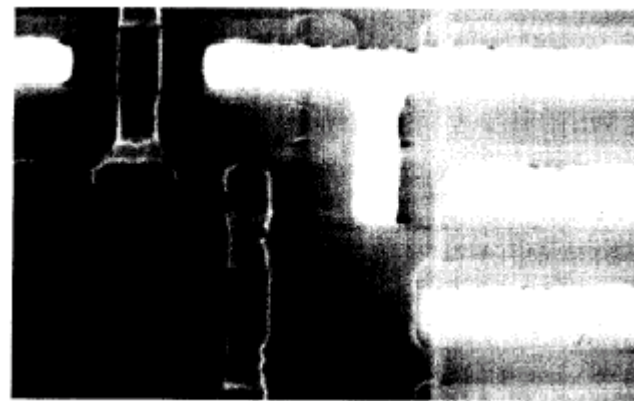
- What is PFA
 - ◆ Open chip package, locate and examine failure mode of defect
 - ◆ Aka.
 - * *Failure Analysis (FA)*
- Why PFA
 - ◆ Verify diagnosis results
 - ◆ Improve fab/test/design
 - * Improve yield
 - ◆ Improve design or test techniques

Failure Analysis

- Examine failure mode of defects
 - ◆ Failure mechanism can be inferred
- Usually requires lots of experience and equipments
- Example FA pictures [Soden 89]
 - ◆ Scanning Electron Microscope picture (Voltage Contrast)
 - ◆ Failure mechanism: photoresist failed to adhere
 - ◆ Failure mode: open circuit



good



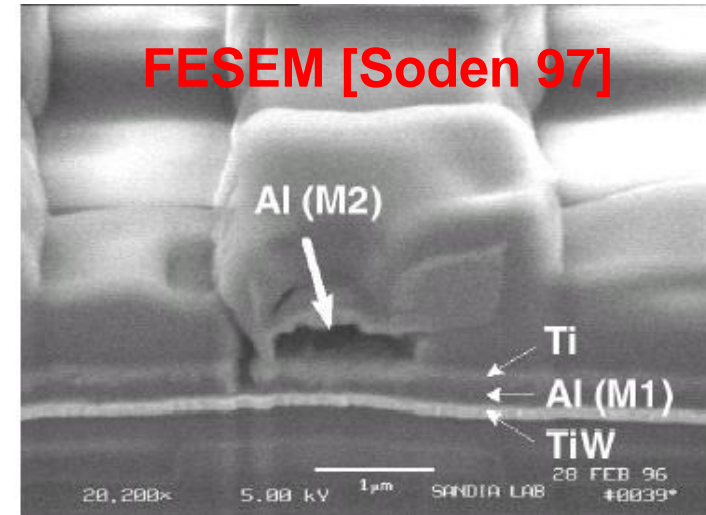
defective

FA Techniques

- **Imaging without power**
- **Imaging with power**
- **Physical process**
 - ◆ **Etching, cross sectioning**
- **See more details [Soden D&T 97]**

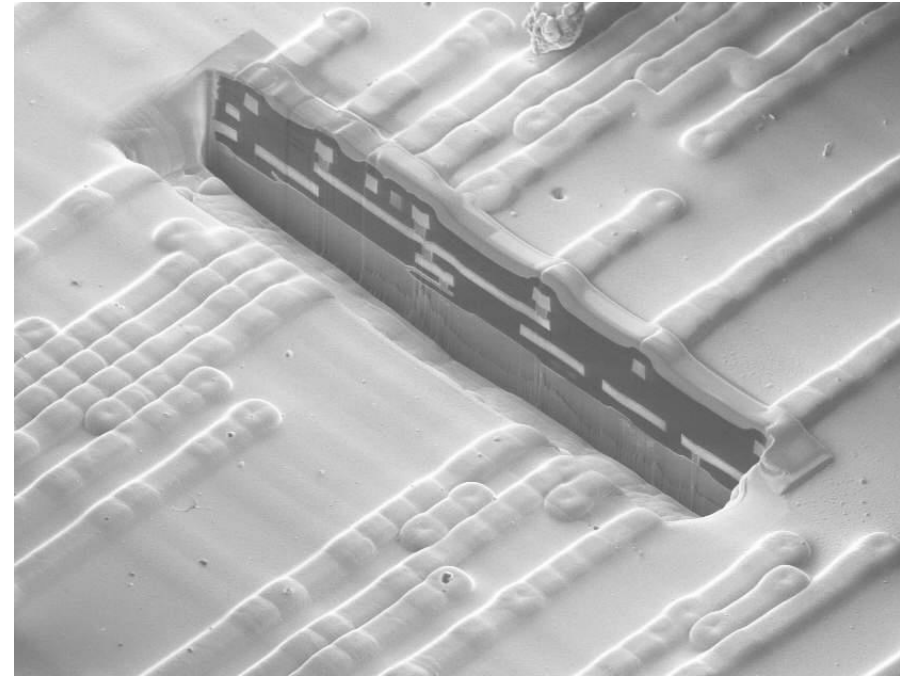
Imaging Techniques (no power)

- Optical microscope (Resolution limit :0.2 to 0.3 μm)
 - ◆ One useful technique: Scanning Optical Microscope (SOM)
 - * focus infrared laser spot scanning over sample
 - + Silicon transparent to infrared
 - Resolution limit: 1 μm
- Scanning Electron Microscope (SEM)
 - ◆ Field emission Scanning Electron Microscope (FESEM)
 - * Resolution limit: 2 to 5 nm
 - ◆ Transmission Electron Microscope (TEM)
 - * Resolution: sub nm
- Scanning probe microscope (SPM)
 - ◆ Sharp probe tip scans sample surface
- Focus Ion Beam (FIB)



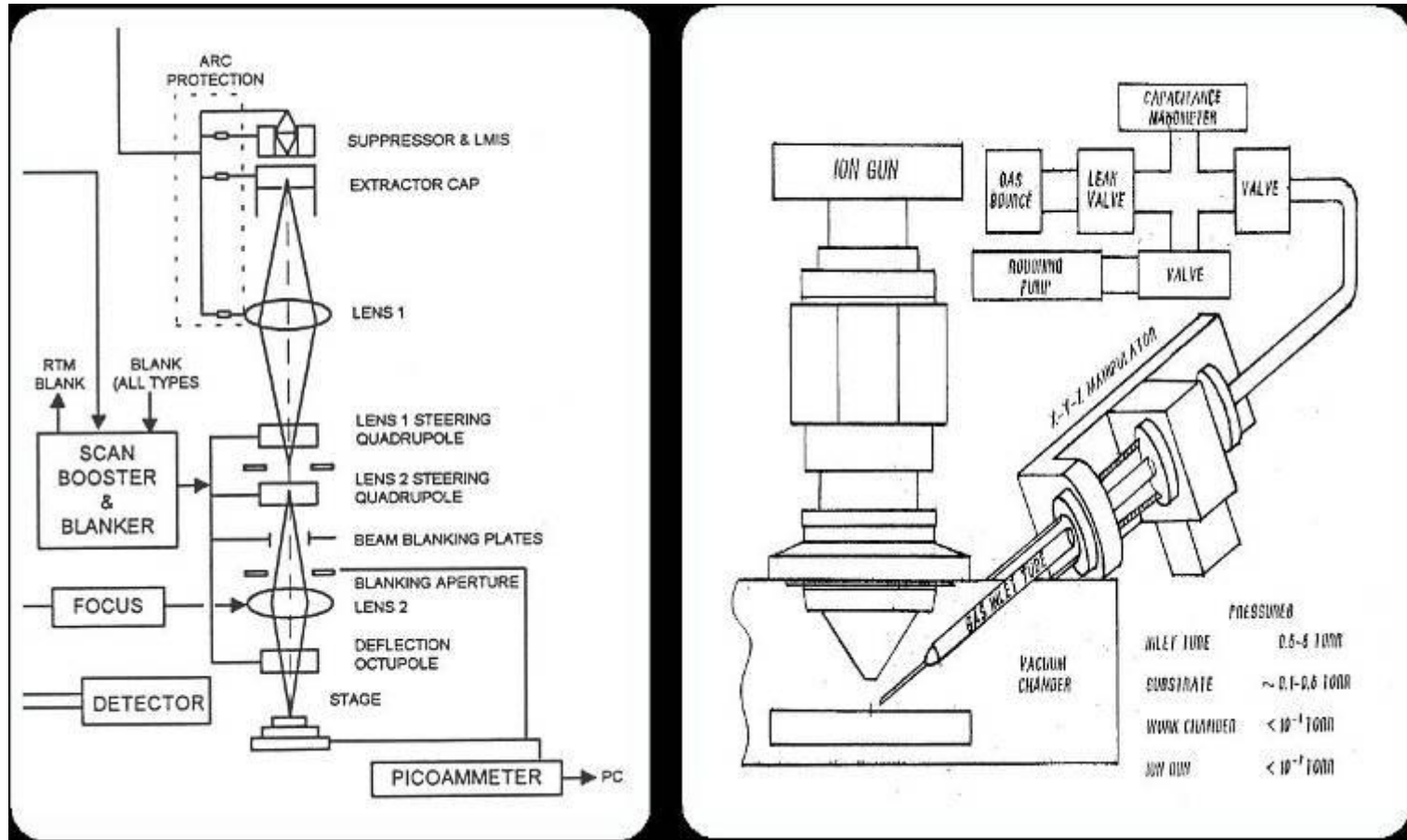
Focus Ion Beam (FIB)

- Focused beam of Ga^+ ion
- Multiple usages
 - ◆ Image
 - ◆ Circuit editing (down to 45 nm),
 - ◆ FA cross-sectioning (wider than 200 μm) with e-beam imaging and ion channeling contrast
 - ◆ Ion Channeling Contrast for grain imaging of crystalline materials
 - ◆ Passive Voltage Contrast for FA
 - ◆ Micro-machining for MEMS
 - ◆ TEM sample preparation, both cross-sectional and plan-view (min. size 18 nm)
 - ◆ Ion implantation (Ga^+)



[image courtesy of SK Lu from FJU]

FIB system

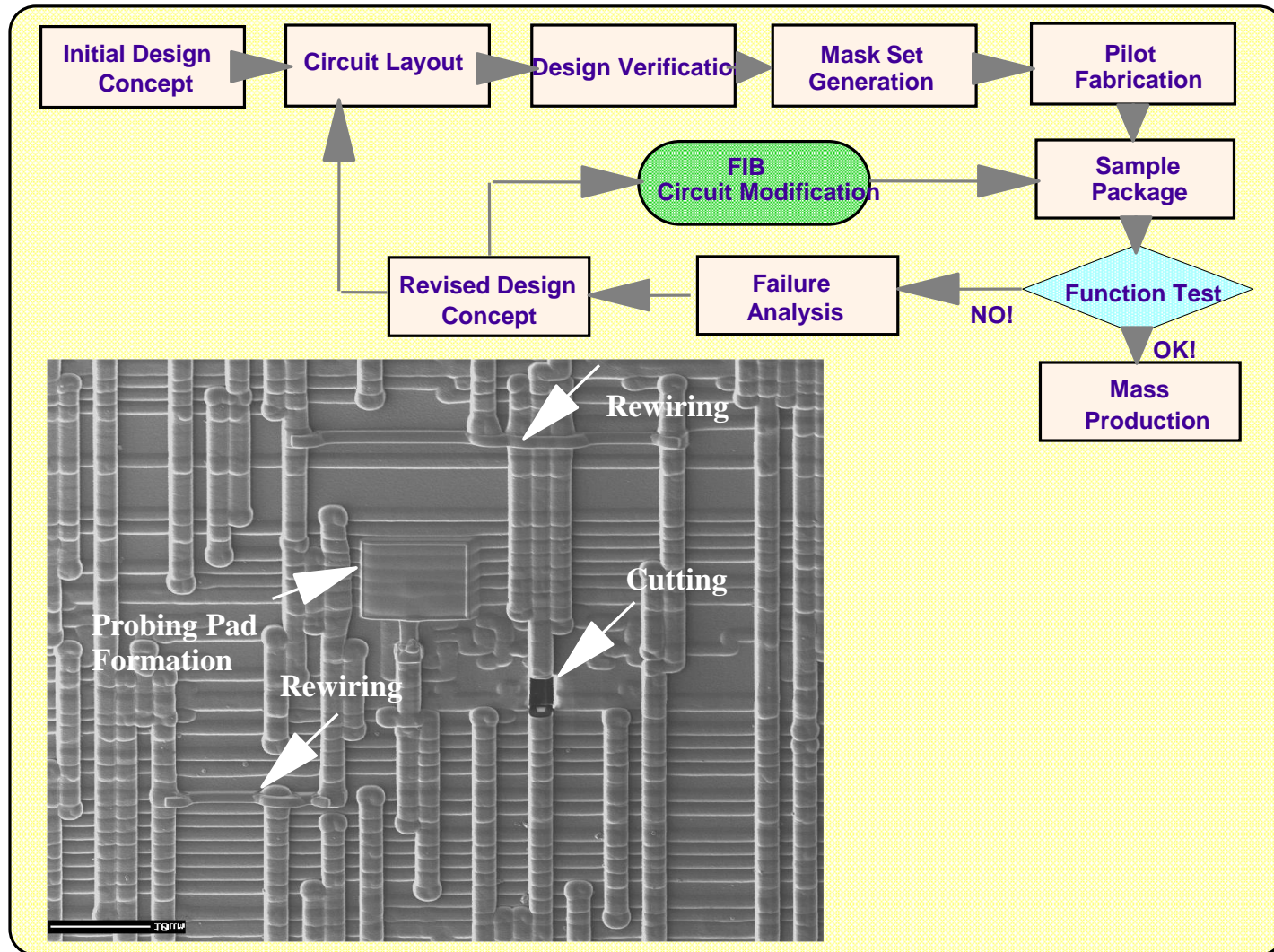


FIB photo

- Source : MA TEK



FIB Circuit Editing



Imaging Techniques (powered)

- Light emission (aka photo emission microscope)
 - ◆ Apply test patterns, capture light by camera
 - ◆ Very commonly used
 - + Feature size independent
 - + Infrared light enable analysis form die backside

Light emission microscopy [Soden 97]

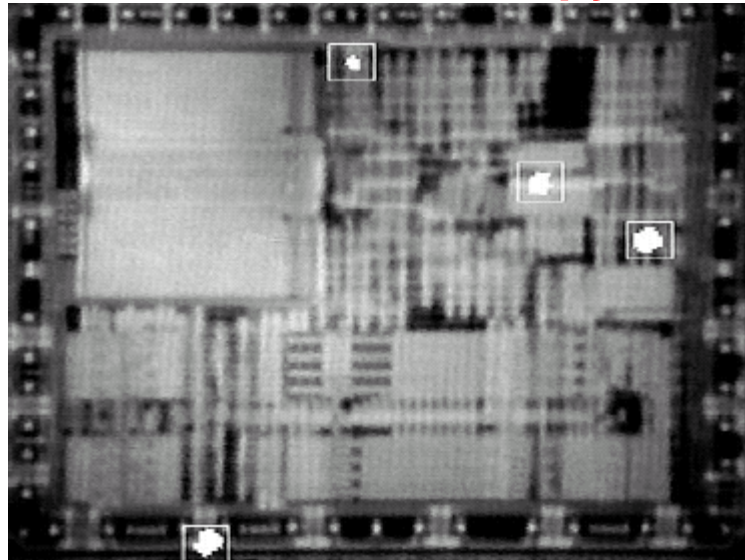


Figure 2. Low-magnification light emission microscopy image of a 32-bit microprocessor with four gate oxide shorts (bright areas in the four boxes).

Imaging Techniques (powered)

- Voltage Contrast (VC) and Electron Beam (E beam)
 - ◆ Probe change of signals as well as voltage measurement
 - + Nondestructive
 - Cannot probe Flip chip package
 - More noise for small geometry and high frequency
 - Difficult to probe lower layer of metals
- Resistive Contrast Imaging (RCI)
 - ◆ SEM that generates relative resistance image between two nodes
 - ◆ Useful for open defects

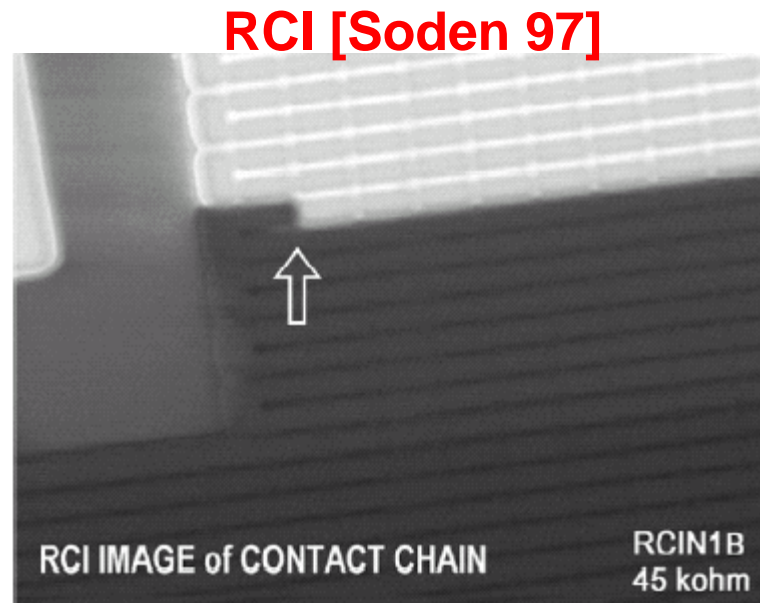


Figure 11. RCI image of contact chain with contrast discontinuity at high-resistance contact (arrow).

Imaging Techniques (powered)

- **Charge and Light-Induced Voltage Alteration (CIVA/ LIVA)**
 - ◆ **Useful for open defects**
- **Scanning Probe Microscope**
- **FIB**
- **Thermal imaging**
 - ◆ **Detects “hot spots” caused by defects**
 - ◆ **Commonly used techniques:**
 - * **Liquid crystal**
 - * **Infrared thermography**

Integrated E-Beam Probe System

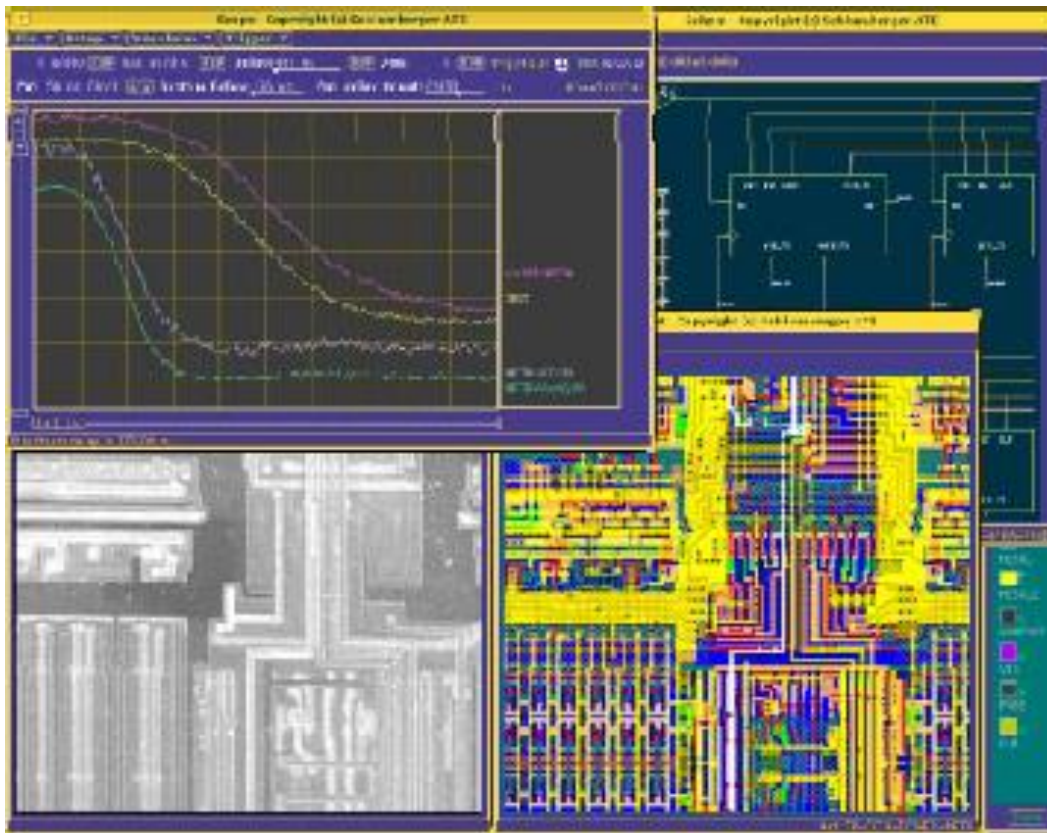
- Show different view all together

Scope

Schematic

SEM

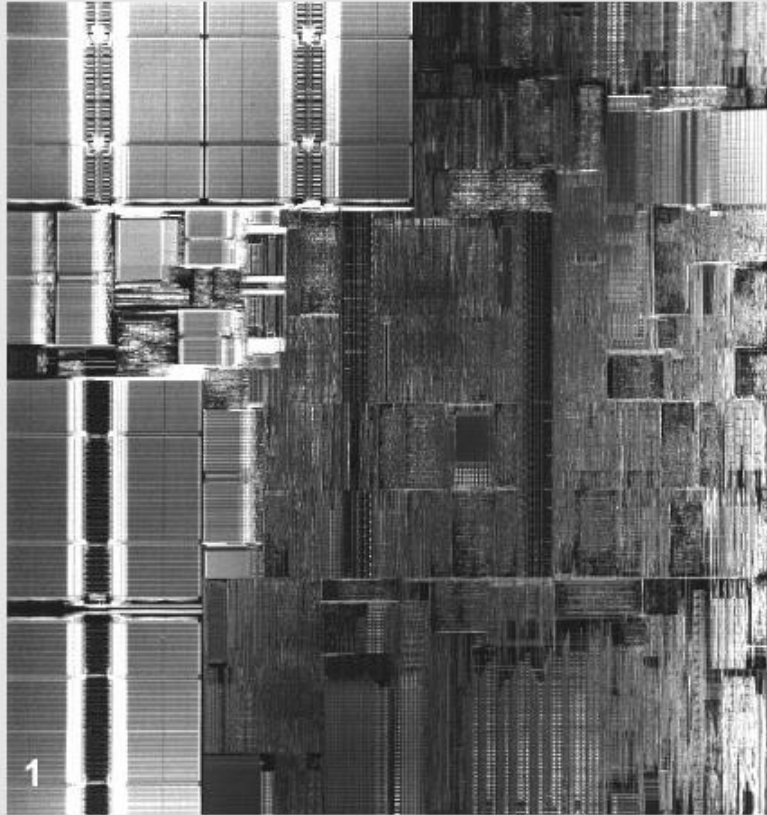
Layout



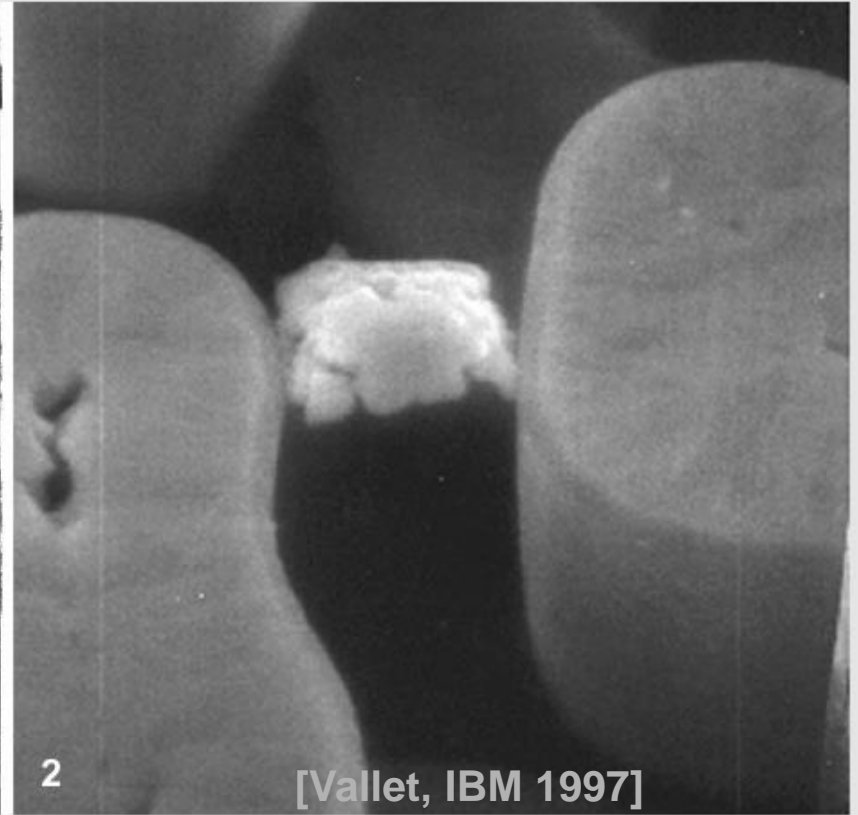
[image courtesy of SK Lu from FJU]

Challenges of Failure Analysis

- # 1 challenge: Looking for a needle in haystack ...
 - ◆ Good software diagnosis is very important



5M Transistor Microprocessor, 196mm²



0.2x0.4μm², nickel particle causing short

- FA equipment are expensive

FA Equipment Costly

- **Cost of useful FA tools (USD)**
 - ◆ **Microscope: 50K**
 - ◆ **X-ray: 150K**
 - ◆ **CSAM: 150K**
 - ◆ **Decapsulator: 40K**
 - ◆ **Automatic curve tracer: 100K**
 - ◆ **SEM: 200K**
 - ◆ **LEM: 150K**
 - ◆ **Probe station: 100K(semi-auto)**
 - ◆ **FIB: 500K**
 - ◆ **E-Beam probe: 300K**

Diagnosis

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Conclusion

- **Diagnosis important for yield improvement and quick time to market**
- **Categories**
 - ◆ **Logic Diagnosis**
 - * **Model-based diagnosis: SSF, delay fault**
 - * **Modeless diagnosis: inject and cure, SLAT**
 - ◆ **Scan chain diagnosis**
- **Diagnosis was usually embedded in ATPG**
 - ◆ **Mentor Graphics: Fastscan**
 - ◆ **Synopsys: Tetramax**
 - ◆ **Cadence: Encounter Test**
- **Now, diagnosis also available as independent tool**
 - ◆ **Mentor Graphics: Yield assist**

References

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