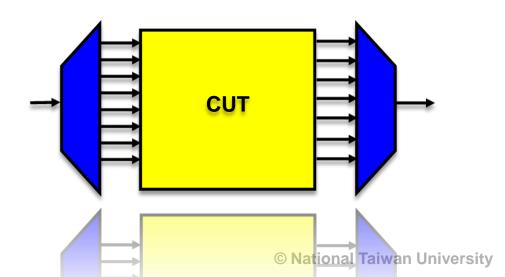
Test Compression

- Introduction
- Test Stimulus Compression
- Test Response Compression
- Industry Practices * (not in exam)
 - OPMISR+ [Cadence, IBM]
 - Embedded Deterministic Test, EDT [Mentor Graphics]
 - VirtualScan and UltraScan [Syntest]
 - DFT Max and Adaptive Scan [Synopsys]
- Conclusion

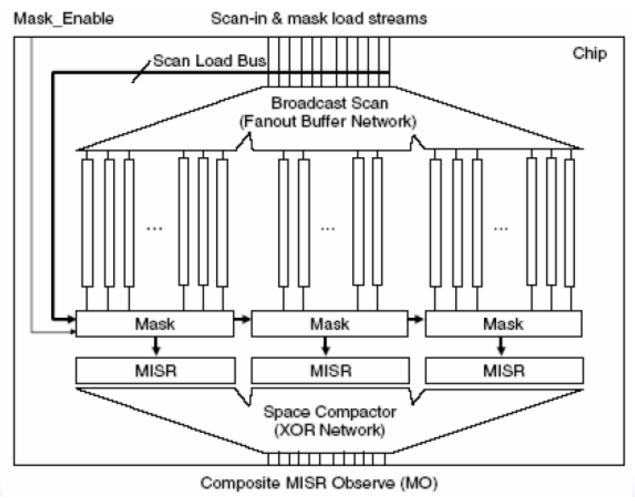


Categories

- Linear-decompression-based schemes
 - Two steps: ATPG followed by compactor design
 - * ETCompression, LogicVision
 - * EDT, Mentor Graphics
 - SOCBIST, Synopsys
 - + ATPG unchanged
 - patterns can increase
 - fault coverage drop
- Broadcast-scan-based schemes
 - Single step: ATPG together with compactor design
 - * OPMISR+, Cadence
 - VirtualScan and UltraScan, SynTest
 - DFT MAX and Adaptive Scan, Synopsys
 - + few patterns
 - + accurate coverage
 - slow ATPG

OPMISR+

- Input: broadcast using fanout buffer network
- Output: XOR network

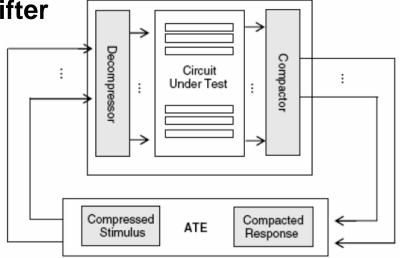


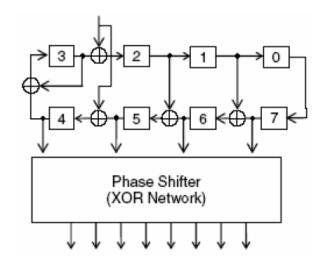
EDT [Rajski 04]

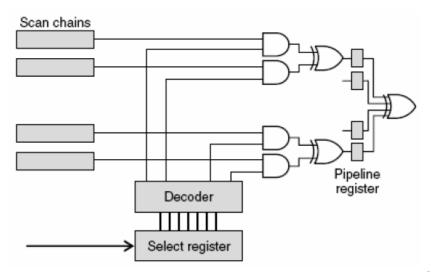
Input: ring generator + phase shifter

Faster than LFSR

- Output:
 - X masking and XOR

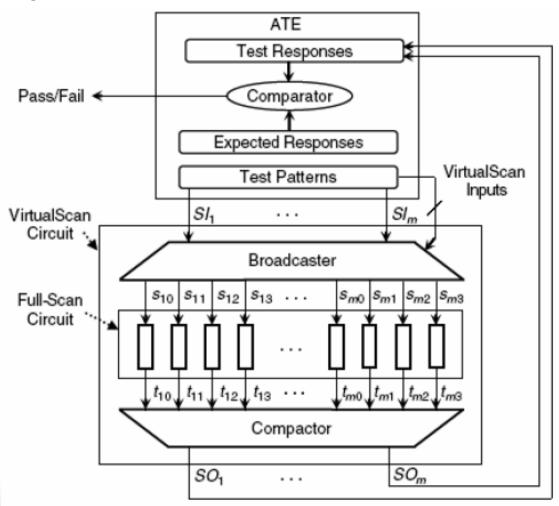






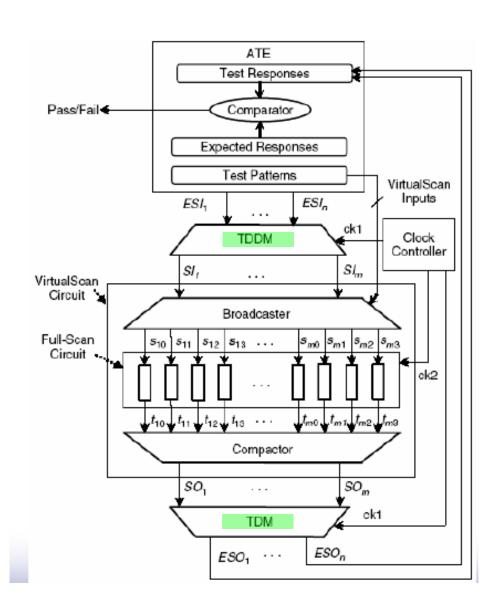
VirtualScan

- Input: broadcast using combinational logic
 - AND OR NAND NOR MUX XOR ...
- Output: X-impact



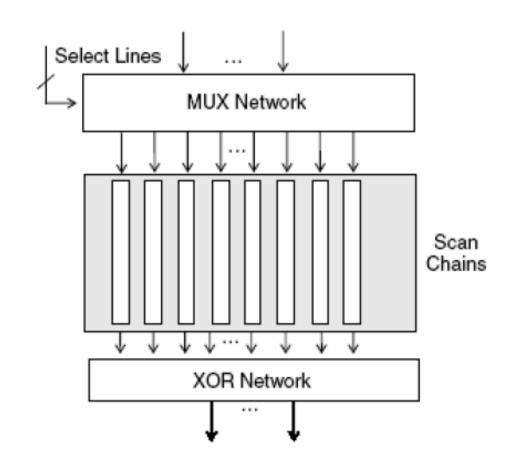
UltraScan

- based on the fact that I/O Pad are faster than scan chains
- Input: Time division demultiplexer, TDDM
- Output: Time division multiplexer, TDM



Adaptive Scan

- Input: broadcast using MUX
- Output: XOR network (like X-compact)



Summary

Industry Practice	Stimulus Decompressor	Response Compactor
OPMISR+ TestKompress VirtualScan DFT MAX ETCompression UltraScan	Broadcast scan (Illinois scan) Ring generator Combinational logic network Combinational MUX network (Reseeding) PRPG TDDM	MISR with XOR network XOR network XOR network XOR network MISR TDM

MISR: multiple-input signature register

MUX: multiplexers

PRPG: pseudo-random pattern generator

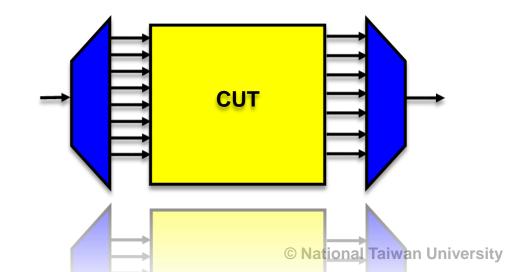
TDDM: time-division demultiplexer

TDM: time-division multiplexers

XOR: exclusive-OR

Test Compression

- Introduction
- Test Stimulus Compression
- Test Response Compression
- Industry Practices
- Conclusion



Concluding Remark

- Test compression now becomes a necessary step in DFT and ATPG
- How to select a suitable compression technique?
 - Trade-off between
 - Compression ratio
 - Fault coverage degradation
 - * X-tolerant
 - Design efforts (CFI, CFS)
 - * ATPG run time

References

- [Goel 81] Goel, Rosales, "PODEM-X: An automatic test generation system for VLSI logic structures, "ACM IEEE DAC, Pages: 412 - 420 , 1981.
- [CLRS 09] Cormen, Leiserson, Rivest, Stien, Introduction to Algorithms, 3rd edition, MIT Press, 2009.
- [McCluskey 56] E. J. McCluskey, "Minimization of Boolean Functions," Bell System Technical Journal, Vol.35, pp.1417-1444, Nov. 1956.
- [Mitra 04] S. Mitra K. Kim, "X-compact, An efficient response Compaction Technique," IEEE TCAD, 2004.
- [Mrugalski 03] G. Mrugalski, J. Rajski, J. Tyszer, "Linear independence as evaluation criterion for two-dimensional test pattern generators", Proc. VLSI Test Symp., pp. 377.
- [Rajski 04] J. Rajski, J. Tyszer, M. Kassab, N. Mukherjee, "Embedded deterministic test," IEEE TCAD, Volume: 23, Issue: 5, May 2004.