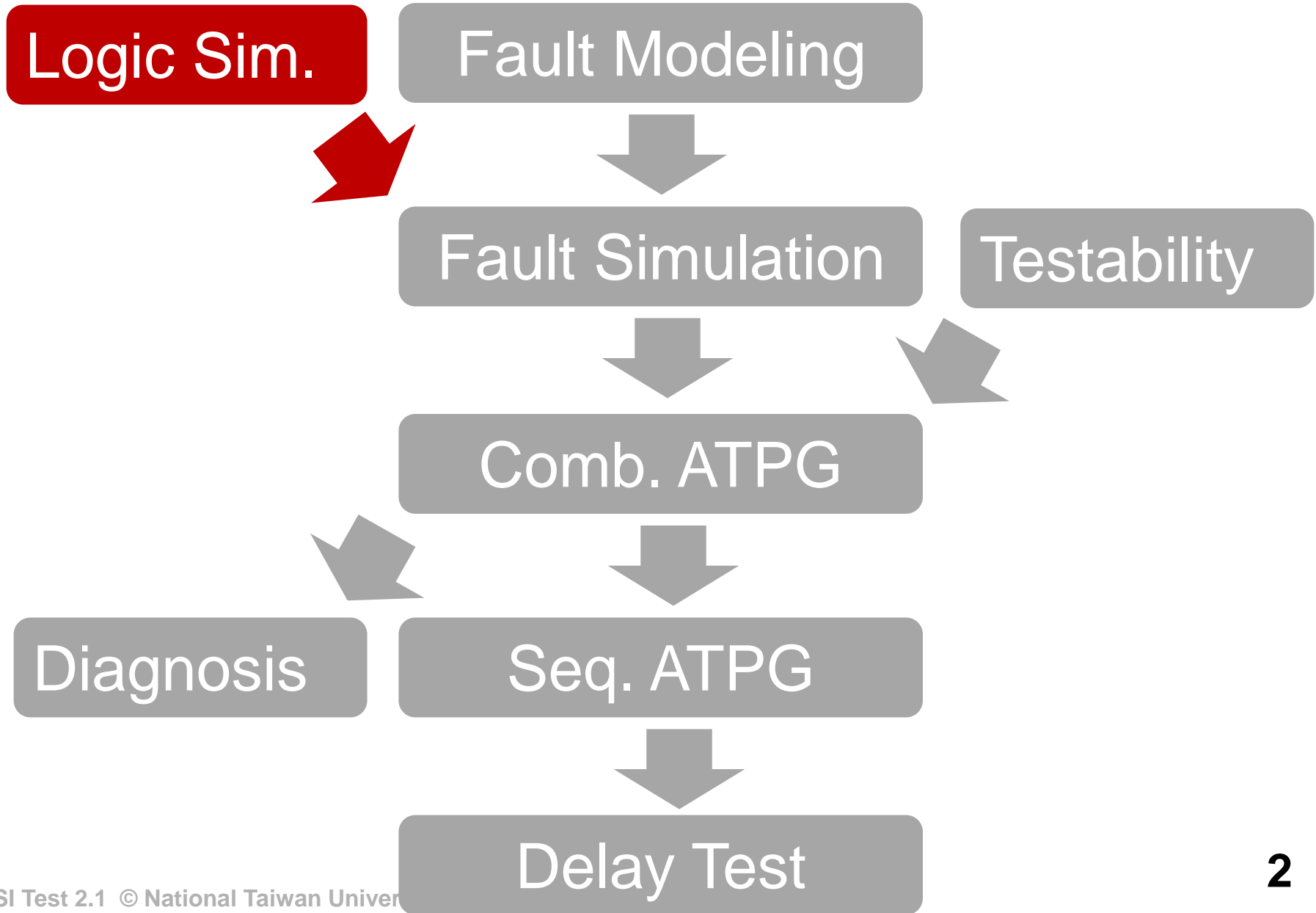# VLSI Testing
積體電路測試

Logic Simulation

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Course Roadmap (EDA Topics)

Logic Sim.

Fault Modeling

Fault Simulation

Testability

Comb. ATPG

Diagnosis

Seq. ATPG

Delay Test
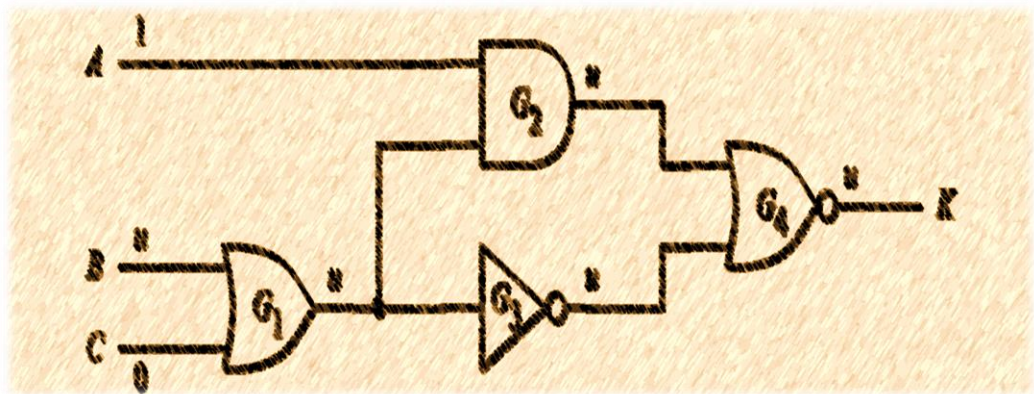
Why Am I Learning This?

- **Logic simulation is essential to verify our**
  - ♦ **Design correctness**
  - ♦ **ATPG patterns**
- **Logic simulation is basic EDA tool for digital circuits**
  - ♦ **Basic building block of many tools**

> *"Logic is the anatomy of thought."*
>
> *(John Locke)*

Logic Simulation

- **<u>Introduction</u>**
- **Simulation Models**
- **Logic Simulation Techniques**
- **Issues of Logic Simulations**
- **Conclusions**

What Is Simulation?

- **Given input stimuli, models, and commands**
  - ♦ **Run software to produces output responses**
- **For digital circuits:**
  - ♦ **Input stimuli are *test patterns***
  - ♦ **Models can be functional/logic/transistors (next slide)**


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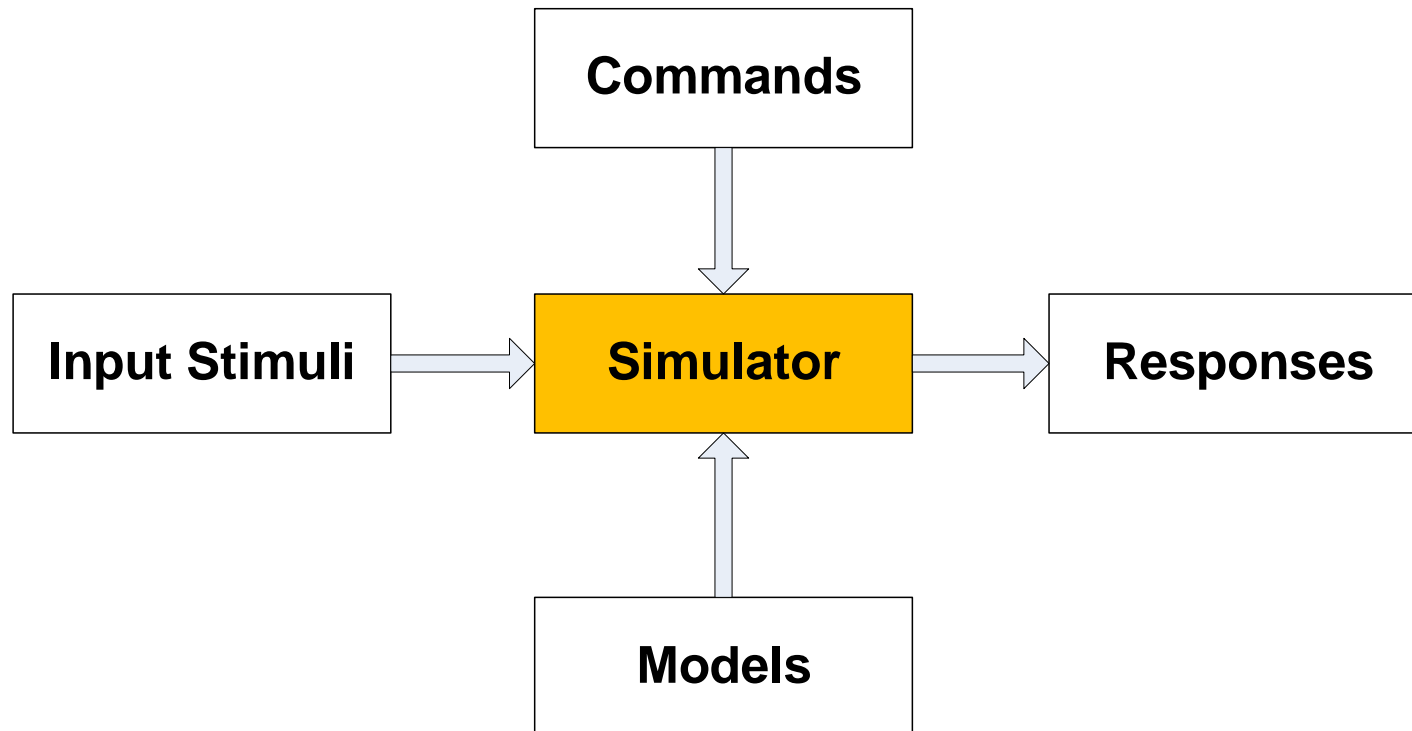
Levels of Circuit Simulation

- *Functional/Behavior level*
  - ◆ **Interconnect of modules (expressed in programming language)**
  - ◆ **Good for architecture and functional verification**
  - ◆ **Fast but inaccurate**
  - ◆ **Example: C, System-C, Verilog (Register-Transfer-Level, RTL)**
- *Logic level*   ← **focus of this chapter**
  - ◆ **Interconnect of Boolean gates (aka. *Gate-level netlist*): AND, OR, NOT …**
  - ◆ **Good for logic verification, test pattern generation**
  - ◆ **Example: Verilog (gate-level)**
- *Transistor level*
  - ◆ **Interconnect of transistors**
  - ◆ **Good for analog/mixed-signal and timing critical digital circuits**
  - ◆ **Slow but accurate**
  - ◆ **Example: SPICE**
- *Mixed-level*
  - ◆ **Mixed functional/logic/transistor levels**
  - ◆ **Trade off CPU time and accuracy**
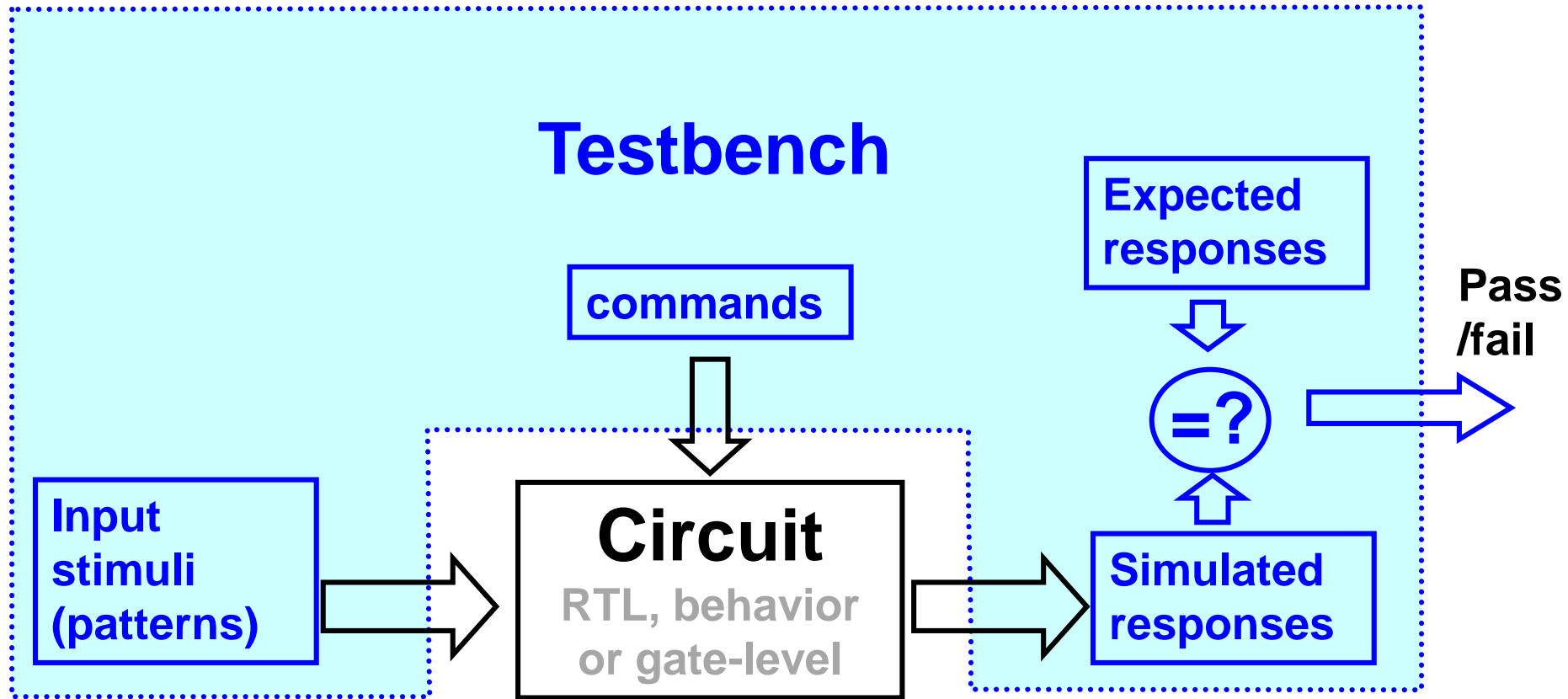
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Verification by Simulation

- **1. Verify design correctness**
- **2. Verify ATPG patterns**

(Manual or Auto.)
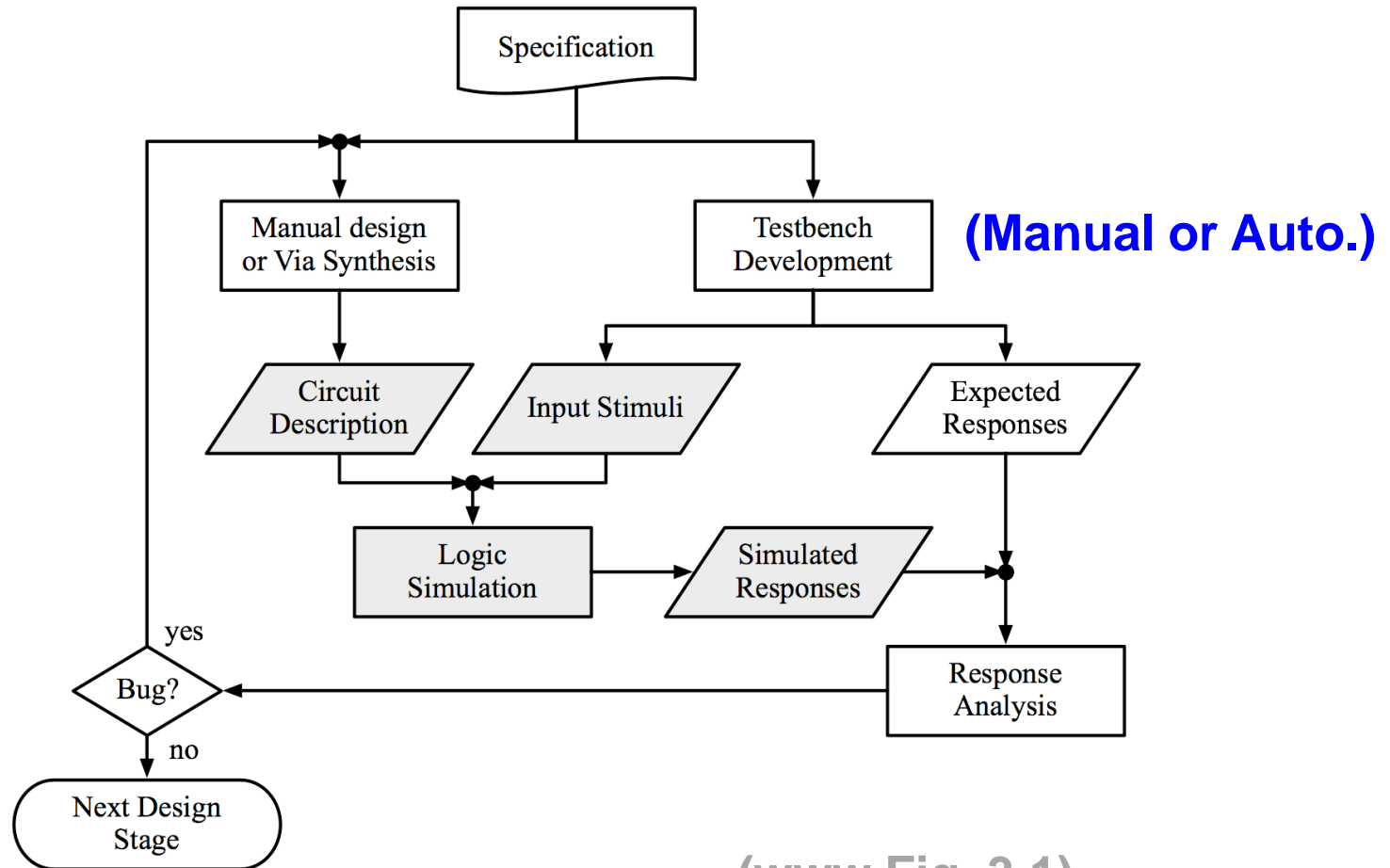
(www Fig. 3.1)

What is Testbench ?

- **Setup a simulation environment**
- **Apply input stimuli; run commands; observe responses**

Testbench

commands

Expected responses

Input stimuli (patterns)

Circuit
RTL, behavior or gate-level

Simulated responses

=?

Pass /fail

- **Testbench is *NOT* implemented as physical circuits**

Summary

- **Introduction**
  - **What is simulation?**
    - ∗ **Produce output based on given input stimuli and model**
  - **Levels of simulation**
    - ∗ **functional, logic, transistor, mixed**
  - **Design verification by simulation**
    - ∗ **testbench**

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