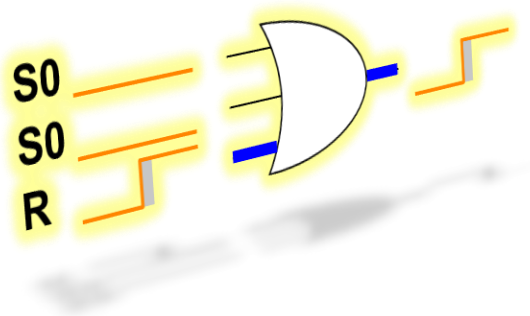
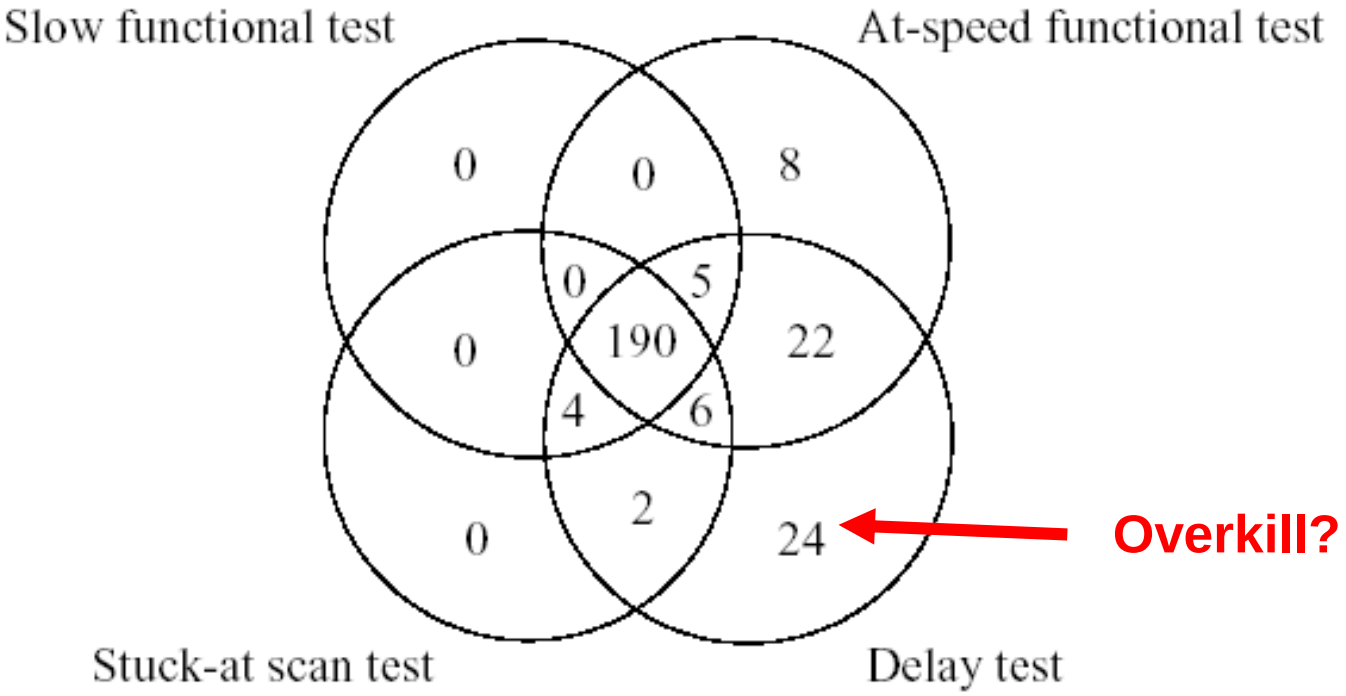
Delay Test

- Introduction and delay fault models
- Path Delay Fault
- Transition Delay Fault
- **Experimental Results* (not in exam)**
- **Issues of Delay Tests* (not in exam)**
- **Conclusions**



HP Experiment [Maxwell 96]

- Delay testing = TDF + some PDF
- Delay testing detects detected unique CUTs
  - that escaped other testing



HP Experiment (Cont'd)

- **Observations: How useful are path delay tests?**
  - **2,000 longest paths chosen and only 148 paths have robust tests**
  - **Path delay fault tests only detect 18.5% of devices with delay faults**

Stanford Experiment [EJM 00]

- Center for Reliable Computing, Stanford

- Murphy Experiment
  - Goal: evaluate effectiveness of different test techniques

- Murphy Chip
  - LSI Logic 150k CMOS Gate Array
  - 25k Gates, all combinational CUTs
  - 120-Pin Ceramic PGA Package
  - $L_{eff} = 0.7\mu m$
  - 5 volt Nominal Supply Voltage
  - Total 5.5K tested
    - 116 defective chips found

SSF Test Results

				Escapes		
SSF Tool	Fault model	Cove-rage	Test length	characte rized	slow (1/3)	slow (1/30)
1**	gate	100	427	4	7	9
2*	gate	100	313	3	5	7
3**	pin	100	857	3	6	7
	gate	100	1,000	2	5	7
4**	pin	100	456	6	8	9
	gate	100	603	2	4	5
5**	pin	100	466	6	9	9
	gate	100	571	4	6	8
6*	gate	100	547	3	7	7
	gate	99	532	4	8	8
	gate	98	490	6	9	10
	gate	95	467	10	12	13
	gate	90	427	15	17	18
	gate	80	334	20	23	23
Weighted random*	gate	100	62,921	2	7	
Weighted random**	gate	100	21,892	2	7	
Exhaustive				0	2	4

* academic ATPG tools ** commercial ATPG tools

Non-SSF Test Results

- **delay fault testing does not detect unique defective chips**
  - **Performance not particular impressive**

			Escapes***		
Tool	Fault model	Test length	Characterized	Slow (1/3)	# of CUTs tested
	IDDQ	100	15		116
	VLV		3	4	116
1**	Transition	1,444	6	8	116
2*	Stuck open	1,610	4	9	116
3*	Gate delay fault		9	11	78§
	Gate delay fault, X->0		8	9	78§
4*	Robust path delay, X->0		5	5	60§
	Robust path delay, X->random		5	5	60§
5*	Robust path delay		3	5	60§
6**	Non-robust path delay		8	8	60§
	Non-robust path delay		2	5	60§
7	Verification		6	7	56§

* academic ATPG tools ** commercial ATPG tools

*** Tests applied at characterized speed

§ These patterns were not available for all of the CUT

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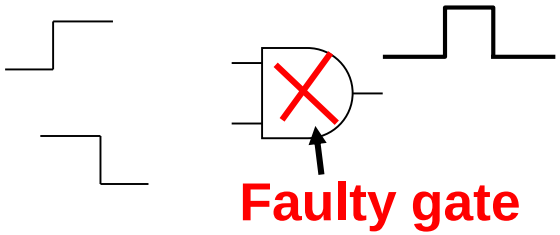
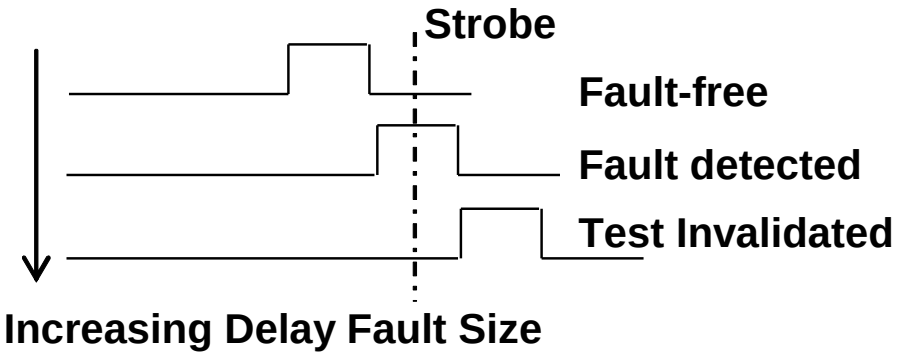
Issues of Delay Tests

- Path selection is difficult
  - Too many paths in real circuits
  - e.g. $2x10^{20}$ paths in 32-bit multiplier (ISCAS'85 benchmark C6288)
  - Usually choose timing critical paths
    - good to verify the speed, but not good for defect testing
- Need fast ATE to detect small delay faults
- Strobe time hard to determine
- Timing-aware ATPG is slow
- Many untestable paths
- Multi-cycle paths

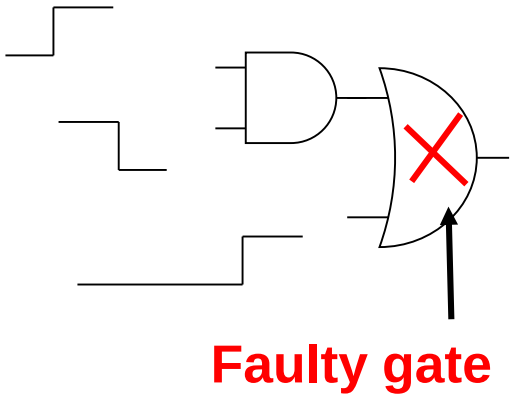
Strobe Time Hard to Determine

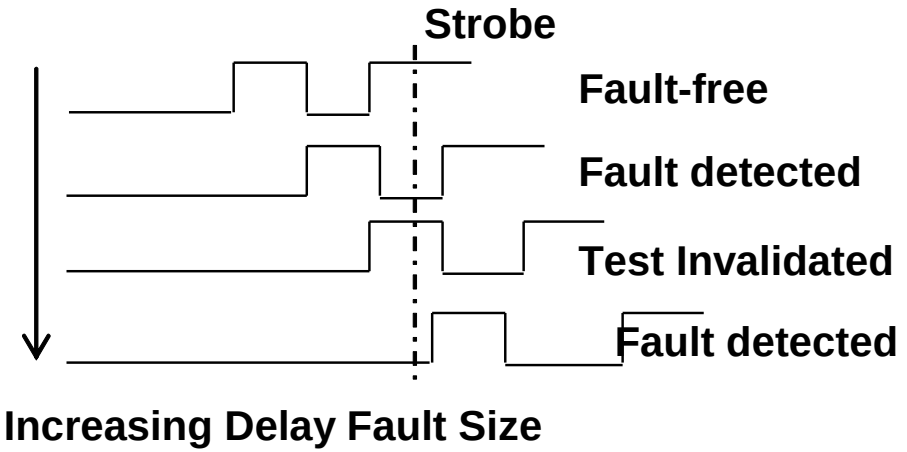
- Strobe time hard to determine in advance
  - Fault size dependent
  - Process variation
- Example:





(a)





(b)

Delay Test

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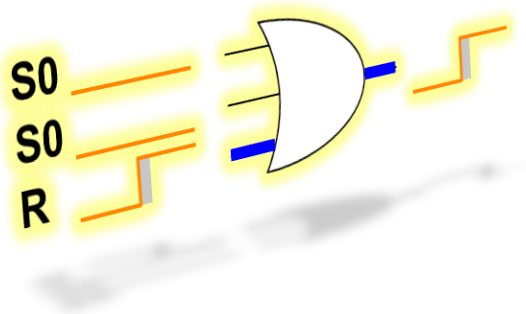
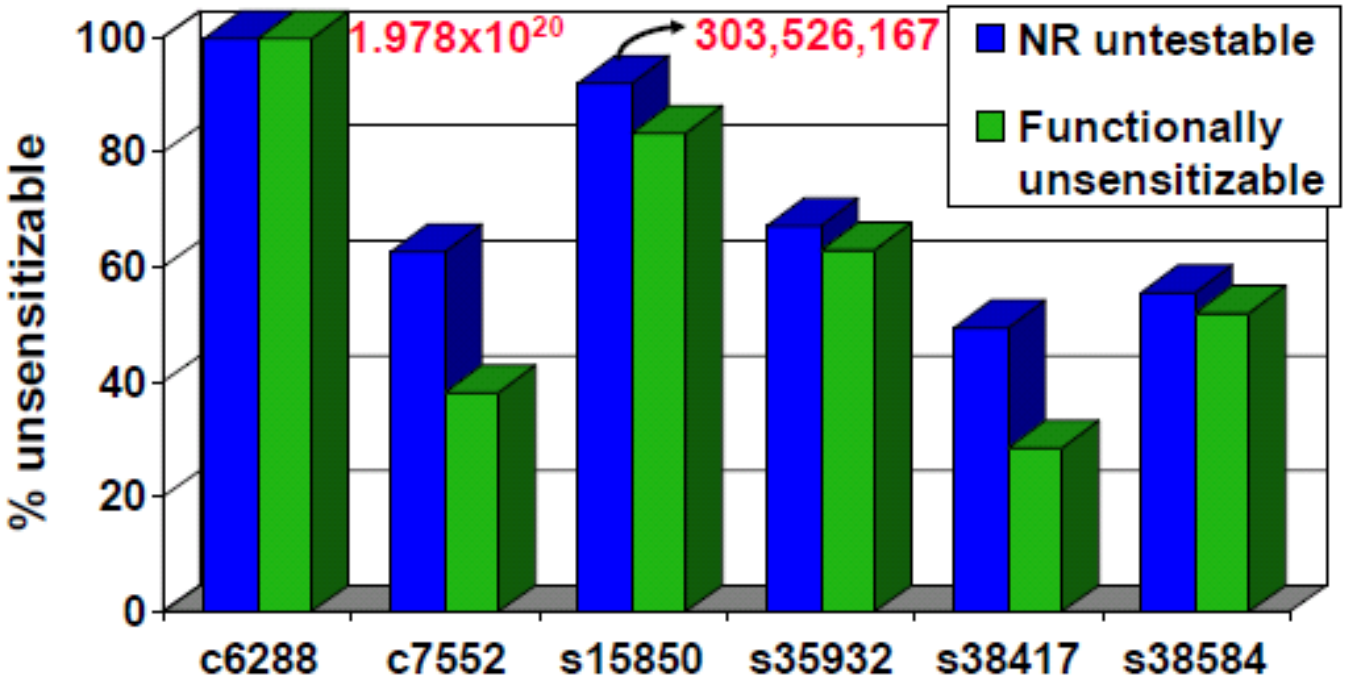


Many Untestable Paths



Difficulties in Delay Tests

- At-speed testing needs expensive ATE
- Path list hard to generate
  - Too many paths
- *Small delay faults* occur more frequent in nano-meter technologies
  - Need propagate fault through long paths
    - Timing-aware ATPG is slow
- At-speed delay testing very difficult
  - How to apply high speed clock in test mode?
  - At-speed delay testing induces signal/power integrity problem
    - IR drop, ground bounce, x-talk noise …
- Overkill
  - Some IC fail delay testing but actually work in system
  - Test too many paths that never used in functional mode?

Delay Testing Recommendation

- Must do transition delay fault ATPG
- Then select some critical paths for PDF ATPG
  - Timing analyzer (STA) selected critical paths
    - e.g. >95% clock period
  - Designers' choice
    - Remove special paths: e.g. multi-cycle paths
- If there are too many paths
  - Choose random samples that are not overlapped
- If they are not testable
  - Increase sample size or reduce threshold

Reference

- [Breuer 74] M.A. Breuer, "The effects of races, delays, and delay faults on test generation." IEEE Transactions on Computers 100.10 (1974): 1078-1092.
- [Barzilai 83] Z. Barzilai, "Comparison of AC self-testing procedures." International Test Conf., 1983.
- [Iyengar 88] Iyengar, “Delay Test Generation: 1 Concepts And Coverage Metrics,” IEEE International Test Conference, 1988.
- [Lin 87] C. J. Lin and S. M. Reddy, “On Delay Fault Testing in Logic Circuits, “ IEEE Trans. on Computer-Aided Design, Vol. CAD-6, No. 5, September 1987, pp.694-703.
- [Levendel 87] Y. Levendel and P. R. Menon, “ Transition Faults in Combinational Circuits: Input Transition Test Generation and Fault Simulation,” Proceedings of International Fault Tolerant Computing Symposium, 1987.
- [Krstic 98] A Krstic, KT Cheng, *Delay Fault Testing for VLSI Circuits*, Kluwer Academic Publisher, 1998.
- [Pomeranz 94] I. Pomeranz, S.M. Reddy, “An Efficient nonenumerative Method to Estimate the Path Delay Fault Coverage in Combinational Circuits,” TCAD VOL. 13, NO. 2, FEBRUARY 1994.
- [Smith 85] G. L. Smith, ”Model for Delay Faults Based upon Paths,” Proceedings of IEEE International Test Conference, 1985.