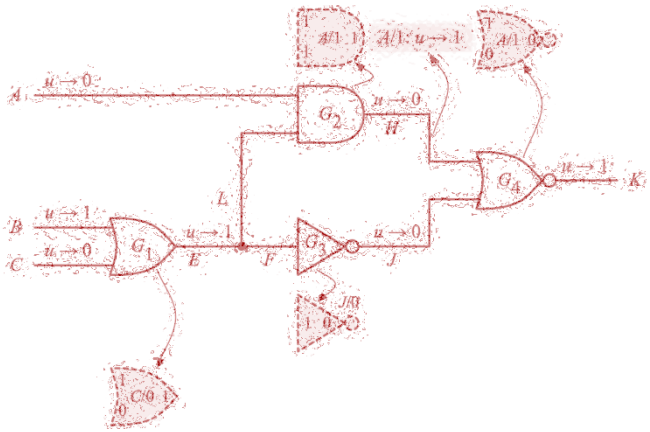
Fault Simulation

- Introduction
- **Fault simulation techniques**
  - Serial fault simulation
  - **Parallel fault simulation (1965)**
  - **PPSFP (1985)**
  - Deductive fault simulation (1972)
  - Concurrent fault simulation (1974)
  - Differential fault simulation (1989)
- Alternatives to fault simulation
- Issues of fault simulation
- Concluding remarks



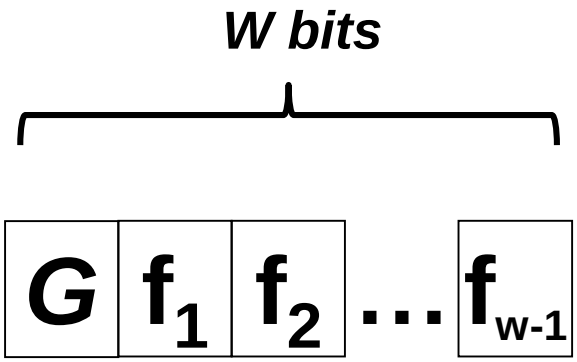
Two Types of Parallelism

- **Exploit parallelism of logic instructions (bit-wise operations)**
  - **1. Parallelism in faults**
    - ***Parallel Fault Simulation*** **[Seshu 65]**
  - **2. Parallelism in patterns**
    - ***Parallel Pattern Single Fault Propagation, PPSFP*** **[Wacukauski 85]**

Two Types of Parallelism

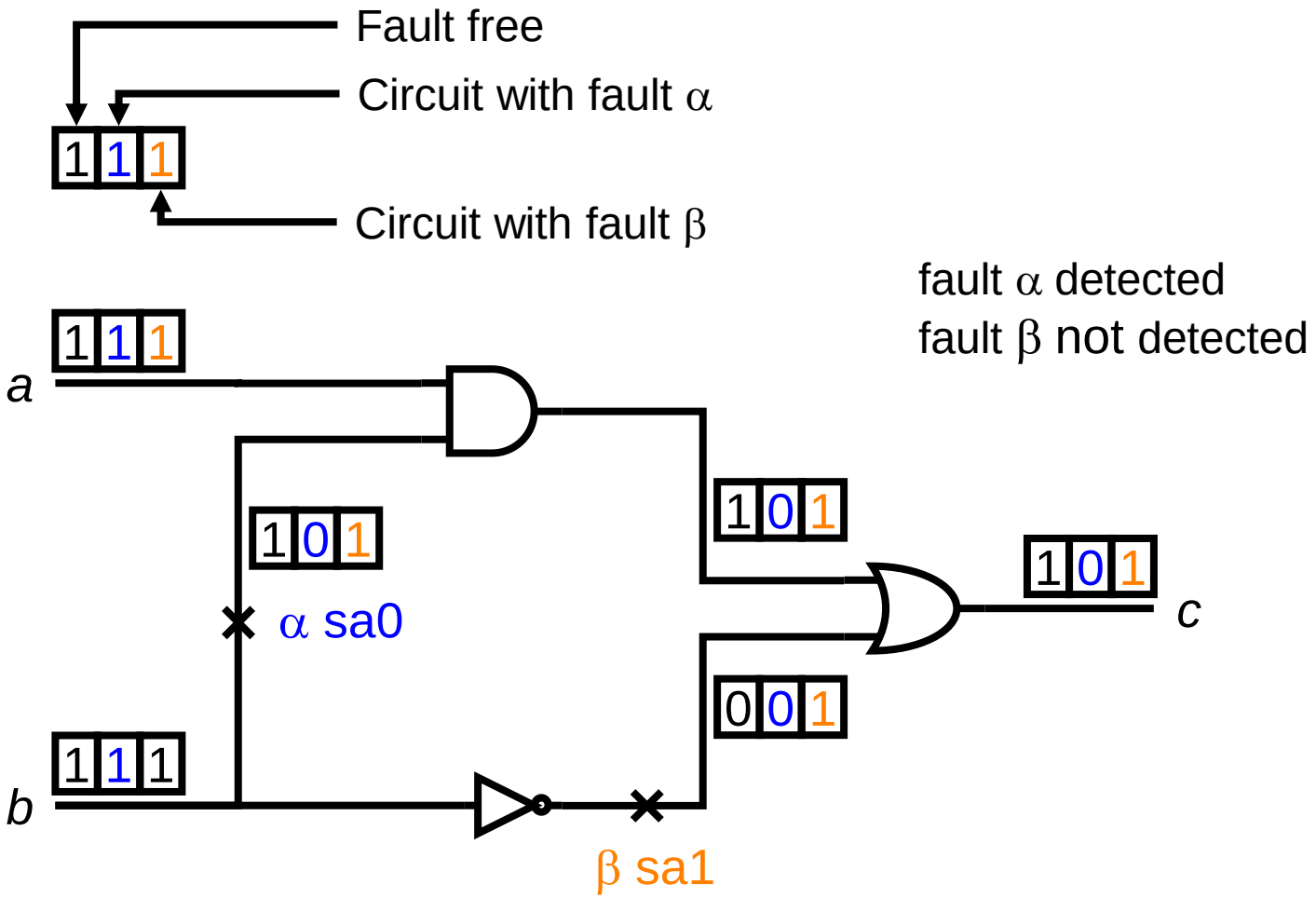
Parallel Fault Simulation [Seshu 65]

- Run parallel logic simulation with *W*-1 faults (*W* is CPU word size)
  - one bit for fault-free circuit
  - *W*-1 bits for faulty circuit
- (*W*-1) times faster than serial fault simulation (w/o fault dropping)



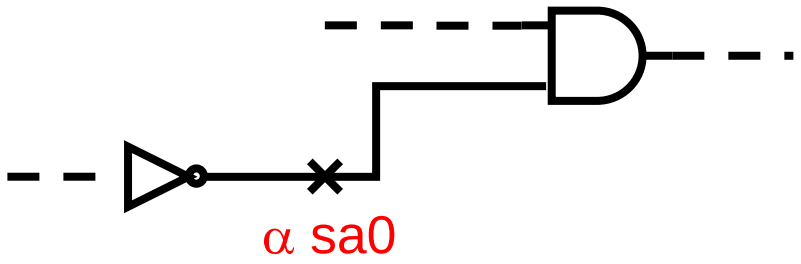
Example

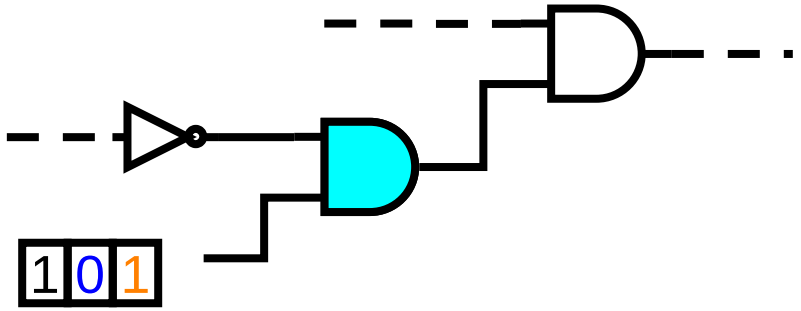
- **Assume *W*=3**



Fault Injection

- ***Fault Injection*** **= inserting fault(s) into circuit**





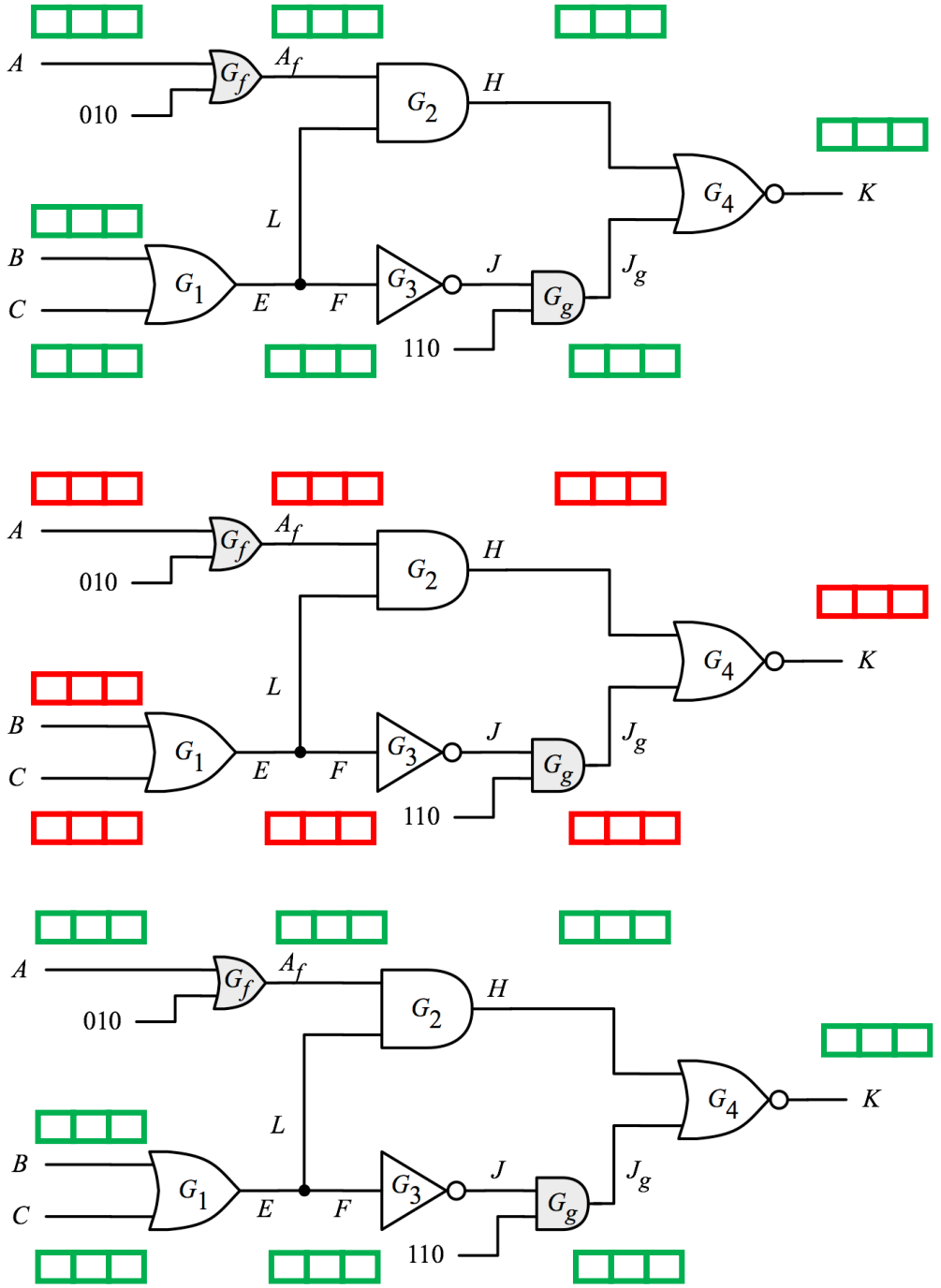
0 = SA0 fault injected
1 = SA0 fault not injected

Quiz: how to insert SA1 fault?
A:

Quiz

Q: Consider two faults: (*f=SA1 , g=SA0)*. Use parallel fault simulation on patterns
***P*$_1$= {010},**
***P*$_2$= {001},**
***P*$_3$= {100}.**

A:

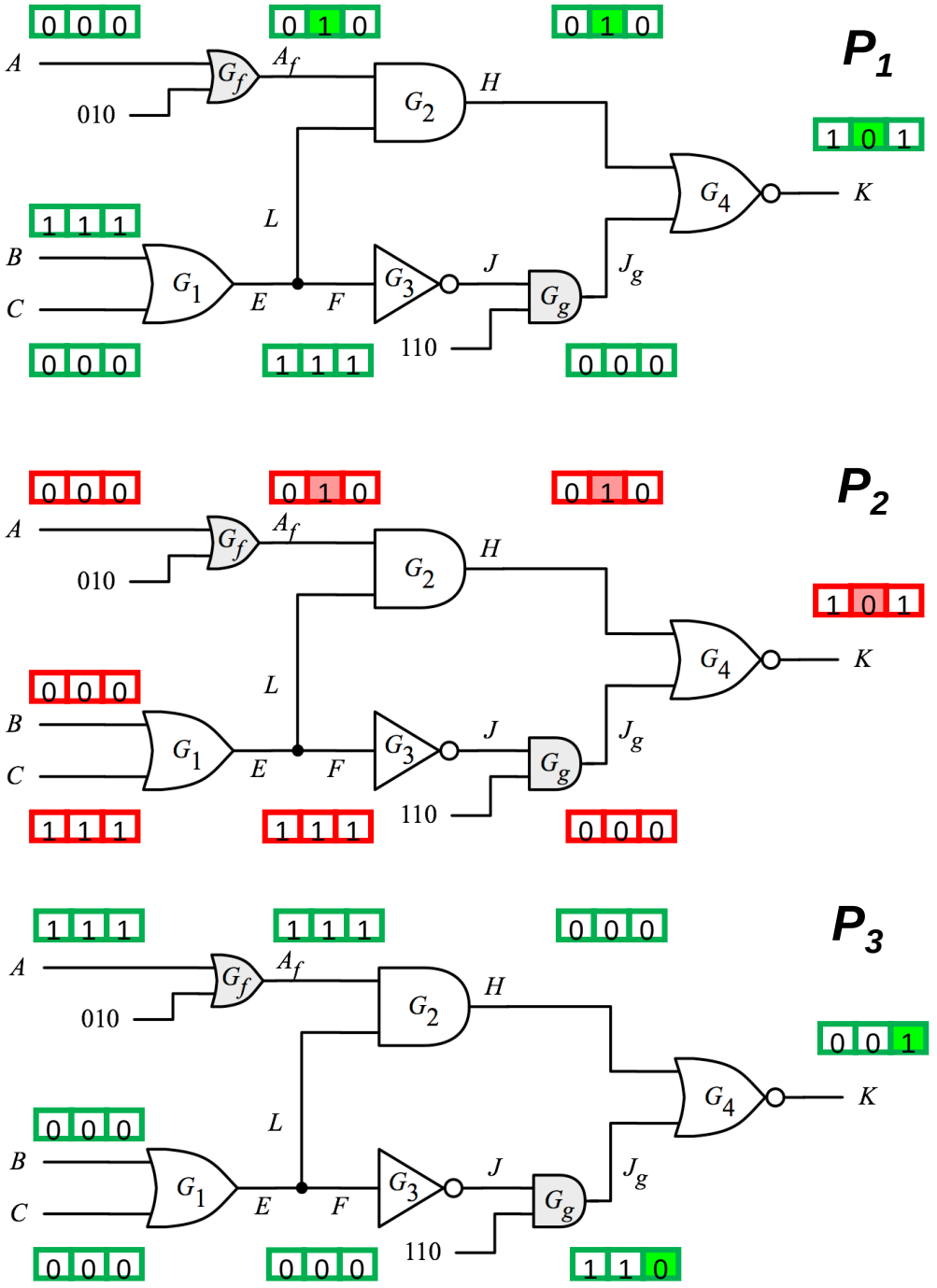


Assume no fault dropping

Solution

Q: Consider two faults: (*f=SA1 , g=SA0)*. Use parallel fault simulation on patterns
***P*$_1$= {010},**
***P*$_2$= {001},**
***P*$_3$= {100}.**

A:
P*$_1$ *P*$_2$ detect *f
P*$_3$ detects *g



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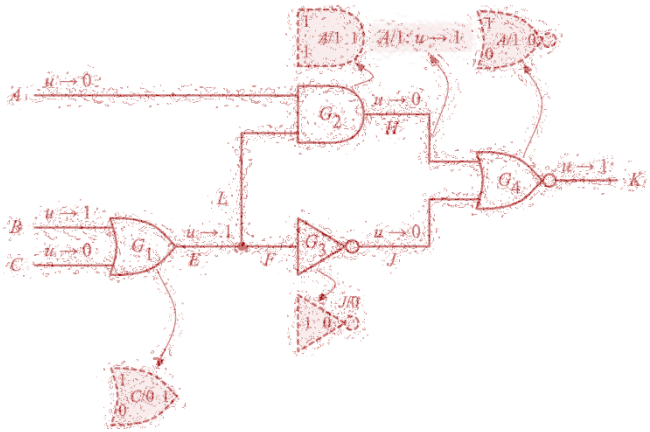
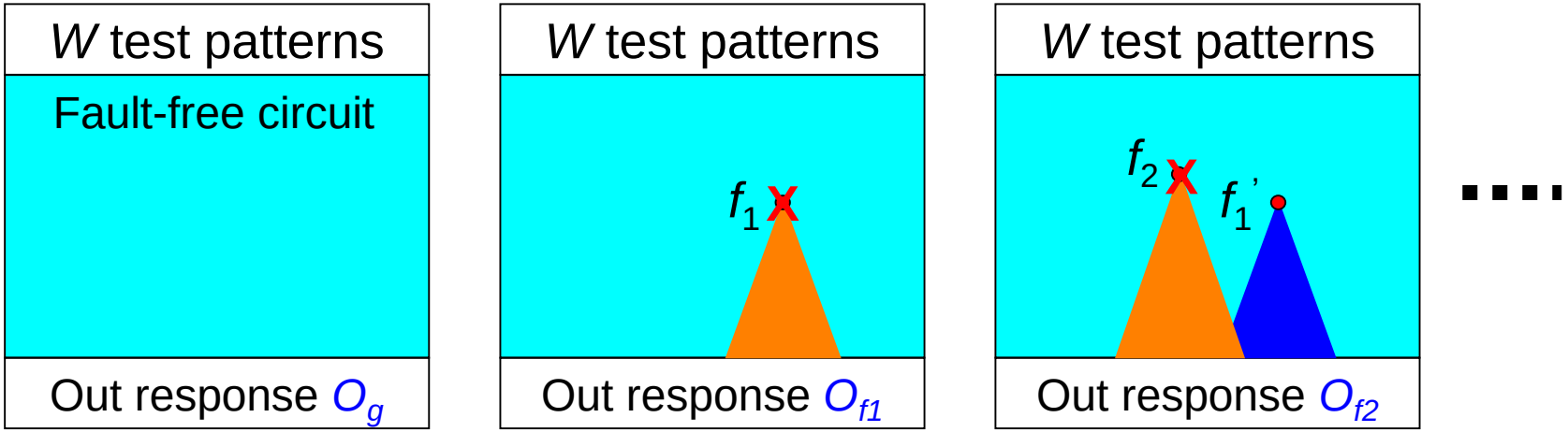


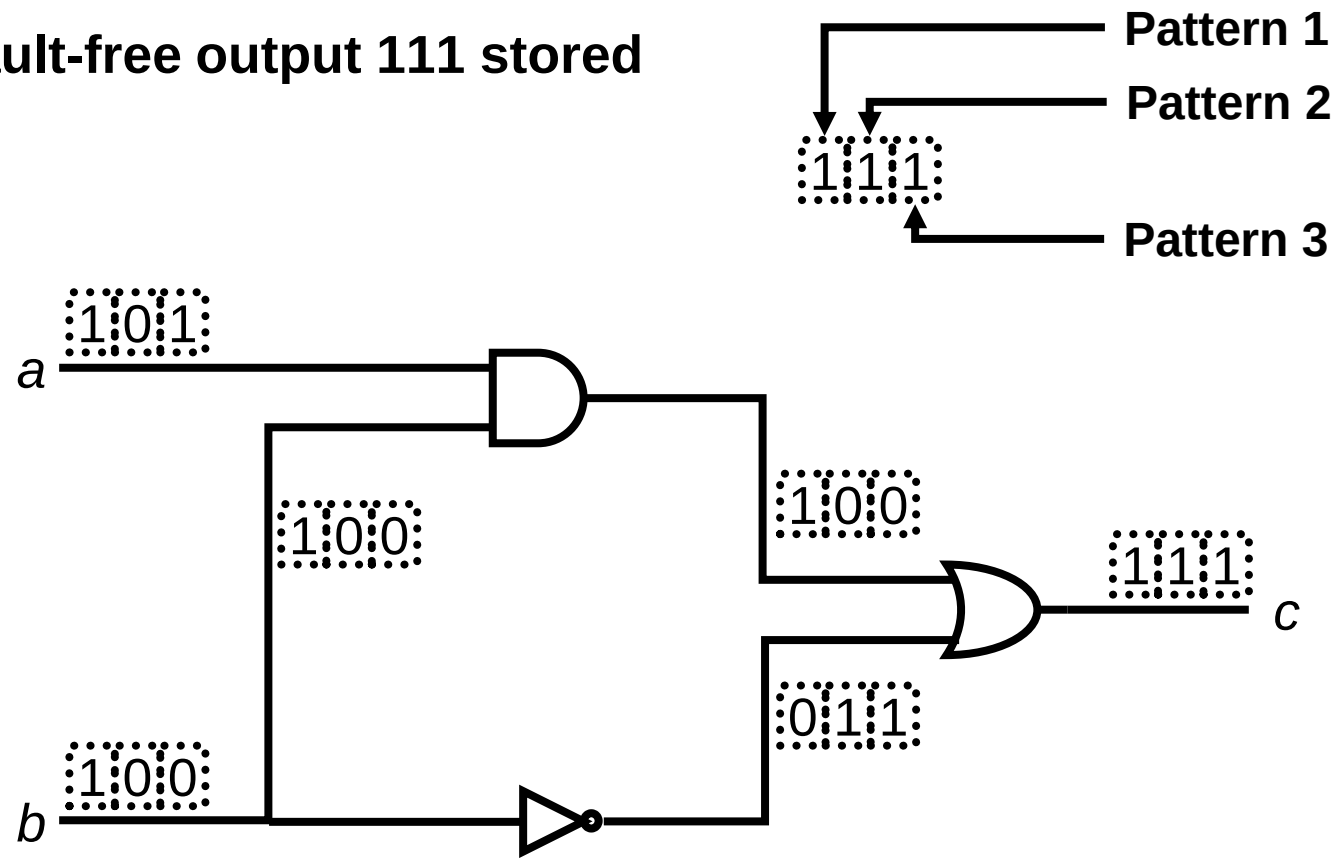
PPSFP

- Parallel pattern assumes combinational circuit
- Procedure
  - Step 0: run logic simulation, store good output O_g
  - Step 1: Inject f_1 by creating an event at the fault site
  - Step 2: Perform event-driven simulation, get output O_{f1}
    - Compare O_g and O_{f1}
  - Step 3. Create an event to undo fault effect of f_1
    - Inject an event for next fault f_2
  - Repeat step 2~3 until all faults simulated



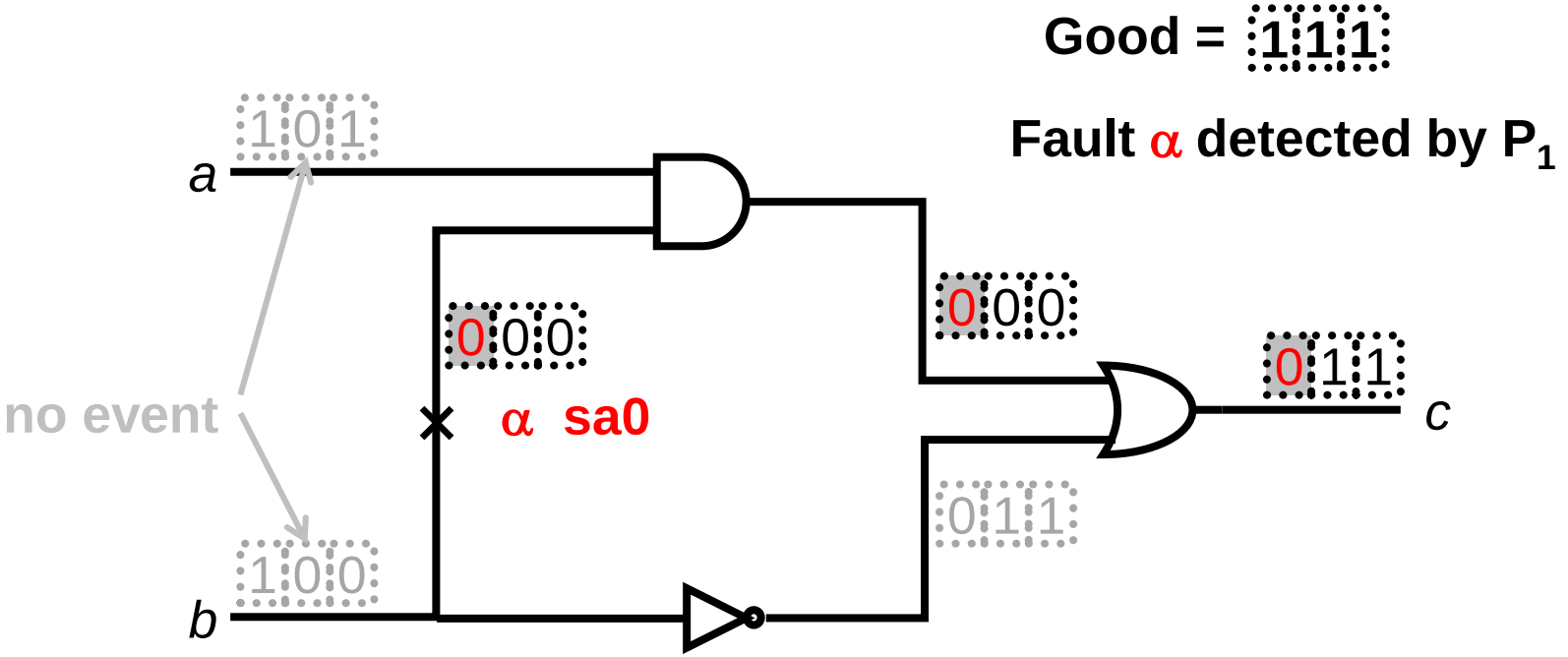
PPSFP Example

- Assume *W*=3
- Fault-free circuit
  - Fault-free output 111 stored



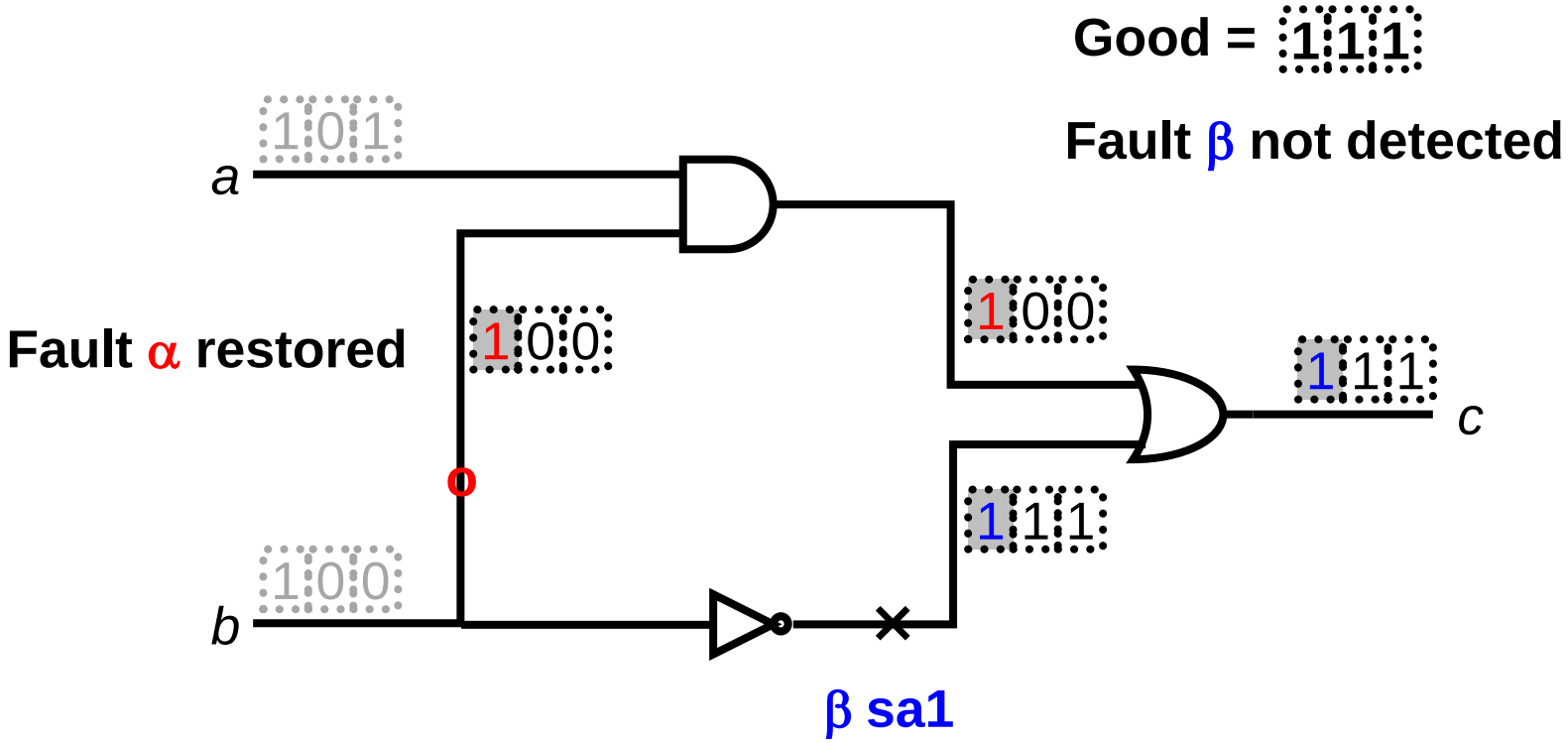
Example- cont'd

- One event created to inject fault α
  - fault effects are then propagated



Example – cont'd

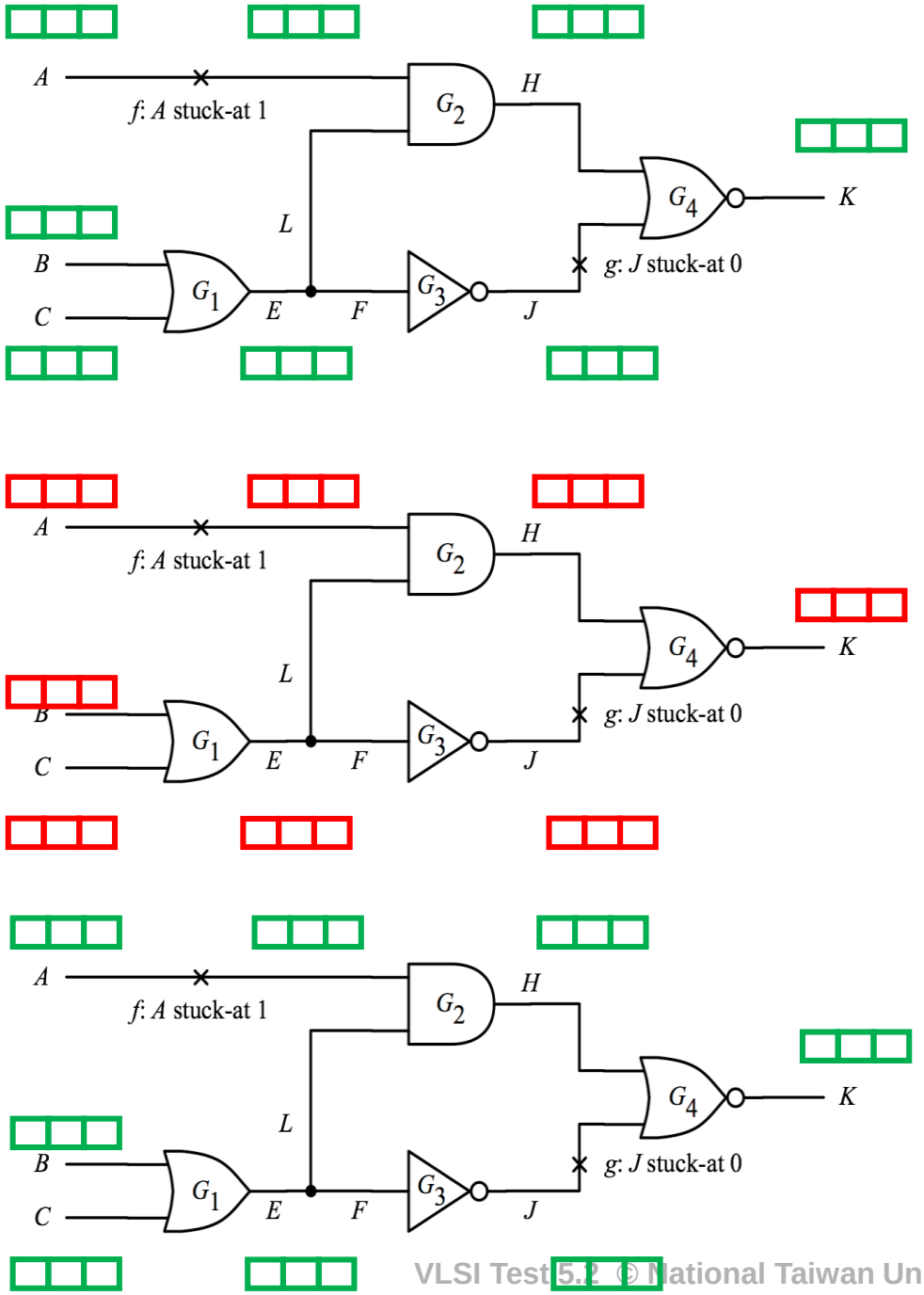
- Two events created:
  - One event to restore fault α
  - One event to inject fault β



Quiz

Q: Consider two faults: (*f=SA1 , g=SA0)*. Use PPSFP on patterns P_1= {010}, P_2= {001}, P_3= {100}.

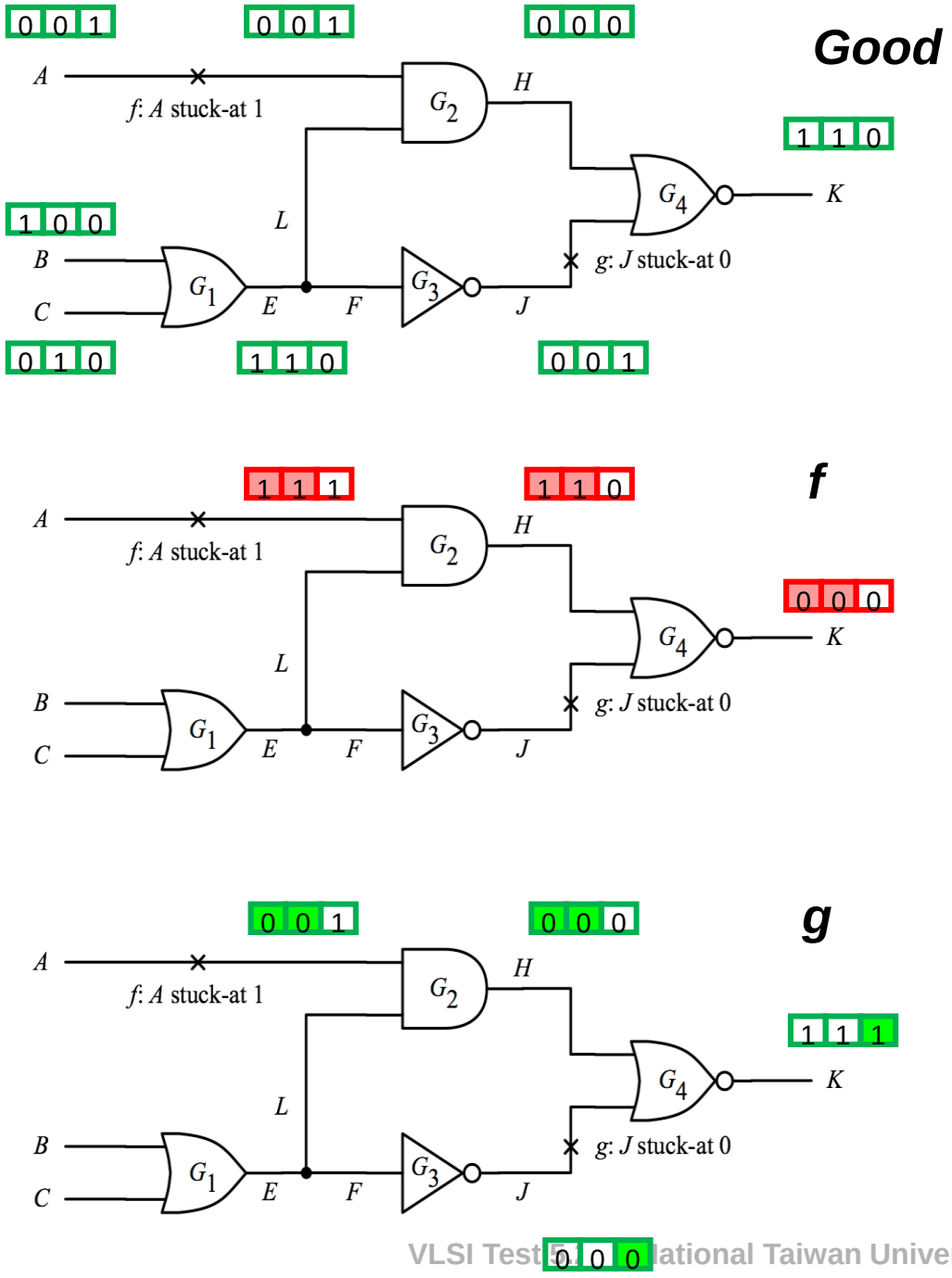
A:



Solution

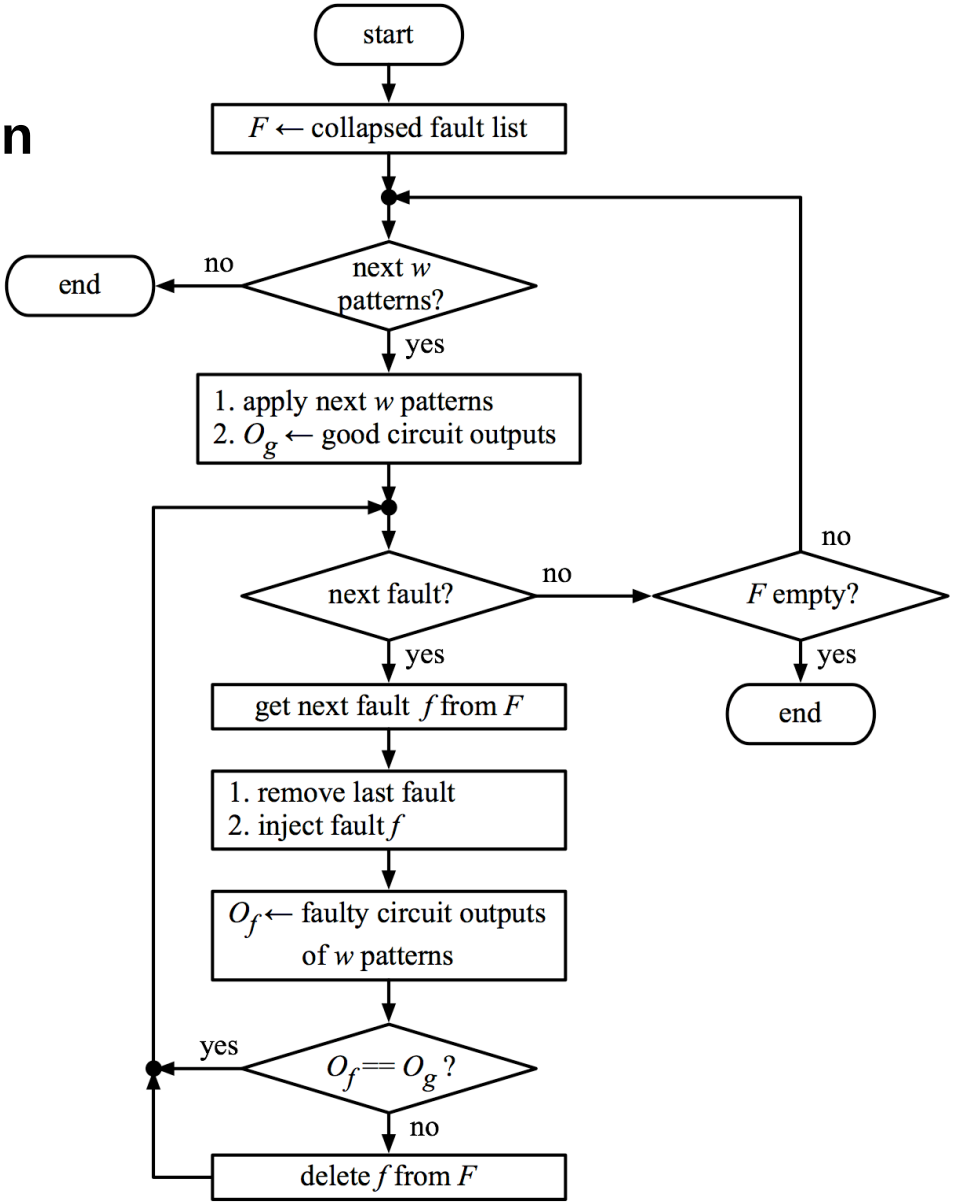
Q: Consider two faults: (*f=SA1 , g=SA0)*. Use PPSFP on patterns P_1= {010}, P_2= {001}, P_3= {100}.

A:
P_1 P_2 detect *f*
P_3 detects *g*



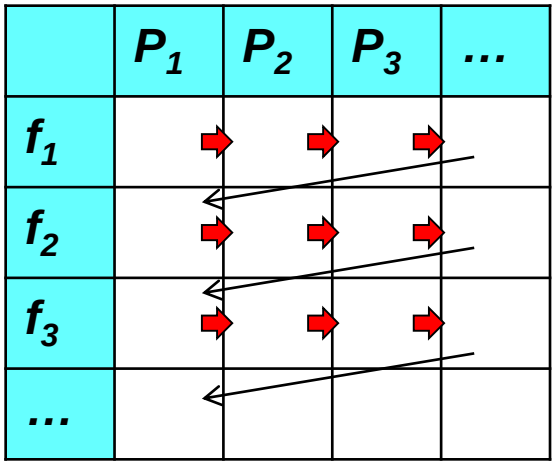
PPSFP Flow Chart

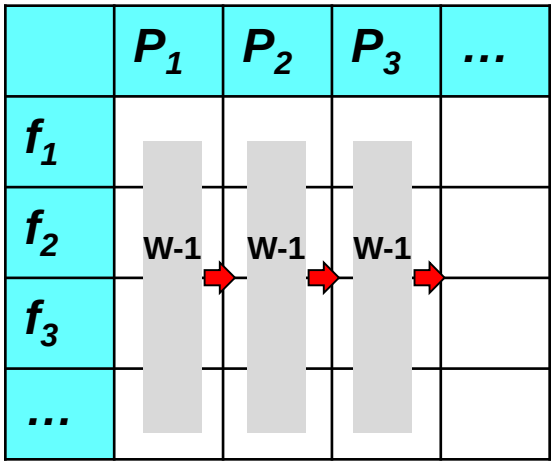
- **inner loop: fault**
- **outer loop: pattern**
- **(WWW Fig 3.25)**

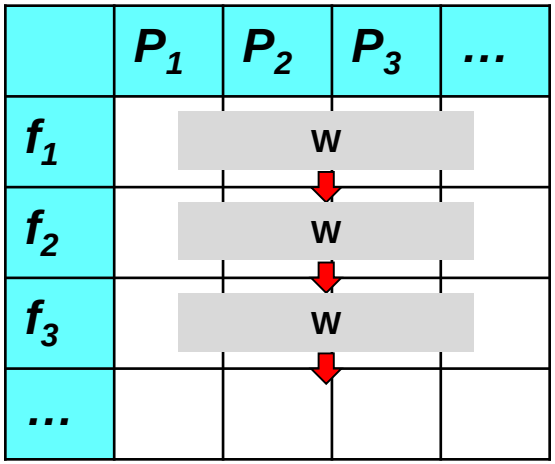


Comparison

- Serial fault simulation: one fault, one pattern
- Parallel fault simulation: multiple faults, one pattern
- PPSFP: multiples pattern, one fault

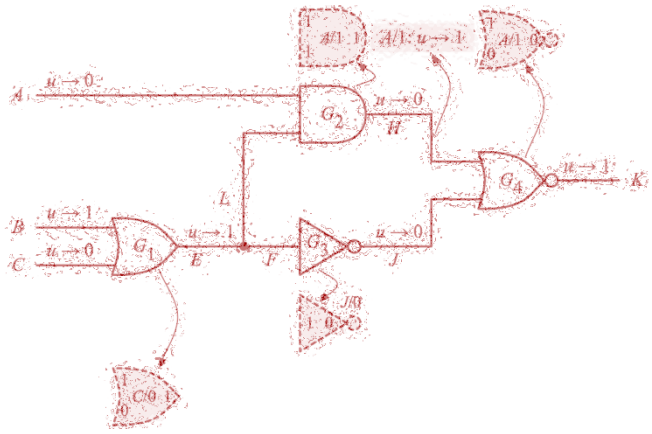






Summary

- **Parallel fault simulation (parallel in fault)**
  - **Run parallel logic simulation for W-1 faults**
  - **Fault injection by circuit modification**
- **Parallel Pattern Single fault Propagation (parallel in pattern)**
  - **Run parallel logic simulation for *W* patterns**



FFT

- Q1: Why parallel fault sim (*W*-1) faults, not *W* faults?
- Q2: Please compare parallel fault sim and PPSFP
- Q3: PPSFP is useful to comb. ckt only, how about sequential ckt?

	Parallel Fault	PPSFP
Applicable to delay fault model?		
Applicable to Sequential ckt ?		
When to drop fault ?		