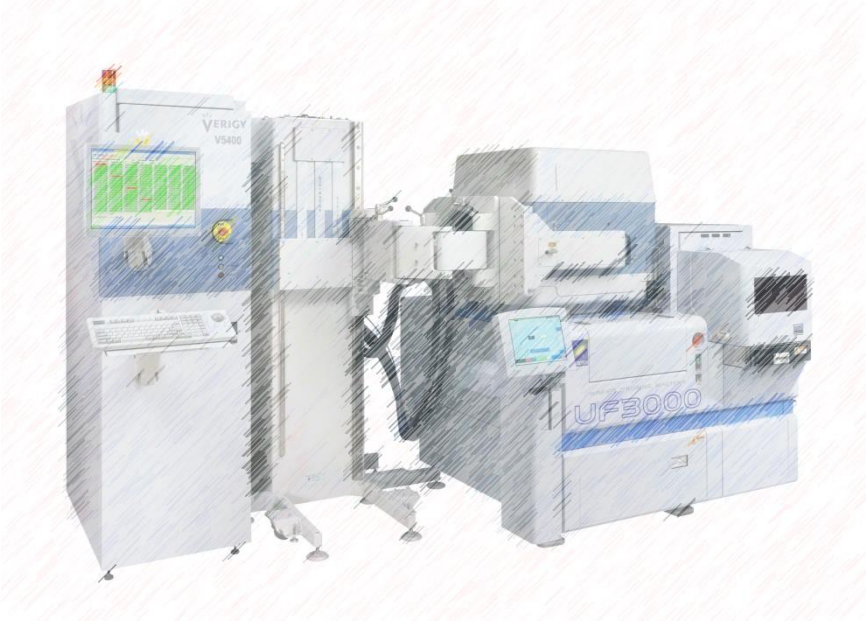
Introduction

- What Is Testing
- **Types of Testing**
- Test Quality
- Test Economics
- Issues in Testing
- Conclusion



Types of Testing

don't worry about names too much

- Testing (generally speaking)
  - Design Verification
  - **Explicit Testing**
    - Characterization Test
    - Production Test
      - Wafer Test
        - Gross Test
        - DC parametric Test
        - AC parametric Test
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        - Delay Test
        - Functional Test
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      - Package Test
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    - Reliability Test
      - Burn-in
      - Acc. Life test
    - Diagnosis Test
  - Implicit Testing Or On-line Testing

Why So Many Tests?

- Design errors → *Design Verification*
  - Logic design errors, physical design errors
- Manufacturing Defects → *Explicit Testing*
  - Mask problems, lithography problem
  - Particles or scratches
  - Bad manufacture recipe
- External or Environmental Disturbance → *Implicit Testing*
  - Electromagnetic interference
  - Alpha particles
  - Power supply disturbance
- Wear out → *Reliability Testing*
  - Electromigration
  - Corrosion

Focus of class

Because There Are Many Different Problems!

Classification of Explicit Testing

- According to purposes
  - *Production test:* for volume production
  - *Characterization test:* for prototype IC, silicon debug
  - *Reliability test:* for reliability defects
  - *Diagnosis test:* for identify defect location
- According to stages
  - *Wafer test* (aka. *Wafer sort, wafer probe*): on wafer
  - *Package test* (aka. *Final test*): after packaging
  - *System test*: in system
- According to test techniques
  - DC parametric test: VOH/VOL/VIH/VIL ...
  - AC parametric test: rise/fall time, operation frequency …
  - Boolean test : apply test patterns at low speed for DC faults
  - Delay test: apply test patterns at fast speed for delay faults
  - Functional test: apply design verification patterns
  - IDDQ test: measure quiescent power supply current
  - Low voltage test: test at reduced power supply voltage

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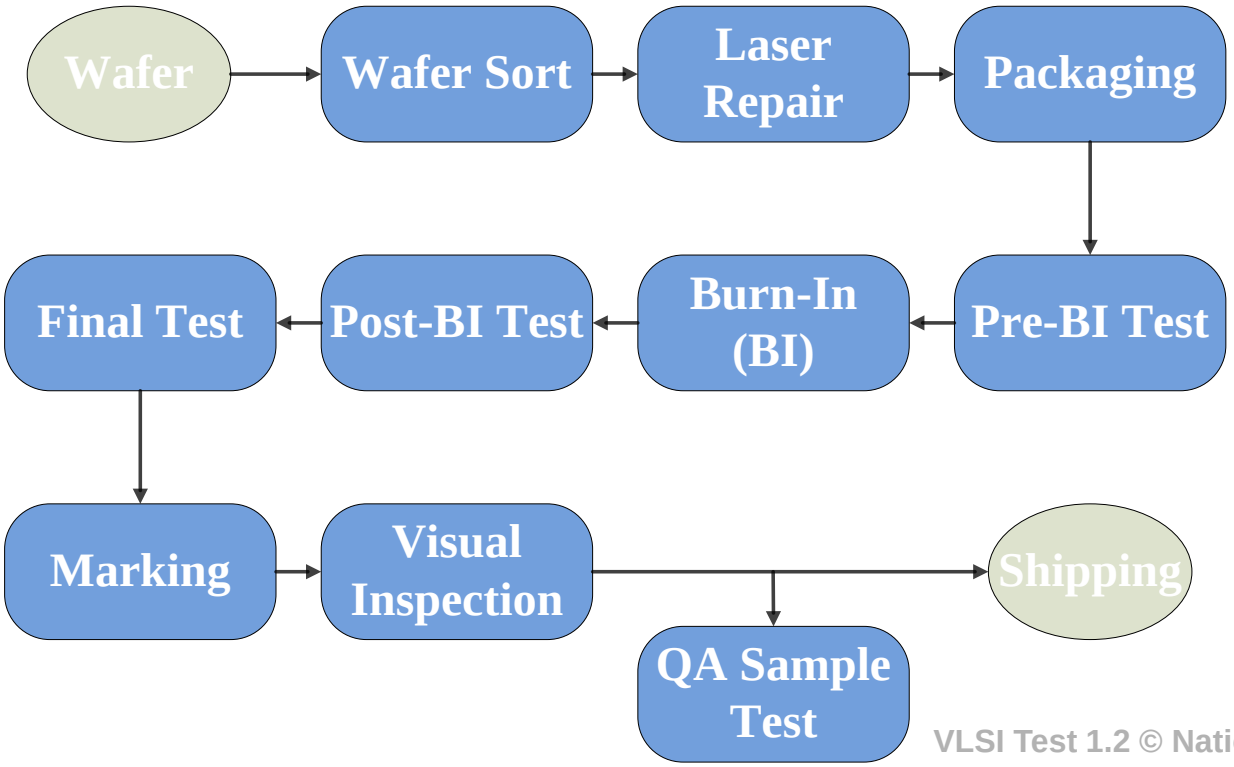
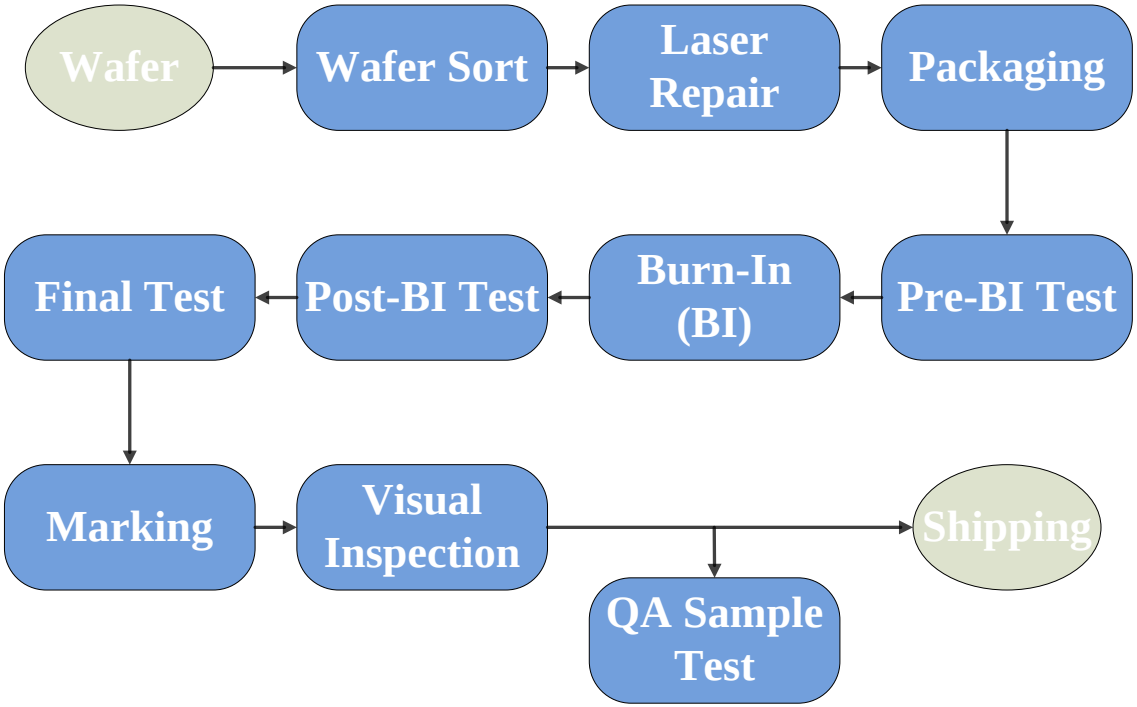
Production Tests

- Purposes:
  - 1. Enforce quality requirements before selling to customers
  - 2. Sort parts for different specifications
    - *e.g.* different speeds of CPU
- Example: a typical production test flow
  - actual flow modified according to test cost and test quality requirements



Food for Thought, FFT

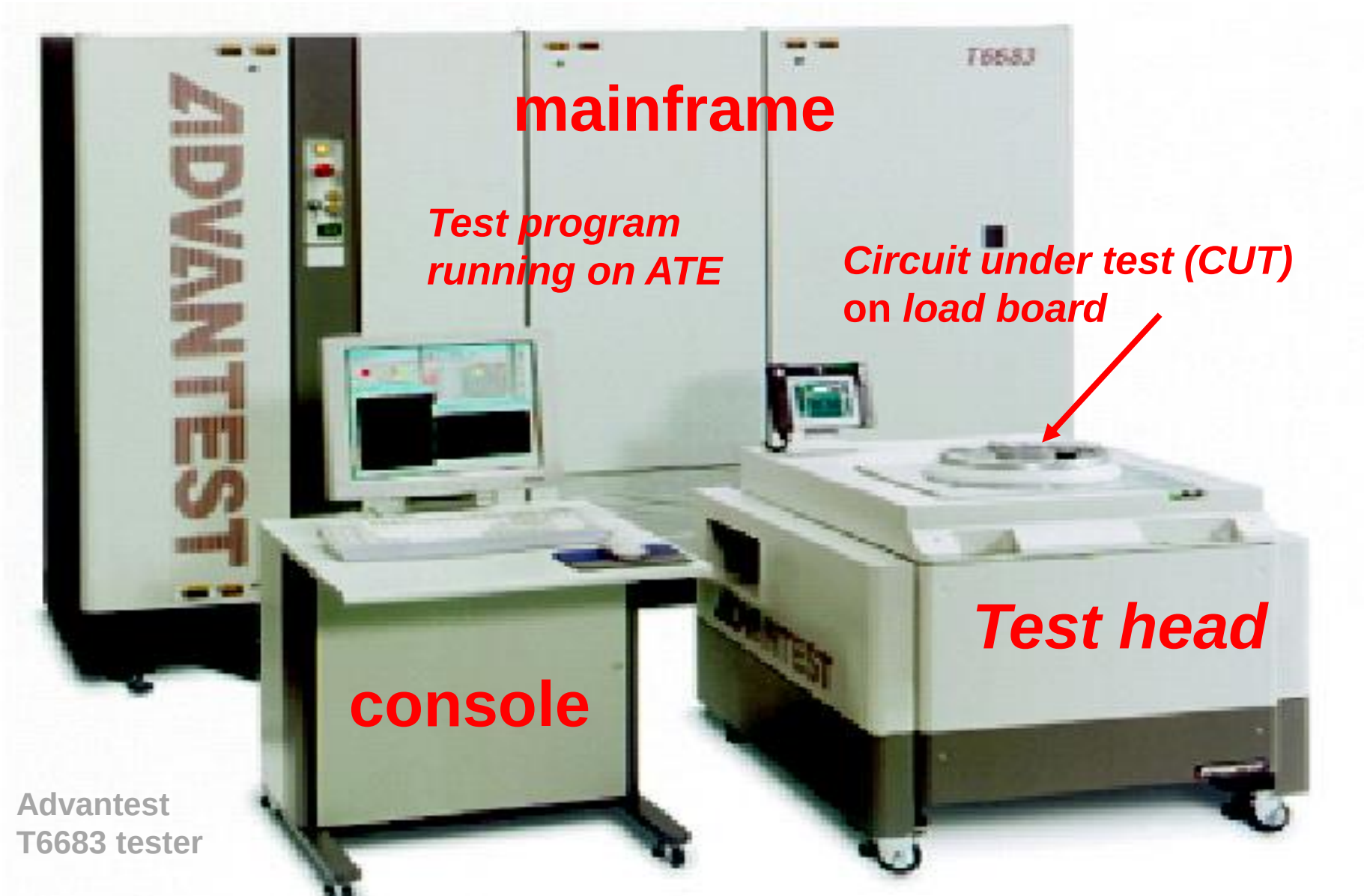
- **Q: If we already have wafer test, why package test again?**



Production Test Floor

Source: micron.com

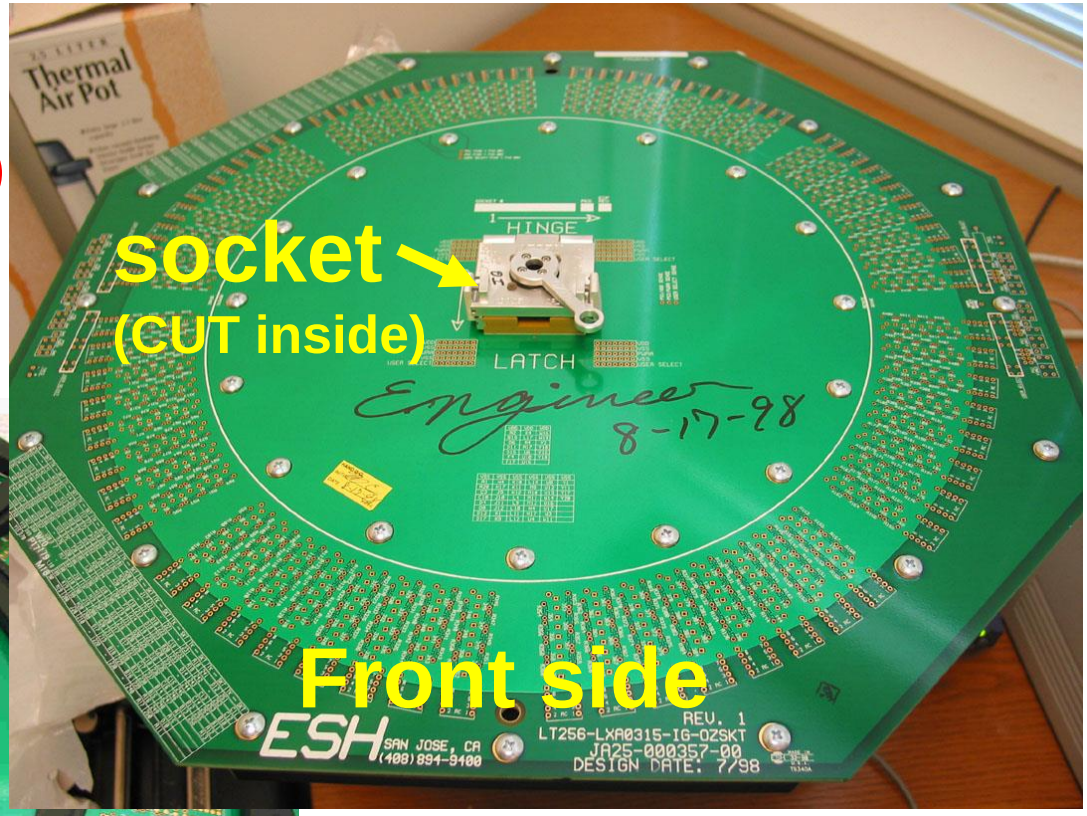
Automatic Test Equipment (ATE), Tester



Advantest
T6683 tester

Load Board

- Test fixture to interface
  - ATE and
  - *circuit under test (CUT)*



Handler

- Robotic arm (inside) for moving packaged IC
- <Video demo>

Advantest
M4541A handler

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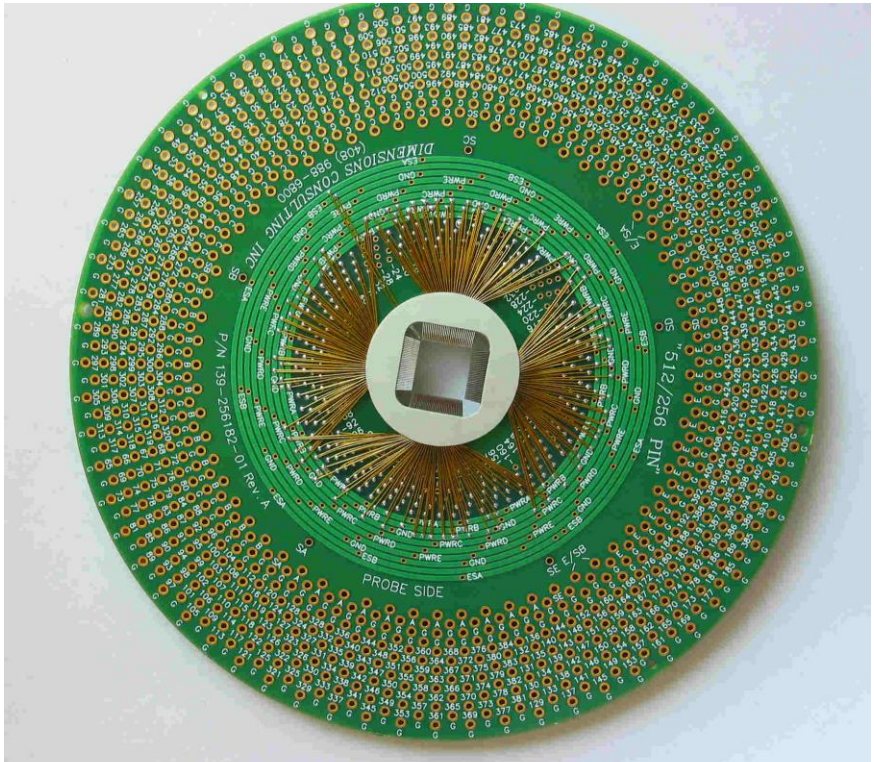
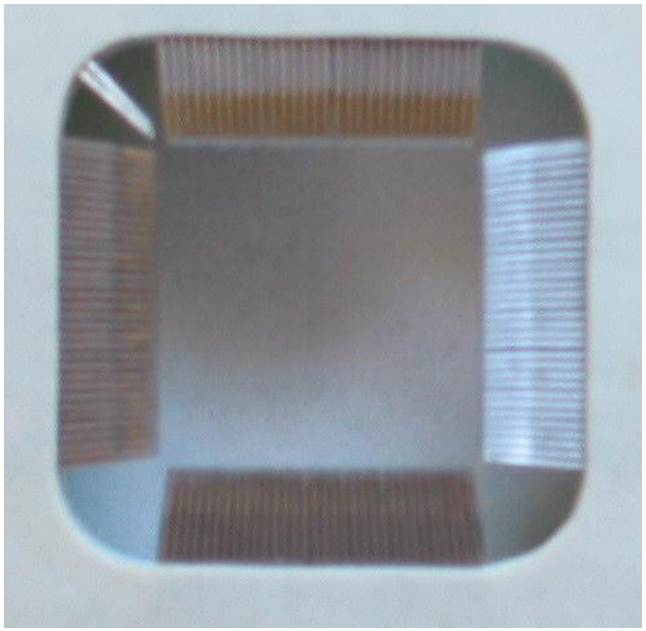
Wafer Test Setup

- **Source: Verigy.com**

Probe Card

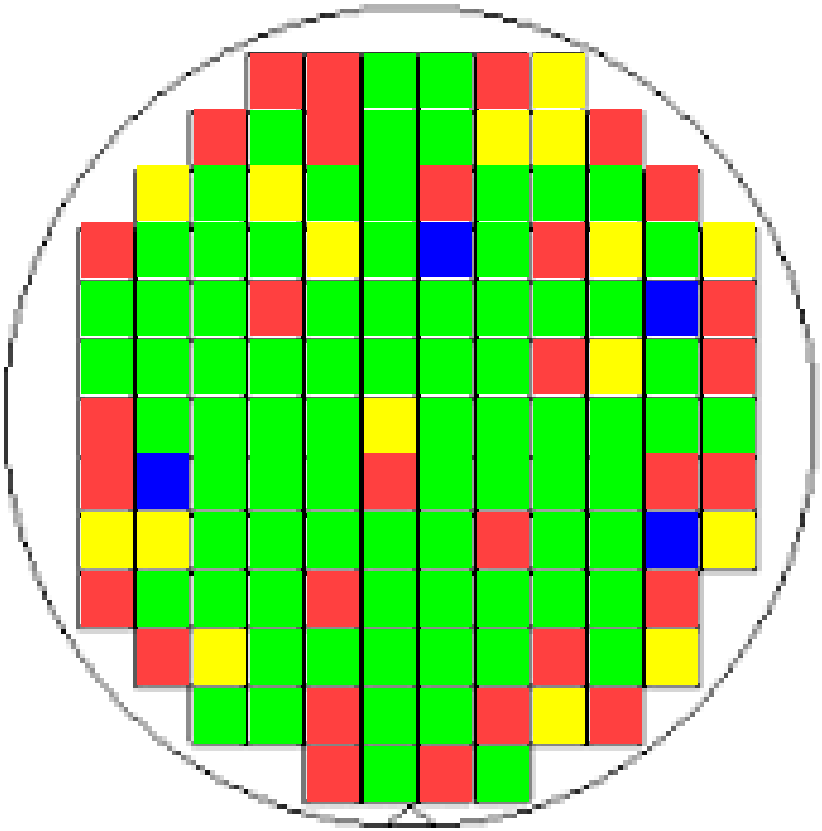
- Test fixture to interface load board and die
- Signal integrity is a big concern
  - Many tiny needles contacting die, cannot probe at fast speed
  - Must carefully balance inductance and capacitance of each pin
  - Need regular cleaning after a numbers of *touch downs*
- Probe card wears out quickly so it should be replaced regularly





Wafer Map

- Why we call it *wafer sort*?
- *Wafer map* shows test results
  - Die are sorted into different *Bins*
- Example:
  - Bin #1: PASS ALL
  - BIN #2: FAIL FUNCTION test
  - BIN #3: FAIL IDDQ test
  - BIN #4: FAIL DC parametric test
- Wafer map very useful for
  - pass/fail decision
  - diagnosis
  - yield improvement



Yield=Bin#1/total = 78/130=60%

Video Clip

- You can see a typical production test environment
- youtube video
  - “DELTA Test solutions since 1976”
  - https://www.youtube.com/watch?v=yKl71IX8Zc0

- Terminology
  - Probe Station =Wafer prober
  - Component test = Package test
  - Electro Anti-static

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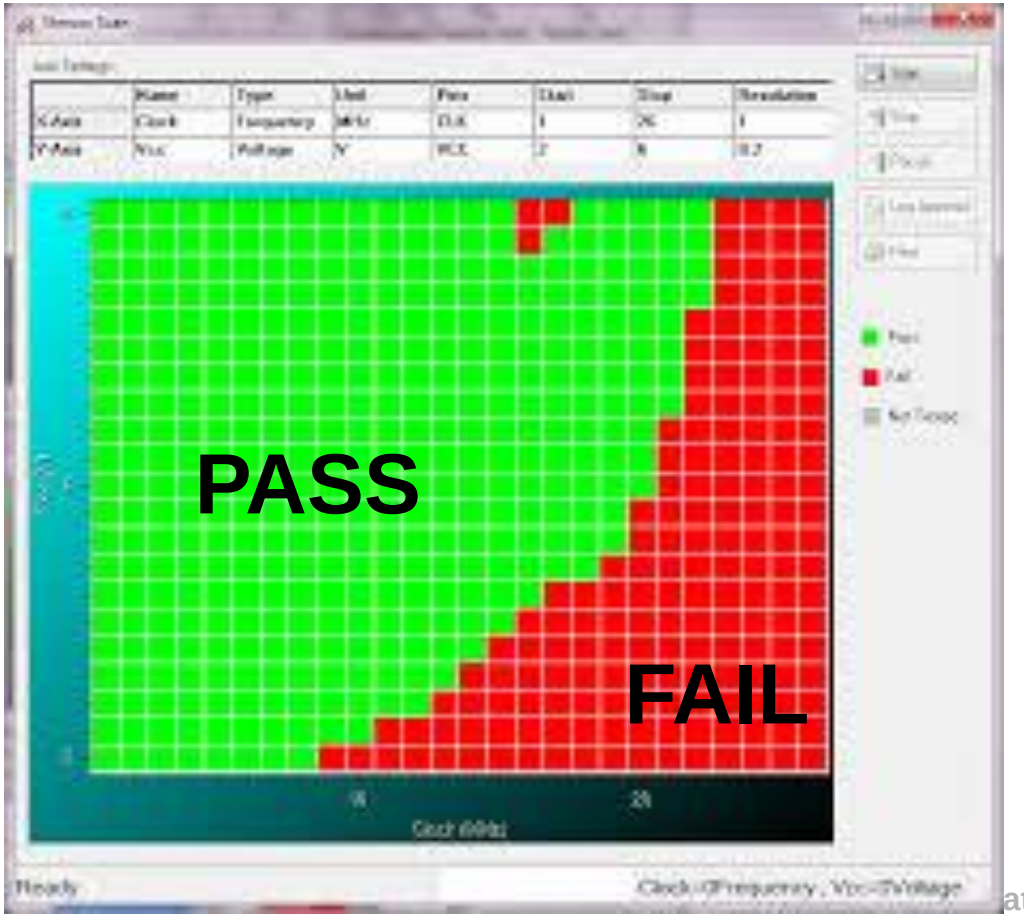
Characterization Tests

- Test a small amount of prototype IC very thoroughly
  - Test cost and test time are not big concerns
- Purpose of characterization test
  - 1. Verify IC function is same as design (silicon debug)
  - 2. Confirm IC specifications under different test conditions
    - Specifications: speed, VOH/VOL, rise/fall time …
    - Conditions: VDD, Temperature …
  - 3. Developing test program for production test
    - Determine Pass/Fail limits

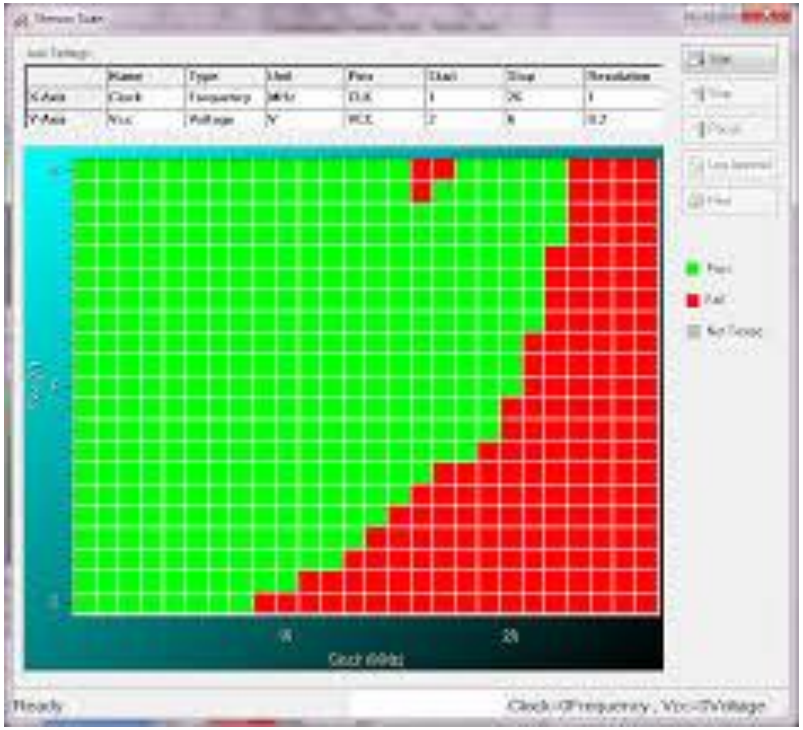
Shmoo Plot

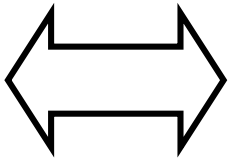
- Graphical display of CUT test results under different test conditions
- Example: clock period vs. VDD
  - Green = PASS ; Red = FAIL

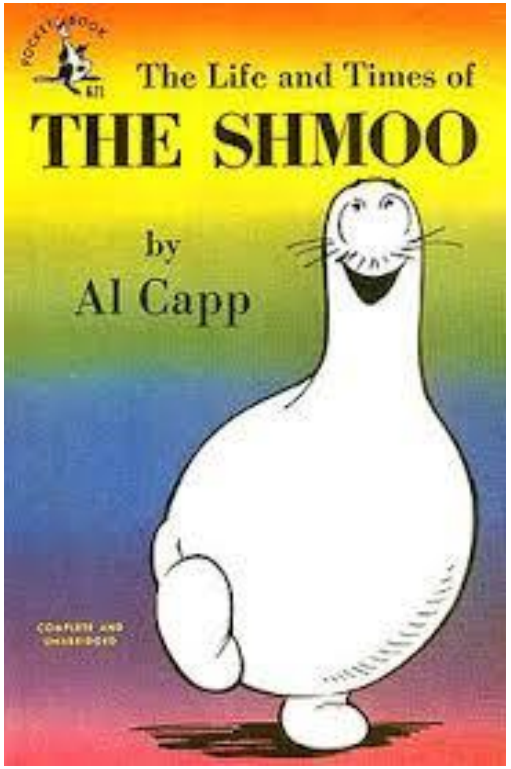


Why Shmoo?

- Funny shape resembles a cartoon character: shmoo
  - Youtube Video: 1979 NBC Cartoon







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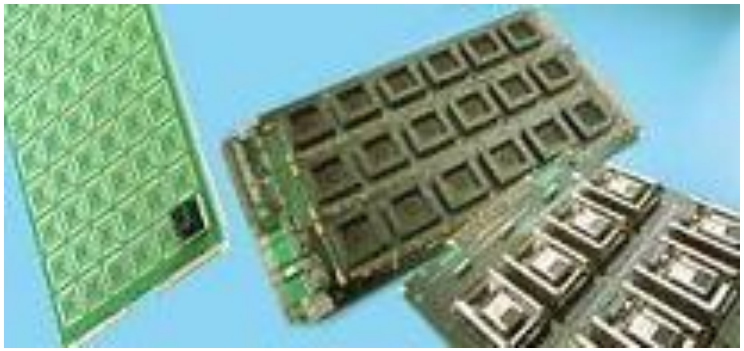
Reliability Tests

- *Burn-in*
  - Goal: screen out *infant mortality* (aka. *Early-life failure*)
  - Method: raised temperature and voltage for hours or days
    - cook IC in oven!
  - Very costly. Only applied to expensive IC
- *Accelerated life test*
  - Goal: estimate life time of IC
  - Method: burn-in until IC are dead
  - Only applied to sampled IC

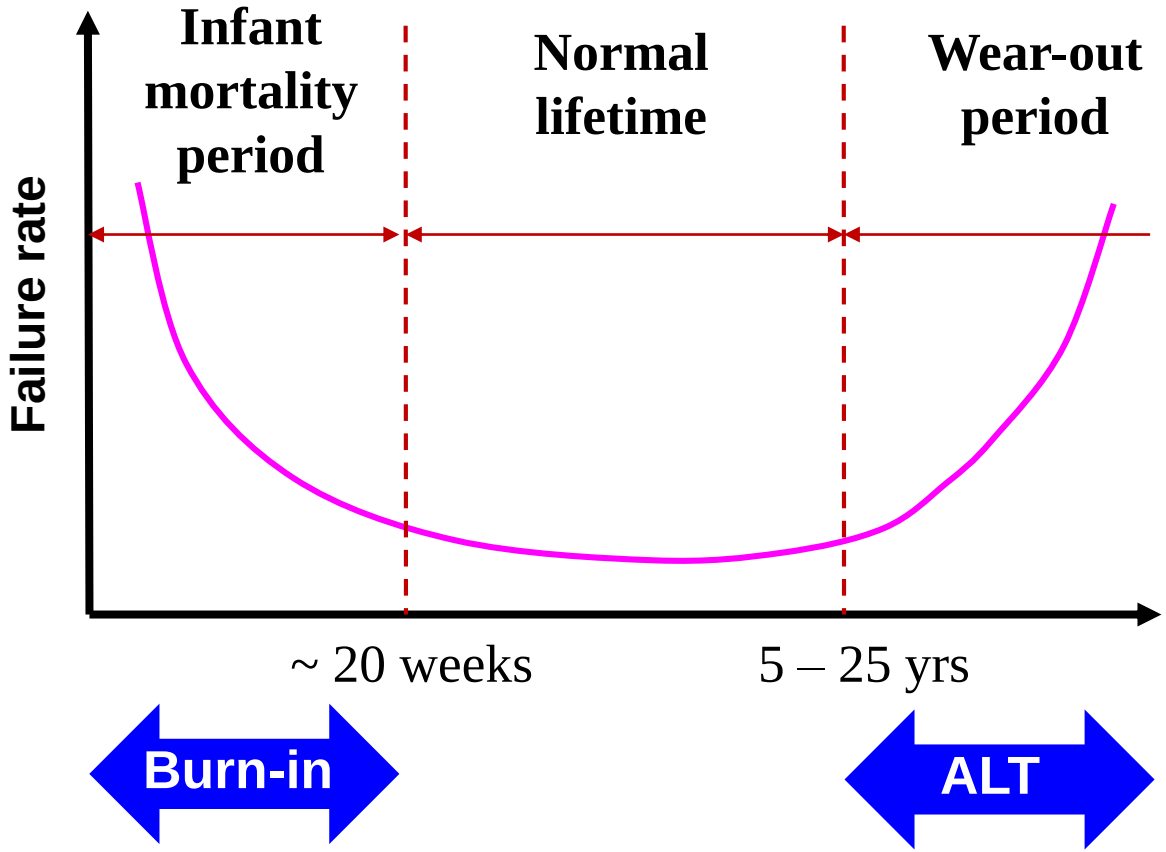


Burn-in board

Burn-in oven siliconfareast.com

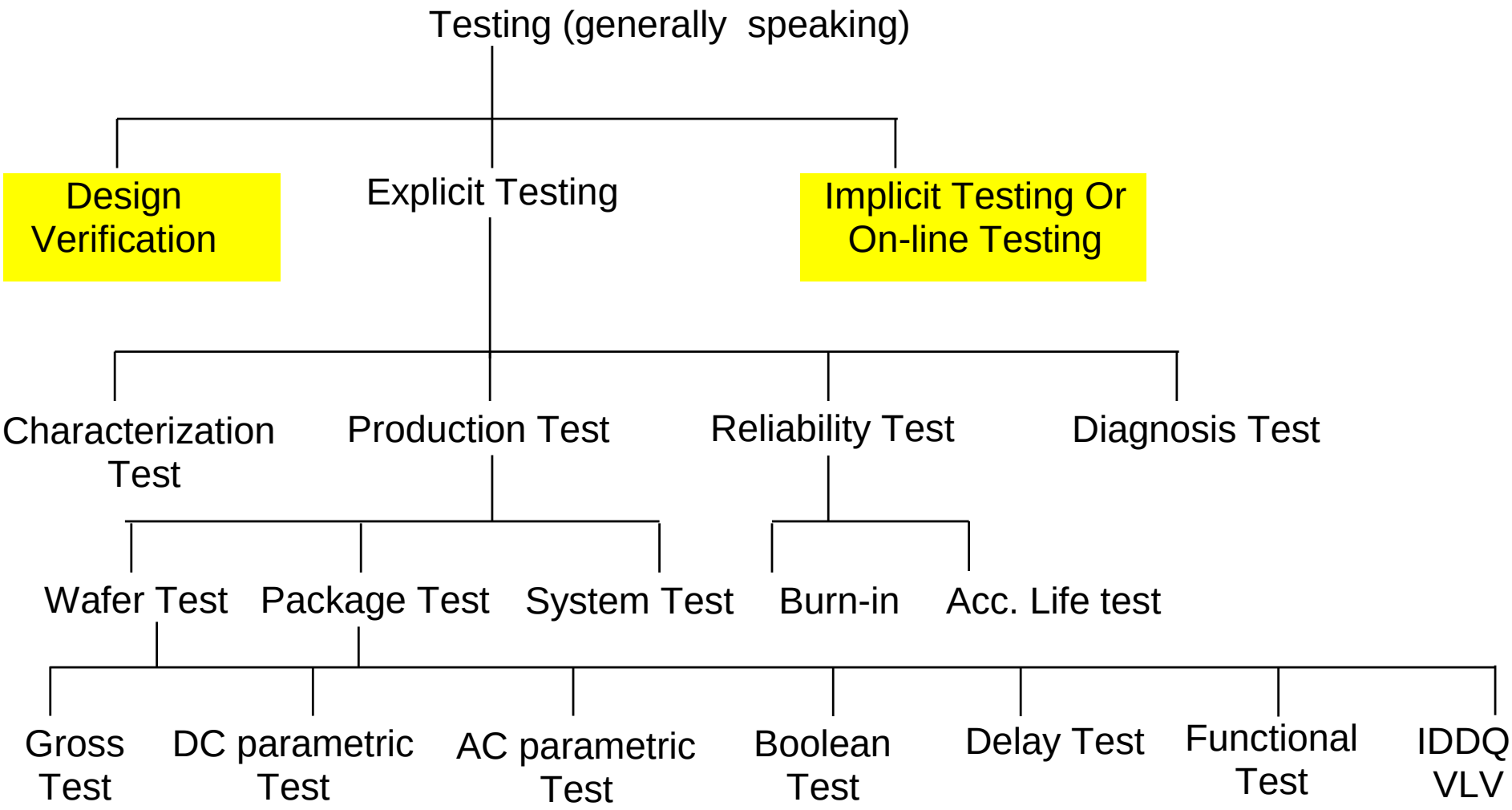
Bathtub Curve

- IC's *failure rate** resembles a bathtub
  - *Infant mortality*: fail early in life, due to *reliability defects*
  - *Wear out*: normal life time, due to *aging*



*Failure Rate = percentage of failures in a period of time

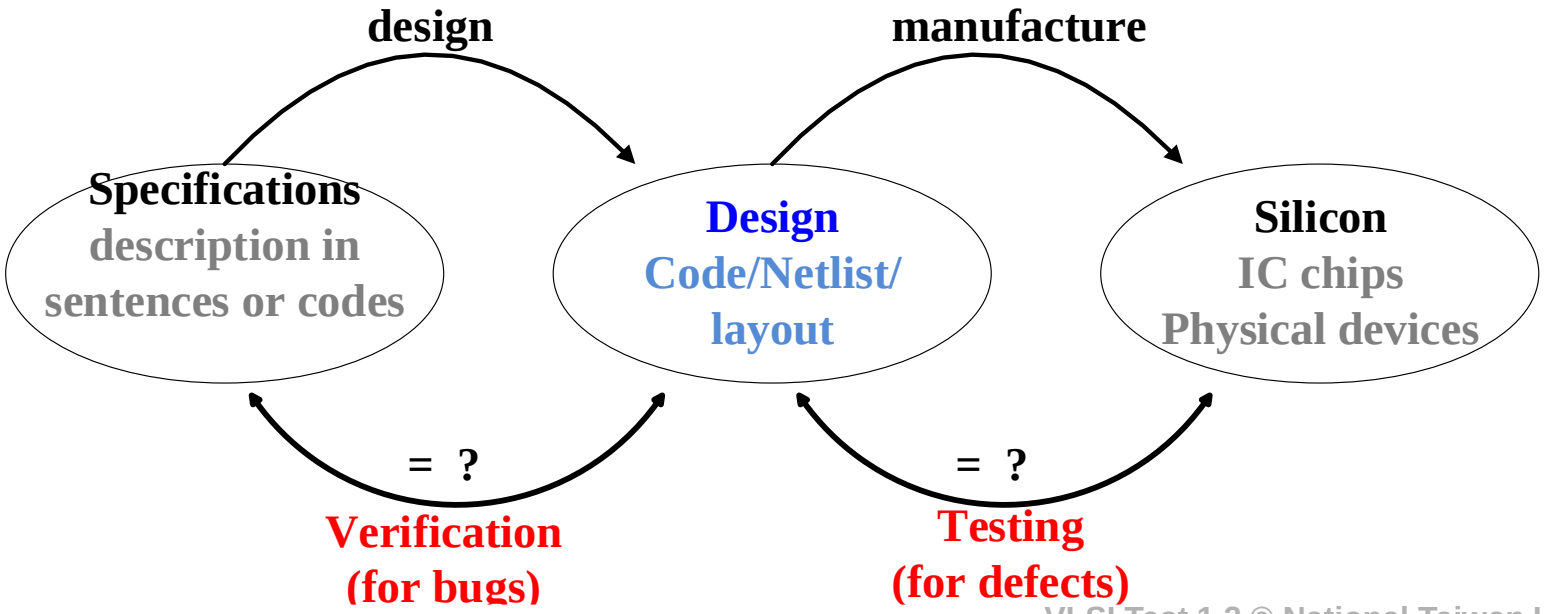
Types of Testing



These Topics Are NOT in This Course

Explicit Testing ≠ Verification

- *Verification*
  - Purpose : check if design correctly implements specified behavior
  - Done *before* manufacture to catch design errors (*bugs*)
  - Approaches: simulation, formal verification, …
- *Explicit testing*
  - Purpose: check if IC is functioning correct or defective
  - Done *after* manufacture to catch *defects*
  - Approaches: apply test patterns by tester, …



Implicit Testing

- **Purpose**
  - **Check IC output correctness during normal operation**
- **Also known As (aka):**
  - ***Concurrent Error Detection* (CED)**
  - ***On-line testing***

- **Important for mission critical systems**
  - **Airplanes, satellites, mainframe computers**

- **Techniques**
  - **Circuit level techniques**
    - ***Error Correction Code* (ECC) protection of memory**
  - **System level techniques**
    - ***Watch dog timer***

Summary

- **Focus of this course: explicit testing**
  - **Off-line IC testing on a specialized tester**
  - **Explicit testing ≠ verification ≠ on-line testing**
- **Many different type of tests for different**
  - **Purposes**
  - **Stages**
  - **Techniques**