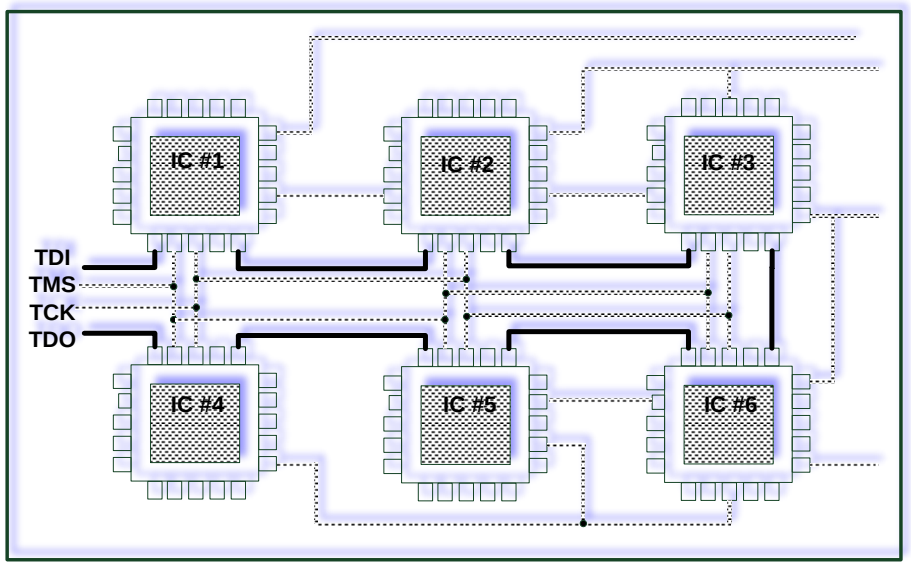
DFT – Part 2

- Introduction
- Components of JTAG
- JTAG Instructions
  - Mandatory Instructions
  - Optional Instructions
- Conclusion

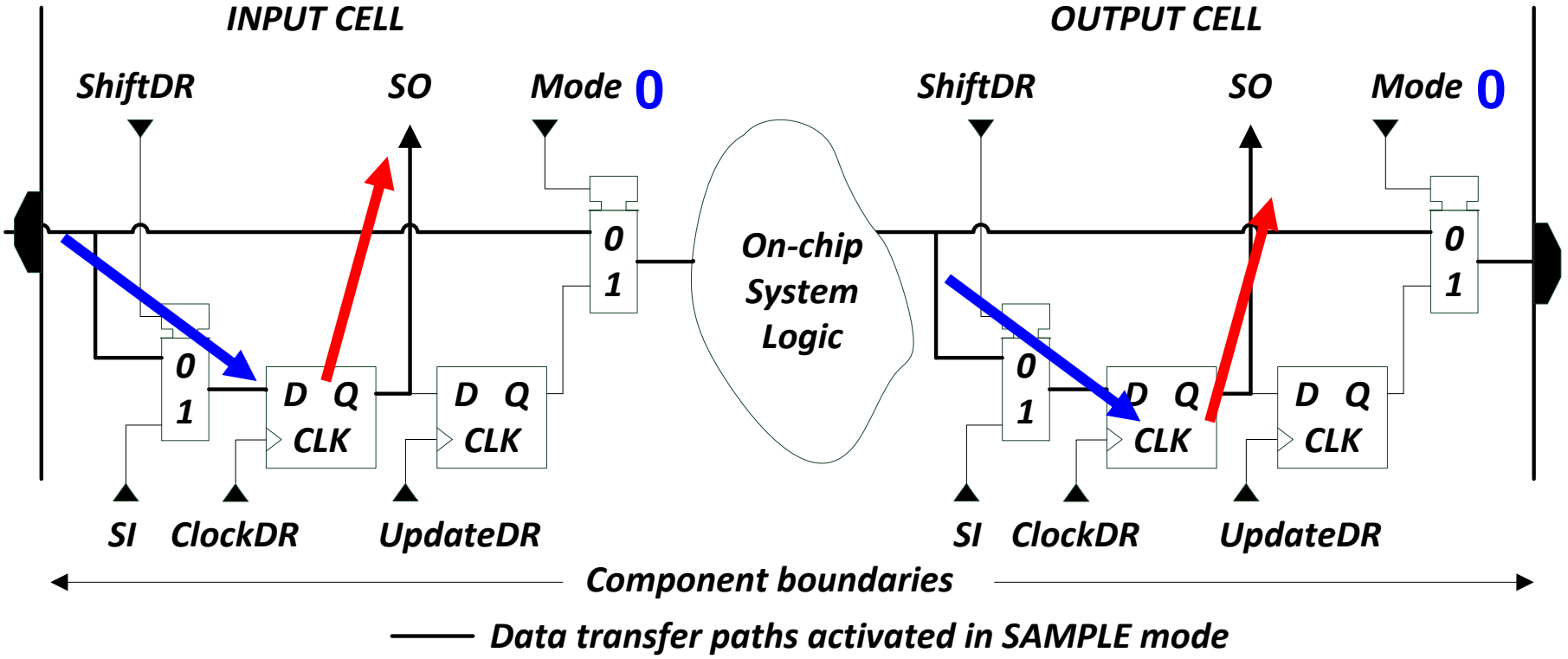


Mandatory Instructions

- EXTEST (000...0)
  - Selects Boundary-Scan Register, External Test
- BYPASS (111...1)
  - Selects Bypass Register
- **SAMPLE/PRELOAD (instruction code decided by designer)**
  - **SAMPLE: Take snapshot of system I/O pins**
  - PRELOAD: Control system I/O pins

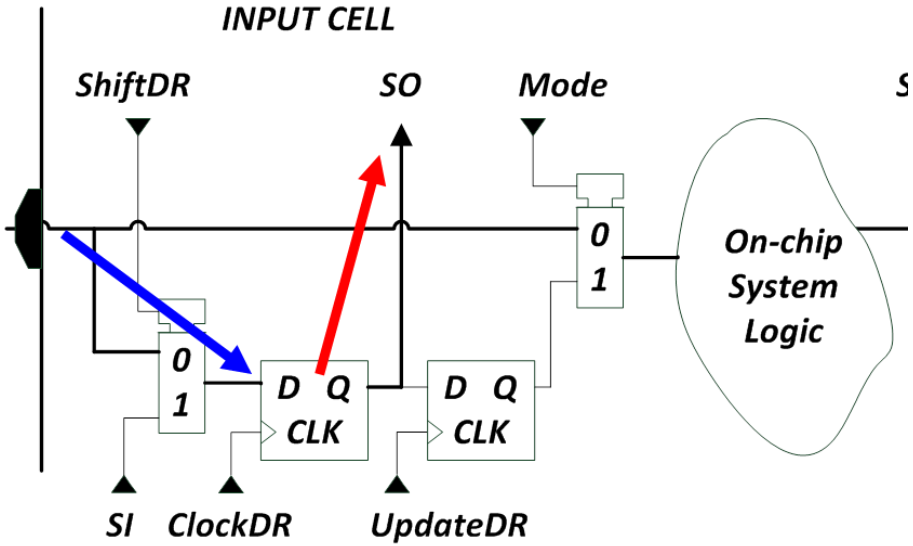
SAMPLE (1/3)

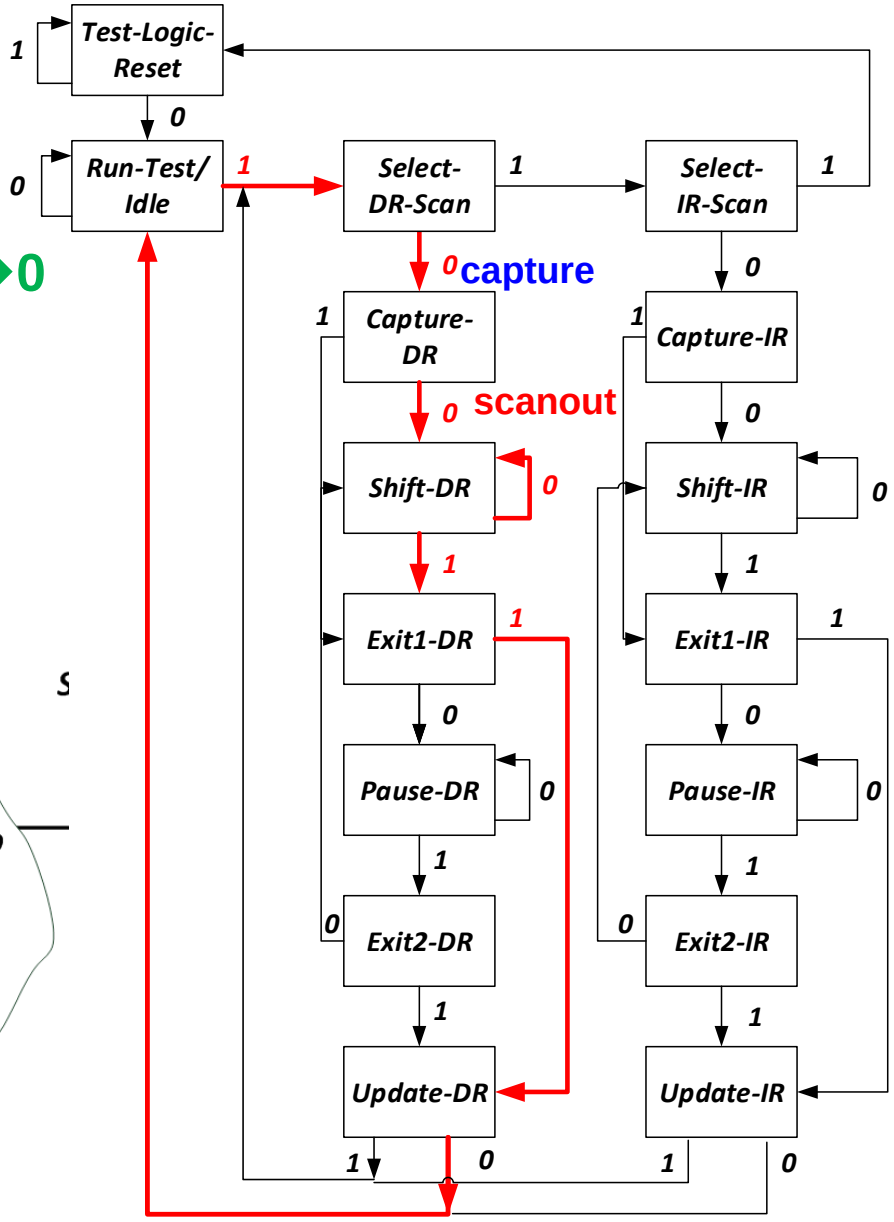
- Step1: Capture: ShiftDR=0, ClockDR
- Step2: Scan out: ShiftDR=1, ClockDR …
- Mode = 0 to isolate system logic
  - Does not interfere with normal operation of system logic



SAMPLE (2/3)

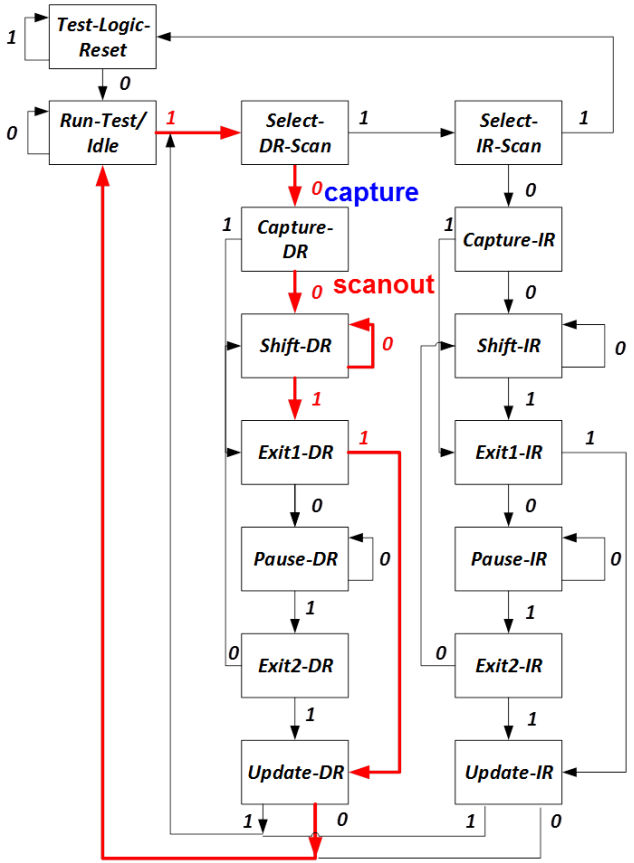
- After instruction loaded
  - Start from Run-test/Idle
- TMS = 1->0->0->0.....0→1→1→0
  - Ends at Run-test/Idle



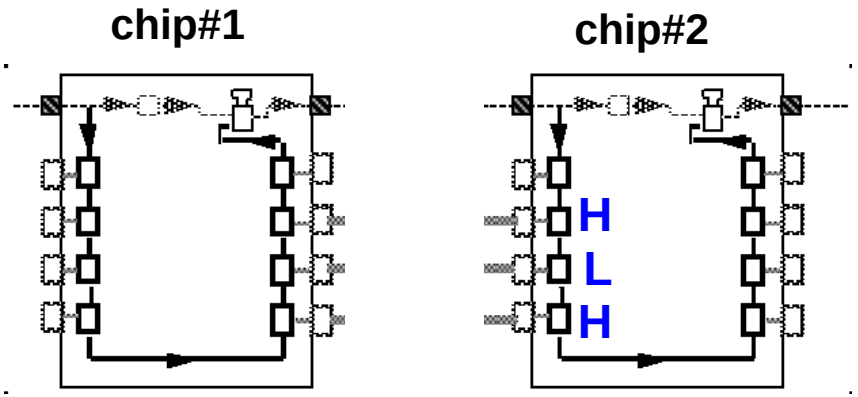


SAMPLE (3/3)

	Capture		Scan out	
TMS	10	0	0000 0000 0000 0000	110
TDI				
TDO			xxxx **HLH**x xxxx xxxx	
Final state	Capture-DR		Shift-DR	run-test/Idle



(assume instruction code already loaded)

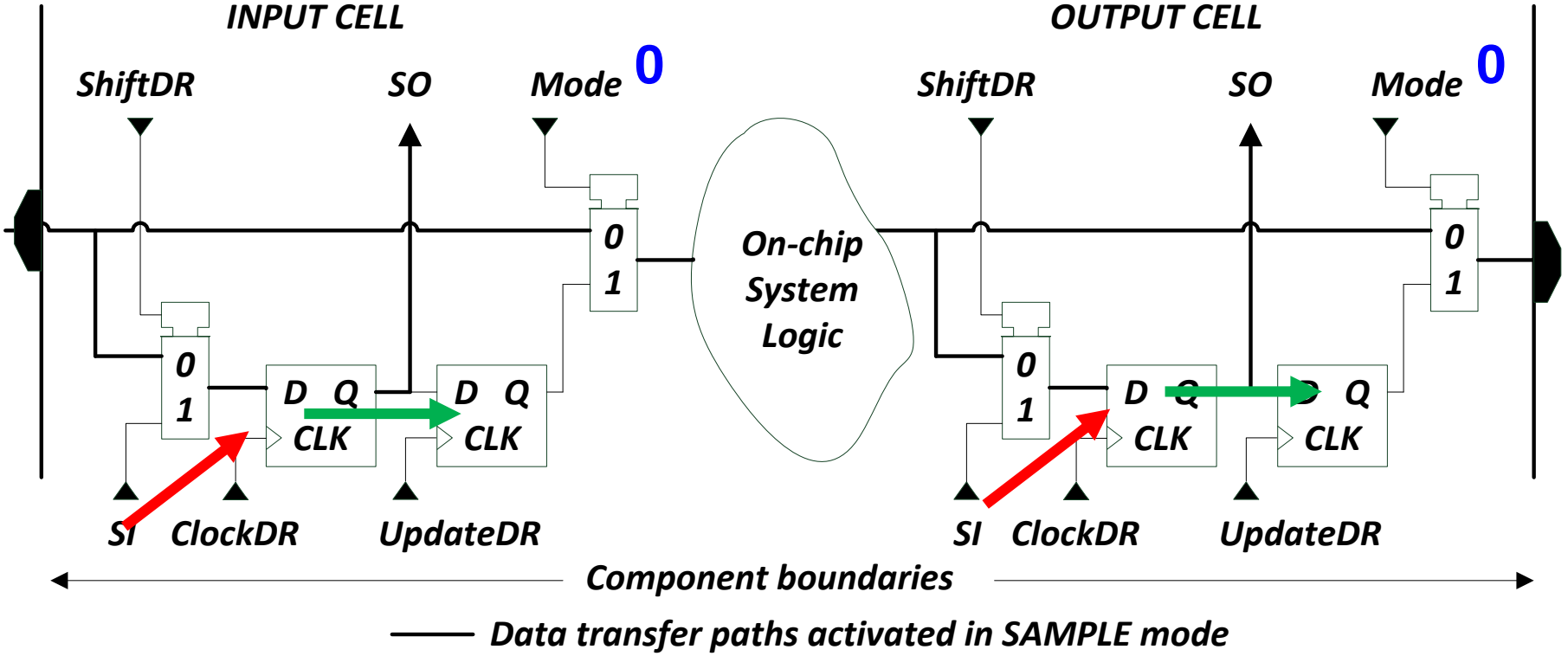


Mandatory Instructions

- EXTEST (000...0)*
  - Selects Boundary-Scan Register, External Test
- BYPASS (111...1)
  - Selects Bypass Register
- **SAMPLE/PRELOAD (instruction code decided by designer)**
  - SAMPLE: Take snapshot of system I/O pins
  - **PRELOAD: Control system I/O pins (by output FF of BSC)**

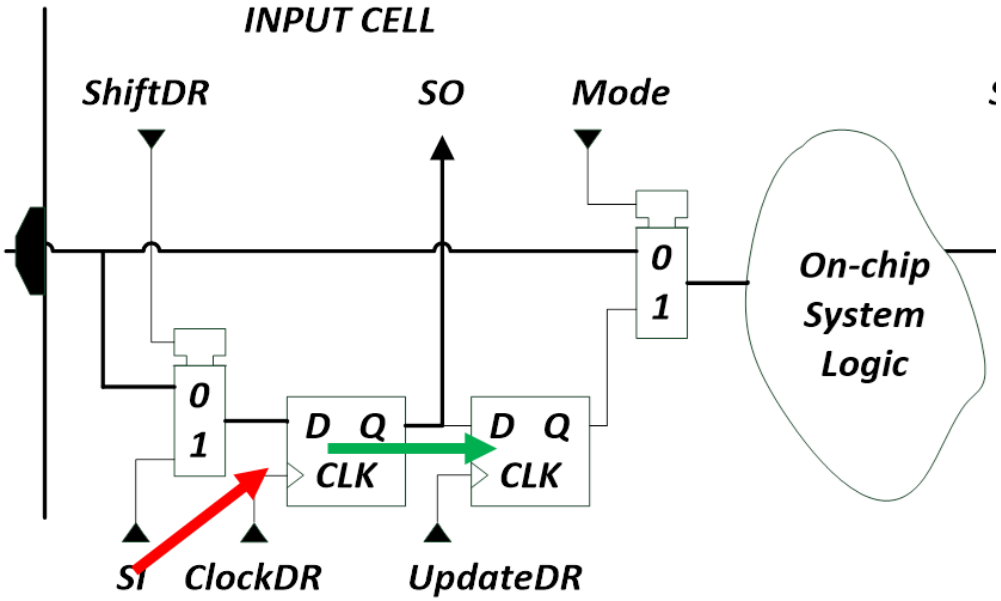
PRELOAD (1/2)

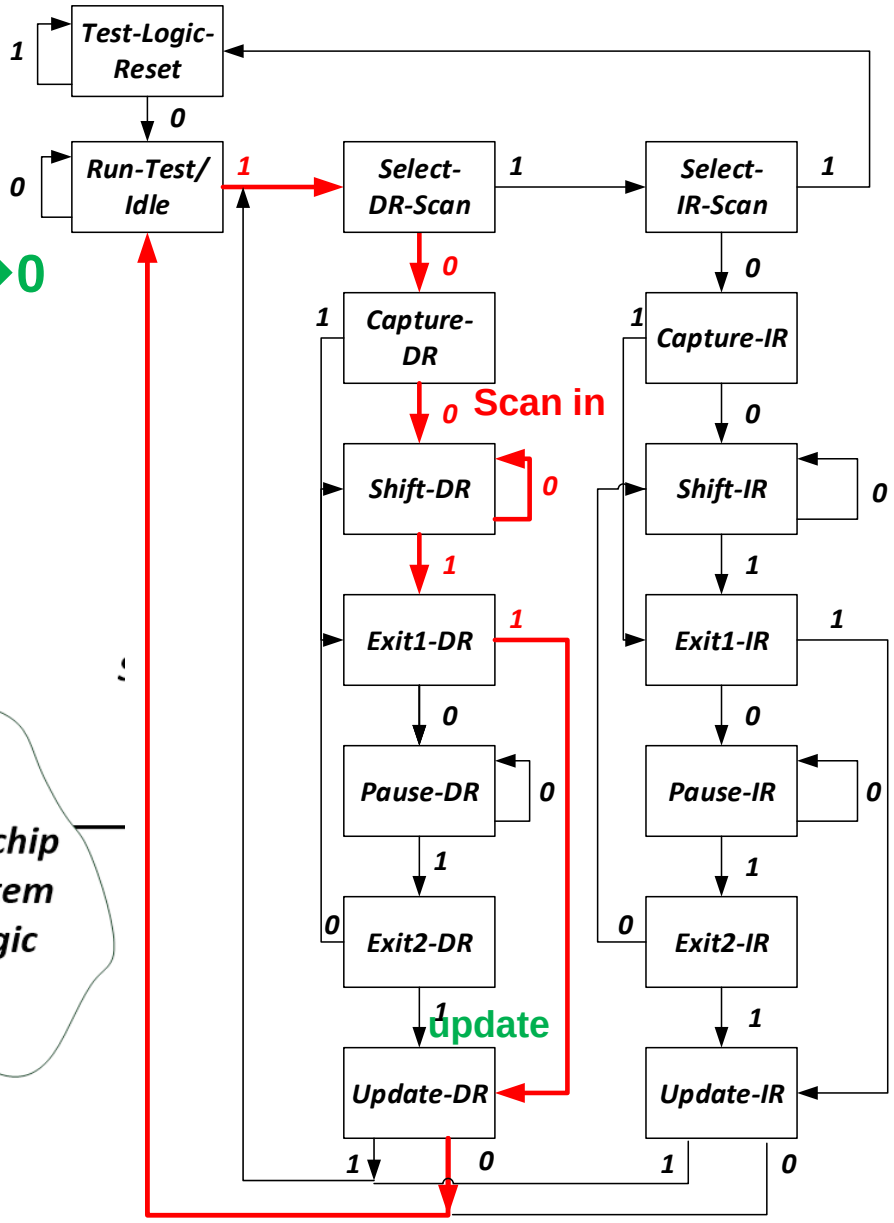
- Step1: Scan in: ShiftDR=1, ClockDR…
- Step2: Update: UpdateDR
- Mode = 0 to isolate system logic



PRELOAD (2/2)

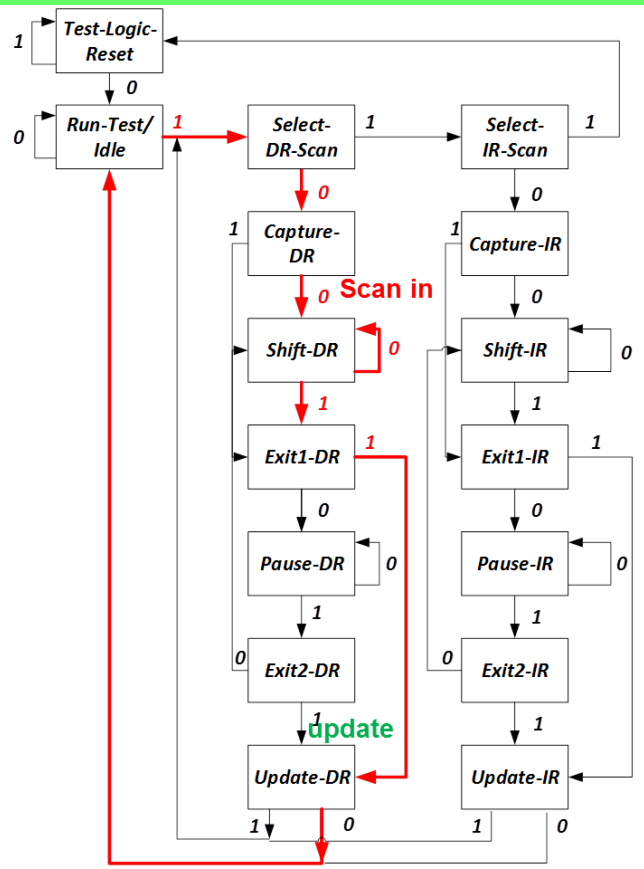
- After instruction loaded
  - Start from Run-test Idle
- TMS = 1->0->0->0.....0→1→1→0
  - Ends at Run-test/Idle



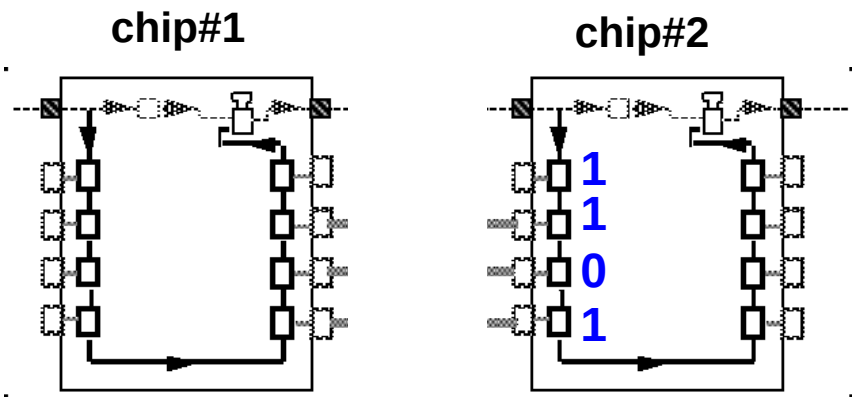


Quiz

			Scan in	Update
TMS				
TDI				
TDO				
Final state	Capture-DR		Shift-DR	run-test/Idle



Q: Suppose we want to preload chip #2 by '1011'.Please fill in blanks. (assume instruction code already loaded)



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  - Mandatory Instructions
  - Optional Instructions
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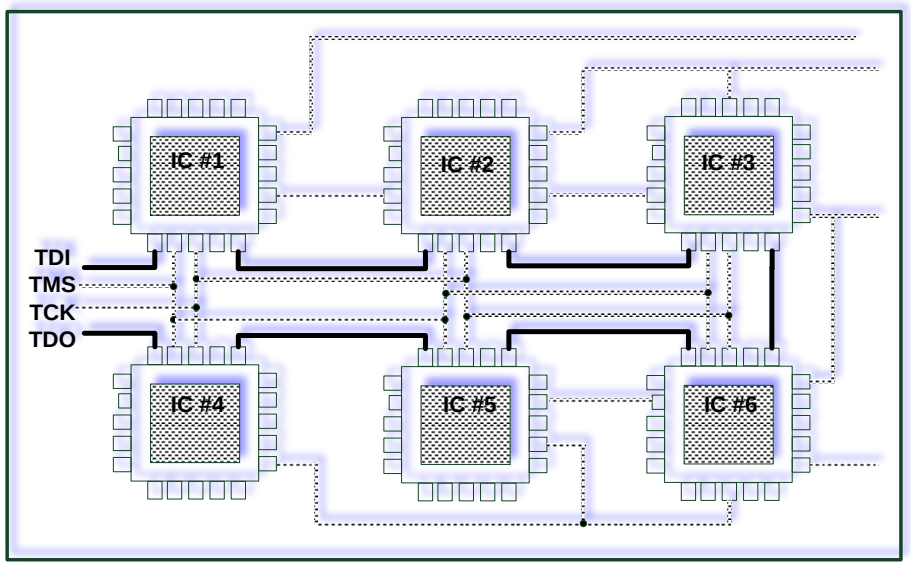
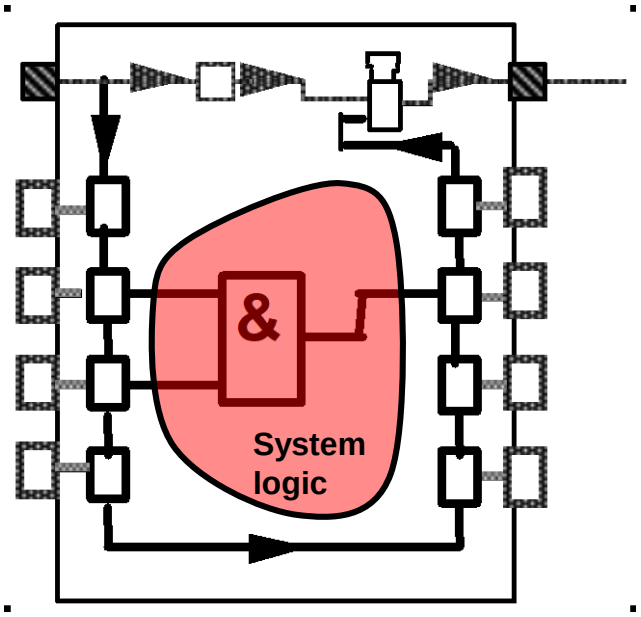


Optional Instructions

- **INTEST**
  - **Selects Boundary scan register. Internal test of system logic**
- **RUNBIST**
  - **Runs built-in self-test (BIST)**
- **IDCODE**
  - **Selects device identification register**
- **Design Specific**
  - **Designer's Choice**

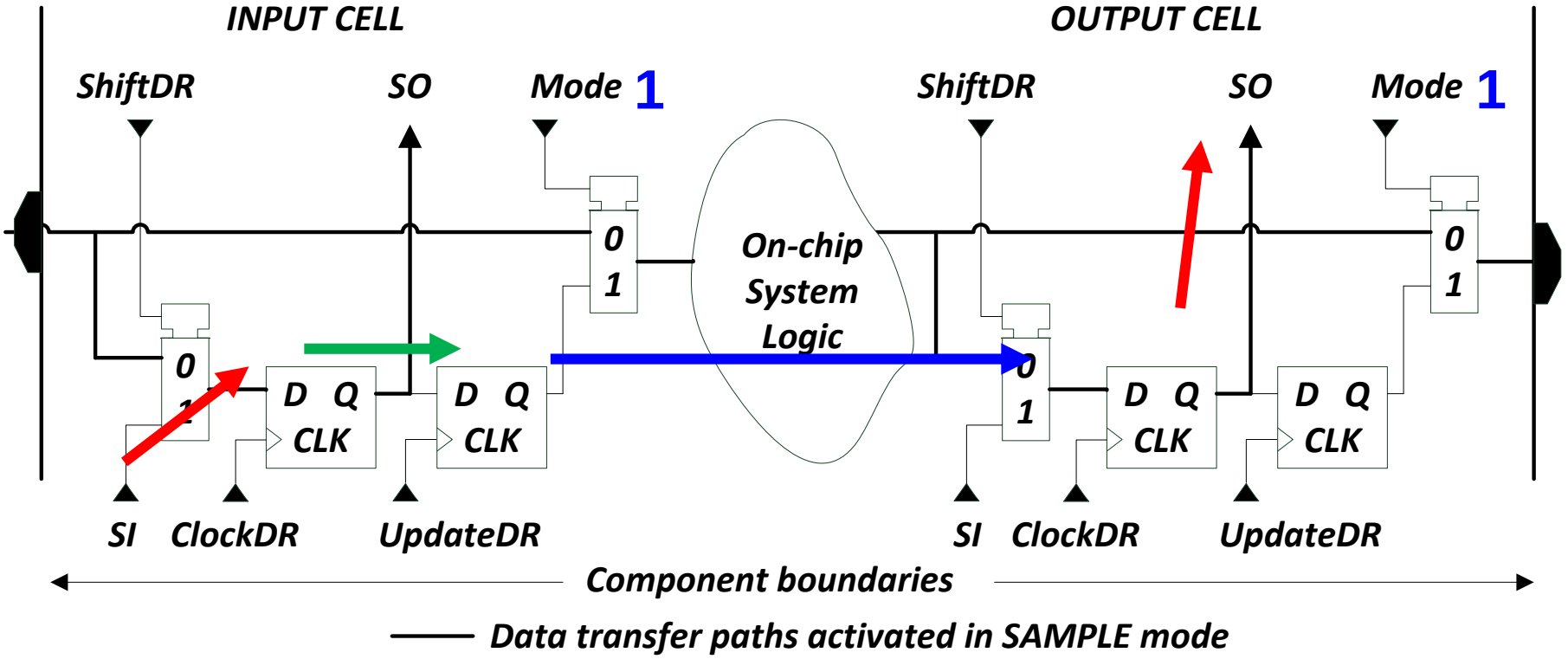
INTEST (1/4)

- **Purpose: Test on-chip system logic**



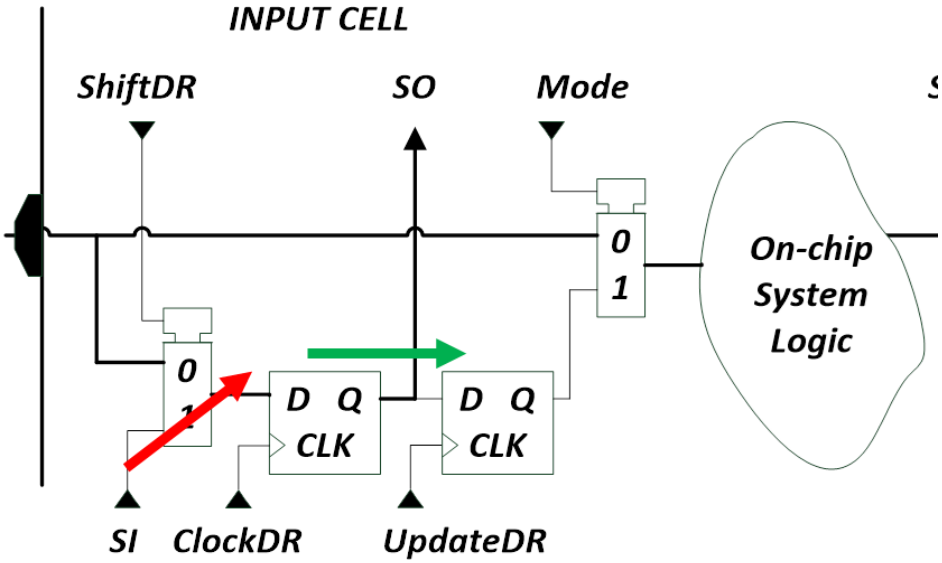
INTEST (2/4)

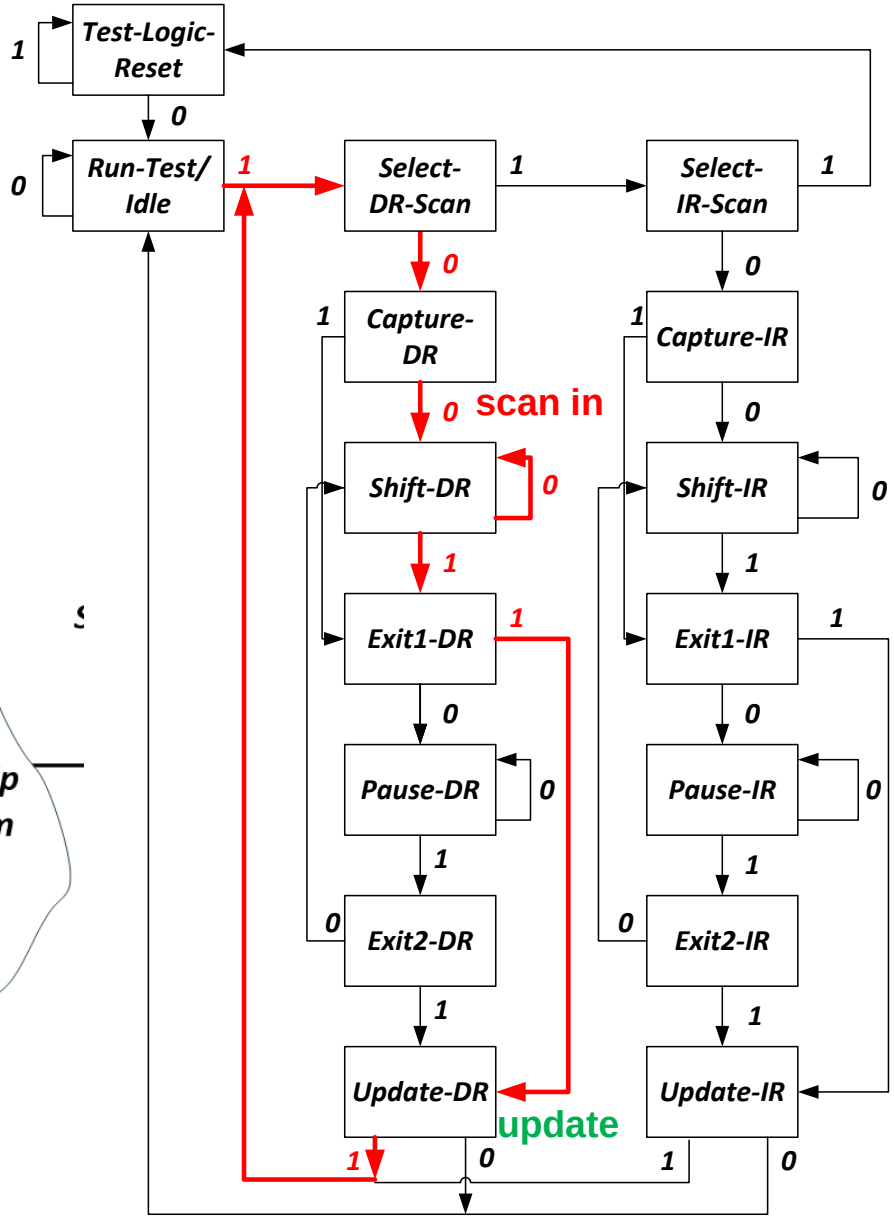
- Step 1: Scan in: ShiftDR=1 ClockDR …
- Step 2: Update Input BSR: UpdateDR
- Step 3: Capture Output BSR: ShiftDR=0 ClockDR
- Step 4: Scan out: ShiftDR=1 ClockDR …
- Mode = 1



INTEST (3/4)

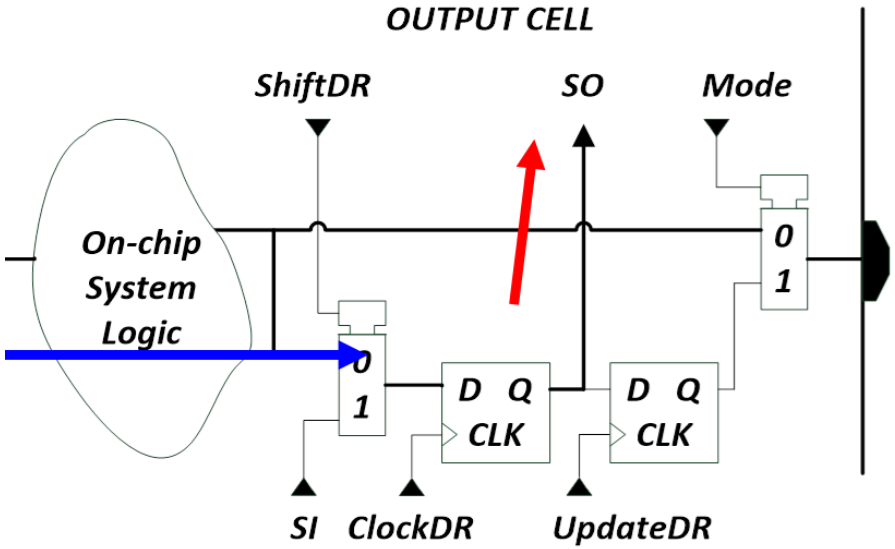
- After instruction loaded
  - Start from Run-test/Idle
- TMS = 1→0→0→0…0→1→1→1

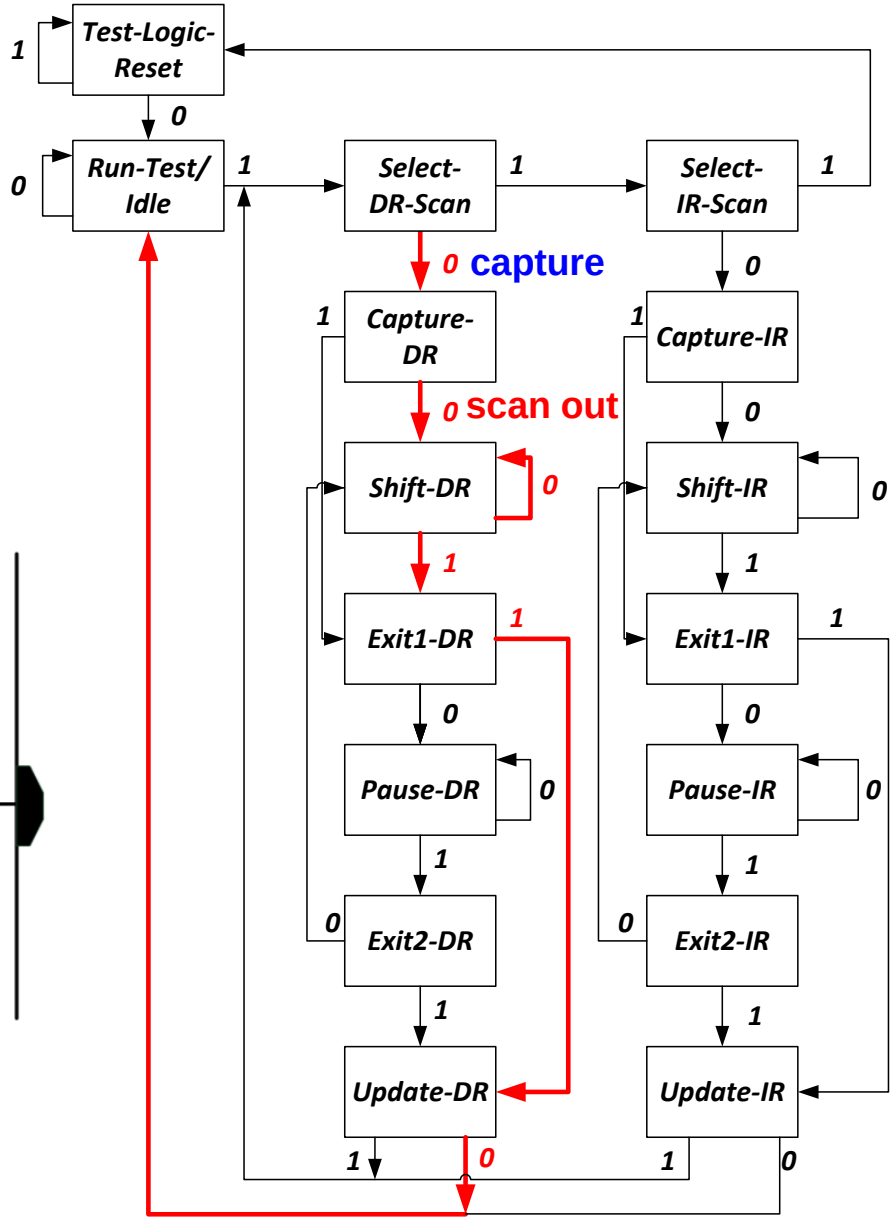




INTEST (4/4)

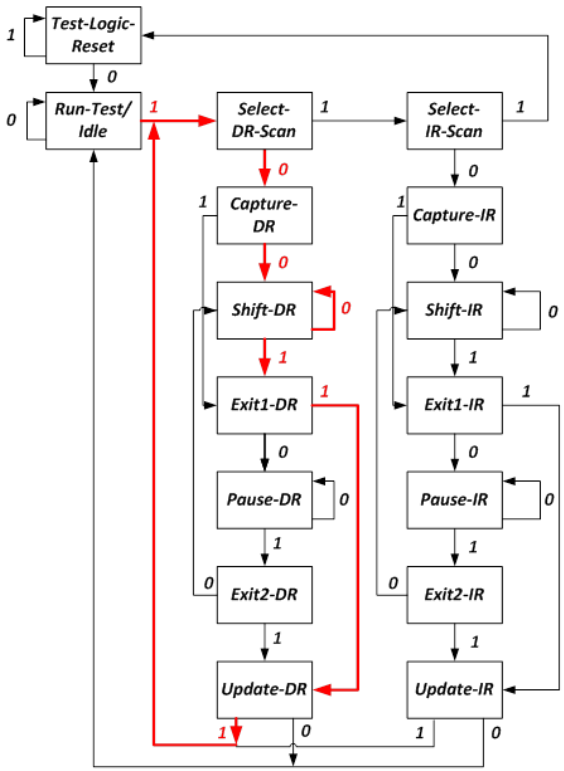
- TMS = 0→0→0…0→1→1→0
- Ends at Run-test/Idle



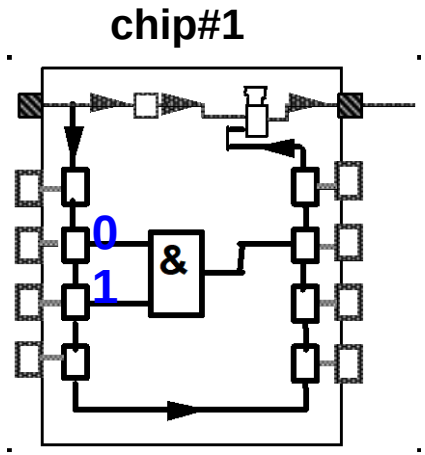


Quiz

			Scan in	Update Capture	Scan-out
TMS					
TDI					
TDO					
Final state	Capture-DR		Shift-DR		Run-test Idle

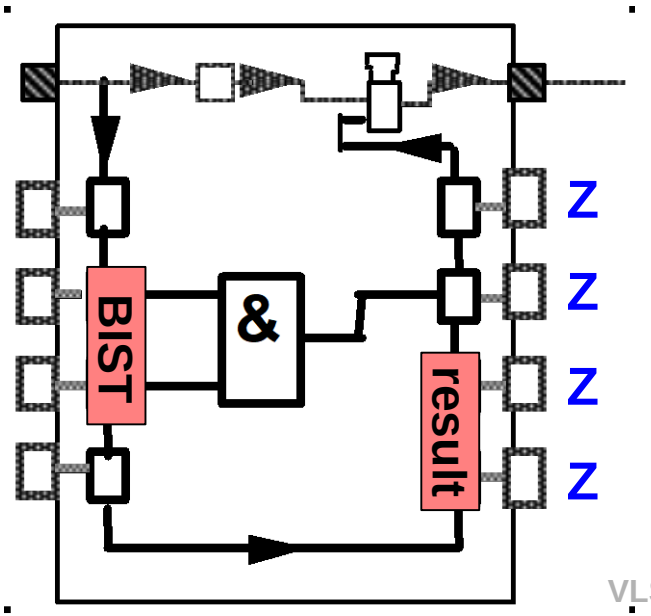


Q: Suppose we want to test AND gate by '10'. Please fill in blanks. (assume instruction code already loaded)



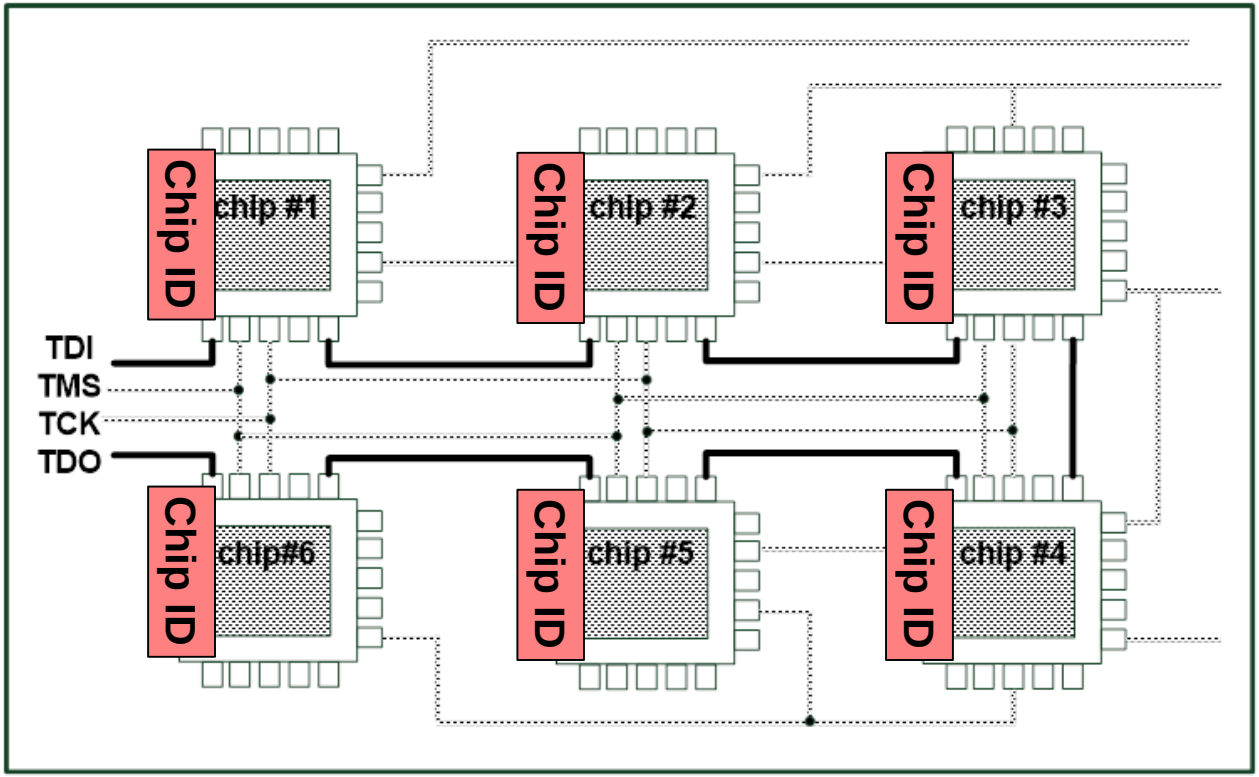
RUNBIST Instruction* not in exam

- Purpose: Run BIST commands
- To avoid random system logic outputs during BIST
  - (1) BSR controls system output pins. (PRELOAD), or
  - (2) Put all output BSR to high-impedance (Z)
- BIST results (PASS or FAIL) can be left in BSR or internal cell
  - Shift out through boundary scan chain



IDCODE Instruction* not in exam

- Purpose: Connects chip ID register serially between TDI and TDO
  - Read out chip ID
- Device ID standard by JEDEC (Joint Electron Device Engineering Council)

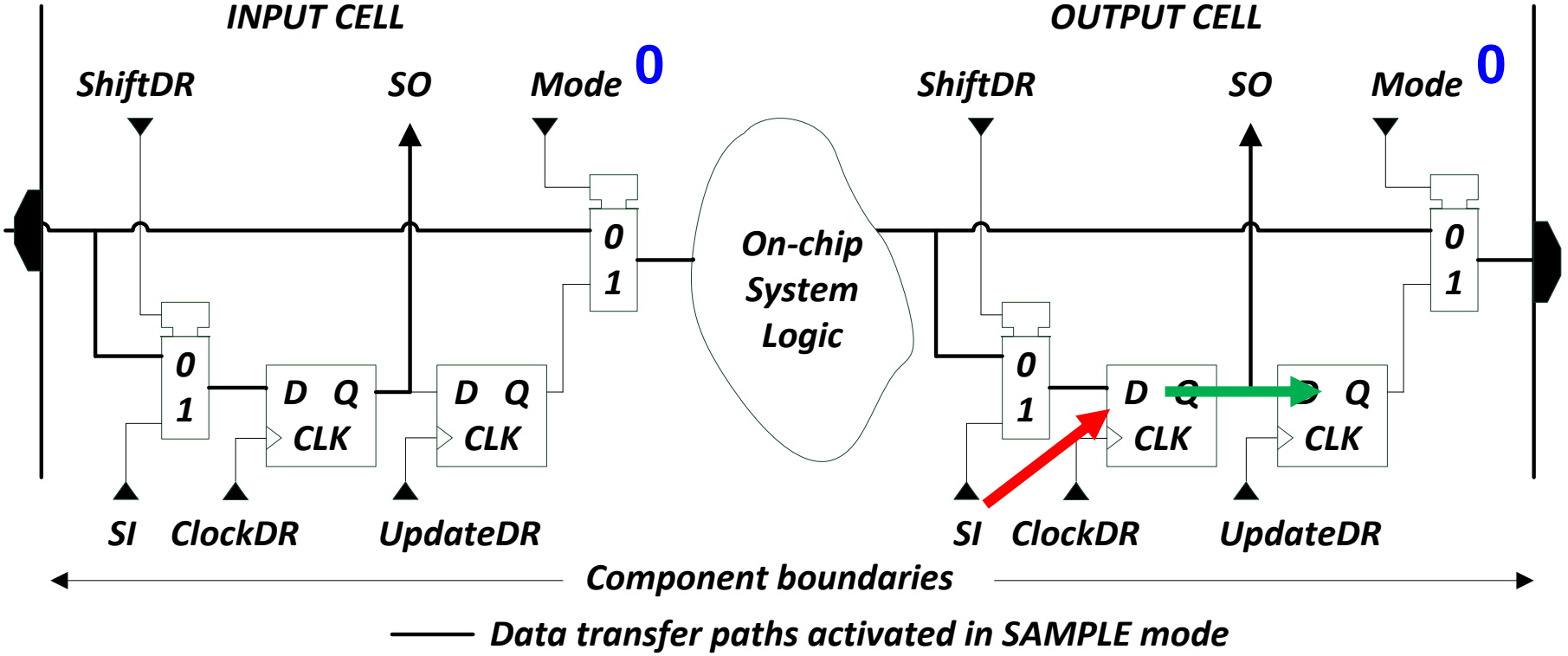


Conclusion

- JTAG IEEE 1149.1 standard
  - Boundary scan for board-level testing
- Components
  - TAP ports, TAP controller
  - Registers (BSR/BR/IR), Instruction decoder
- Instructions
  - Mandatory: EXTEST, BYPASS, SAMPLE/PRELOAD
  - Optional: INTEST, RUNBIST, IDCODE …
- JTAG area overhead is small
  - Has been widely adopted by industry
  - Automatic compiler is widely available

FFT

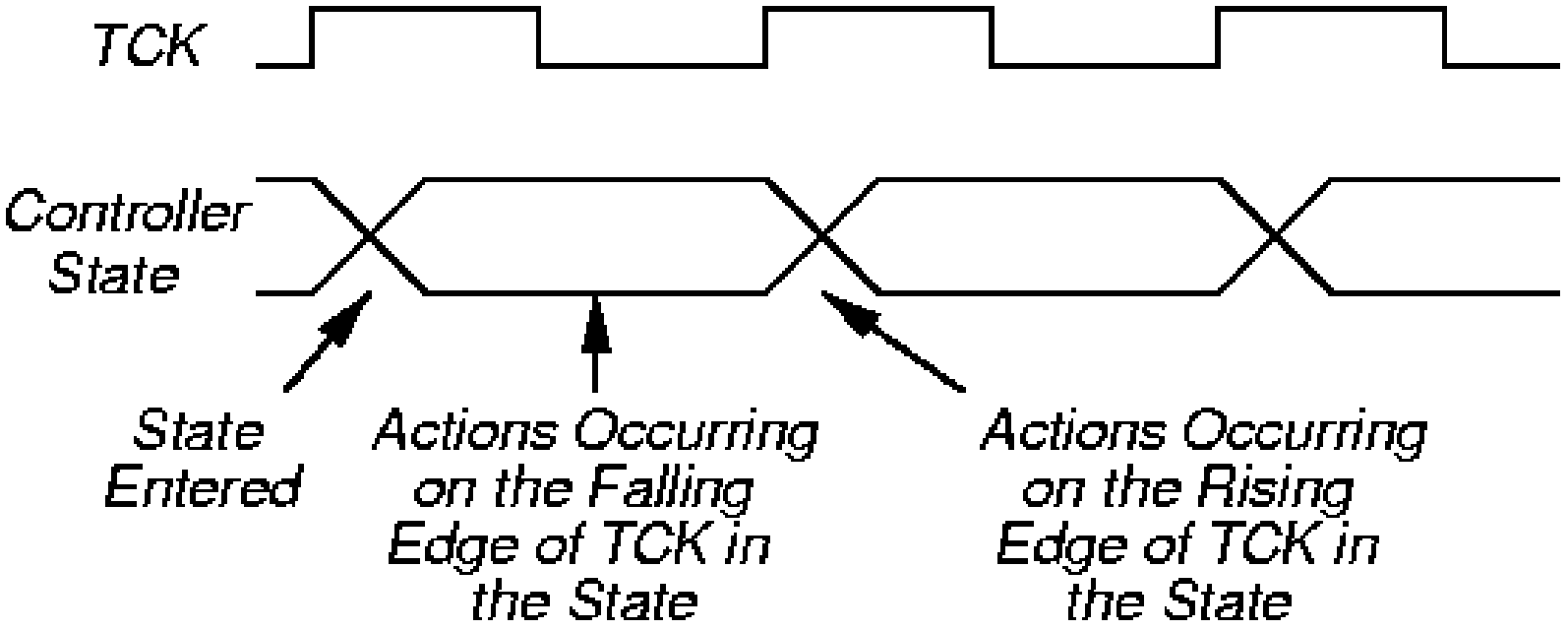
- Q1: INTEST is exactly the same as EXTEST, why?
- Q2: During PROLOAD, Why do we need to control system output?



Reference

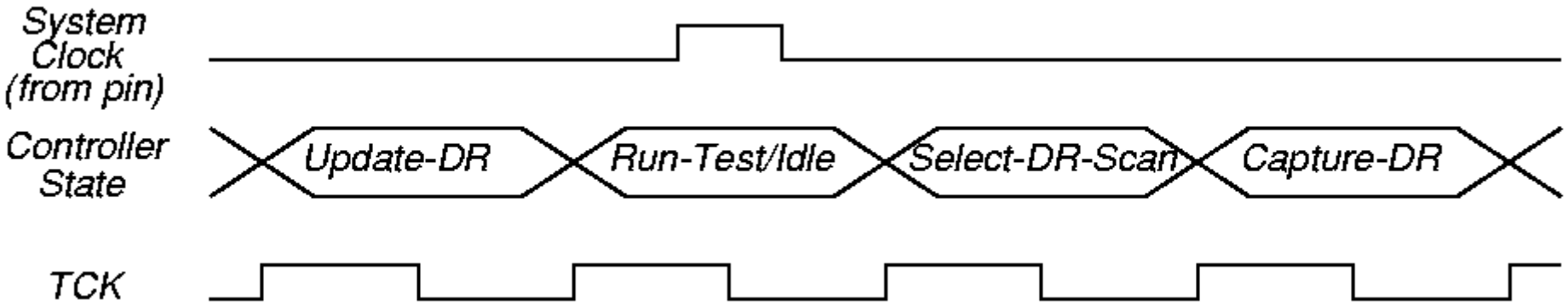
- JTAG Verilog Code Example
  - M. D. Ciletti, "Advance Digital Design with the Verilog HDL," Prentice Hall, 2002, Ch11.
- K.P. Parker, *The Boundary Scan Handbook*, Springer.

Appendix: TAP controller timing

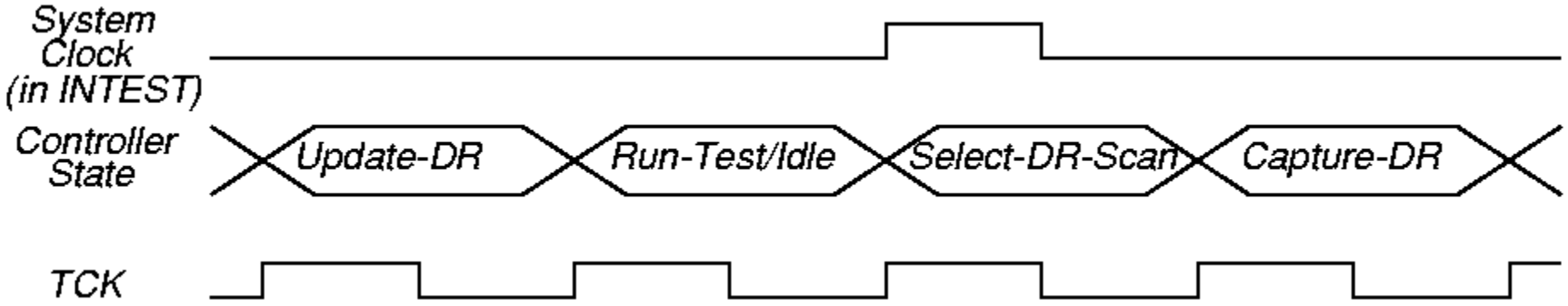


INTEST Instruction Clocks

Control of applied system clock during *INTEST*



Use of *TCK* for on-chip system logic clock



CLAMP Instruction

- **Purpose: Forces chip outputs to be driven by BSR**
- **Can bypass boundary scan chain by using one-bit Bypass Register**
- **May have to add RESET hardware to control on-chip system logic**
  - **so that it does not get damaged (by shorting 0's and 1's onto an internal bus, etc.)**