

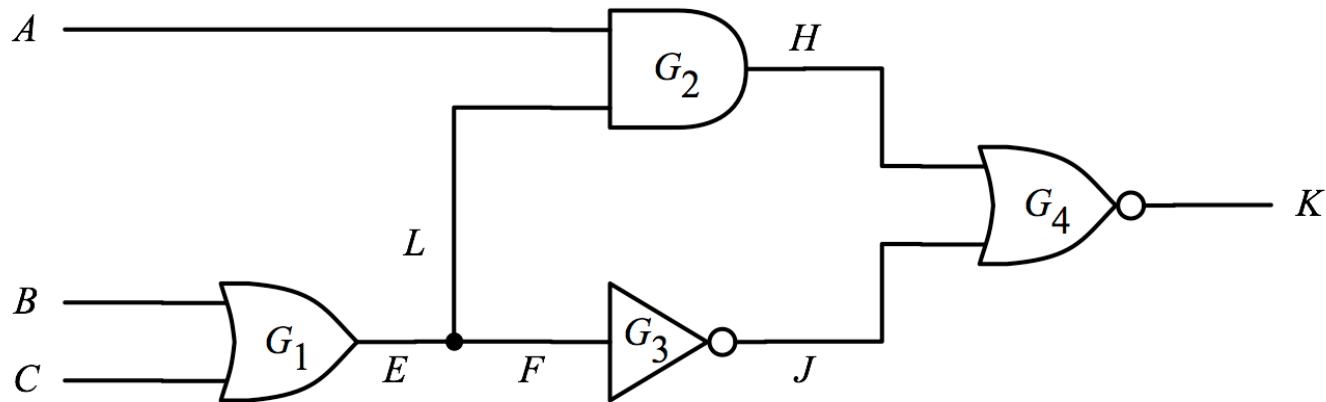
Outline

- **Course objective & roadmap**
- **Notation & references**
- **Dedication**

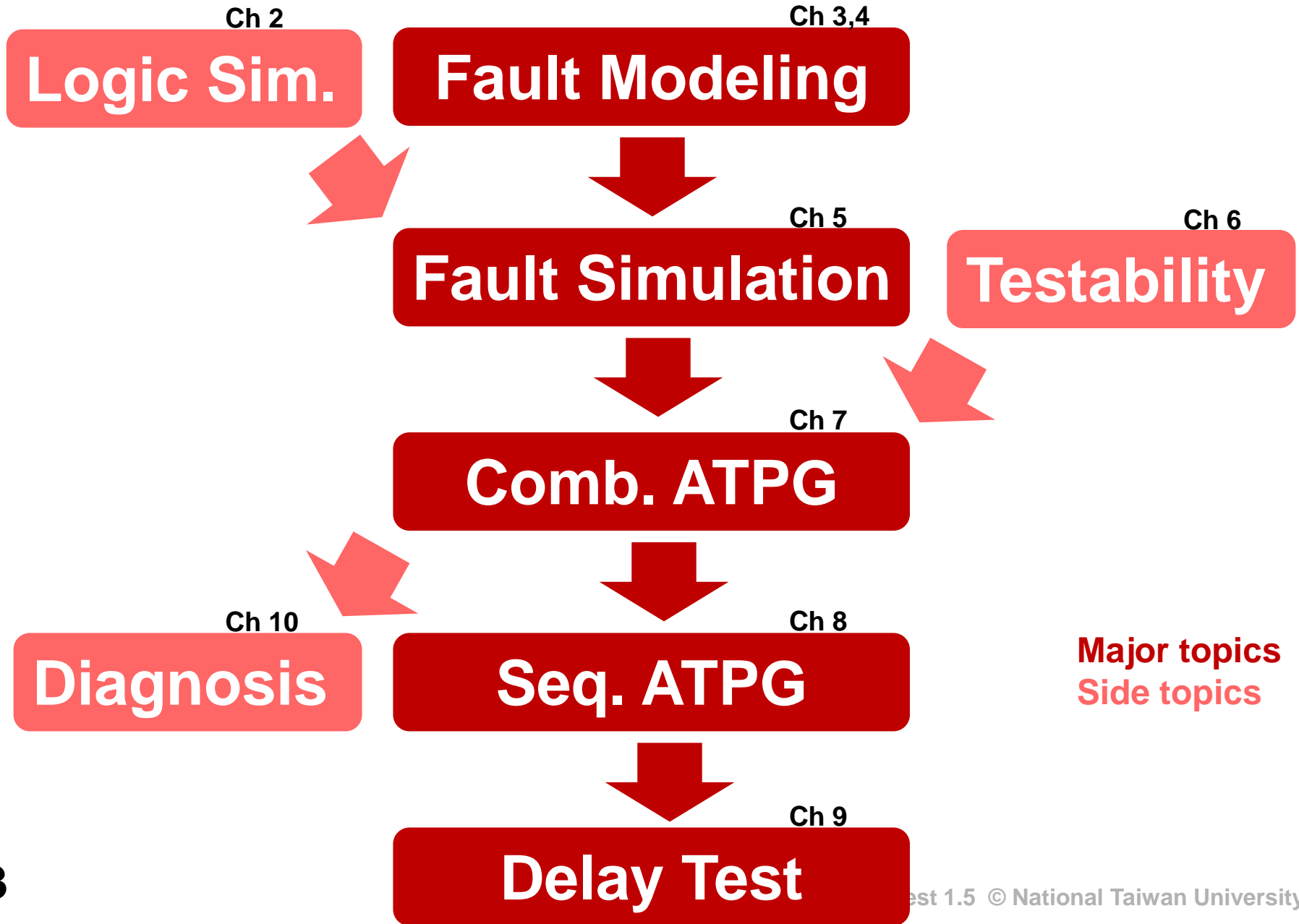


Course Objectives

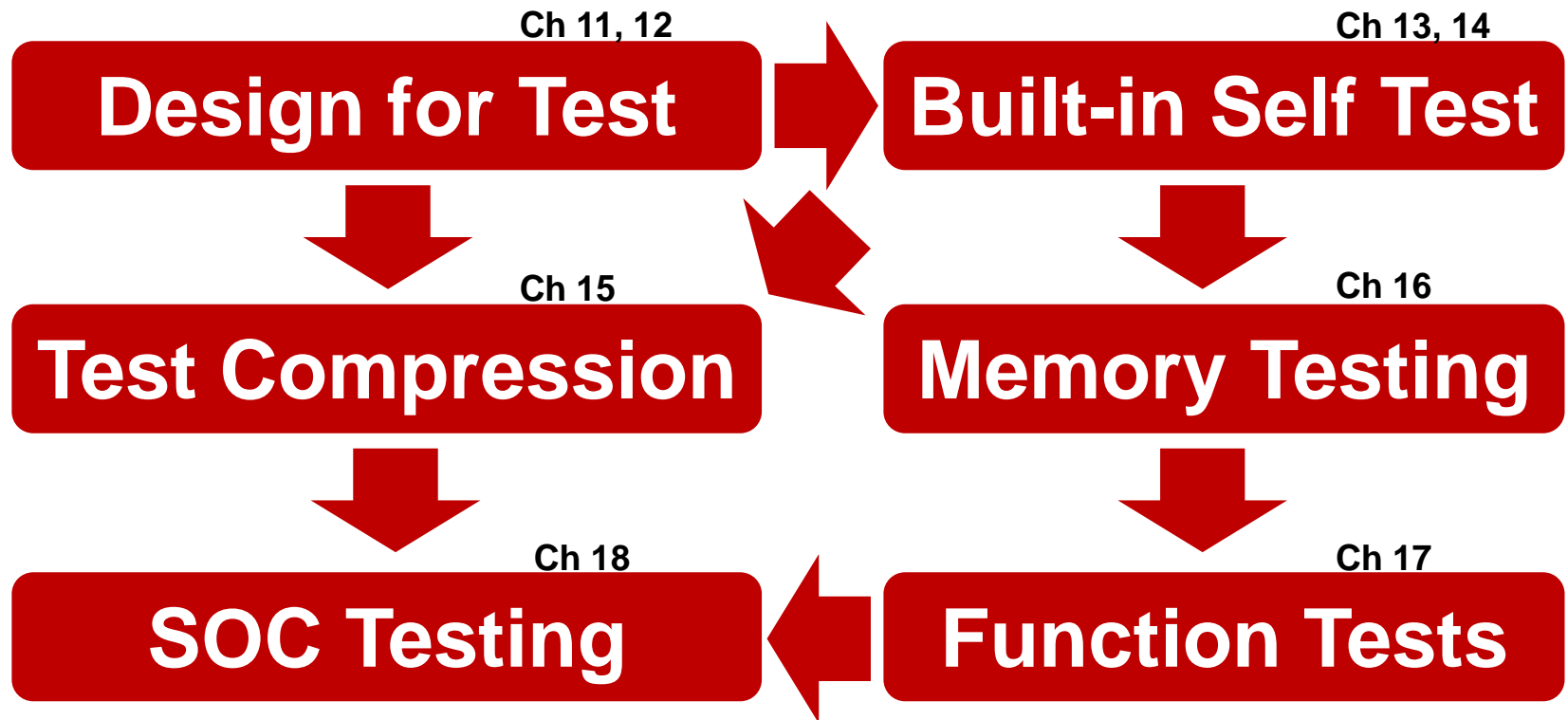
- You will learn
 - ♦ What is VLSI testing
 - ♦ Why is testing important
 - ♦ How do we achieve good testing
 - ♦ What are important issues in testing and their solutions
- This course focus on VLSI **digital circuits**



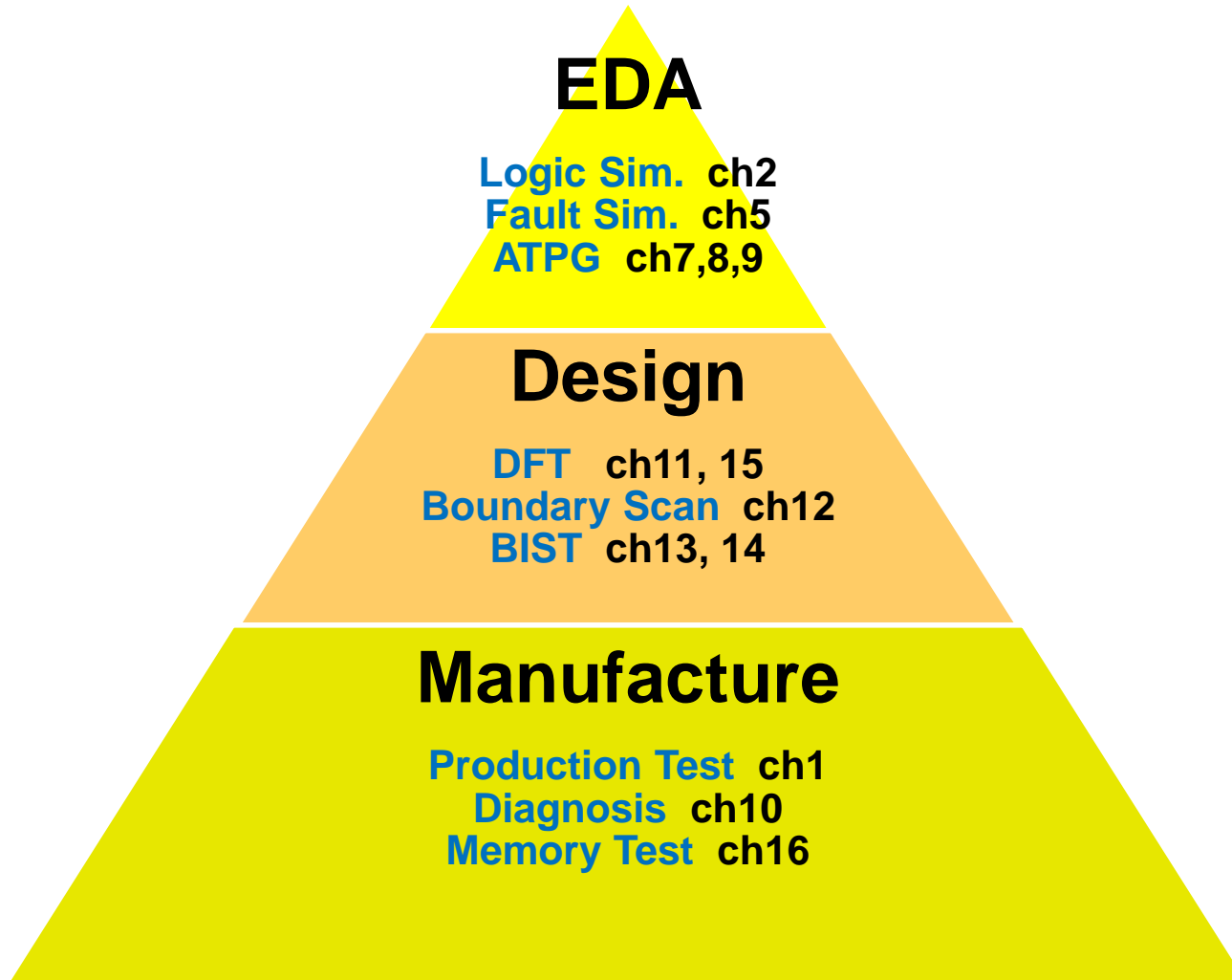
Course Roadmap (EDA Topics)



Course Roadmap (Design Topics)



Test in Semiconductor Pyramid



Lecture Notes

- Important keywords highlighted in **red *Italic***
- Important concepts highlighted in **blue color**
- Paper references [McCluskey 84]
- Book references (WWW) (BA)
- FFT (Food for Thoughts)
 - ♦ Encourage thinking and discussion
 - ♦ No fixed answer !

Quiz

Q: What does FFT stands for?

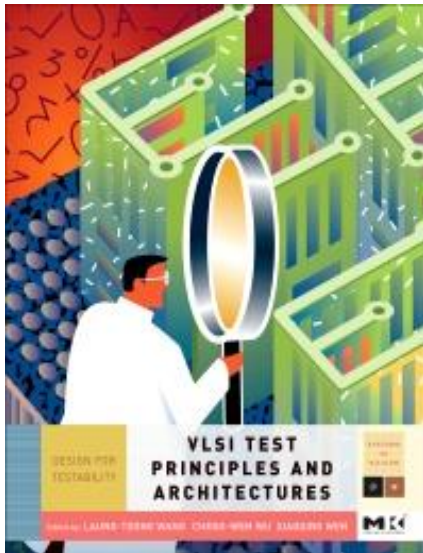
A:



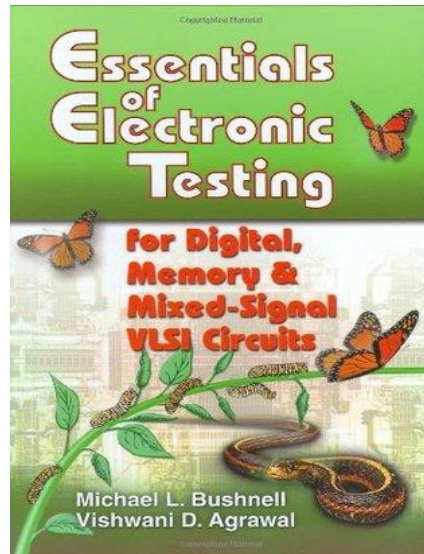
Summary is Highlighted at Bottom

Reference Books

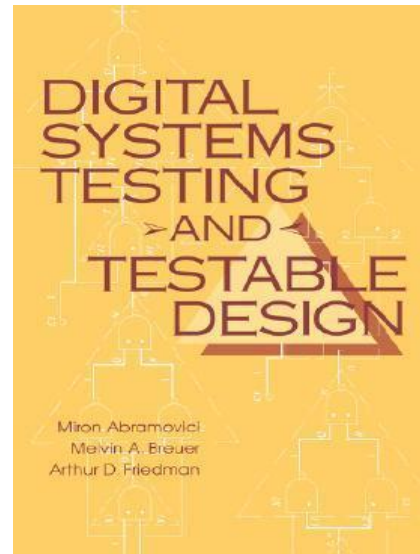
- (WWW) L.T. Wang, C.W. Wu, and X. Wen, “*VLSI Test Principles and Architectures*”, Morgan Kaufmann, 2006.
- (BA) M.L. Bushnell and V.D. Agrawal, “*Essentials of electronic testing*,” Kluwer Academic Publishers, 2000.
- (ABF) M. Abramovici, M. A. Breuer and A.D. Friedman, “*Digital systems testing and testable design*,” IEEE Press, 1994
- (BMS) P.H. Bardell, W.H. McAnney, J. Savior, “*Built-in Test for VLSI: Pseudorandom Techniques*,” Wiley Interscience, 1987,



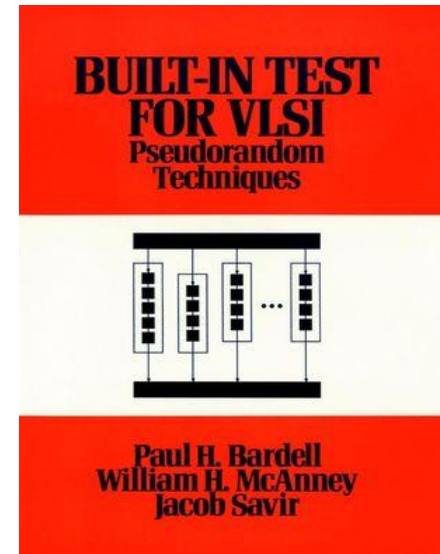
(WWW)



(BA)



(ABF)



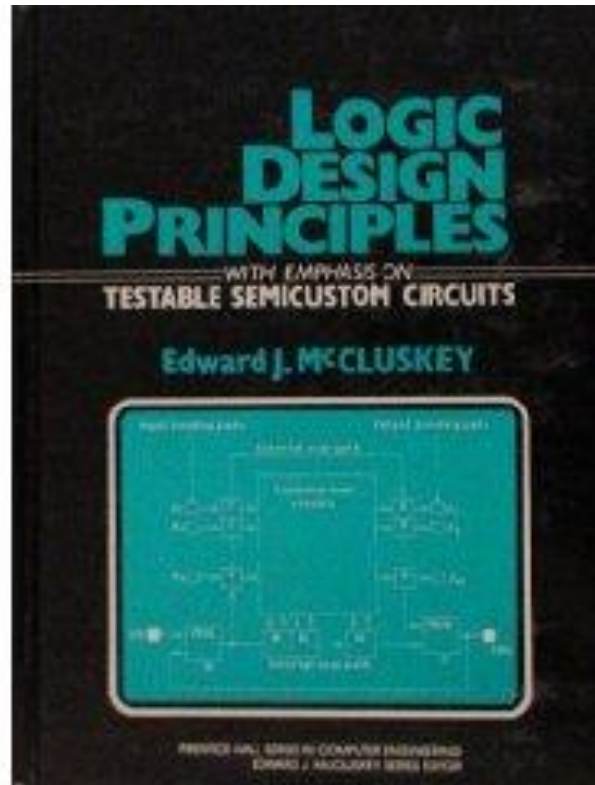
(BMS)

Recommended Reading

Topics	Our Chapters	WWW	BA
Introduction	1	1.1, 1.2	1.4, 2.1, 3.2, 3.3
Logic Simulation	2	3.2, 3.3	5.1 ~ 5.4
Fault Models	3	1.3	4
Fault Collapsing	4	-	4.5
Fault Simulation	5	3.4	5.5, 5.6
Testability Measure	6	2.2	6.1
Comb. ATPG	7	4.1 ~ 4.4	7.5
Seq. ATPG	8	4.5	8.2, 8.3
Delay Test	9	4.10	12
Diagnosis	10	7.2	-
Design for Test (DFT)	11, 12	2.3 ~ 2.5, 10.2	14, 16
BIST	13, 14	5.3 ~ 5.5	15
Test Compression	15	6	-
Memory Testing	16	8.2	9.5 ~ 9.7
SOC Testing	18	10.3	-

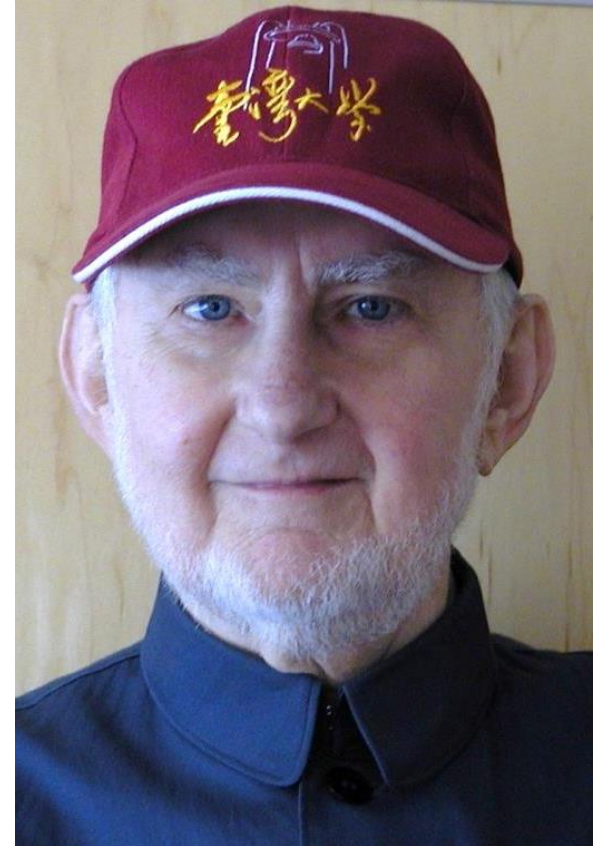
Classic Textbook

- The classic textbook of logic design (and testing)
- **Logic Design Principles with emphasis on testable semicustom circuits**, Prentice Hall 1986



Edward J. McCluskey (1929-2016)

- 1959-1967: Professor of Princeton University
- 1967~2008: Professor of Stanford University
- Trained 75 PhD
- Important contributions
 1. *Quine-McCluskey Algorithm* (video 15.2)
 2. *Hazards* (video 2.6)
 3. *Pseudo Exhaustive Testing* (video 17.3)
 4. *Sequential circuits modes*
- First President of IEEE Computer Society
- Founder of Stanford CS program
- IEEE *Life Fellow*
- IEEE *Emanuel R. Piore Award*
- IEEE *John von Neuman Medal*
- Member of *National Academy of Engineering*



Prof. McCluskey wearing NTU hat

<http://www-crc.stanford.edu/>

Dedication

This course is dedicated to

Prof. Edward McCluskey

Pioneer researcher and educator

