

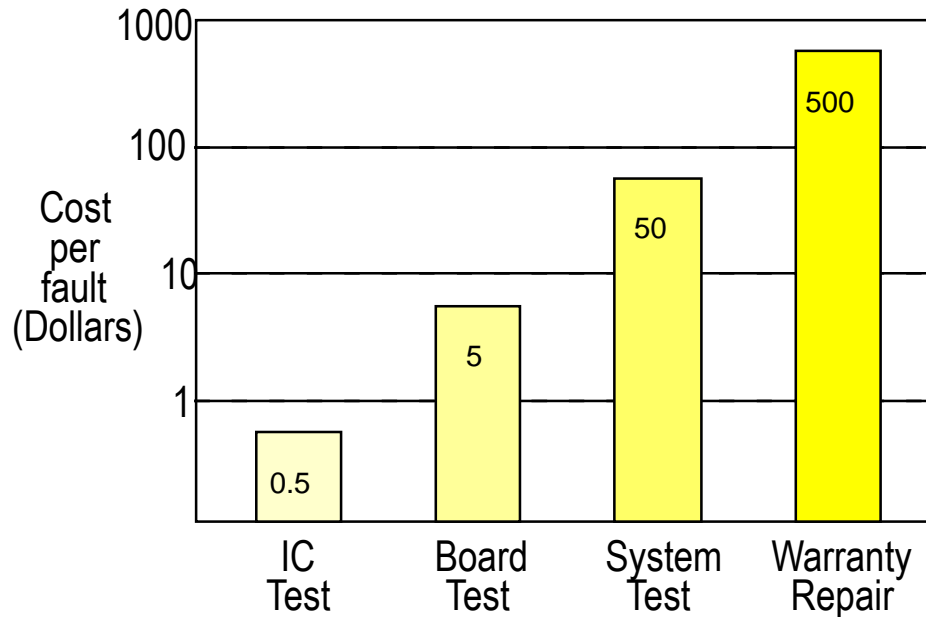
Introduction

- What Is Testing
- Types of Testing
- Test Quality
- **Test Economics**
 - ♦ **Why and Who Invests in Test?**
 - * **Global Semiconductor Industry**
 - ♦ **How to Make Optimal Test Decision?**
- Important Research Topics
- Conclusion



Why Invest in Testing?

- Although testing is expensive
 - ♦ Repair cost is even **more expensive!**
- **Rule of Tens** [Davis 82]



A Stitch in Time Saves Nine

15% Semiconductor Market Goes to Test

- 2019 global semiconductor market **\$412.3B USD WSTS)**
 - ◆ Packing and test about **15%**
- 2019 Taiwan **\$86.3B USD**, ~**21%** of global market
 - ◆ Fabless design **\$22.4B USD**
 - ◆ Manufacture **\$42.5B USD**
 - ◆ Packaging **\$11.2B USD**
 - ◆ **Testing \$5.0B USD**

Source TSIA

單位：億新台幣

億新台幣	2016	2016 成長率	2017	2017 成長率	2018	2018 成長率	2019	2019 成長率	2020 (e)	2020 (e) 成長率
IC 產業產值	24,493	8.2%	24,623	0.5%	26,199	6.4%	26,656	1.7%	27,742	4.1%
IC 設計業	6,531	10.2%	6,171	-5.5%	6,413	3.9%	6,928	8.0%	7,227	4.3%
IC 製造業	13,324	8.3%	13,682	2.7%	14,856	8.6%	14,721	-0.9%	15,285	3.8%
晶圓代工	11,487	13.8%	12,061	13.8%	12,851	6.6%	13,125	2.1%	13,649	4.0%
記憶體與其他製造	1,837	-16.8%	1,621	-11.8%	2,005	23.7%	1,596	-20.4%	1,636	2.5%
IC 封裝業	3,238	4.5%	3,330	2.8%	3,445	3.5%	3,463	0.5%	3,615	4.4%
IC 測試業	1,400	6.5%	1,440	2.9%	1,485	3.1%	1,544	4.0%	1,615	4.6%
IC 產品產值	8,368	2.9%	7,792	-6.9%	8,418	8.0%	8,524	1.3%	8,863	4.0%
全球半導體市場(億美元) 及成長率(%)	3,389	1.1%	4,122	21.6%	4,688	13.7%	4,121	-12.1%	4,330	5.1%

Many Companies Invest Heavily in Test

IDM



Fabless/Foundry



EDA

ATPG
Fault Sim.

Design

BIST, DFT
Boundary Scan

Manufacture

Fabrication, Assembly, Test
Physical Failure analysis

World's Top EDA Companies

- 2019 global EDA market is about **\$10B** USD
 - ♦ Growing ~10% each year

Company	Rank	Revenue	Country
Synopsys	1	\$3.36 B	USA
Cadence	2	\$2.33 B	USA
Mentor Graphics (now Siemens EDA)	3	\$1.28 B (*2017)	Europe



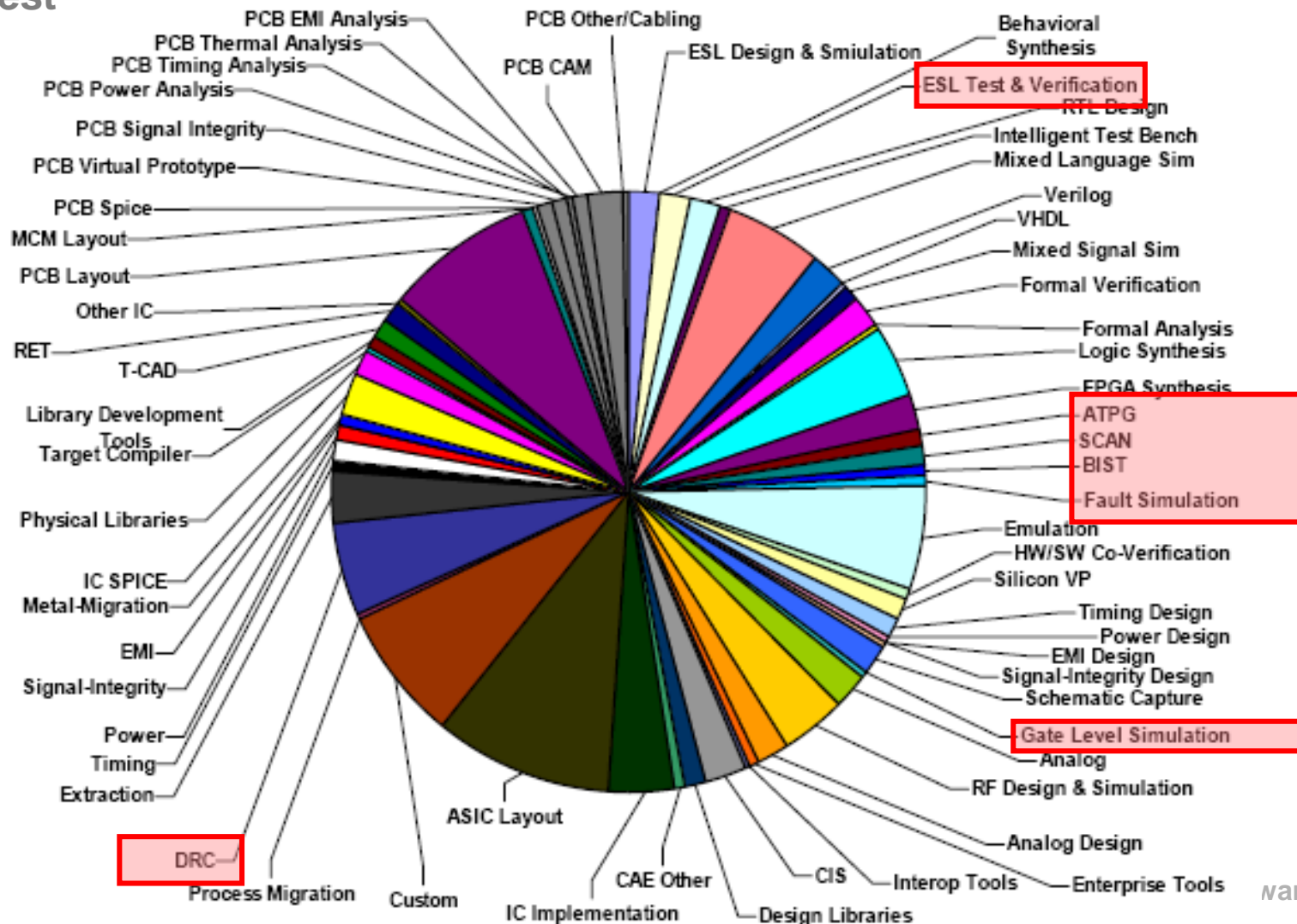
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EDA Market by Tool

- Test-related tools are about 5~10% EDA revenue

dataquest
2012



World's Top OSAT Companies

- **OSAT** = outsourced semiconductor assembly and test
- About 1/2 IC tested by Taiwan

Analysis, 2020

Company	Rank	Market	Country
日月光 ASE	1	21.8%	Taiwan
艾克爾 Amkor	2	18.5%	USA
矽品 SPIL	3	14.4%	Taiwan
長電科技JCET	4	13.4%	China
力成 PTI	5	10.3%	Taiwan



Test Important for IC Industry

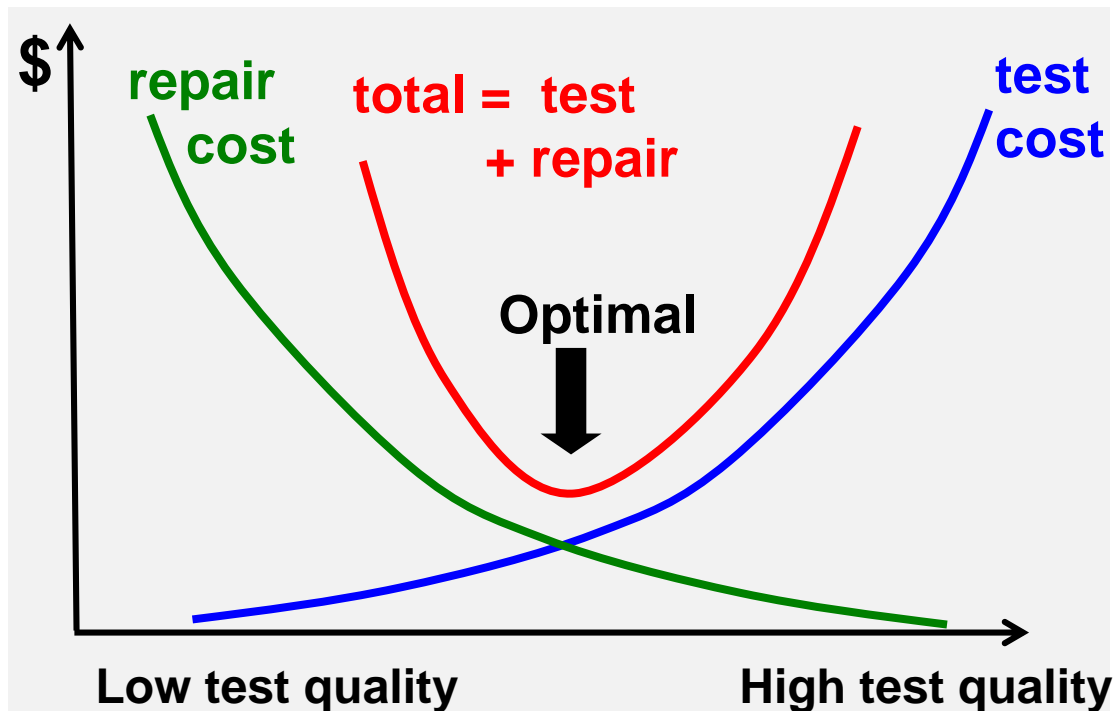
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How to Make Optimal Decision?

- Optimal test not only **technical** issue, but also **economics** issue
 - ♦ Trade off between **test cost** and **repair cost**
- Different product has different optimal decision
 - ♦ **No single best decision** for all products!



What Cost Can We Optimize?

- **EDA:** ATPG, fault simulator ...
 - ◆ Typically **10K ~ 100K** USD
- **Design:** insert DFT/BIST circuitry
 - ◆ Area/power/delay overhead about **5~10%**
- **OSAT:**
 - ◆ Equipment
 - * Tester (Automatic Testing Equipment, ATE)
 - Typically **0.5~3 M** USD
 - * Handler, probe station, Burn-in oven
 - ◆ Test application time (TAT)
 - * Around **\$50 to \$300** USD per hour
 - * ASIC takes **2~3** seconds. CPU can be **0.5~1** minute
 - ◆ load board, probe card
 - * **\$1K ~ 20K** USD

Many Decisions to Make

Case 1: DFT or Not?

Q1: Without DFT

Y=98%, FC=70%. DL=?

$$DL = 1 - Y^{(1-FC)}$$

A: 6,043 DPM

Q2: With DFT

Y=97%, FC=99%. DL=?

A: 304 DPM

Technically, DFT Improves DPM
Economically, Is DFT Worth Doing?

Case 1: DFT or Not? (Cont'd)

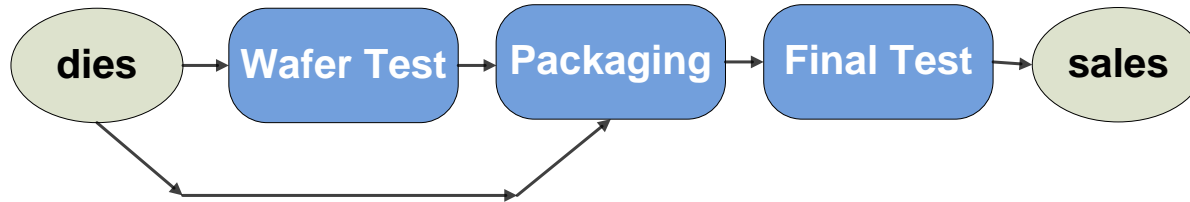
- Q: Is it economical to insert DFT?
- A: Yes. This is true for many products.
 - ♦ Although Y drops, DL improves significantly

$$DL = 1 - Y^{(1-FC)}$$

Item	w/o DFT	with DFT
Total # of Dies	1,000,000	900,000
Yield	98%	97%
FC fault coverage	70%	99%
$DL = 1 - Y^{(1-FC)}$	6,043 DPM	304 DPM
Sales = D x Y x \$1	980,000	873,000
Repair cost = D x Y x DL x \$100	592,163	26,587
Profit = S - R	387,837	846,413

DFT Is Worth Doing!

Case 2: Wafer Test or Not?



Item	bad yield = 64%		good yield = 81%	
	with WT	no WT	with WT	no WT
Total # of Dies	1,000,000	1,000,000	1,000,000	1,000,000
$C_{WT} = D \times \$0.02$	20,000	0	20,000	0
Y_{WT}	80%	100%	90%	100%
$C_{PK} = D \times Y_{WT} \times \0.1	80,000	100,000	90,000	100,000
$C_{FT} = D \times Y_{WT} \times \0.06	48,000	60,000	54,000	60,000
Y_{FT}	80%	64%	90%	81%
$Sales = D \times Y_{WT} \times Y_{FT} \times \1	640,000	640,000	810,000	810,000
$Cost = C_{WT} + C_{PK} + C_{FT}$	148,000	160,000	164,000	160,000
$Profit = S - C$	492,000	480,000	646,000	650,000

WT or not Depends on Yield

Case 3: To Burn or Not To Burn?

Q: Is it worth doing burn-in (BI)?

BI cost is \$2 per die. BI improves quality by 1,000DPM.

Fabrication cost is 30% of price. Repair cost is 30 times price.

Item	ASIC, Price per die= \$10		CPU, Price per die= \$100	
	with BI	no BI	with BI	no BI
D_F =# of Dies fab	1,000,000	1,000,000	1,000,000	1,000,000
D_S =# of dies sold	999,000	1,000,000	999,000	1,000,000
D_B =# of bad dies sold	0	1,000	0	1,000
Sales = $D_S \times P$	9,990,000	10,000,000	99,900,000	100,000,000
$C_{FB}=D_F \times P \times 30\%$	3,000,000	3,000,000	30,000,000	30,000,000
$C_{BI}=D_F \times \$2$	2,000,000	0	2,000,000	0
$C_{RP}=D_B \times P \times 30$	0	300,000	0	3,000,000
Profit= $S-C_{FB}-C_{BI}-C_{RP}$	4,990,000	6,700,000	?	?

BI or not Depends on Price

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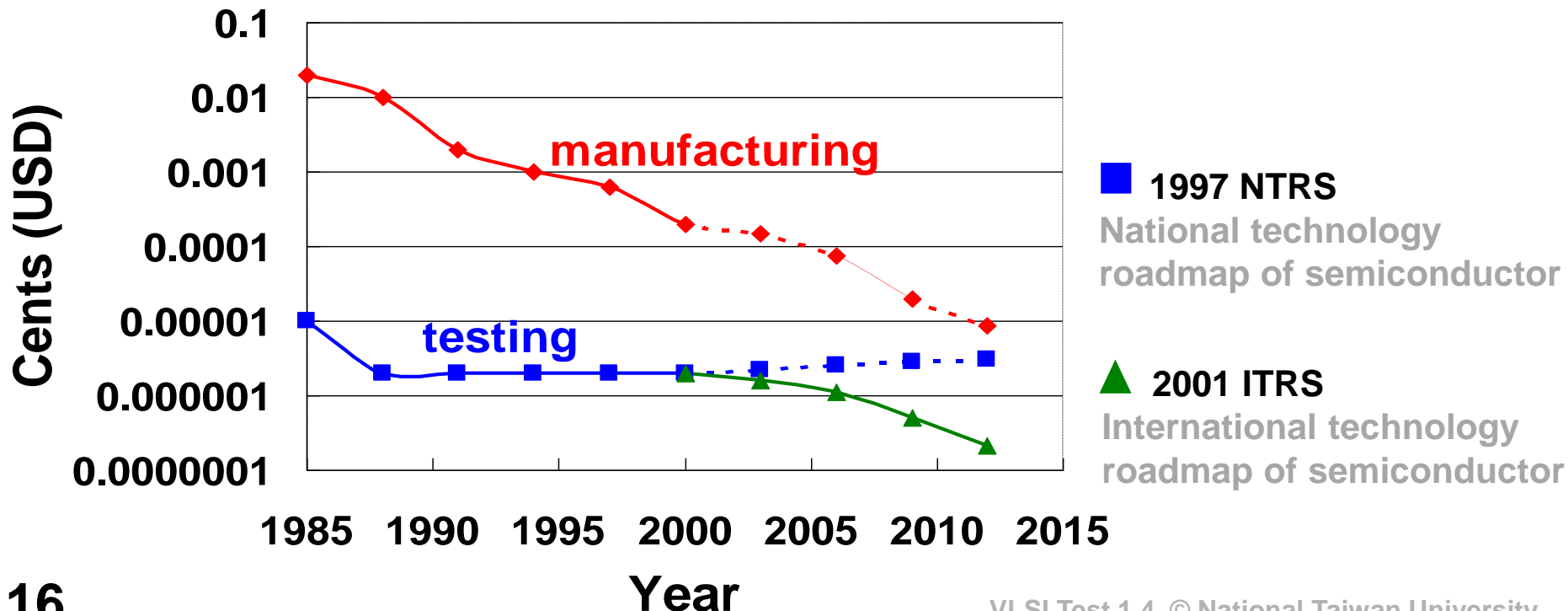
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Test Needs Continuing Improvements

- **NTRS 1997** predicted test cost will be greater than manufacturing cost
 - ♦ assume that historical trends continued
- **ITRS 2001** revised the prediction
 - ♦ Significant research efforts applied to push test cost down

Cost per Transistor



Important Research Topics

- **Reduce test cost**
 - ◆ Reduce test equipment cost
 - * *Built-in Self Test (BIST)*
 - ◆ Reduce test data volume, test application time
 - * *Test compression, ATPG, Memory tests*
- **Improve test quality**
 - ◆ Better *fault models, delay tests*
 - ◆ *Design for testability (DFT)*
- **Improve yield**
 - ◆ *Diagnosis*
- **Better/faster EDA tools**
 - ◆ ATPG, Fault simulator, optimization algorithms

Major Conferences and Journals

- International Conferences

- ◆ IEEE Int'l Test Conference (**ITC**)
- ◆ IEEE/ACM Design Automation Conference (**DAC**)
- ◆ IEEE VLSI Test Symposium (**VTs**)
- ◆ IEEE Asian Test Symposium (**ATS**)
- ◆ IEEE European Test Symposium (**ETS**)
- ◆ IEEE Design and Test in Europe (**DATE**)
- ◆ IEEE Int'l Conference on CAD (**ICCAD**)

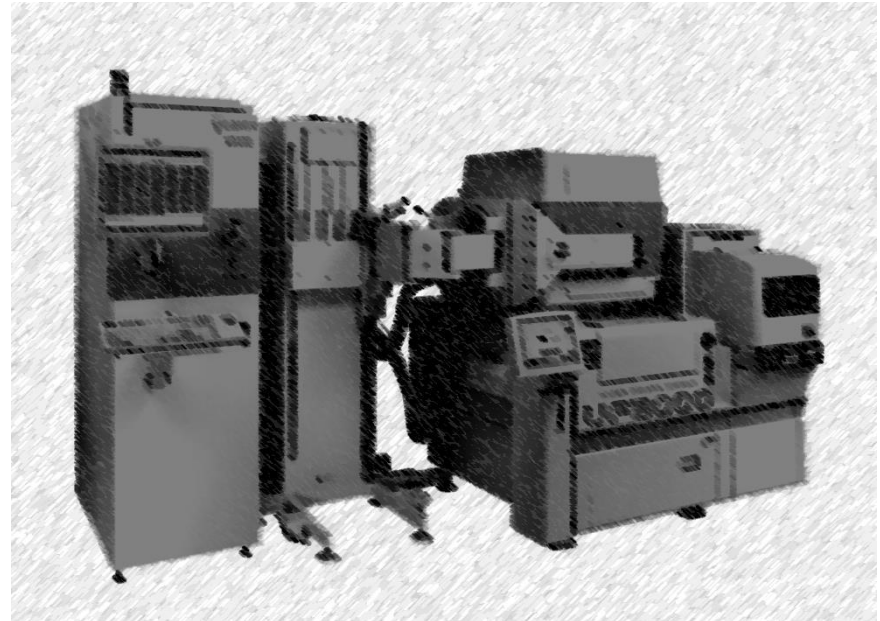
- Journals

- ◆ IEEE Trans. On Computer-Aided Design (**TCAD**)
- ◆ IEEE Trans. On VLSI Systems (**TVLSI**)
- ◆ IEEE Trans. On Computers (**TC**)
- ◆ ACM Trans. On Design Auto. of Electronic Systems (**TODAES**)
- ◆ Journal of Electronic Testing : Theory and Application (**JETTA**)

- IEEE Design & Test Magazine (**D&T**)

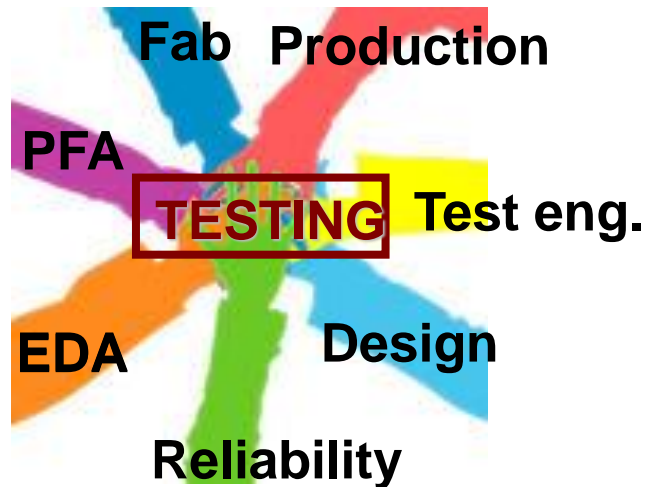
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Conclusion

- WHY test?
 - ◆ It is **important to invest** in test because of **rule of ten**
- HOW to test?
 - ◆ Optimal test not only **technical issue**, but also **economics issue**
 - ◆ **No single best test solution for all products!**
- WHO responsible?
 - ◆ Testing is joint responsibility of **everybody**



Without Testing, It Is a Gamble!



**Testing Does, and Also Will,
Play Very Important Role
in High-tech Industry.**



References

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