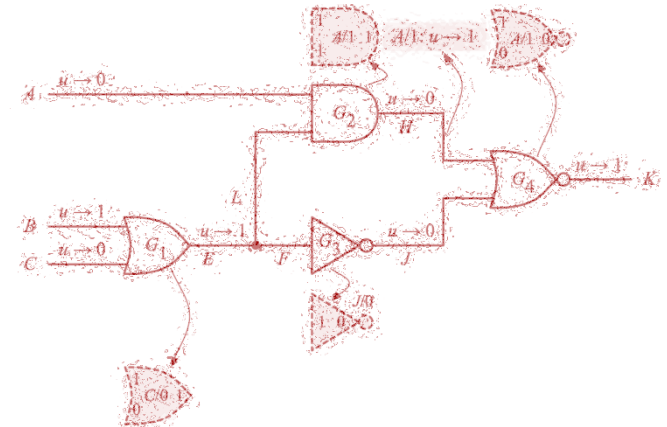


# Fault Simulation

- Introduction
- Fault simulation techniques
- Alternatives to fault simulation
- Issues of fault simulation
- Conclusion

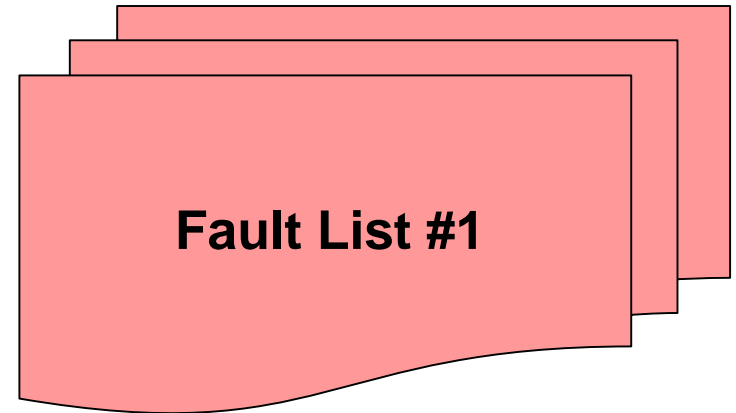


# Issues of Fault Simulations

- Long CPU time
  - ◆ Distributed computing, or Fault sampling
- Large memory requirement
  - ◆ Partition faults into multiple simulation passes
- Potentially detected faults
- Compatibility with logic simulation

# Speed and Memory Solutions

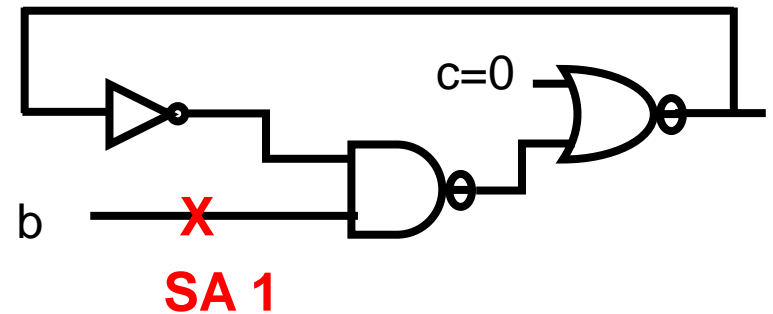
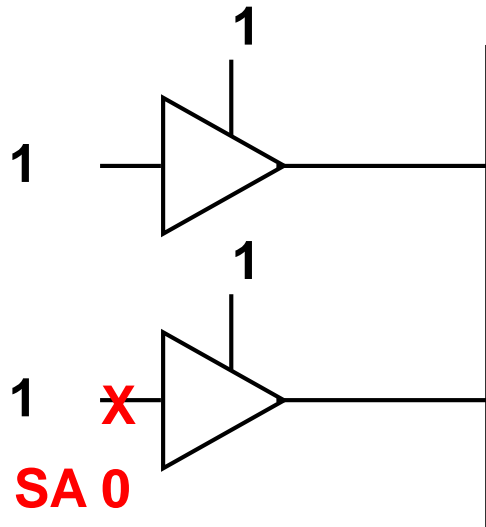
- 1. **Multiple-pass fault simulation**
  - ♦ Run only small portion of faults per pass
- 2. **Distributed fault simulation**
  - ♦ Distribute faults to more than one computers
- 3. **Emulation**
  - ♦ Use hardware emulator, like FPGA



- \*A **simulation pass** is a single simulation run
  - ♦ from beginning to end of test patterns

# Potentially Detected Faults

- DEF: faults that may or may not be detected in practice
  - ♦ Detection cannot be determined by fault simulation
- Possible reasons for potentially detected faults
  - ♦ Bus contention, Oscillation, High impedance, Unknown
- Examples:



**Fault detected?**

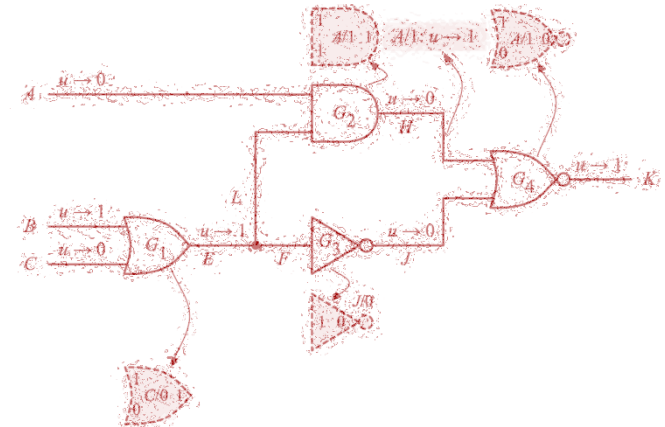
- Different tools have different ways to calculate FC
  - ♦ Please see tool manual for details

# Compatibility with Logic Simulation

- To speed up fault simulation, many tools requires circuits to be represented in a library models pre-defined by tools
- Functional verification logic simulations often involve mixed-level codes, which make such modeling very difficult
  - ◆ Circuit delay
  - ◆ RTL behavior description
  - ◆ *User Defined Primitives* (UDP)
    - \* DFF, MUX

# Fault Simulation

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# Quiz: Comparison of Techniques

Items	Serial	PPSFP	Deductive	Concurrent	Differential
unknown logic value	😊	😊	😞	😊	😊
Delay model					
Run time					
Sequential circuits					
Memory					

# Conclusion

- **Usage of fault simulation**
  - ◆ **ATPG, fault grading, diagnosis**
- **Techniques**
  - ◆ **Serial, parallel, PPSFP, deductive, concurrent, differential**
- **Most popular technique in industry now**
  - ◆ **PPSFP is simple for comb. ckt (or seq. ckt with full scan)**
  - ◆ **Concurrent and differential good for both comb./seq. ckt**



# Commercial Tools

- **Cadance**
  - ◆ **Verifault**
- **Mentor Graphic:**
  - ◆ **Fastscan, flextest**
- **Synopsys**
  - ◆ **Tetramax**
- **Syntest**
  - ◆ **Turboscan**
  - ◆ **TurboFault**

# References

- [Abramovici 1984] M. Abramovici, P. R. Menon, and D. T. Miller, “Critical Path Tracing: An Alternative to Fault Simulation,” IEEE Design and Test of Computers, 1984.
- [Armstrong 1972] D. B. Armstrong, A deductive method for simulating faults in logic circuits, IEEE Trans. Comput., C-21(5), 464–471, 1972.
- [Butler 1974] T. T. Butler, T. G. Hallin, J. J. Kulzer, and K. W. Johnson, LAMP: Application to switching system development, Bell System Tech. J., 53, 1535–1555, 1974.
- [Cheng 1989] W. T. Cheng and M. L. Yu, Differential fault simulation: A fast method using minimal memory, in Proc. Des. Automat. Conf., June 1989, pp. 424–428.
- [Jain 1985] S. K. Jain and V. D. Agrawal, Statistical fault analysis, IEEE Des. Test Comput., 2(1), 38–44, 1985.
- [Seshu 1965] S. Sesuh and D. N. Freeman, On improved diagnosis program, IEEE Trans. Electron. Comput., EC-14(1), 76–79, 1965.
- [Ulrich 1974] E. G. Ulrich and T. Baker, Concurrent simulation of nearly identical digital networks, IEEE Trans. Comput., 7(4), 39–44, 1974.
- [Waicukauski 1985] J. A. Waicukauski, E. B. Eichelberger, D. O. Forlenza, E. Lindbloom, and T. McCarthy, Fault simulation for structured VLSI, Proc. VLSI Syst. Des., 6(12), 20–32, 1985.