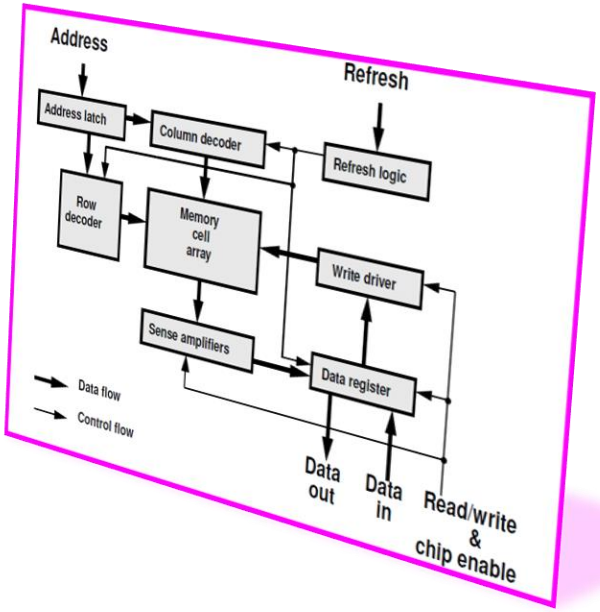
Outline

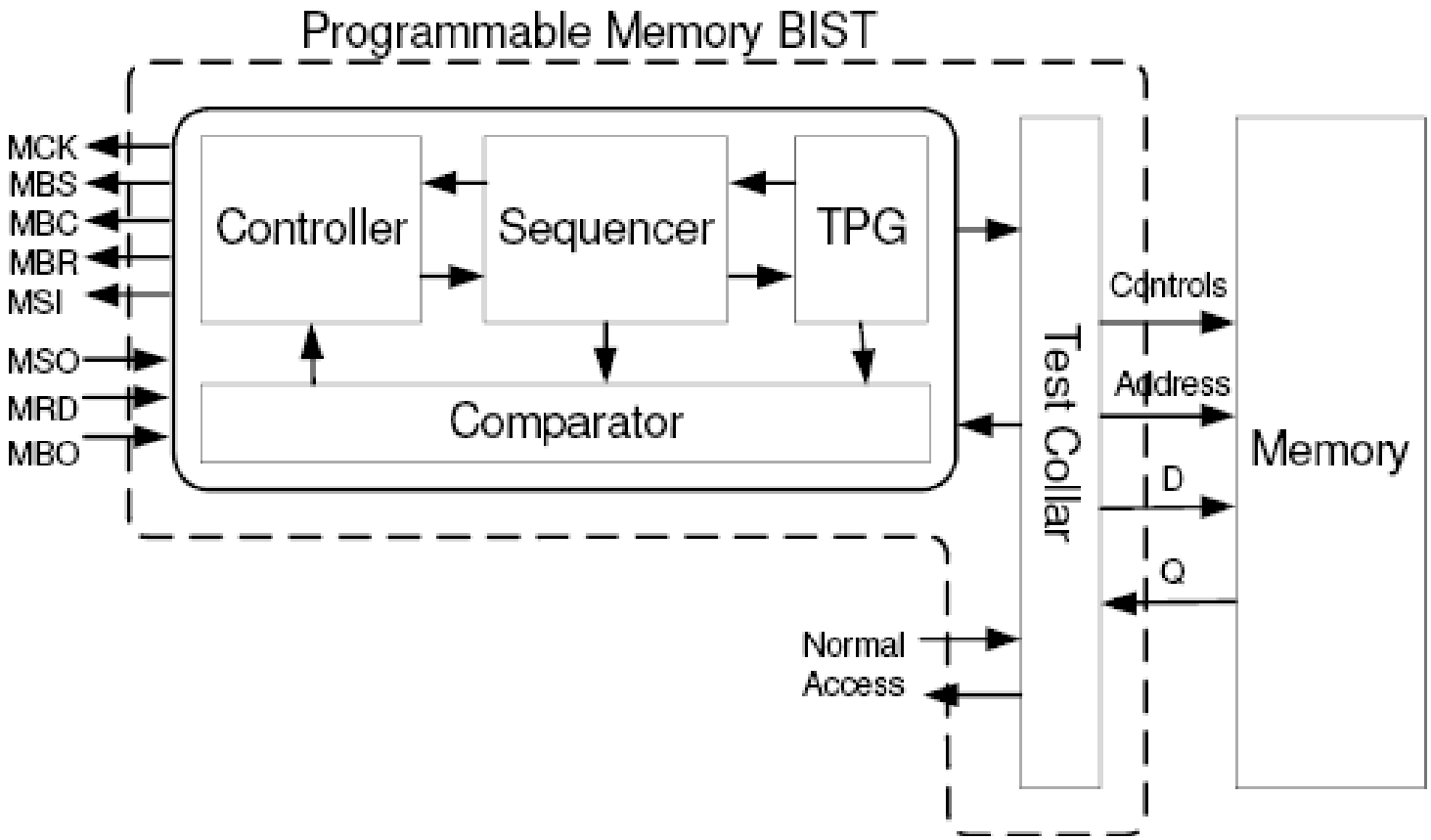
- Introduction
- Memory Fault Model
- Memory Test Algorithms
- Memory Fault Simulation* (not in exam)
- Memory Test Generation* (not in exam)
- Memory BIST* (not in exam)



Typical RAM BIST Approaches

- Methodology
  - Processor-based BIST
    - Programmable
  - Hardwired BIST
    - Fast
  - Compact
  - Hybrid
- Interface
  - Serial (scan, 1149.1)
  - Parallel (embedded controller; hierarchical)
- Patterns (address sequence)
  - March & March-like
  - Pseudorandom
  - Others

General RAM BIST Architectures

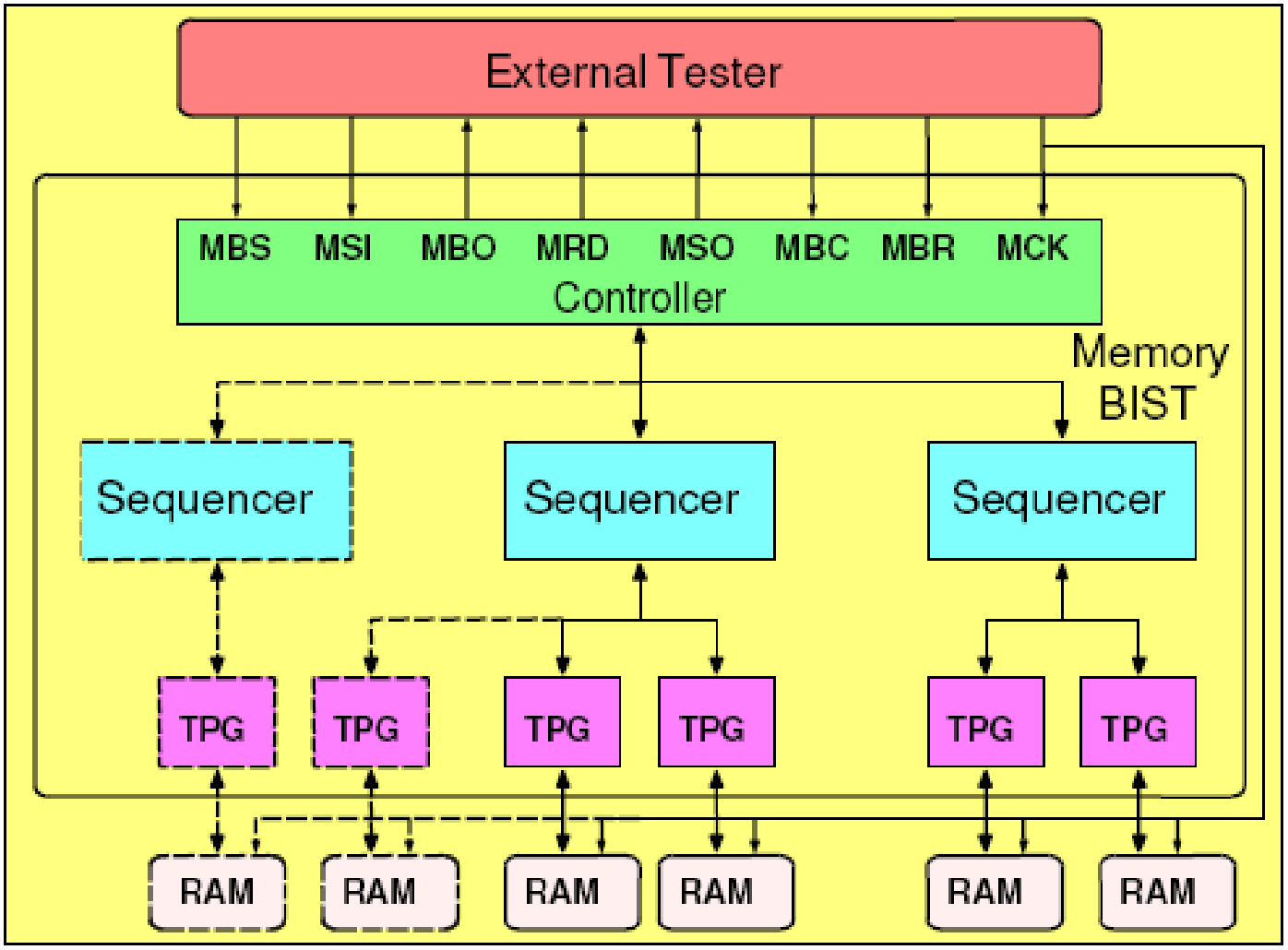


BIST I/O Pins

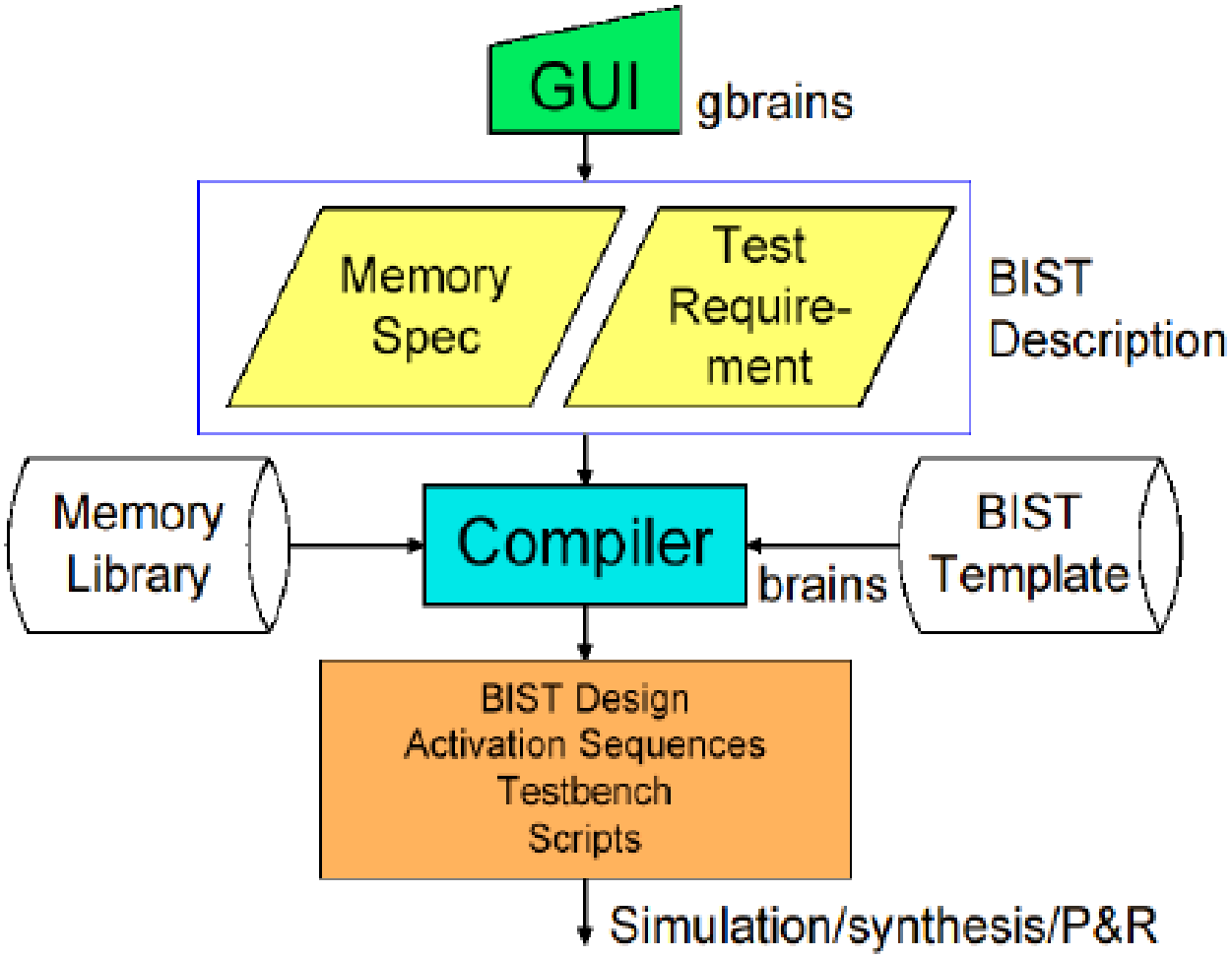
Name	IO	External IO	Descriptions
MBS	I	Yes	Memory BIST Selection
MBC	I	Yes	Memory BIST Control
MCK	I	Yes	Memory BIST Clock
MBR	I	Yes	Memory BIST Reset
MSI	I	Yes	Memory BIST command/data serial in
MSO	O	Yes	Memory BIST command/data serial out
MBO	O	Yes	Memory BIST Output
MRD	O	Yes	Memory BIST Output Ready
ADDR	O	No	Address Signals
D	O	No	Memory Data In
Q	I	No	Memory Data Out
CS	O	No	Chip Select
OE	O	No	Output Enable
WE	O	No	Write Enable

Multiple RAM Cores

- **Controller and sequencer can be shared**



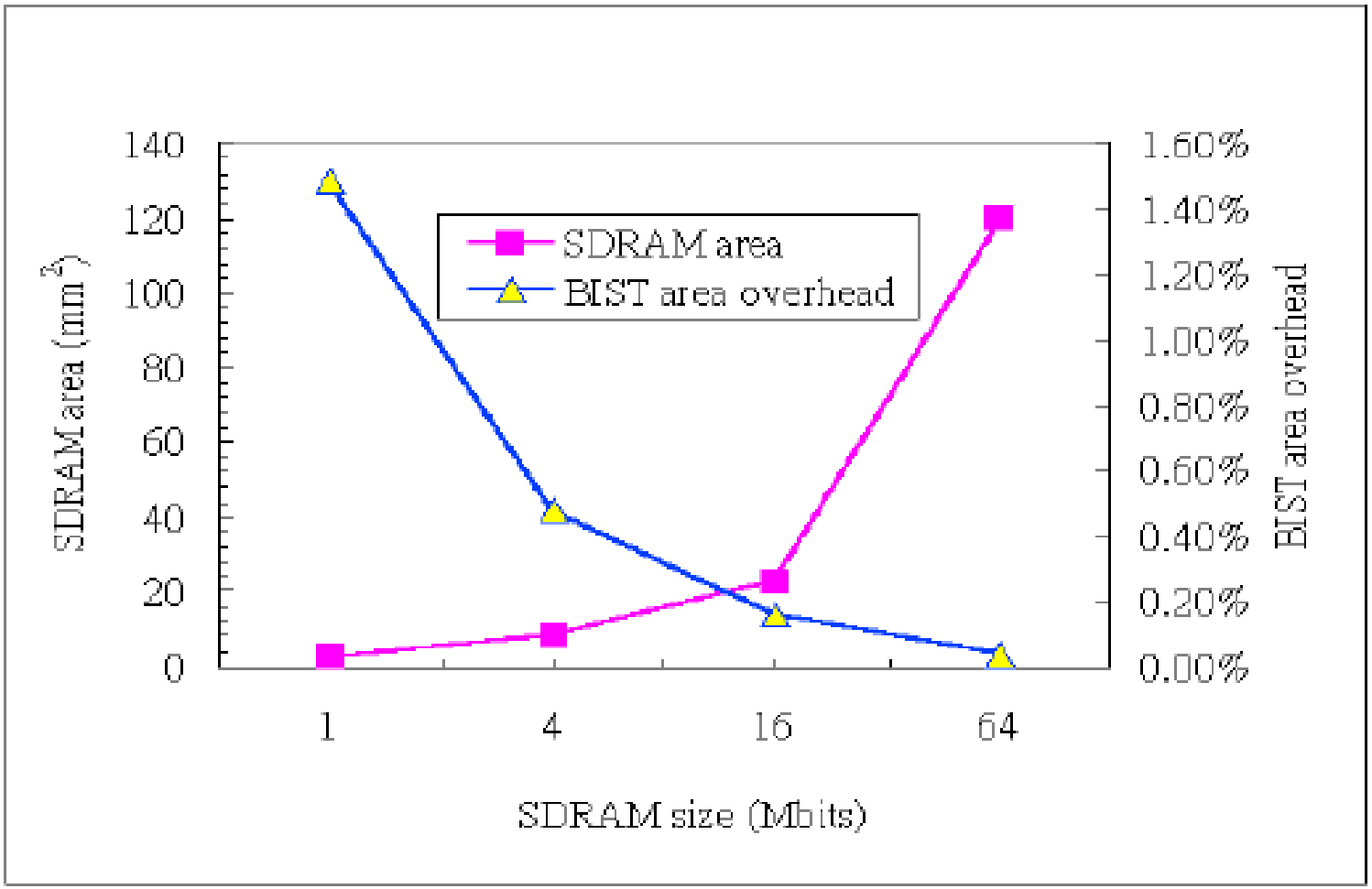
BRAINS Inputs and Outputs [Huang 99]



BRAINS Outputs

- Synthesizable BIST design
  - At-speed testing
  - Programmable March algorithms
  - Optional diagnosis support
    - Built-in Self Diagnosis, BISD
- Activation sequence
  - Test bench
  - Synthesis script

Area Overhead



Summary

- Memory testing are important
- Different memory requires different fault models
- March C is shortest march that detect all 4 fault models: 10N
- RAM BIST are needed for embedded memories
  - EDA tools available

References

- [Abadir 1983] M.S. Abadir and J.K. Reghbati, "Functional Testing of Semiconductor Random Access Memory," ACM Computing Survey, Vol. 15, no.3, pp.175-198, 1983.
- [Huang 1999] C.T. Huang, J. R. Huang, C. F. Wu and C. W. Wu and T. Y Chang, "A Programmable BIST core for embedded DRAM," *IEEE Des. Test Comput.*, 16(1), 59-70, 1999.
- [Marinescu 1982] M. Marinescu, "Simple and Efficient Algorithms for Functional RAM Testing, " IEEE Int'l Test Conf., pp.236-239, 1982.
- [Nair 1979] R. Nair, "Comments on 'An Optimal Algorithm for Testing Stuck-at Faults in Random Access Memory," IEEE Trans. on Computers, Vol. C-26, no. 11, pp.1141-1144, 1979.
- [van de Goor 1991] A.J. van de Goor, *Testing Semiconductor Memories: Theory and Practice*, John Wiley & Sons, Chichester, 1991.
- [Wu 2000] C.F. Wu, C.T. Huang, K. L. Cheng, and C. W. Wu, "Simulation-based test algorithm generation for Random Access Memories," *IEEE VLSI Test Symp.,* pp. 291-296, 2000.
- [Wu 2002] C.F. Wu, C.T. Huang, K. L. Cheng, and C. W. Wu, "Fault Simulation and test algorithm generation for random access memories," *IEEE Trans. CAD*, 21(4), pp.480-490, 2002