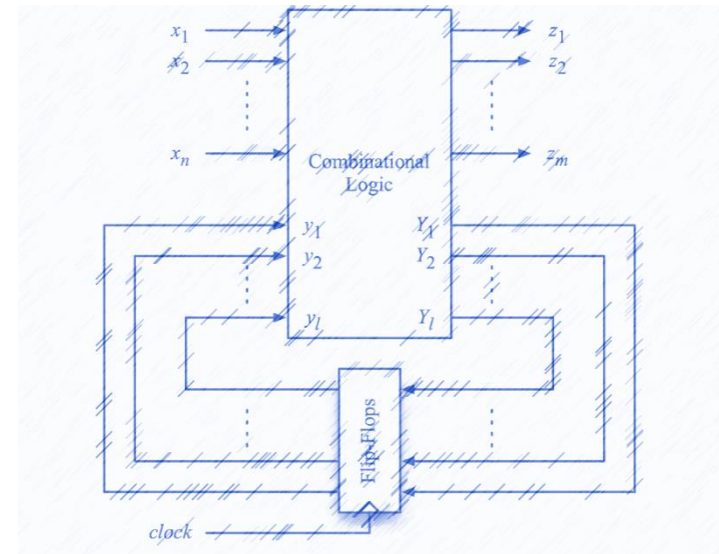


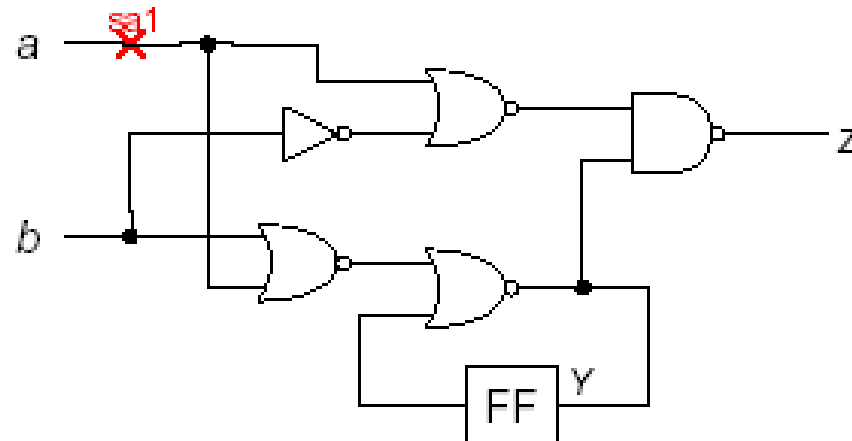
Sequential ATPG

- Introduction
- Time-frame expansion methods
 - ◆ The Extended D-algorithm [Kubo 68]
 - ◆ 9-valued D algorithm [Muth 76]
 - ◆ EBT [Marlett 78], BACK [Cheng 88] *
 - ◆ Summary
- Simulation-based methods*
- Issues of Sequential ATPG*
- Conclusions



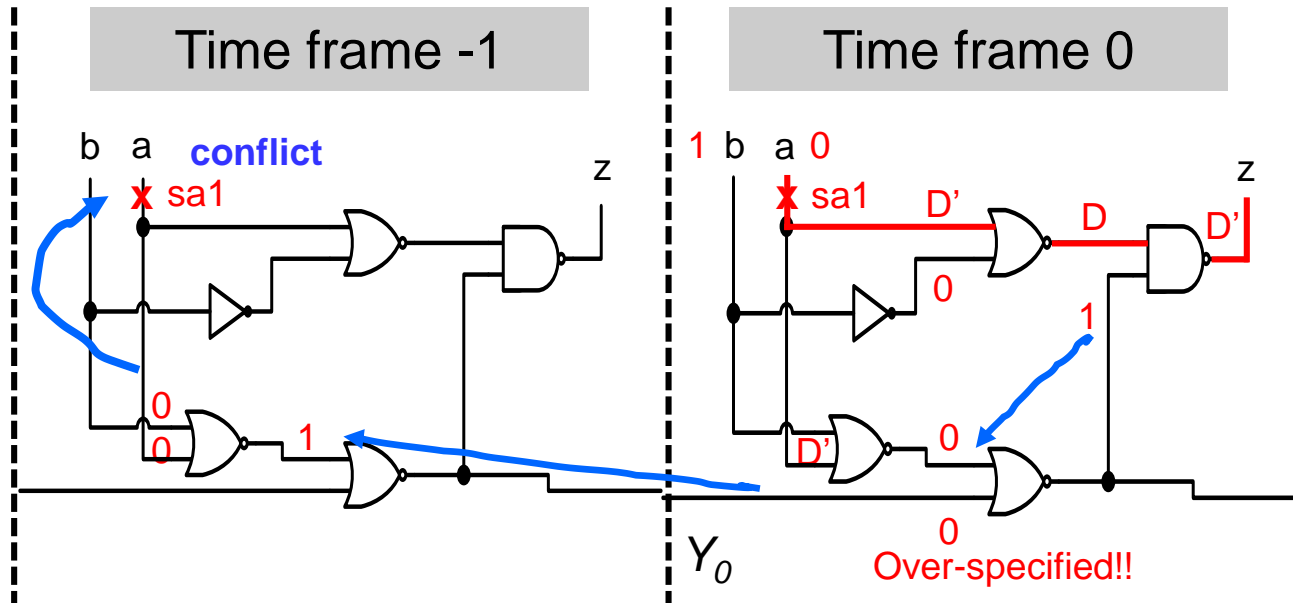
Quiz

Q: Given this test, can we detect the fault?
ANS:



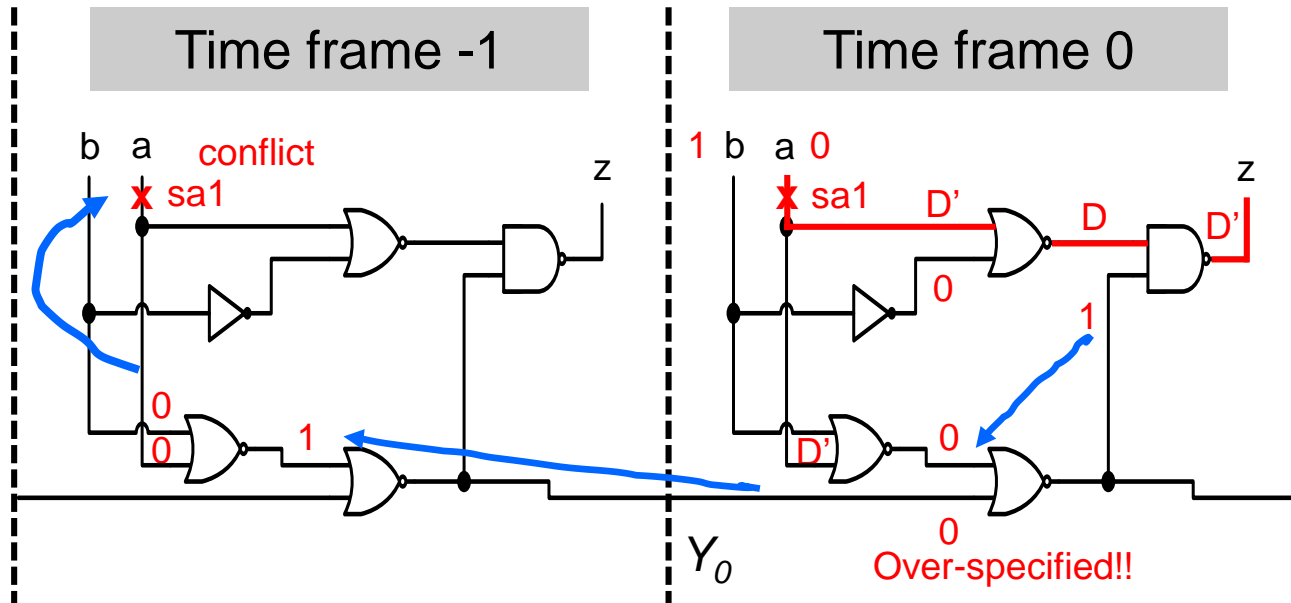
	a	b
v_1	0	0
v_2	0	1

Extended D-algorithm Fails!



- Extended- D algorithm fails due to a conflict
 - ◆ Requires $a=0$ in time frame -1, but SA1
 - ◆ Actually, Y_0 is **over-specified** in 5-valued logic

Why Fails?



- Traditional 5-valued logic (0/0, 1/1, x/x, 0/1, 1/0) is **NOT** sufficient
 - ◆ cannot express **1/x, 0/x, x/0, x/1**

Q: How many total cases do we need?
ANS:

Nine-valued D-algorithm [Muth 76]

- Solution: use **9-valued logic**, instead of 5-valued logic

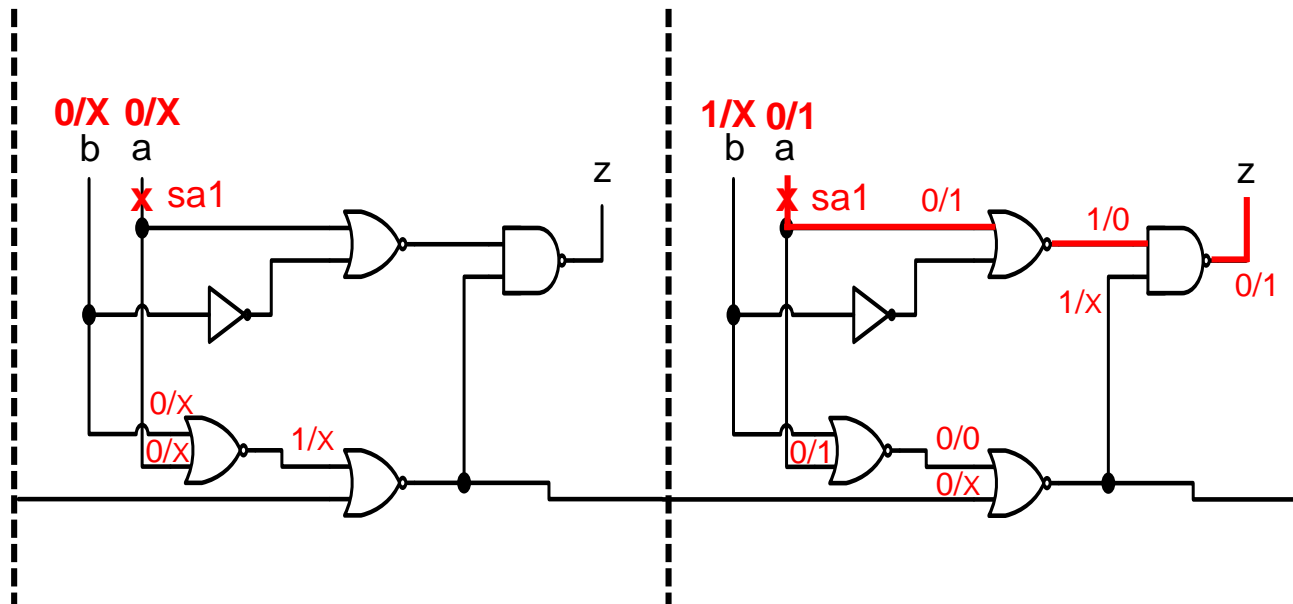
Symbol	Meaning	Roth's 5-valued logic		Muth's 9 valued logic	
		Fault-free	faulty	Fault-free	faulty
D	(1/0)	1	0	1	0
D'	(0/1)	0	1	0	1
0	(0/0)	0	0	0	0
1	(1/1)	1	1	1	1
X	(x/x)	X	X	X	X
G0	(0/x)	-	-	0	X
G1	(1/x)	-	-	1	X
F0	(x/0)	-	-	X	0
F1	(x/1)	-	-	X	1

Nine-valued Truth Table

- Example of AND gate

AND	0	0/x	D'	x/0	x/x	x/1	D	1/x	1
0	0	0	0	0	0	0	0	0	0
0/x	0	0/x	0/x	0	0/x	0/x	0	0/x	0/x
D'	0	0/x	D'	0	0/x	D'	0	0/x	D'
x/0	0	0	0	x/0	x/0	x/0	x/0	x/0	x/0
x/x	0	0/x	0/x	x/0	x/x	x/x	x/0	x/x	x/x
x/1	0	0/x	D'	x/0	x/x	x/1	x/0	x/x	x/1
D	0	0	0	x/0	x/0	x/0	D	D	D
1/x	0	0/x	0/x	x/0	x/x	x/x	D	1/x	1/x
1	0	0/x	D'	x/0	x/x	x/1	D	1/x	1

Nine-Valued Test Generation



Test pattern successfully generated

	a	b
V_1	0	0
V_2	0	1

The figure consists of four logic diagrams arranged in a 2x2 grid, illustrating fault propagation in 9-valued and 5-valued logic.

Top Row: 9-valued logic

- Top-left:** Inputs $b = 0/x$, $a = 0/x$. A fault $sa1$ is on line a . The circuit has two OR gates and one AND gate. The output z is $0/1$.
- Top-right:** Inputs $b = 1/x$, $a = 0/1$. A fault $sa1$ is on line a . The circuit has two OR gates and one AND gate. The output z is $0/1$.

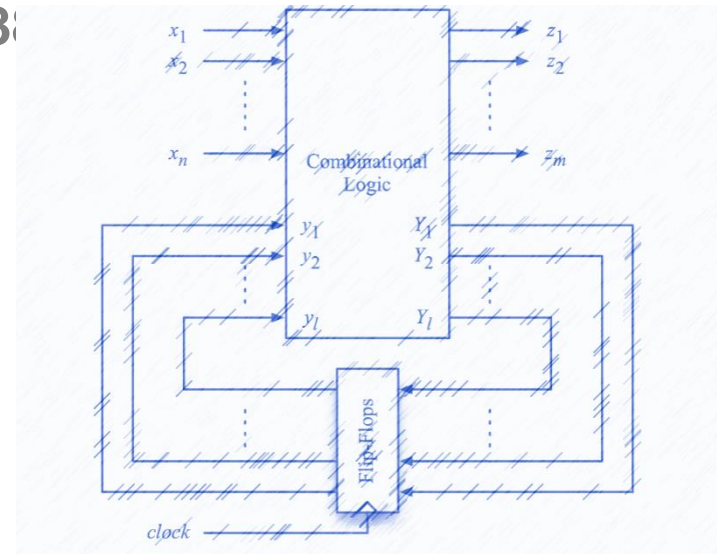
Bottom Row: 5-valued logic

- Bottom-left:** Inputs $b = 1$, $a = 0$. A fault $sa1$ is on line a . The circuit has two OR gates and one AND gate. The output z is 0 .
- Bottom-right:** Inputs $b = 1$, $a = 0$. A fault $sa1$ is on line a . The circuit has two OR gates and one AND gate. The output z is 0 .

The diagrams show how faults propagate through OR and AND gates, with 9-valued logic using more specific values like $1/x$ and $0/x$ compared to 5-valued logic's 1 and 0 .

Sequential ATPG

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- Time-frame expansion methods
 - ◆ The Extended D-algorithm [Kubo 68]
 - ◆ 9-valued D algorithm [Muth 76]
 - express **all nine** possible logic states
 - avoid **over-specification**
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FFT

- Q1: Why **NOT** consider $1/x$, $0/x$, $x/0$, $x/1$ in combinational ATPG?
- Q2: Why **NOT** **backtrace** Y_{-1} one more time frame to the left?

