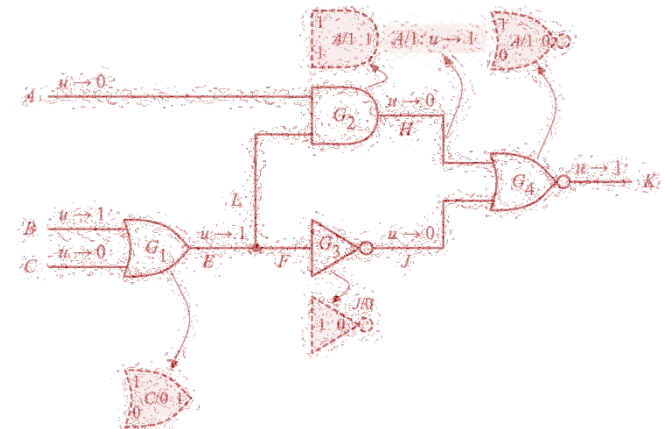


Fault Simulation

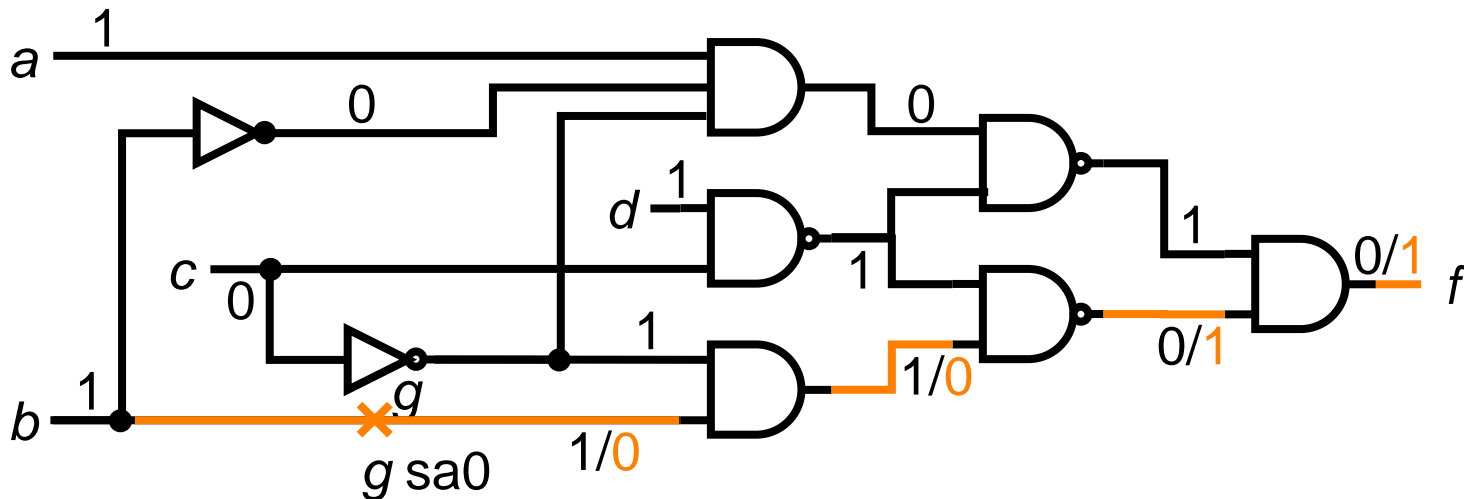
- **Introduction**
- **Fault simulation techniques**
 - ◆ **Serial fault simulation**
 - ◆ **Parallel fault simulation (1965)**
 - ◆ **PPSFP (1985)**
 - ◆ **Deductive fault simulation (1972)**
 - ◆ **Concurrent fault simulation (1974) ***
 - ◆ **Differential fault simulation (1989)**
- **Alternatives to fault simulation**
- **Issues of fault simulation**
- **Concluding remarks**



*** Based on textbook
“VLSI Test Principles and Architectures”
by Wang, Wu, and Wen**

Concurrent Fault Simulation [Ulrich 74]

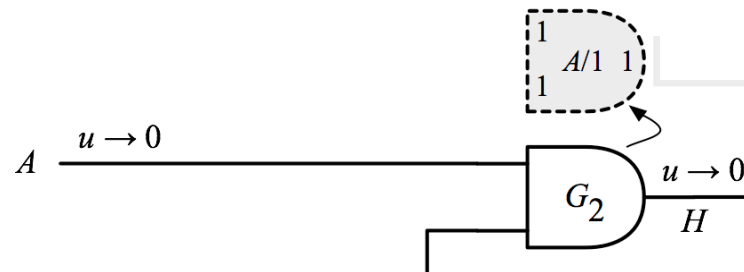
- Observation
 - ♦ Fault activity is often sparse both in time and space
 - ♦ Example: *g sa0* fault only affects lower part of circuit
- Idea: can we just simulate parts of faulty circuit that **differs** from good circuit?



**Concurrent fault sim. Is
event-driven sim. with good/bad events together**

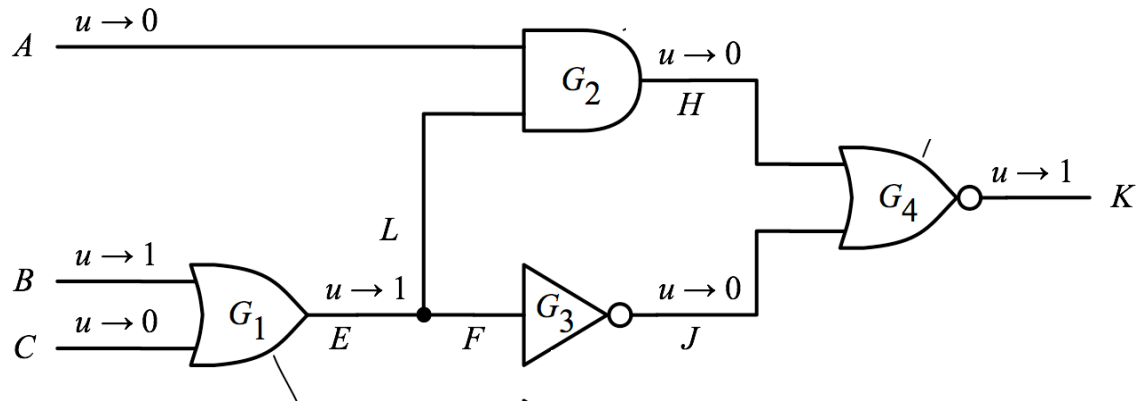
Bad Gate

- Every **good gate** has a list of **bad gates**
- Bad-gate
 - ♦ Represents fault effect of a fault
 - ♦ At least **one gate input or output differs** from its corresponding good-gate if the fault is present
 - ♦ A bad gate is denoted by
 - * Fault: a stuck-at 0 , b stuck-at 0
 - * Faulty input value, faulty output value



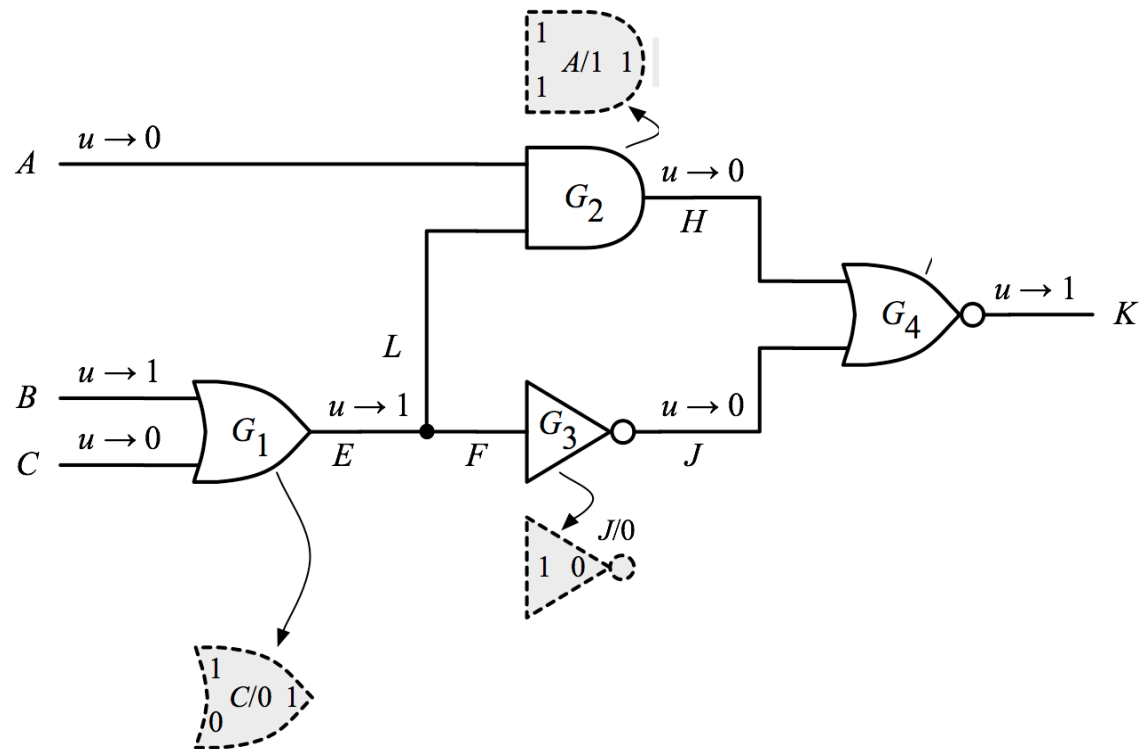
Example (P_1)

- Fault-free simulation, Pattern $P_1 = 010$
- Event-driven simulation
 - **Good events** are events occur in a good circuit



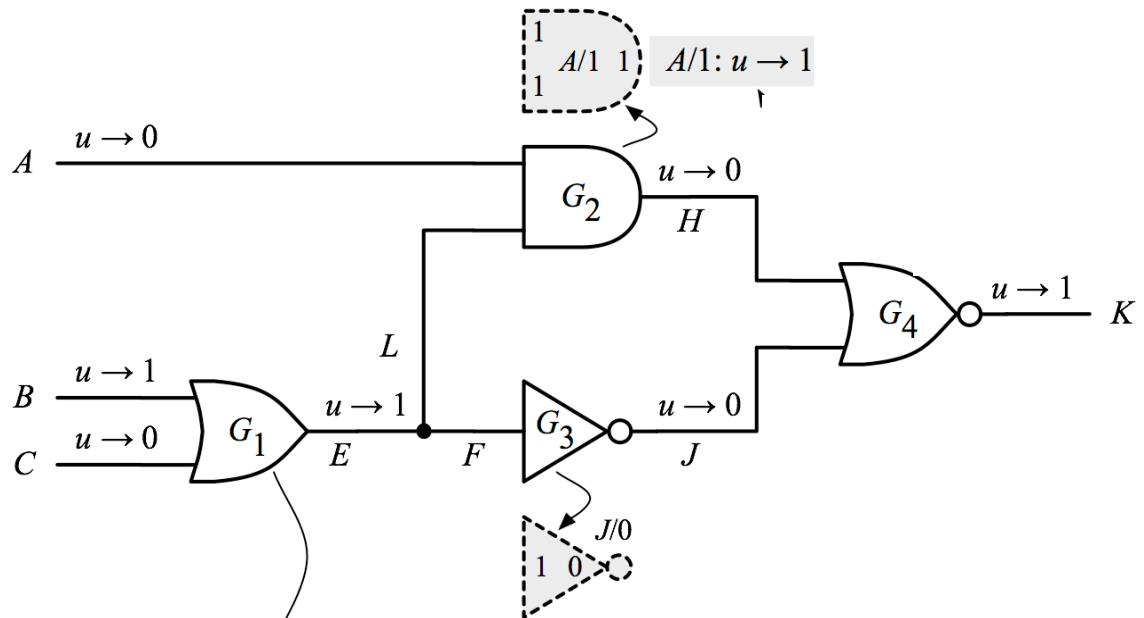
Example (P_1)

- Consider only three faults: $A/1$, $J/0$, $C/0$ (WWW Fig 3.30)
 - Good gates in white: $G_1 \sim G_4$
 - Bad gates in gray: $A/1$, $J/0$, $C/0$
- A bad gate is **invisible** if its faulty output same as good values
 - $C/0$ $J/0$ are invisible
- A bad gate is **visible** if its faulty output different from good values
 - $A/1$ is visible



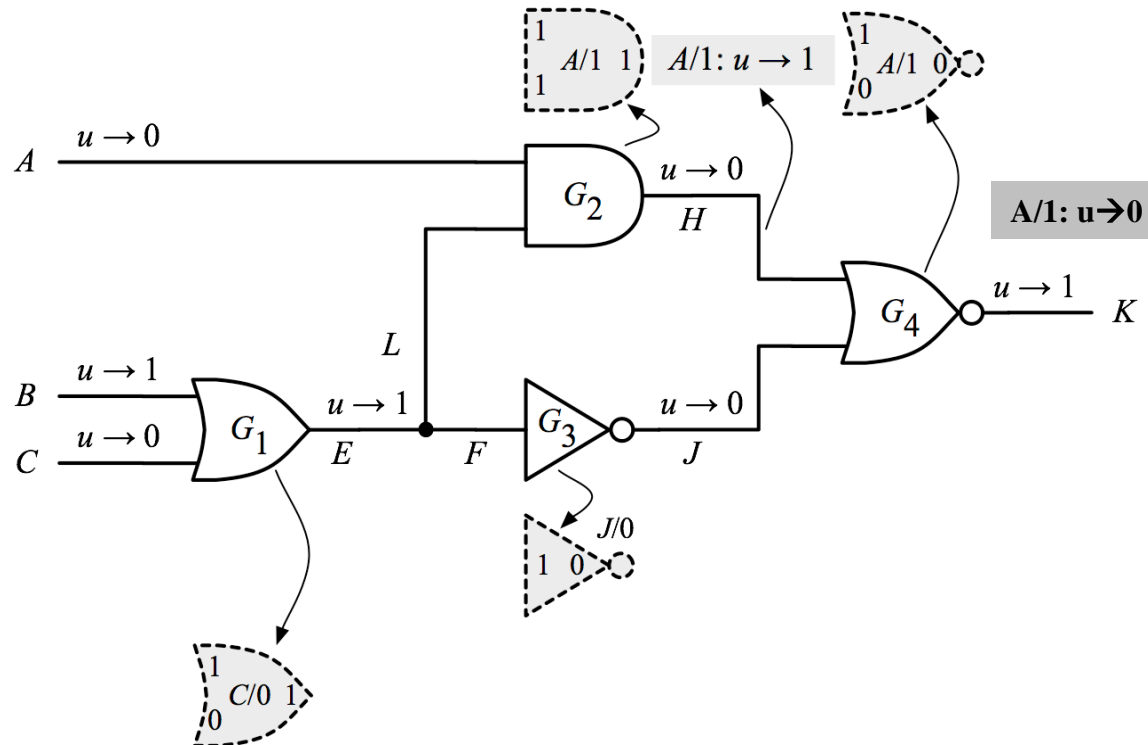
Bad Events

- **Bad events:** Events in faulty circuit, and **different** from good events
- Good events activate both good-gates and bad-gates for evaluation
- Bad events only activate bad-gates of same fault for evaluation
- Only events of visible bad gates will be propagated
 - ♦ Invisible bad gates will not trigger any bad event
- Example:
 - ♦ Good events in white: $A \rightarrow 0$, $H \rightarrow 0$, ...
 - ♦ Bad events in gray
 - * $G_2 \quad A/1: u \rightarrow 1$



Example (P_1)

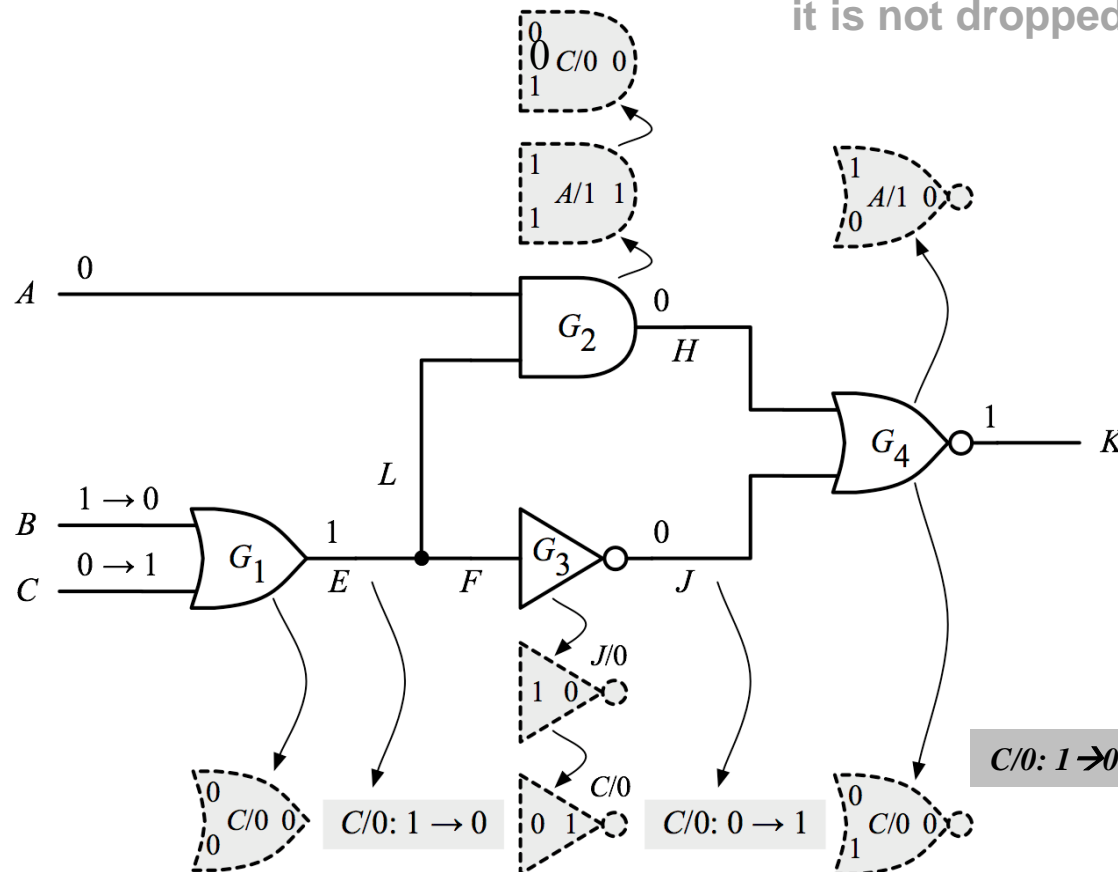
- Bad gate **diverges** from its good gate if its faulty I/O values are different from good values
- Example:
 - ♦ Bad gate (G_4 $A/1$) *diverges* from its good gate
 - ♦ $A/1$ is detected by P_1



Example (P_2)

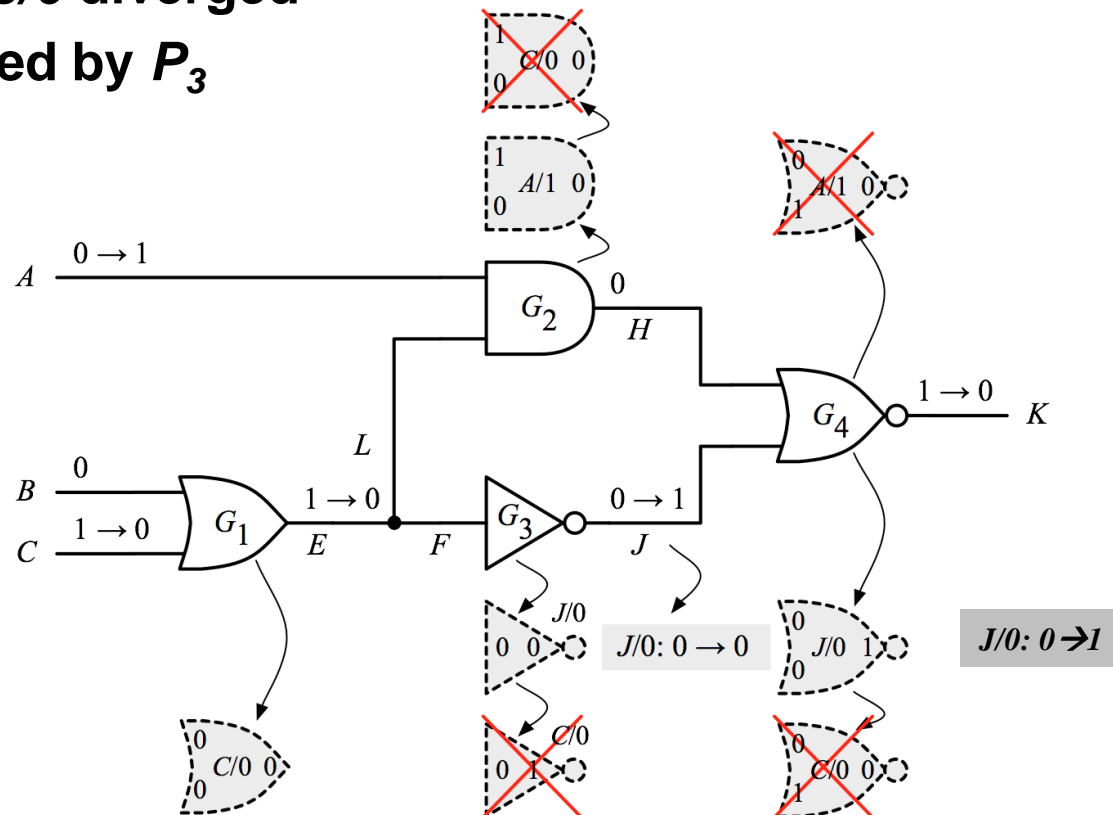
- $P_1 \rightarrow P_2$ 010 \rightarrow 001; Note: **no other good event inside circuit**
- **C/0** becomes newly visible
- **A/1, C/0** detected by P_2

Although A/1 has been detected, it is not dropped for demo purpose



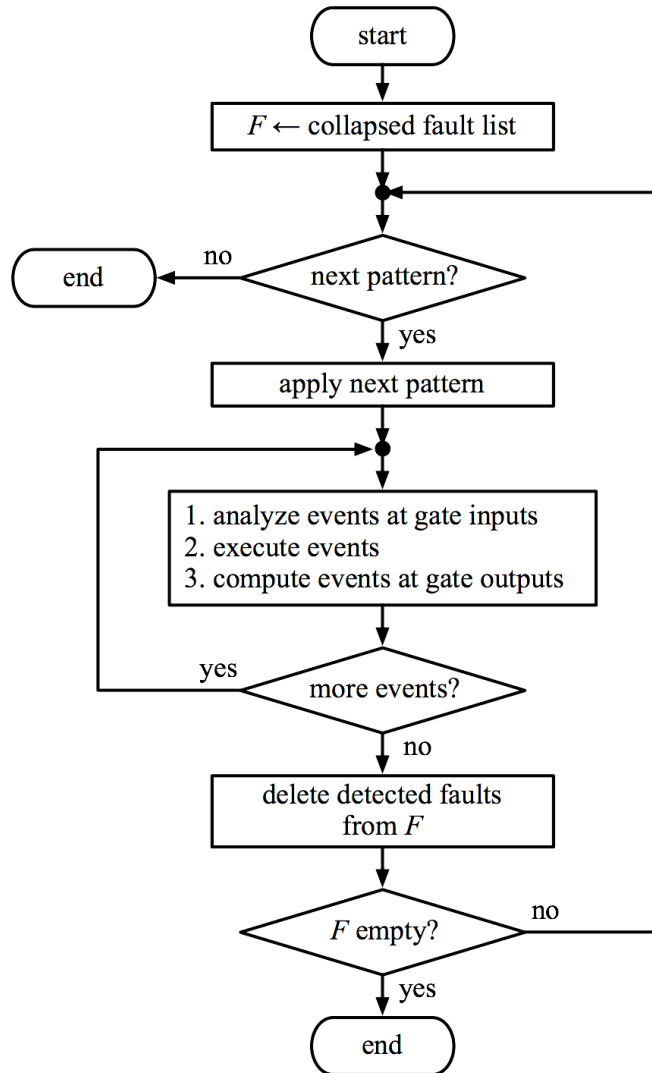
Example (P_3)

- $P_2 \rightarrow P_3$ 001 \rightarrow 100
- Bad gate **converges** (disappear) to its good gate if its faulty I/O values become same as good values
- Example : Bad gates A/1 C/0 converged
 - ♦ Bad gate J/0 diverged
 - ♦ J/0 detected by P_3



Concurrent Fault Sim. Flow

- WWW Fig 3.33



Concurrent Fault Simulation Summary

- **Advantages**
 - ◆ Even faster than deductive fault simulation
 - ◆ Delay fault can be supported
 - ◆ Sequential fault simulation can be supported
- **Disadvantage**
 - ◆ Difficulty in memory management
 - * Memory requirement not predictable

FFT

- Q1: In P2, why no bad events there?
- Q2: Why delay fault is supported?
- Q3: Why sequential circuit ok?

Q: why no bad events here?

