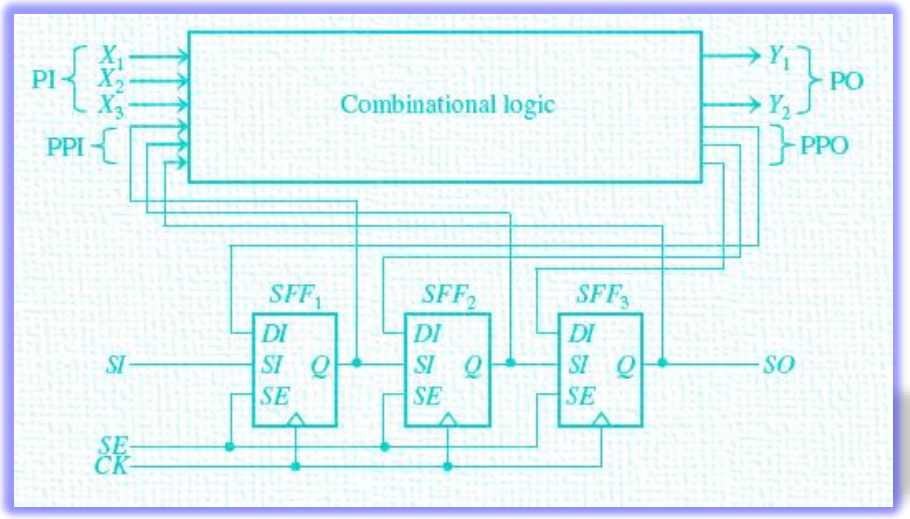
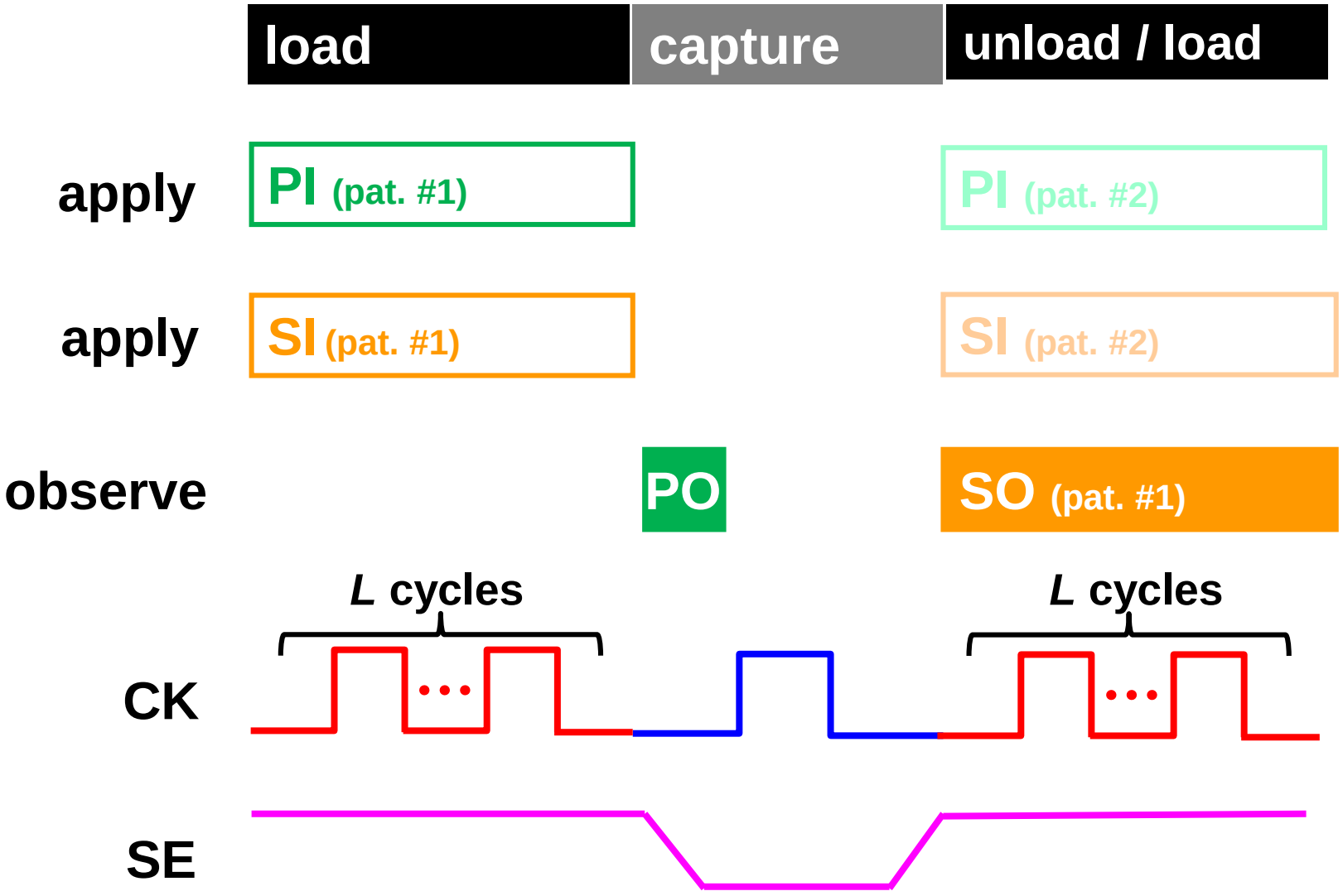
DFT - Part 1

- Introduction
- Internal Scan
- Scan Design Flow
- **Issues and Solutions**
  - **Long test time**
  - **Large test data**
  - **Too much overhead**
  - **How to Test DFT**
- **Conclusion**



SSF Operation (review)



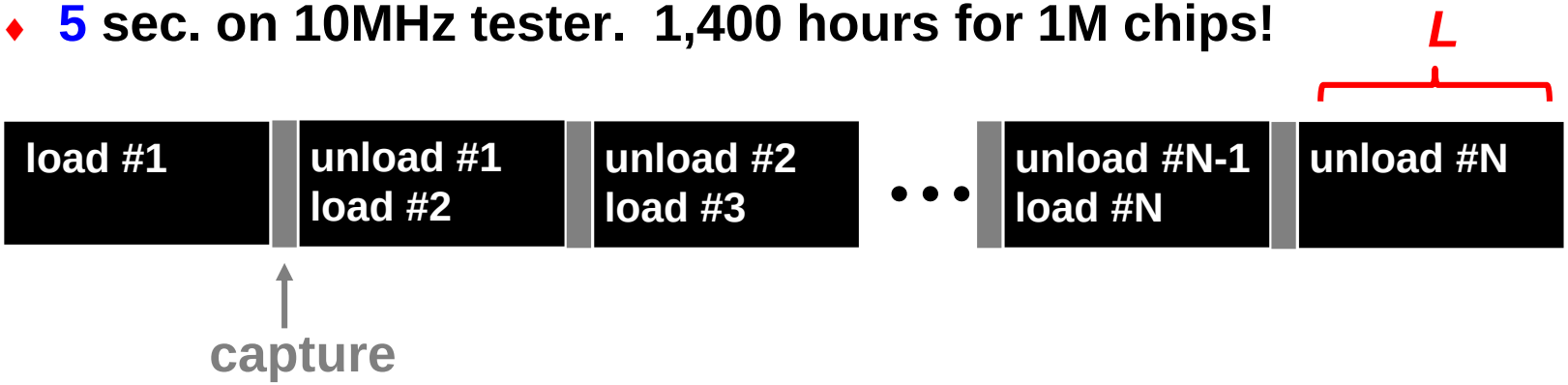
Issue #1: Long Test Time

- How many test cycles do we need?
  - L = length of scan chain ; $N_{pattern}$ = *number of test patterns*

$$(N_{pattern} + 1) \times L + N_{pattern}$$

shift capture

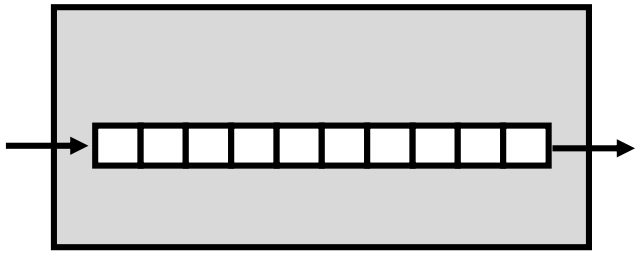
- Example: Apply 5,000 test patterns to a CUT of 10K SFF
  - Single scan chain L = 10,000 ; $N_{pattern}$ = 5,000
  - Total 50,015,000 cycles
    - (5,000+1) x 10,000 shift cycles
    - 5,000 capture cycles
  - 5 sec. on 10MHz tester. 1,400 hours for 1M chips!



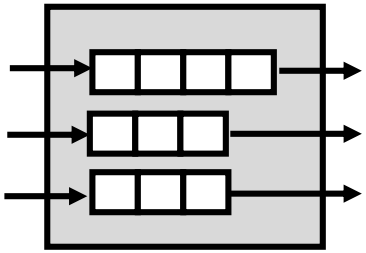
How to Save Test Time?

- To shorten *L*, we can partition SFF into *n* scan chains
  - *L* is determined by *longest* scan chain in CUT
    - because ATE shifts all scan chains together
  - Penalty: More scan I/O pins (see FFT)
- Example: 10K SFF partitioned into three scan chains
  - *L* = max { 3K, 3K, 4K} = 4K
  - 60% reduction in test time!

Single scan chain
n=1, N_{SFF}=10K, *L*=10K



Three scan chains
n=3, N_{SFF}=1K, *L*=4K



Multiple Chains Reduce Test Time

Quiz

Q1: Apply 10K patterns to CUT of 6M SFF in three scan chains

L_1 = 1M ; L_2 = 1M; L_3 = 4M

How many cycles do we need to test this CUT?

Q2: What if we balance scan length: L_1 = 2M ; L_2 = 2M; L_3 = 2M

$$(N_{pattern} + 1) \times L + N_{pattern}$$

shift capture

A1:

A2:

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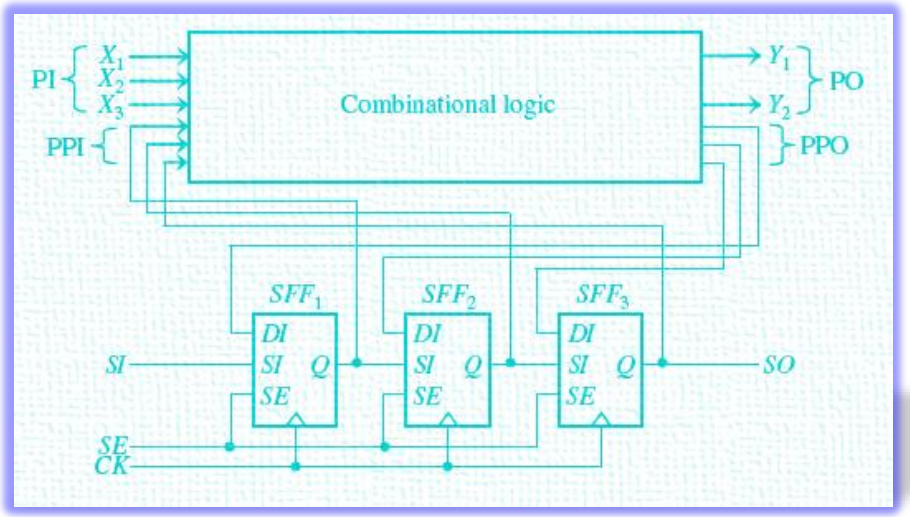


Issue #2: Large Test Data

- How many test data stored on ATE?

  Scan in data: $N_{pattern}$ x N_{SFF}

  Scan out data: $N_{pattern}$ x N_{SFF}

  PI data: $N_{pattern}$ x N_{PI}

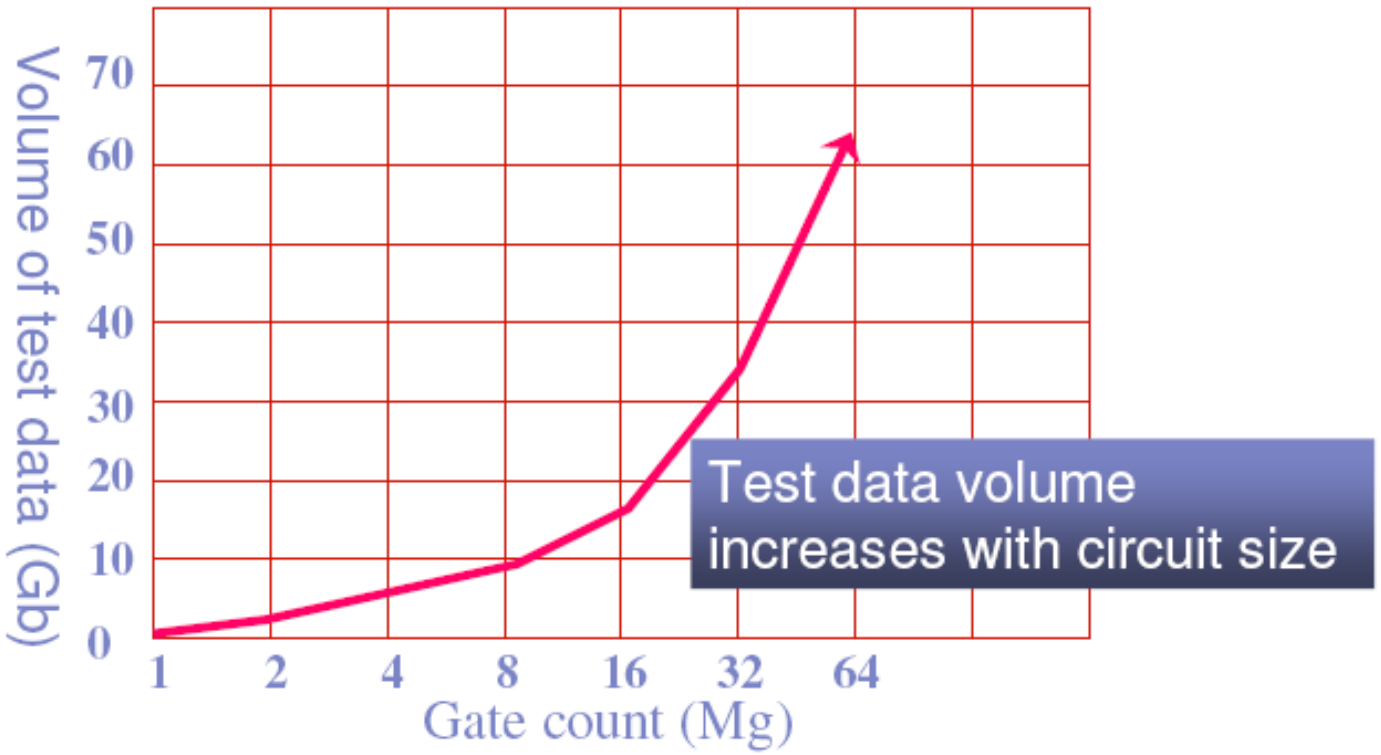
  PO data: $N_{pattern}$ x N_{PO}

N_{SFF} =number of scan FF
N_{PI} =number of PO
N_{PO} =number of PI

- Example:
  - Apply 10K patterns to CUT of 6M SFF
  - Suppose N_{PO}=50, N_{PI}=20
    - PI data = 10K x 20 = 200M bits
    - PO data = 10K x 50 = 500M bits
    - Scan in data = 10K x 6M = 60G bits!
    - Scan out data = 10K x 6M = 60G bits!

Test Data Volume Skyrockets

- Suppose ATE has 500 pins, each has 64Mb memory
  - Total ATE memory available = 32Gb
  - 60Gb cannot fit in ATE!
- Q: Does multiple scan chain reduce test data volume?



(Source: Blyler, Wireless System Design, 2001)

Quiz

Q: Apply 10K patterns to CUT of 6M SFF in three scan chains
L_1 = 2M ; L_2 = 2M; L_3 = 2M
How many scan test data do we need?

A:

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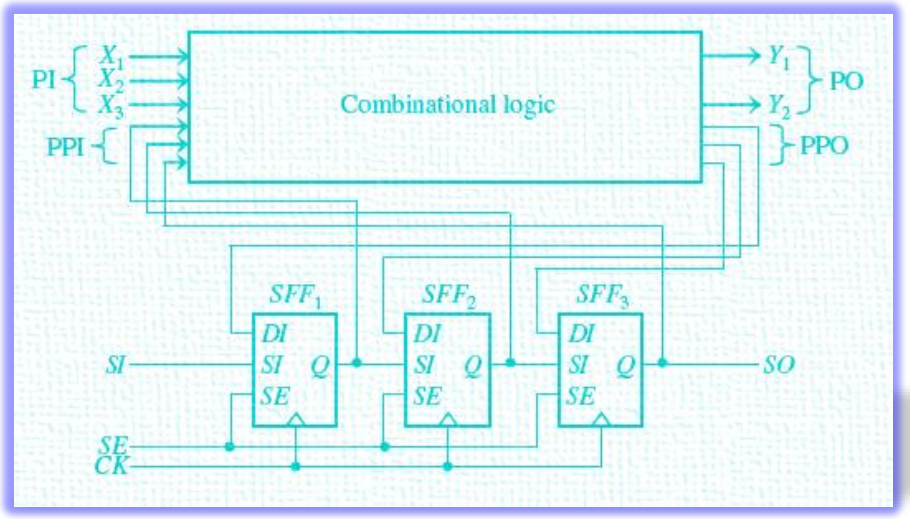
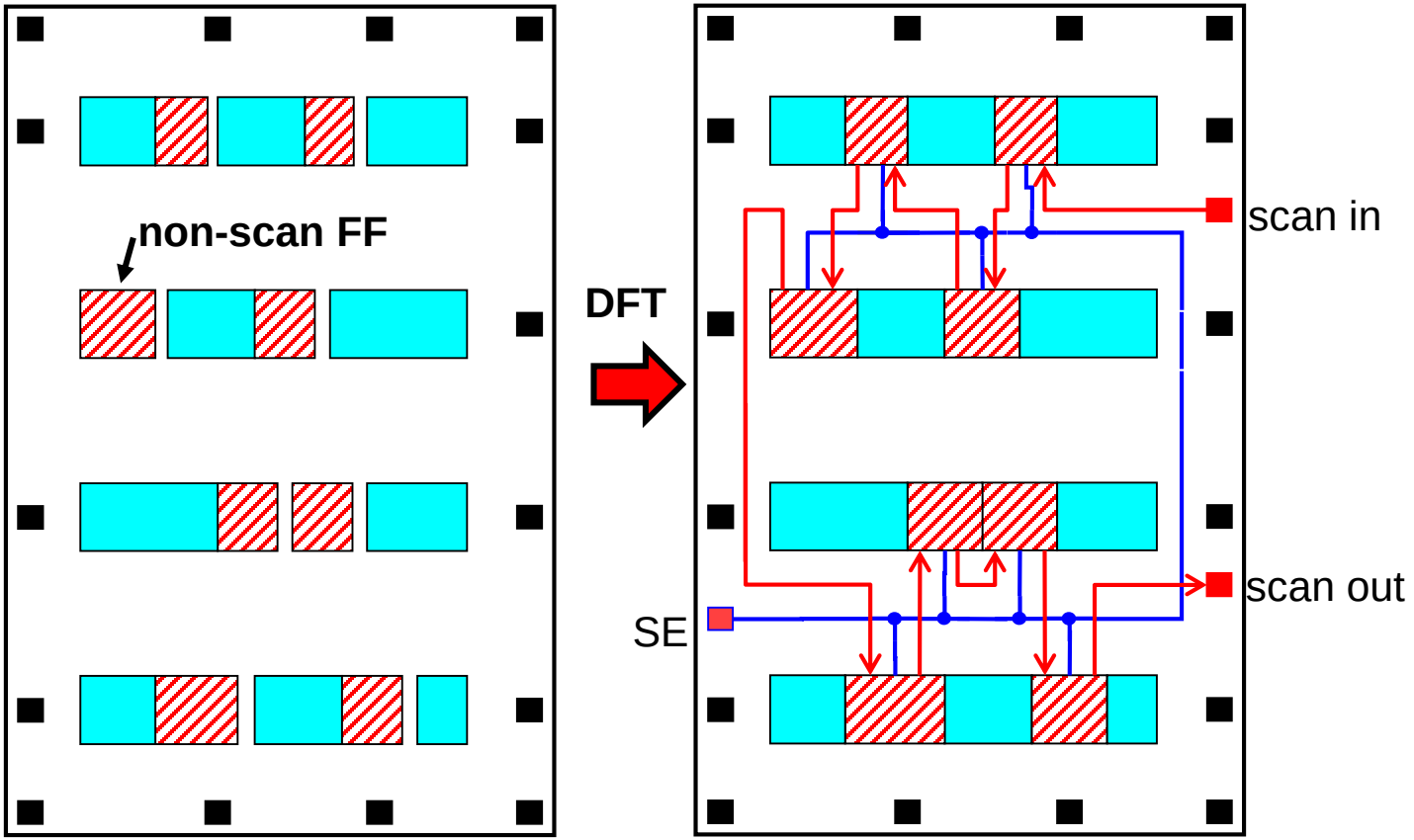


Issue #3: Too Much Overhead

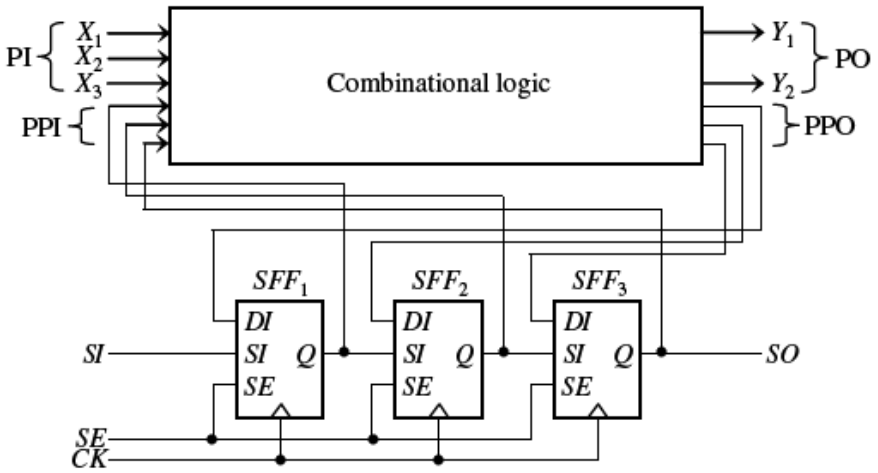
- **Area** overhead, **Timing** overhead, **Power** overhead



DFT about 5% Timing, 10% Area/Power Overhead

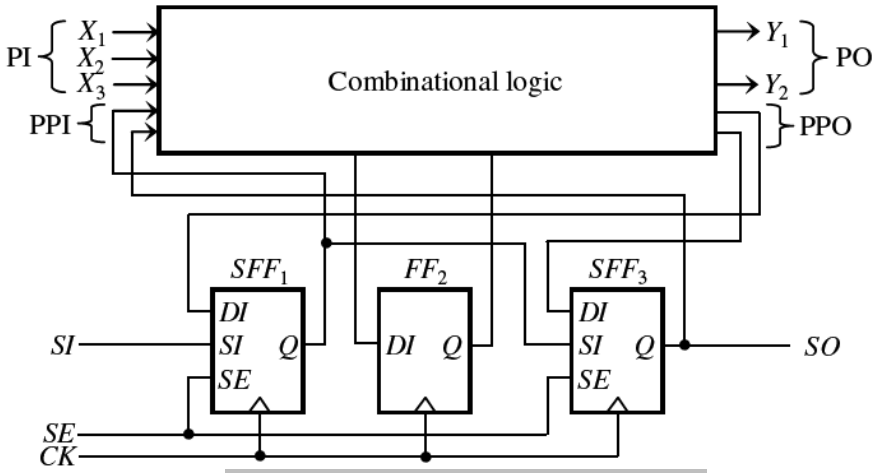
How to Reduce Overhead? Partial Scan

- ***Full Scan***
  - ♦ **Every FF scannable**
  - ☹ **More overhead**
  - ☺ **Higher fault coverage**
  - ☺ **Shorter ATPG run time**



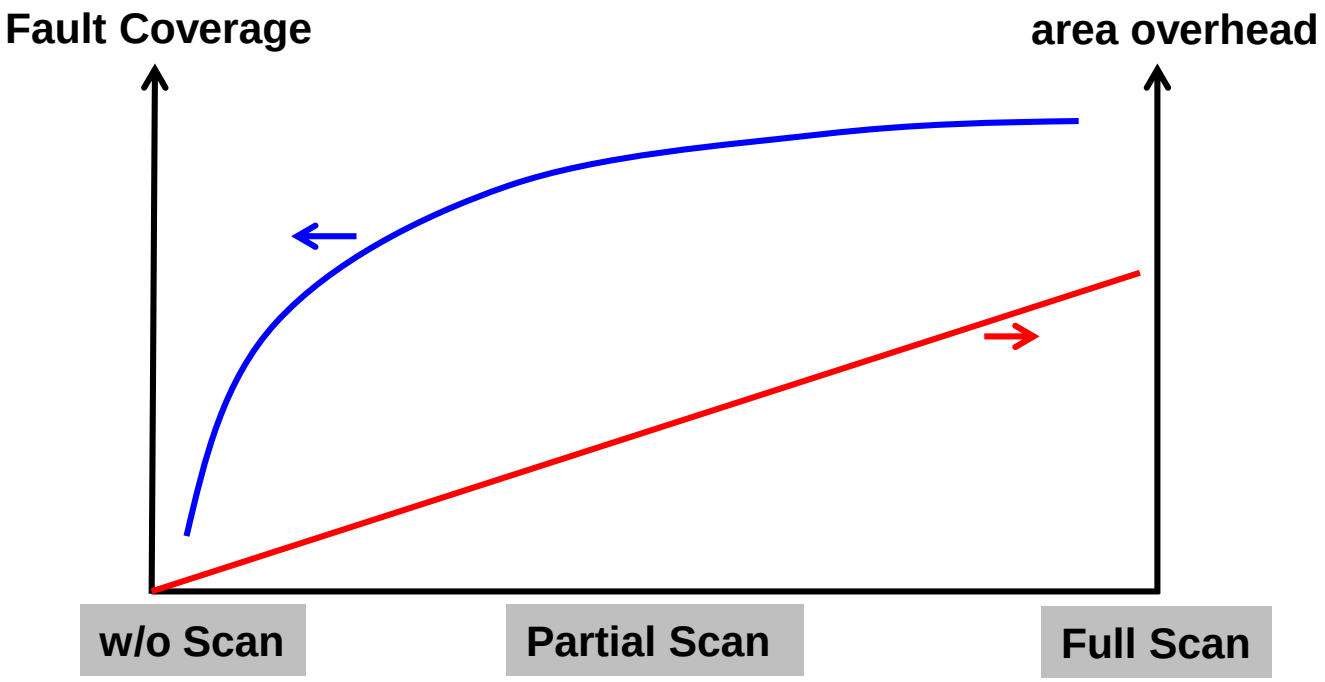
MUXed-D full scan

- ***Partial Scan***
  - ♦ **Some FF not scannable**
  - ☺ **Less overhead**
  - ☹ **Lower fault coverage**
  - ☹ **Longer ATPG run time**



MUXed-D partial scan (WWW Fig. 2.17)

Trade-off Area and FC



S5378 Example (BA Table 14.1 modified)

	w/o scan	Partial scan	Full scan
no. of logic gates (N_L)	2,781	2,781	2,781
no. of non-Scan FF (N_{NFF})	179	149	0
no. of Scan FF (N_{SFF})	0	30	179
area overhead*	0.0%	1.63%	9.73%
no. of faults	4,603	4,603	4,603
(PI+PPI) / (PO+PPO)	35/49	65/79	213/228
Fault Coverage	70.9%	93.7%	99.1%
CPU time (SUN 200MHz)	5,533 s	727 s	5 s
no. of Test Patterns	414	1,117	585
no. of Test Cycles	414	34,657	105,479

$$*overhead = \frac{Scan - w/o\_scan}{w/o\_scan}$$

1 non-scan FF = 5 logic gates
1 scan FF = 7 logic gates

Quiz

Q: Please calculate partial scan area overhead

Assume 1 non-scan FF = 5 logic gates

Assume 1 scan FF = 7 logic gates

$$*overhead = \frac{Scan - w/o\_scan}{w/o\_scan}$$

	w/o scan	Partial scan	Full scan
no. of logic gates (N_L)	2,781	2,781	2,781
no. of non-Scan FF (N_{NFF})	179	79	0
no. of Scan FF (N_{SFF})	0	100	179
area overhead	0.0%	?	9.73%

A:

CH1: DFT or Not?

- Q: Is it economical to insert DFT?
- A: Yes. This is true for many products.
  - Although *Y* drops, *DL* improves significantly

$$DL = 1 - Y^{(1-FC)}$$

Item	w/o DFT	with DFT
Total # of Dies	1,000,000	900,000
Yield	98%	97%
FC fault coverage	70%	99%
DL =1-Y$^{(1-FC)}$	6,043 DPM	304 DPM
Sales=D x Y x $1	980,000	873,000
Repair cost=D x Y x DL x $100	592,163	26,587
Profit = S – R	387,837	846,413

Despite Overhead, DFT Is Worth Doing!

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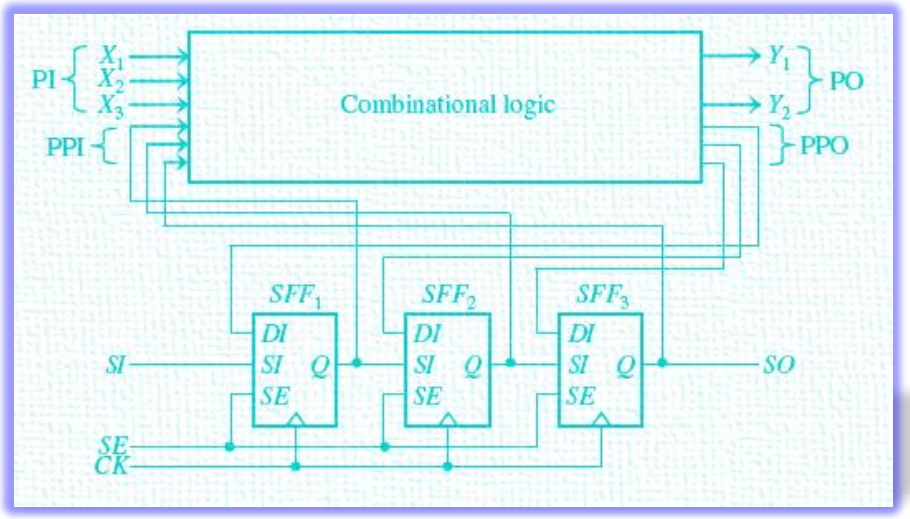
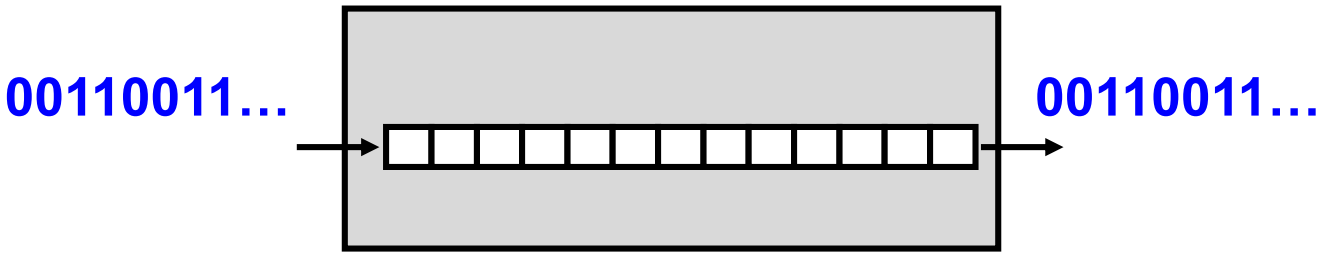


How to Test FF Scan Chain?

- Scan chains themselves can be faulty. Must be tested too
- Scan chain *integrity test*
  - A sequence 00110011… is shifted in and shifted out
  - No capture clock
  - Each SFF undergo four transitions: 0→1, 0→0, 1→1, 1→0
- Detects all stuck-at faults, transition faults in scan chains

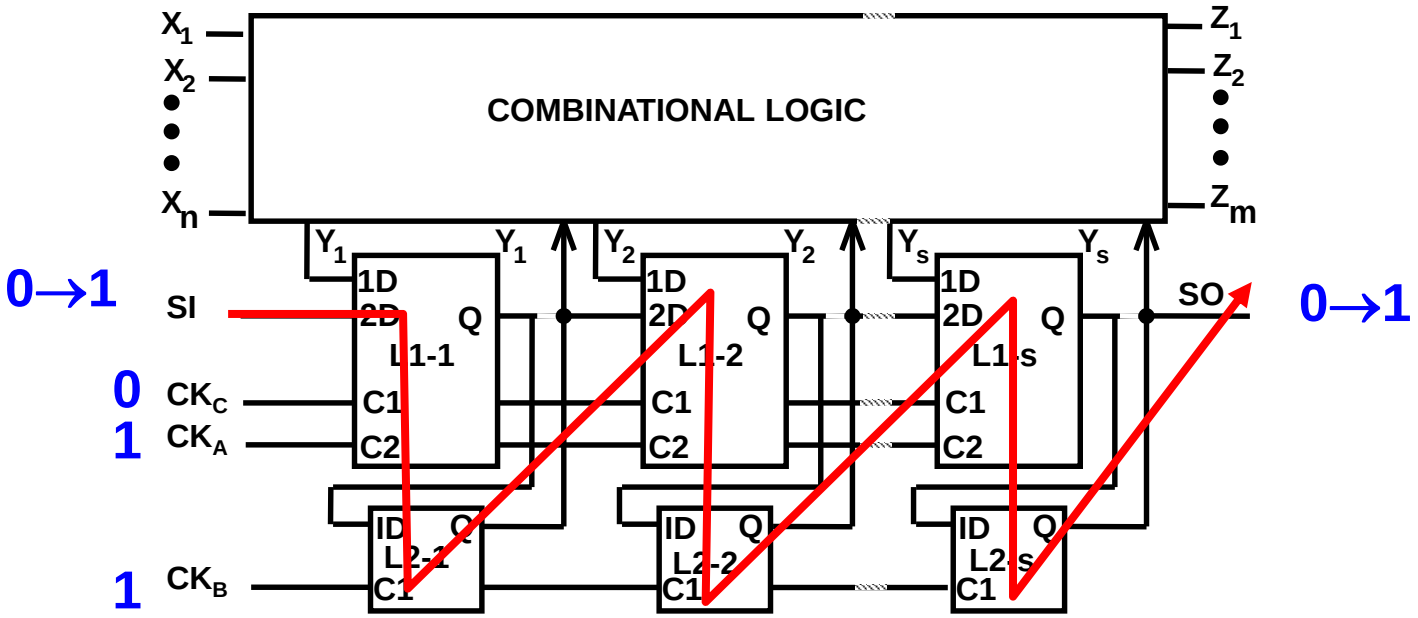


$$(N_{pattern} + 1) \times L + N_{pattern} + 2L$$

shift capture scan integrity

How to Test LSSD Scan Chain?

- LSSD *scan chain* ***Flush Test***
- CK_C = 0, CK_A =1, CK_B = 1
  - A combinational path from SI to SO is formed
  - Apply SI= 0→1 transition at SI
  - Measure delay time from SI to SO



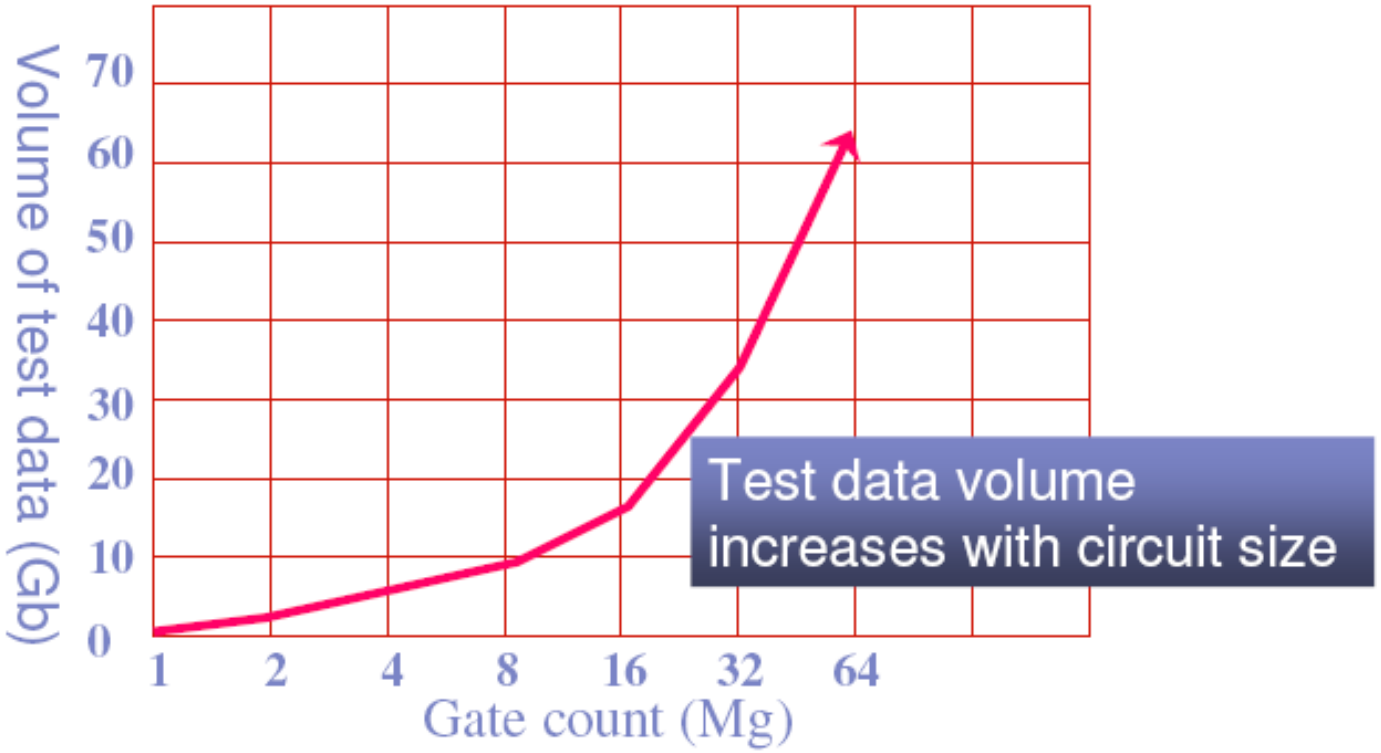
Summary

- Four Issues of scan
  - Long test time
    - Multiple scan chains
  - Large test data volume
    - see *Test Compression* chapter
  - Too much overhead
    - Partial scan
  - Test scan chain itself
    - 00110011 or flush test
- Despite above issues, scan is worth doing!

$$(N_{pattern} + 1) \times L + N_{pattern} + 2L$$

FFT

- **Q1: We want to reduce test time so we have many scan chains. Can we share scan I/O pins to reduce pin overhead ?**
- **Q2: Multiple scan chain does NOT reduce test data. What can we do?**



(Source: Blyler, Wireless System Design, 2001)

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