VLSI Testing
積體電路測試

Logic Built-In Self Test (BIST)
Part 1: Test Pattern Generator

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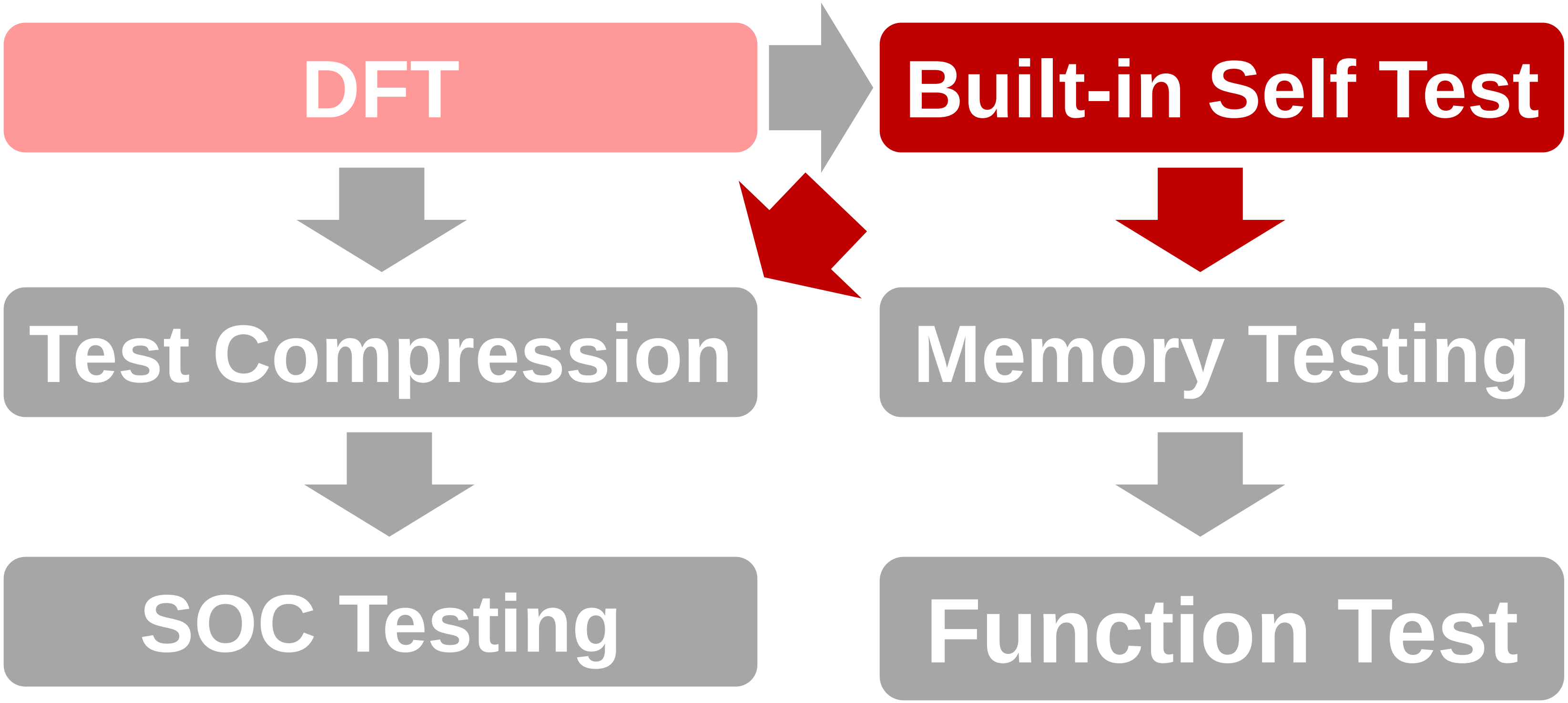
* Some pictures are courtesy of Prof. Shi-yu Huang, NTHU

Course Roadmap (Design Topics)



DFT

Built-in Self Test

Test Compression

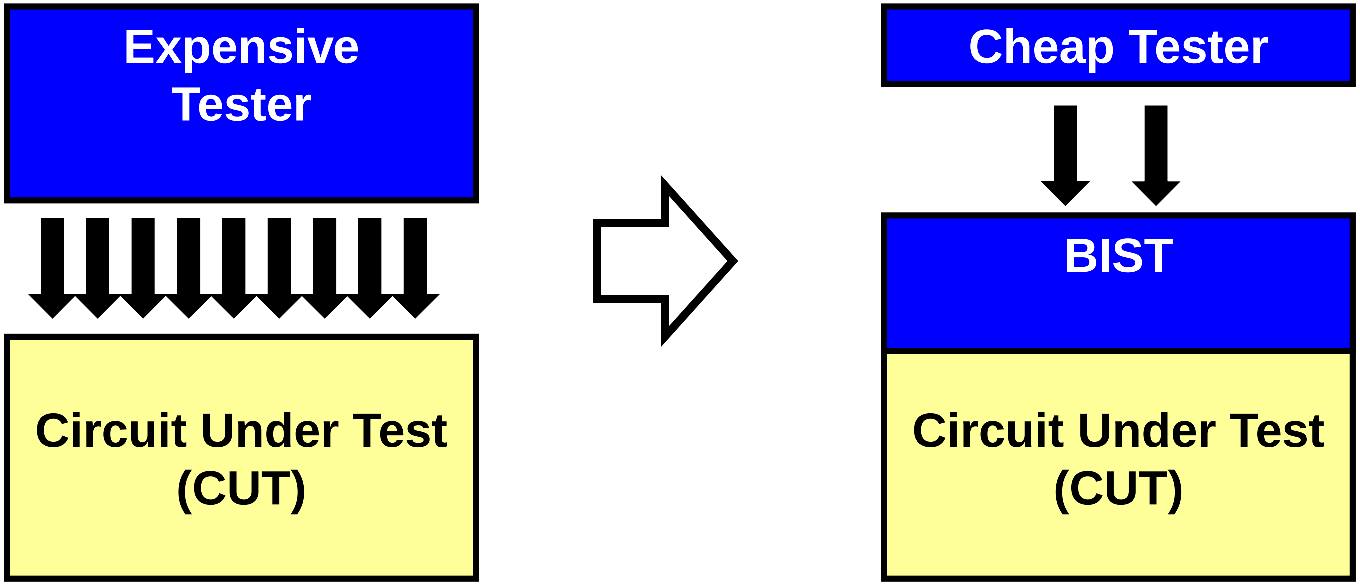
Memory Testing

SOC Testing

Function Test

Motivating Problem

- Your manger complains tester is too expensive.
- Please design a circuit to test the chip itself!



Why Am I Learning This?

- **Built-in Self Test (BIST) can**
  - **Remove large expensive testers**
  - **Test chips at high speed**
  - **Test chips online**

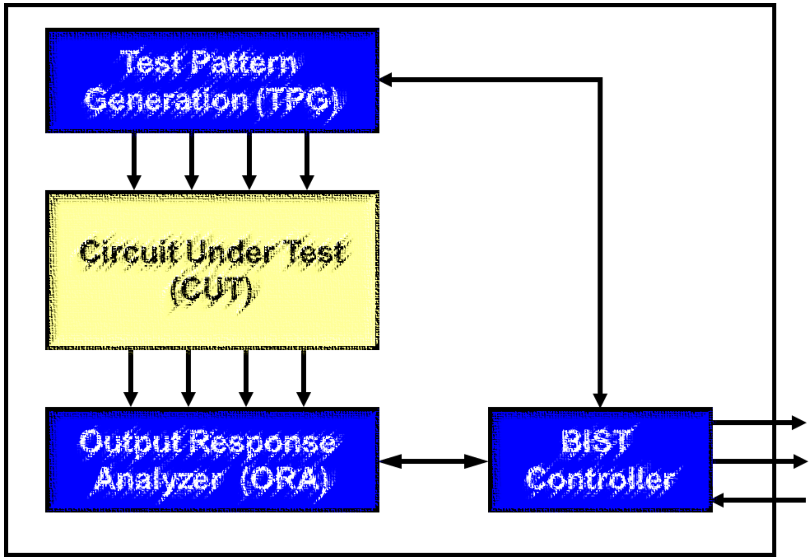
"Testing oneself is best when done alone. "

君子慎其獨也

(Jimmy Carter)

BIST Outline

- Part 1
  - Introduction
  - Test Pattern Generation
- Part 2 (Next chapter)
  - Output Response Analysis
  - BIST Architecture
  - Problems and solutions
  - Conclusions



Built-in Self Test

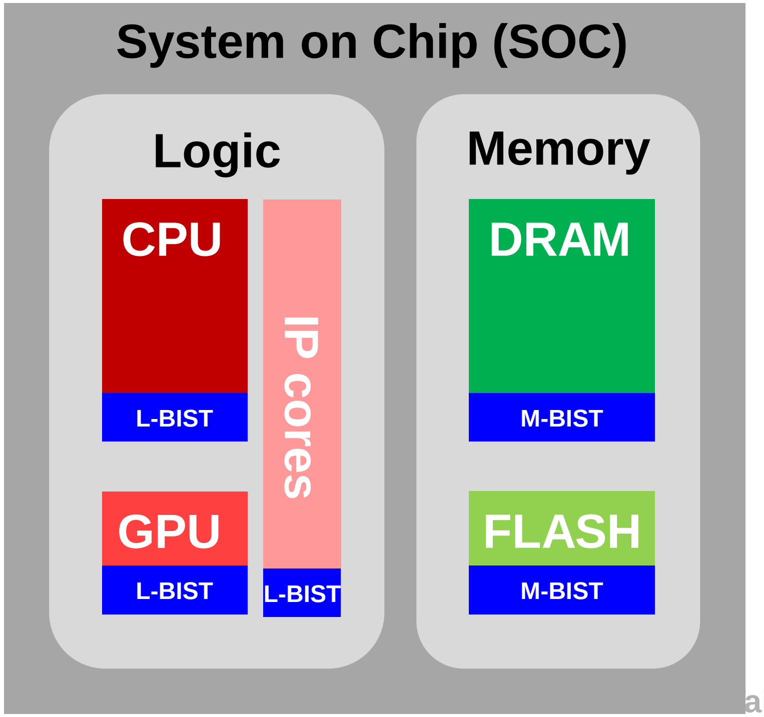
- Definition
  - Capability of hardware/software to carry out explicit test of itself
- Levels of BIST
  - System-level self test
    - system self test of mainframe computer
  - Board-level self test
    - so we can replace a bad board in a system
  - Chip-level self test
    - focus of this lecture

123rf.com

IBM Blue Gene

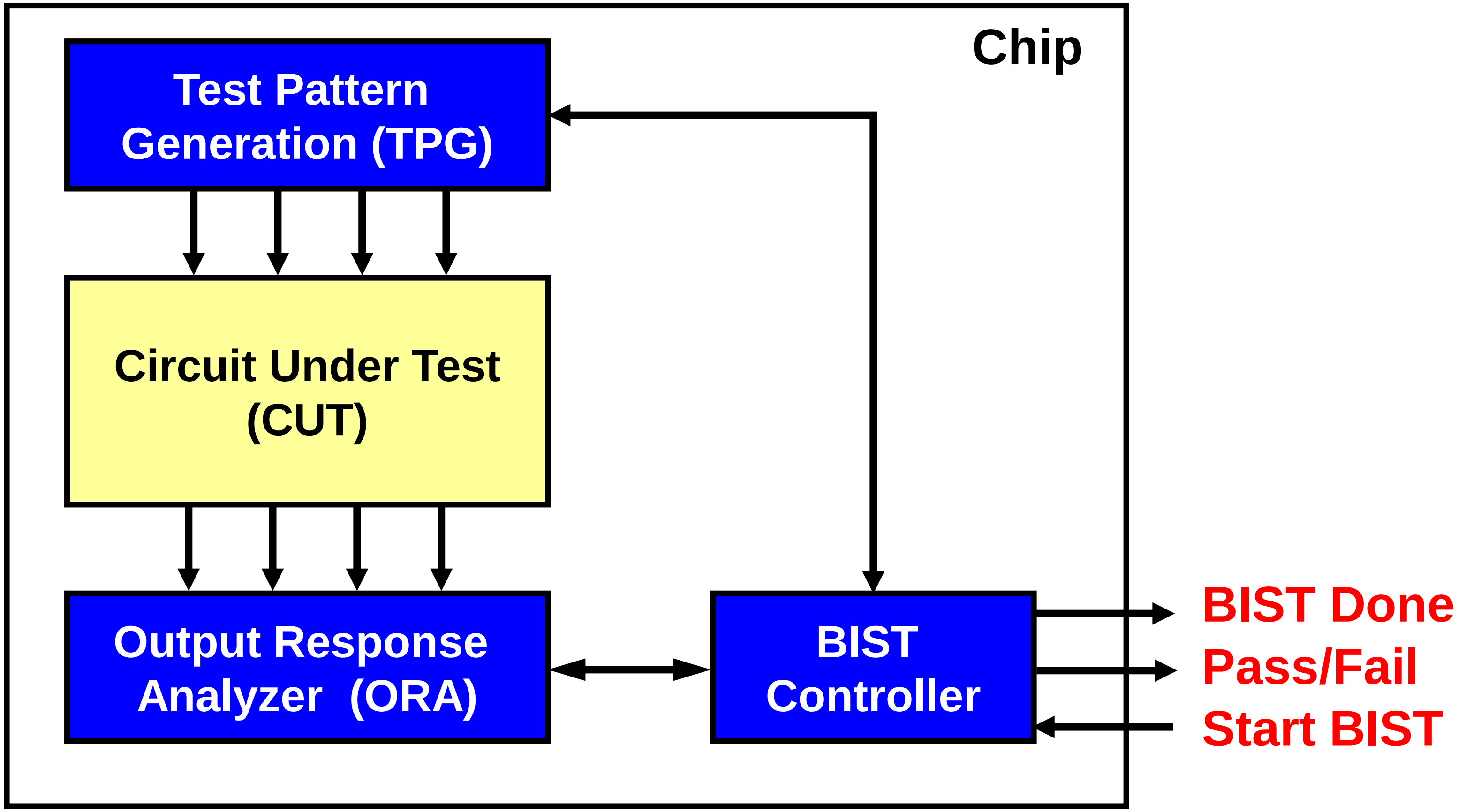
Categories of Chip-level BIST

- Based time of test
  - *On-line BIST*
    - On-line testing while chip in normal operation
    - e.g. error detection and correction for RAM
  - *Off-line BIST*
    - Off-line testing while chip not in normal operation
    - Focus of this talk
- Based on CUT
  - Logic BIST
  - Memory BIST



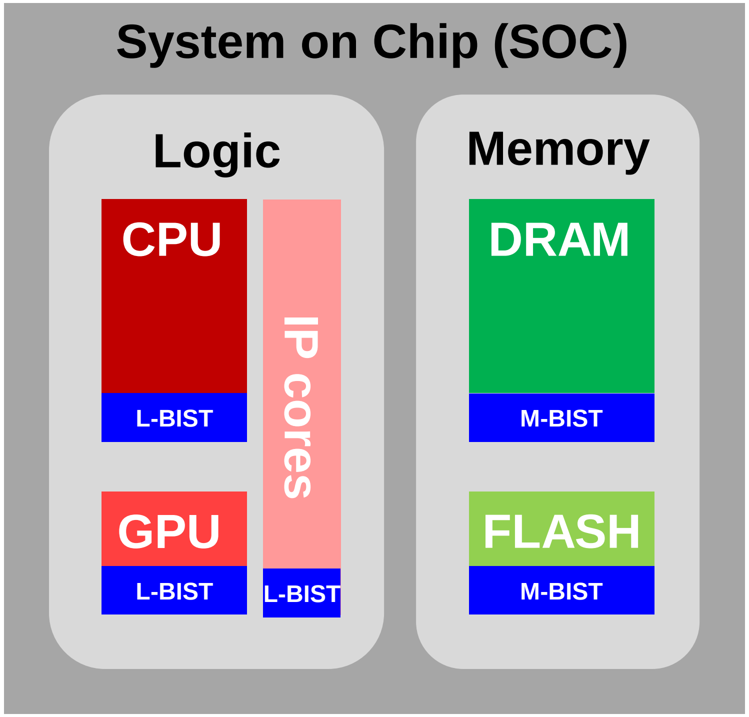
Architecture of BIST

- Three components: *BIST Controller, TPG, ORA*
- Three I/O Pins: *Start BIST, BIST Done, Pass/Fail*



Why BIST?

- 1. Save ATE cost
  - Smaller test pattern storage
  - Fewer DFT pins
  - Slower tester speed
- 2. Better IC quality
  - Test speed higher than ATE
- 3. Easier integration of tests
  - *Intellectual Property* (IP) cores
- 4. Easier test access
  - Test embedded memory in SOC
- 5. Enable on-line testing
  - Ensure reliability



BIST Has Many Unique Advantages

ATE Cost w/wo BIST

- Consider a 1 GHz μP with 1000 pins.

- Test w/o BIST
  - 1 GHz ATE: $3,000/pin×1,000pins = $3,000,000 USD
  - Huge initial capital cost
- Test w/ BIST
  - 20 MHz ATE: $400/pin×1,000pins = $400,000 USD
    - Test I/O pad contact
    - Provide test commands, and read out test results

BIST Reduced ATE Cost

Disadvantages of BIST

- 1. Area Overhead
  - Yield loss due to BIST circuitry
- 2. Performance degradation
  - Extra hardware
- 3. Extra design effort
  - Test point insertion, BIST insertion, verification …
- 4. Lack information for debug and diagnosis
  - Need to bypass BIST when diagnosis
- 5. Long test length but fault coverage may not good enough
  - Random test patterns not as good as ATPG patterns
  - Mixed solution (BIST + ATE) is often needed

BIST can NOT Solve All Problems

Quiz

Q: Which of the following is NOT true for BIST?

A. BIST reduces test cost because of good fault coverage

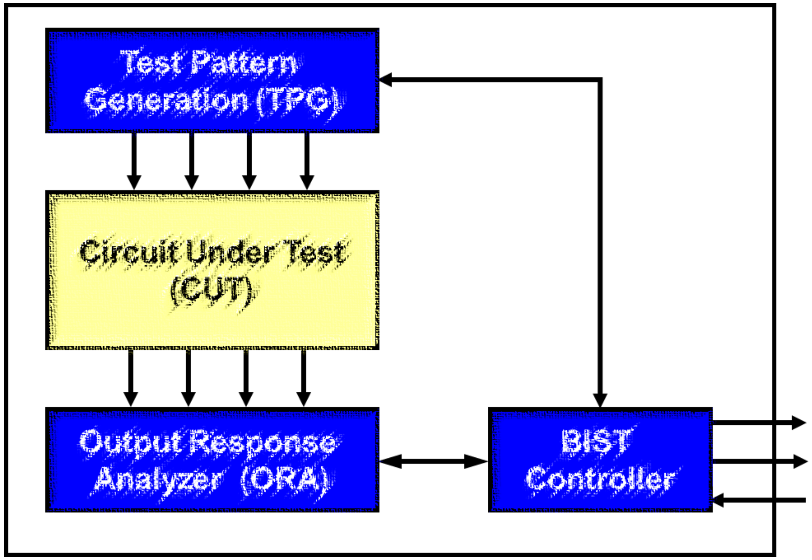
B. BIST reduces DFT pins required

C. BIST improve test quality because test speed is higher

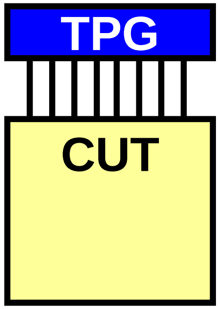
ANS:

BIST Part1 - TPG

- Introduction
- Test Pattern Generation (TPG)
  - Deterministic: ROM, Algorithm, Counter
  - Pseudo Random:
    - Linear Feedback Shift Register (LFSR)
    - Cellular Automata (CA)



ROM/Algorithm as TPG



- **ROM as TPG**
  - **Store test patterns in ROM**
  - **Very expensive for chip-level BIST**
  - **Maybe doable for system-level BIST**
    - **e.g. self test program in BIOS (Basic Input/Output System)**

- **Algorithm as TPG**
  - **Test pattern generation based on certain mathematical rule**
  - **Suitable for regular structure like memory, FPGA**
    - **Not very useful for random logic**

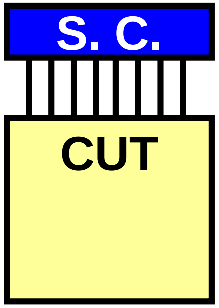
No Good for Logic BIST

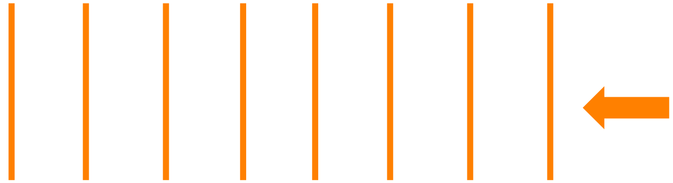
Shift Counters as TPG

- Generates regular test sequences
  - Such as walking sequence for interconnect testing
- Advantage: Linear test time
- Disadvantage: Too regular, not useful for random logic

Walking Sequence

cycle								
1	1	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0
3	0	0	1	0	0	0	0	0
4	0	0	0	1	0	0	0	0
5	0	0	0	0	1	0	0	0
6	0	0	0	0	0	1	0	0
7	0	0	0	0	0	0	1	0
8	0	0	0	0	0	0	0	1



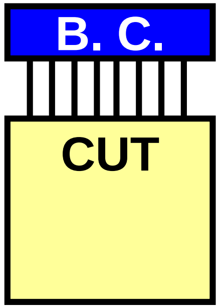


Bridging faults between lines can be detected

line 1 2 3 4 5 6 7 8

Binary Counters as TPG

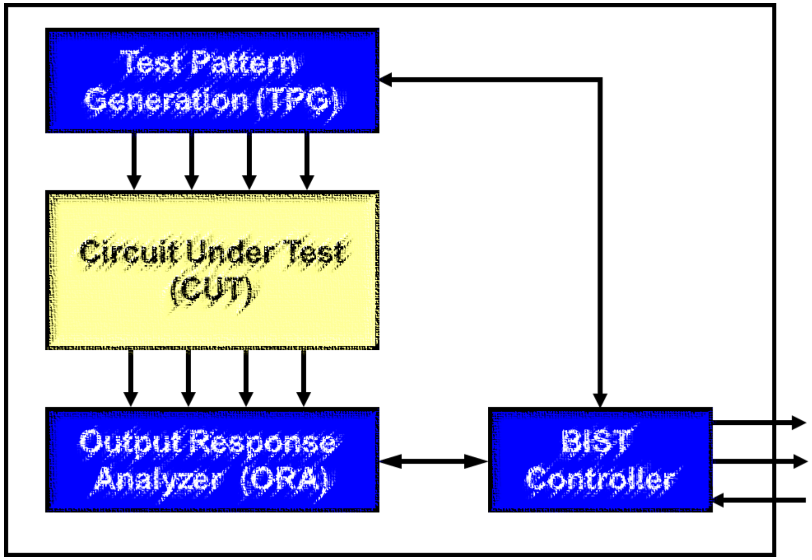
- N-stage binary counters
  - Generate test patterns in sequence
    - from 0 to 2^N-1, or from 2^N-1 to 0
- Advantage
  - + Simple design
  - + Exhaustive test is high quality
- Disadvantages
  - – Exhaustive test length is very long
    - ⇒ No randomness, deterministic pattern sequence
    - ⇒ e.g. Need 2^{N-1} test length to reach a 1 at MSB
  - – Large area overhead (compared to LFSR)



Need Random Counter for Logic BIST

Summary

- Introduction
  - BSIT components: TPG, ORA, and controller
  - Pros: reduced pins, tester cost, on-line testing
  - Cons: area overhead, performance degradation, lower FC
- Test Pattern Generation
  - Deterministic: ROM, Algorithm, Counter


Test Pattern Generation (TPG)
Circuit Under Test (CUT)
Output Response Analyzer (ORA)
BIST Controller