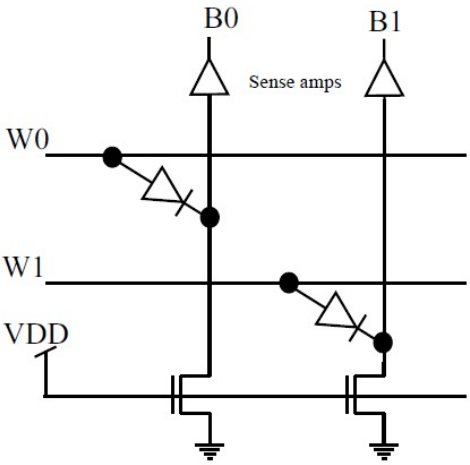
1. A 2 x 2 ROM array is built with the help of diodes as shown in the circuit below. Here W0 and W1 are signals that select the word lines and B0 and B1 are signals that are output of the sense amps based on the stored data corresponding to the bit linesc during the read operation.




$$\begin{array}{c} \quad B_0 \quad B_1 \\ W_0 \begin{bmatrix} D_{00} & D_{01} \\ D_{10} & D_{11} \end{bmatrix} \\ W_1 \end{array}$$

Bits stored in the ROM Array

Figure 1: circuit

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During the read operation, the selected word line goes high and the other word line is in a high impedance state. As per the implementation shown in the circuit daiagram (*Fig.* 1) above, what are the bits corresponding to $D_{ij}$ (where i=0 or 1 and j=0 or 1) stored in the ROM?

**(A)** $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ **(B)** $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$ **(C)** $\begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix}$ **(D)** $\begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}$