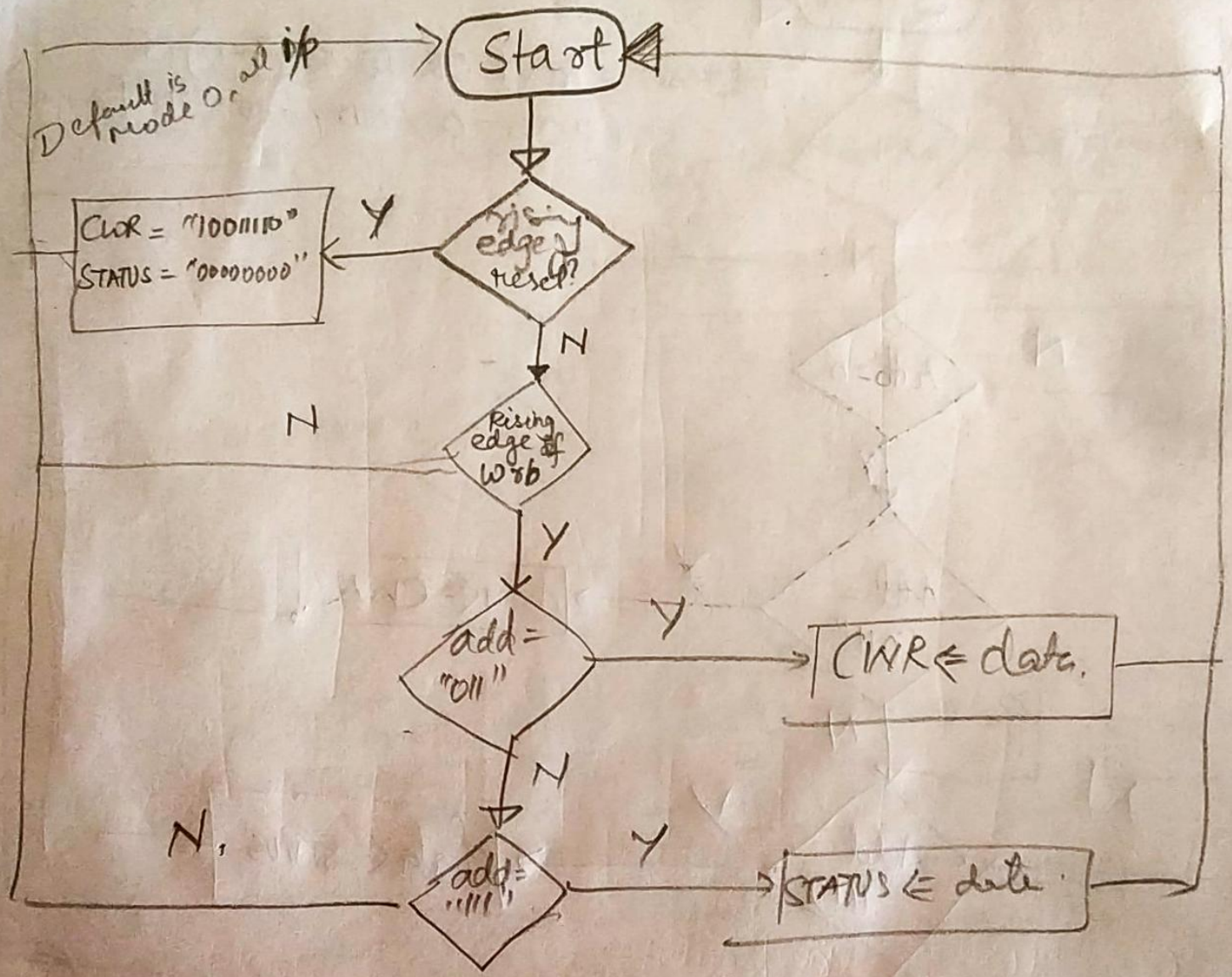
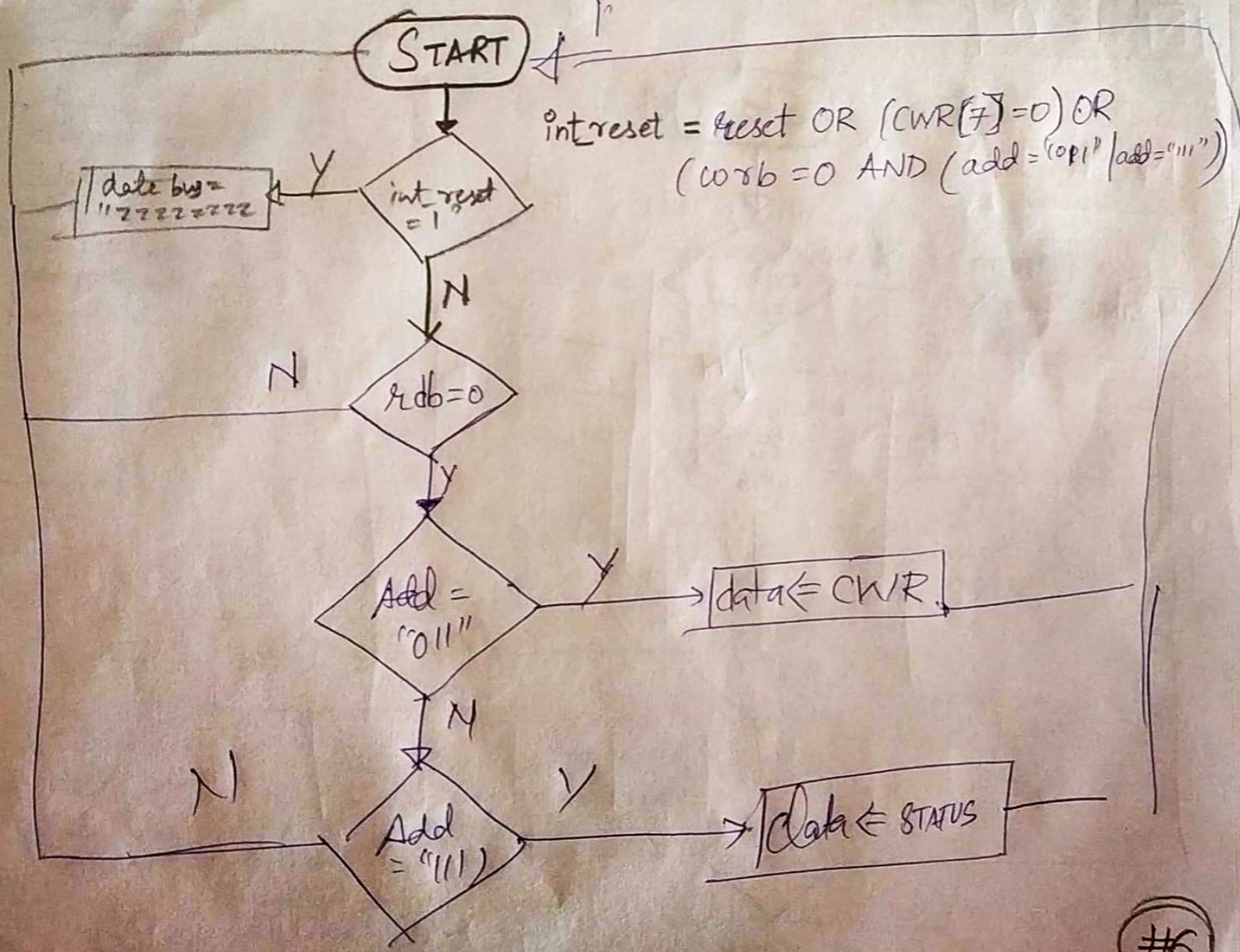
4] Flow diagram

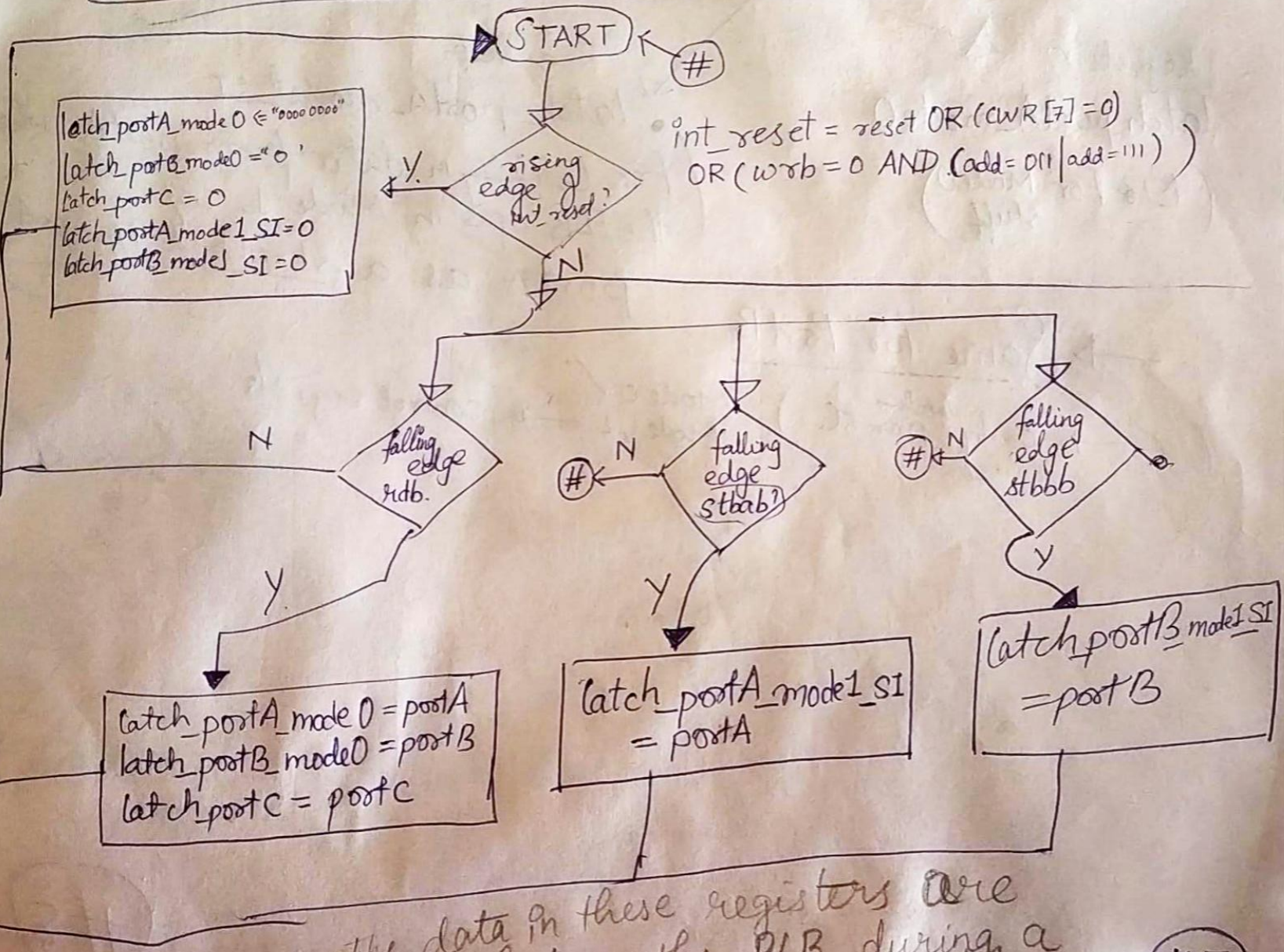
→ Write data to the CWR register & STATUS register



→ To read the contents of CWR register & STATUS register.



Flow diagram that latches in the data from data bus onto latch data bus



The data in these registers are read from the PLB during a read cond.

→ There are 2 ~~types~~ sets of registers to latch in the values at portA

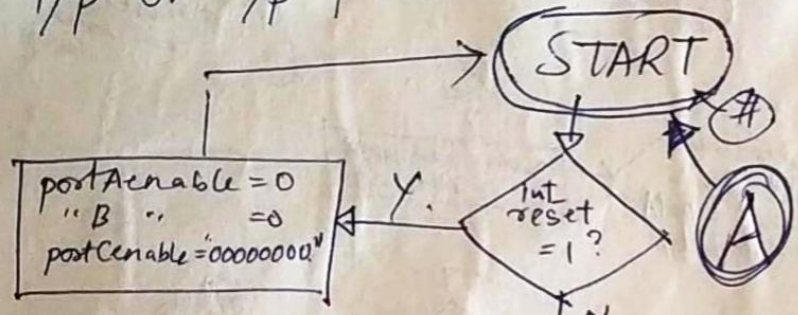
Register
latch_portA_mode0
(~~I/O~~ For Mode0 stuff)

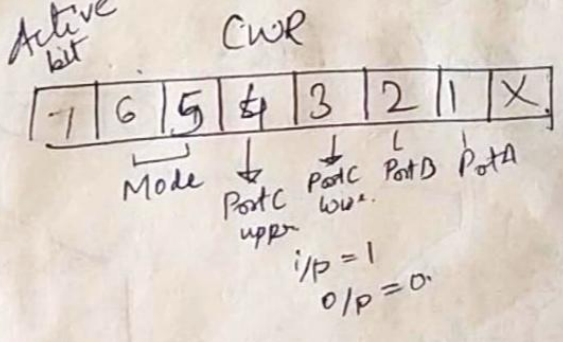
Register
latch_portA_mode1_SI
(for latching in data from portA when the PLB ops in Mode 1 w/ the portA as a strobbed i/p port).

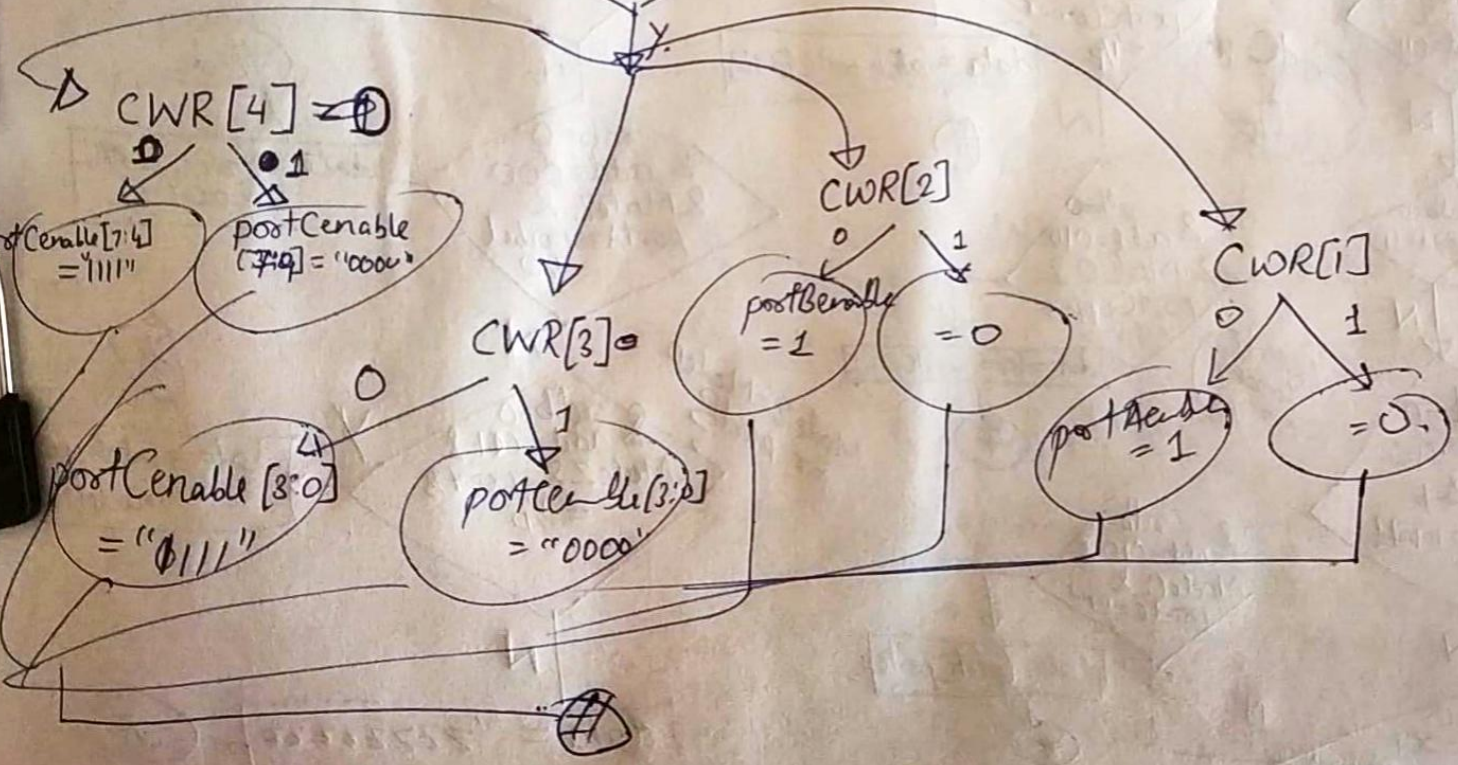
→ Same for PortB
(C → only latch-portC) Mode 0 ✓
Mode 1, 2 → control signals

#8

→ Flow diagram for generating the enable signals that determine whether portA, portB & portC are i/p or o/p ports in mode 0. #10.



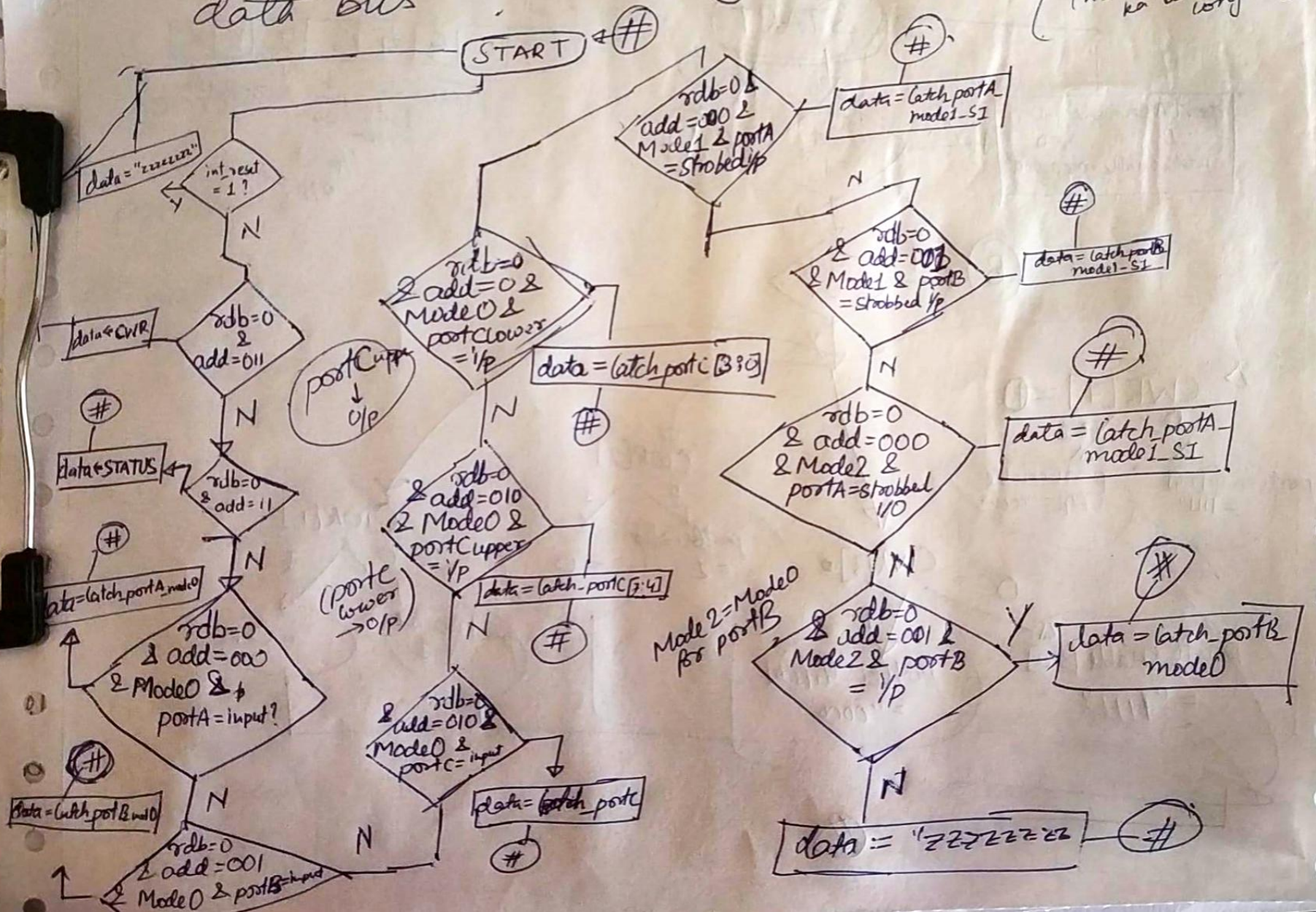




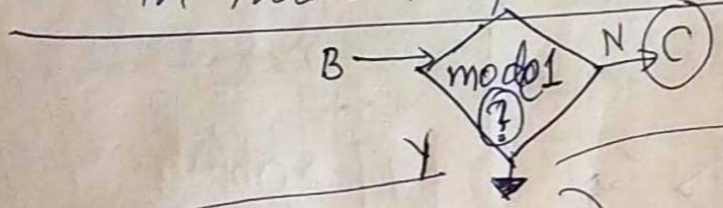
#9

→ Flow diagram for reading data from these registers to external devices using data bus.

(latch_portA_mode0
latch_portB mode1_SI
int_reset ka usual long name)



→ Flow diagram for Gen. of enable signals in mode 1 op.



portB = strobed o/p port.

↓

portBenable = 1 (enables portB to be an o/p port).

else portB = strobed i/p

portBenable = 0.
(enables portB to be an i/p port).

portA = strobed o/p.

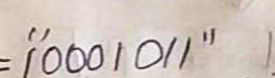
0 → portAenable = 0

1 → portAenable = 1

portA AND portB = strobed o/p

if (portA AND portB = strobed o/p)

portCenable = "00001011"



(o/p ports ko 1 kiya)

acc to this

else if (portA AND portB = strobed i/p).

portCenable = "00101011"

else if (portA = strobed o/p AND portB = strobed i/p)

portCenable = "10001011"

else if (portA AND portB = strobed i/p ports)

portCenable = 00101011

portC { [7] → obfab, [3] → intra, [1] → obfbb, [0] → intrb } o/p ports

portC { [7] → ibfa, [3] → intra, [1] → ibfb, [0] → intrb } o/p ports

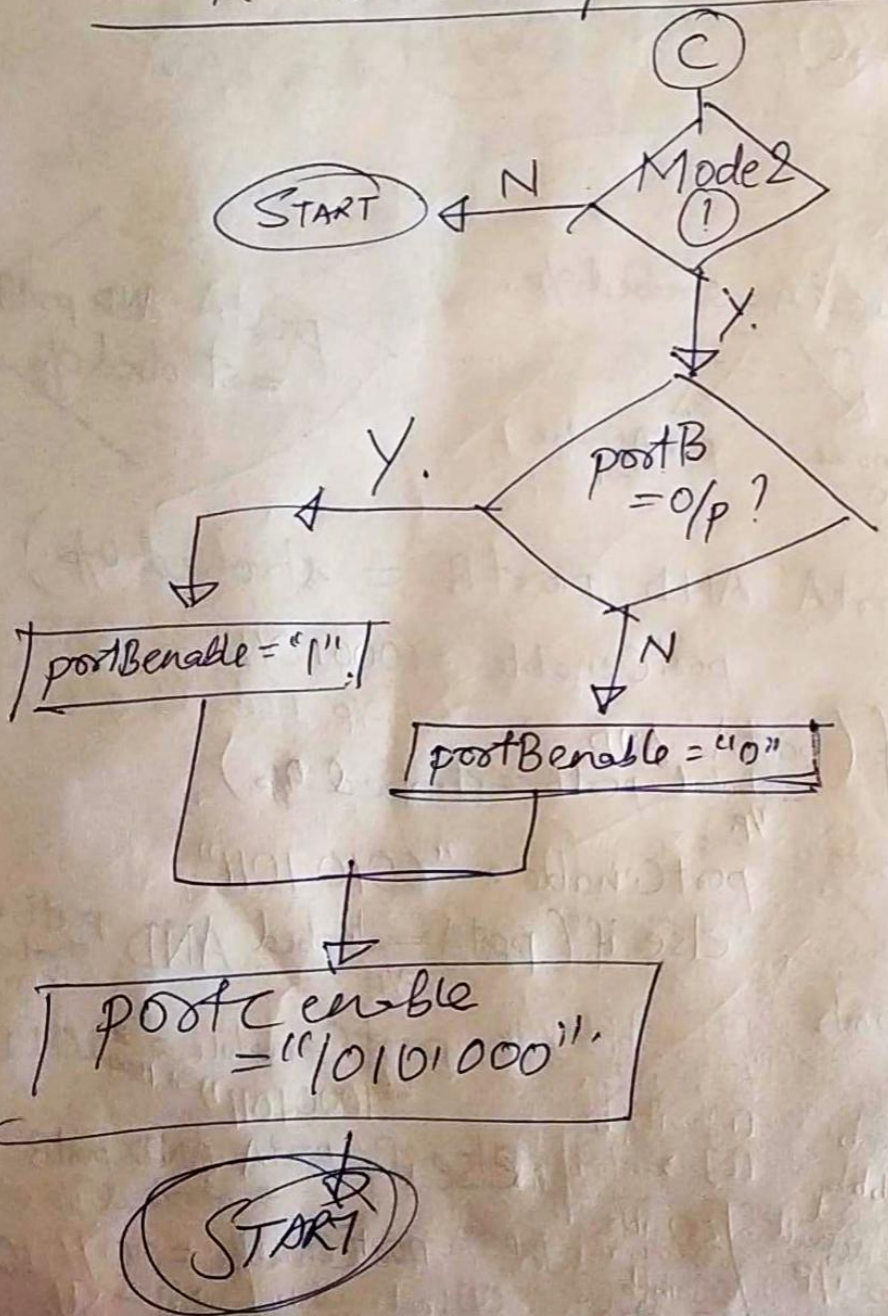
portC { [6] → ackab, [2] → ackbb, [5] } not used but default to i/p, [4] } i/p ports

portC { [6] → ackab, [2] → stbbb, [5] } not used but default to i/p, [4] } i/p ports

portC { [7] → obfab, [3] → intra, [1] → ibfb, [0] → intrb } o/p ports

portC { [7] } not used but default = i/p, [6] } i/p ports, [4] → stbab, [2] → stbbb

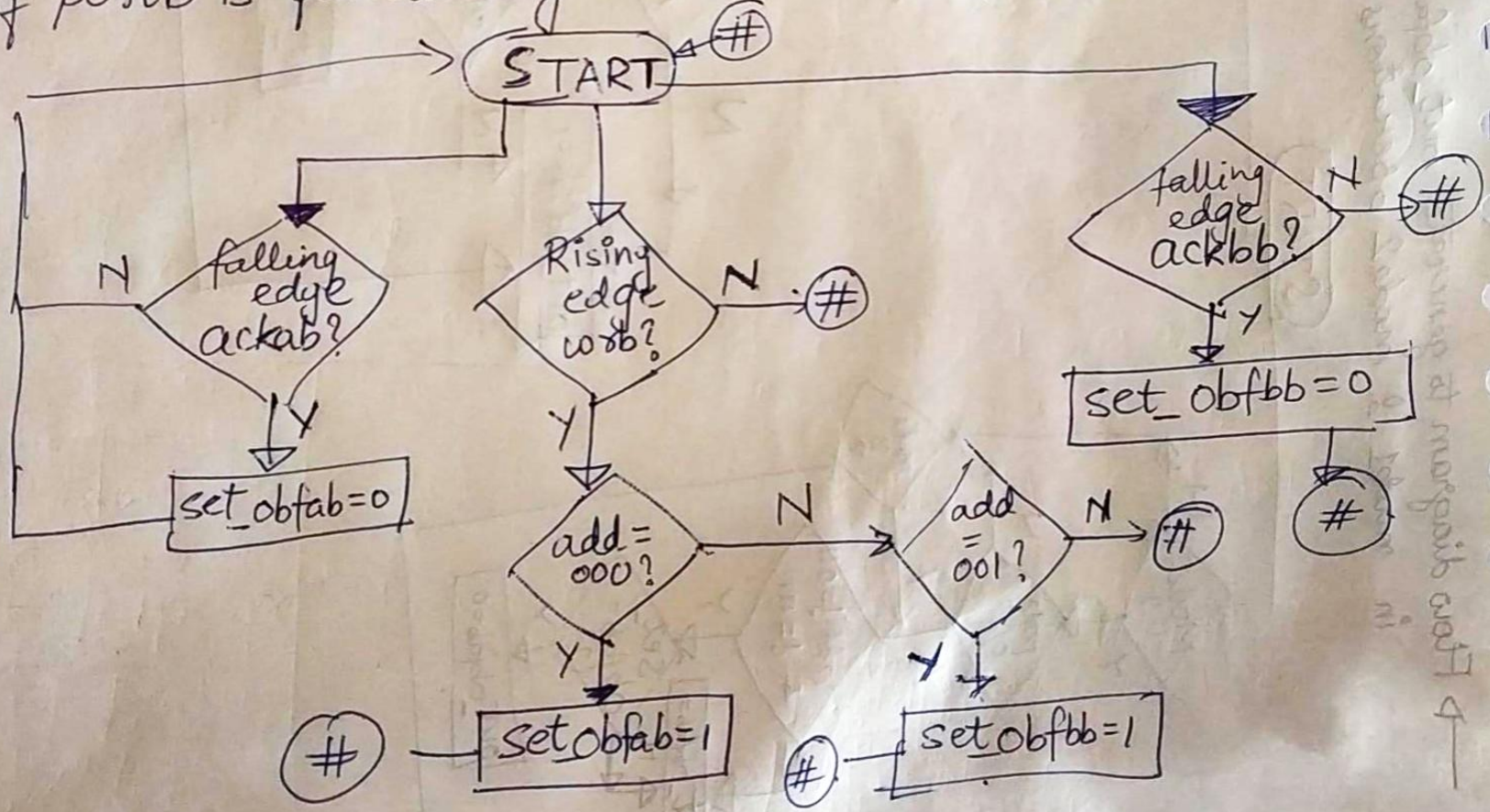
Flow diagram for generating ~~signals~~ enable signal in mode 2 operation



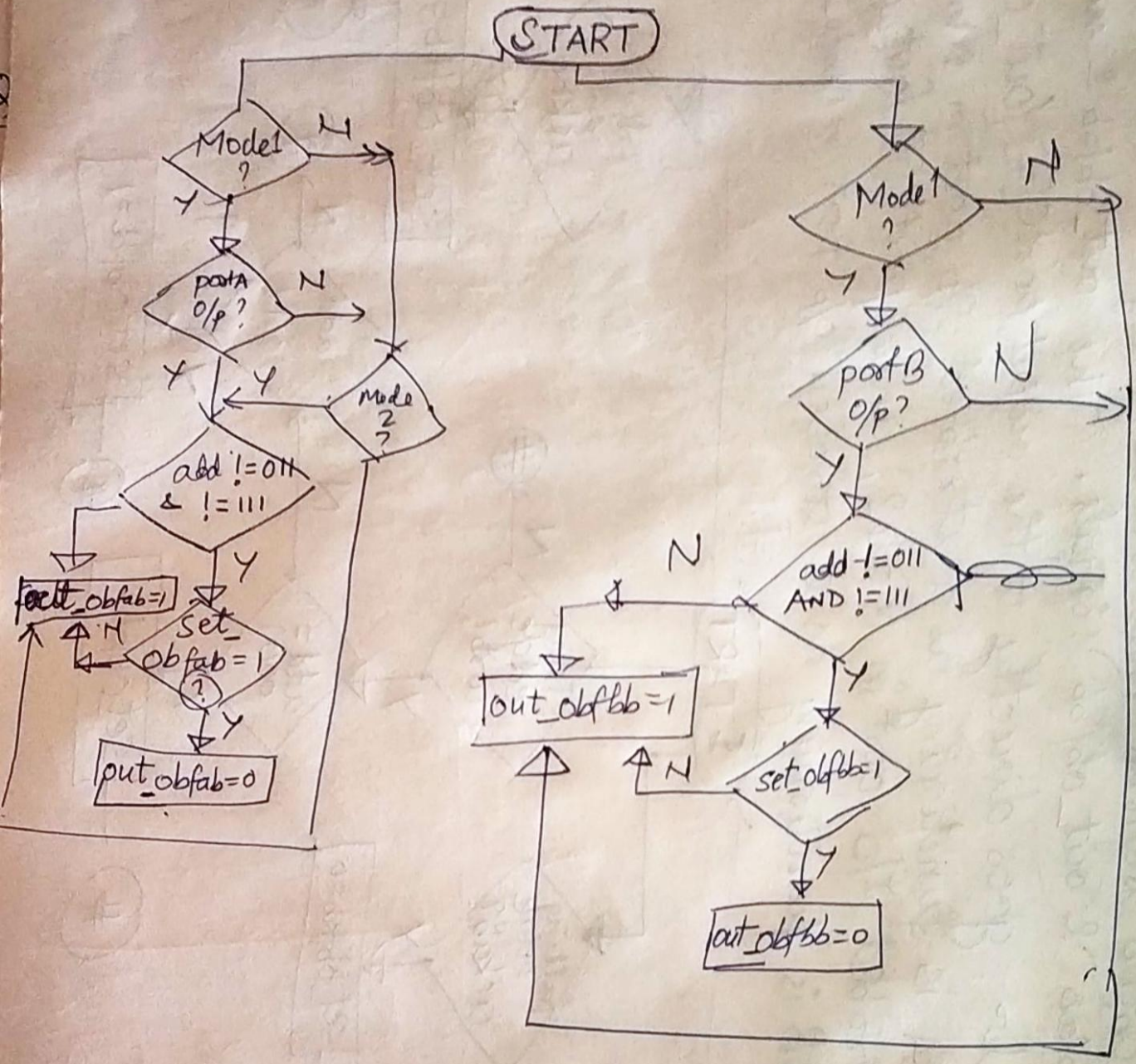
[7] → obfab
[5] - ibfa
[3] — intra
} o/p ports

[6] - ackab
[4] - stbab
[2]
[1]
[0]
} not used but deflt to i/p
} i/p ports

→ Flow diagram to generate set_obfab and set_obfbb signals that are used to generate out_obfab & out_obfbb signals. The out_obfab & out_obfbb signals goes directly to the output portC[7] (out_obfab) if portA is functioning as a strobed o/p port in Mode1 or strobbd I/O port in Mode2, and portC[1] (out_obfbb) if portB is functioning as a strobed o/p port in Mode1.



→ Flow diagram to generate out_obfab and out_obfbb signals in mode1 & mode2 operations.



#14