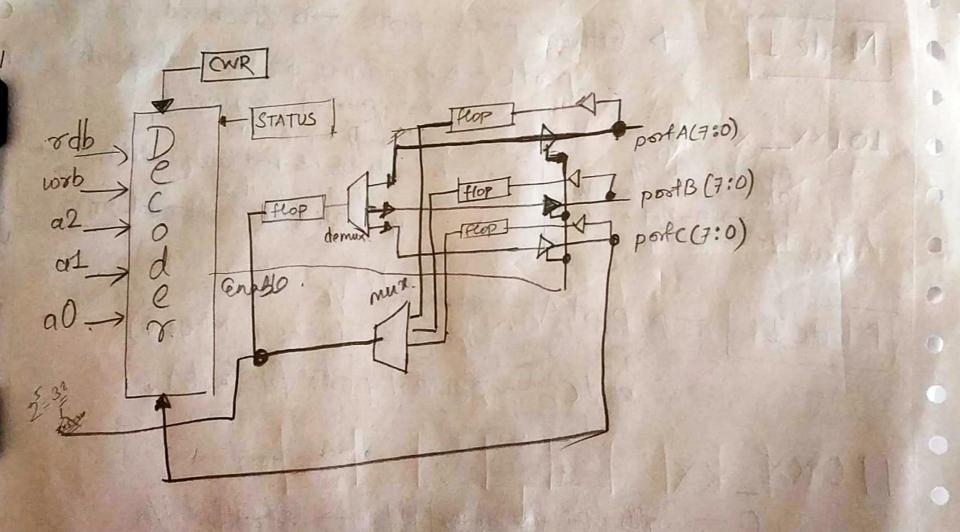
Programmable logic Block for Peripheral Infertio pot A (7:0) Adivelow postB(7:0) 001-ports 010-ports 010-ports 011-CWR 111-STATUS post c(7:0) Modes 1 for reading 24 1/0 pins & B C - polCupper Internal Registers - 2 (1) CWR functionality & 2) STATUS direction of ports - Not used. 6 5 4 3 2 1 0 50-Mode b 0-10/0 01 - Mode 1 1) - Mode 2.

Mode "00" - PortA & ip or o/P -Strobed O/P - 0 postA strobbed. Mode "10" -> postA -> strobbed 1/0 post. postB - Doperates in Mode o as leither i/p or o/p. STATUS Register Lo Controls % Port C when the PLB is operated in Controls 0/p post [[3] when postA when postA is operating as strobed 0/p is and 1. mode 1 and mode 0. mode 2. - Controls the of porto) 76.5.4.3210 as stocked up in contrals Opport([0] when post ops is Controls the Op post C[0] in male! -When pot B is operating as stoophed ofp in

2] Modes of Operation Mode 0] - > Self emplainatory Mode 1] -> Bither postA postB -> Strobbed i/p/0/p. port - > functions as control ports for post A & post B intra - D Interrupt seq for is intra - D Interrupt rey por latch until it is i/pto stbab - D loads data into port latch until it is i/pto 101××__× 00 -> both ofp ibfa -> 0/p indicating that information. 01 -> B-0/p A-1/P 10 -> B-1/p A-0/p 11. -> both 1/p Mode 2 D post A - strobbed 1/0.

Mode 2 D post B - 1/p 50 0/p (like in Mode 0) port c - Control ports for portA. IIXX XX 0-PostBops as on 0/2 | PotA -> stoobbed 1/6 1-" " " " 1/p | 33")))

3 Microarchitecture Defination for Programmable Peripheral Interface



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