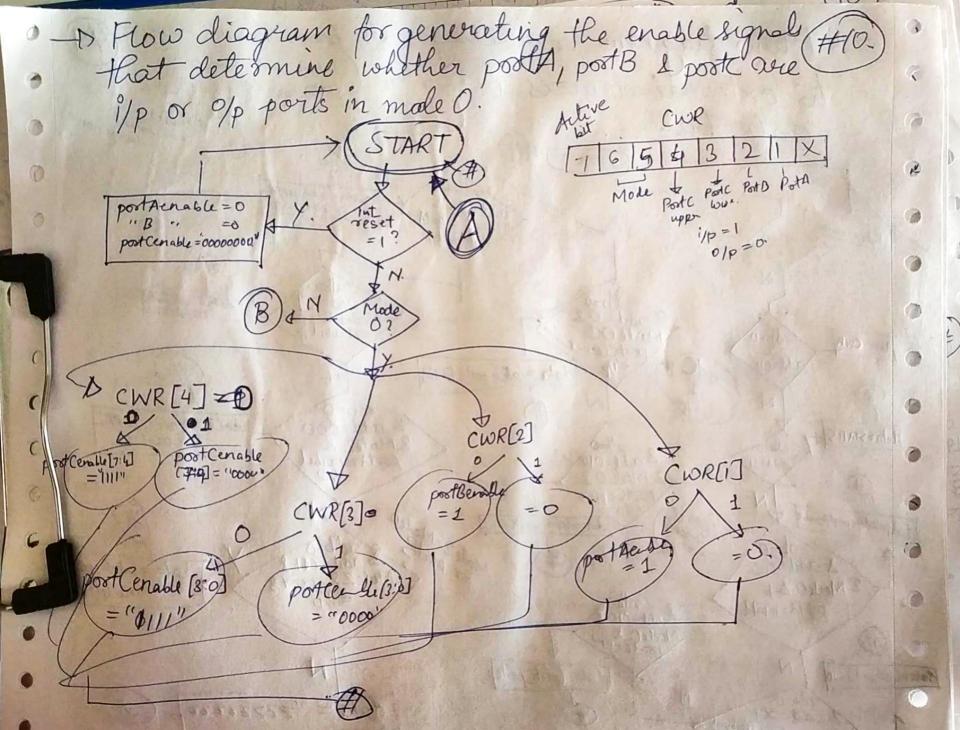
Flow diagram D Write data to the CWR register & STATUS register Defould is or all if CLOR = "1001110" edge theself STATUS = "000000000" CWR & data STATUS & date

#5

DTO suad the contents ) Register & STATUS negister. intreset = reset OR (CWR(7)=0) OR (corb = 0 AND (add = "0p1" |add="11")) Add = lata = CN/R 2 gla = STATUS

Flow diagram that latches in the Late form data bus onto latch data bus START)K int\_reset = reset OR (CWR[7] = 0) atch postA mode 0 € "0000 0000" OR (worb = 0 AND (add = 011 add = 111)) latch\_port 8\_mode0 = 0 edge de de latch post C = 0 latch\_postA\_mode1\_SI=0 latch\_postB\_model\_SI=0 edge stbbb (atchpostB model SI latch\_postA\_model\_SI =postB Catch\_portA\_mode 0 = pootA = postA latch\_postB\_mode0 = postB latchipost c = post c The data in these registers were read from the PLB during a

-D There are 2 types sets I registers to latch in the values at porta & Register Register & " latch\_postA\_model\_SI (for latching in data from portA)
the PLB ops in Mude 1 w/ latch\_postA\_modeO porta as a strobbed i/p port) (190 For Model) - D Same for Post B (C-> only portC) Mode 0 / control signt **20** 三分本系统品通 (#8)



- & Flow diagram for reading data from these regist to enternal devices using ( cotch\_post) mode 1\_51 I'nt resetual name) data bus START &# rdb=01 data = Catch portA add = 200 2 model-SI data = "zueun" = Strobea intrest sab=0 deta = latch ports - add-003 Model & pools add=08 Moderas = Stoobbed YP 8db=0 data & CVIR post CLOW 27 DOOKCUTE add=011 data = (atch port ( 1390) adb=0 data = Catch postA. mode I\_SI 2 add = 000 Hata+STATUS 4 2 Mode 2 & DONA=Stoobbe add=010 add= 11 2 Model 2 DOT CUPPER Made 2 Modeo (Porte ata=latch\_port Amako) deta = (atch-port( [3:4]) 20/8/ data = latch\_postB rob=0 25 add = 001 1 2 add = 000 Mede 22 post B model 2 Modeo & p poot A = input? ald=010 Model & Idata = both porty Stata = Cutch pot B mill dota = 12272222 2 odd =001 Mode O & postB=1

Flow diagram for Gen. J. enable signals in mode 1 op. B model NC (START) 4 port B = strobed %p portA = stoobed %. DostA AND potB = strobed ofp postBenable = 1 (enables postB to be an oppost) postAenable postAeruble else portB = stoobed 1/P. postBenable = 0.

[enables postB tobe)

[enables postB tobe)

[an yp post )

are totals

[an yp post )

[an yp post |

[an yp else if (postA AND cop posts ko 1 kip)

else if (postA AND postB = stoobed 9/p). post([7] -> obtab 0 1/2 [3] - intra [3]-intra post Cenable = "0010 1011" [1]-obfbb else if (post A = strobed AND post B = o/p o/p [1] -> obfb col-intro [4] not used
[6] but default 1/p ports
[6] -> Stbab [[0] -sintab [7] - obfob lop port Cenable = 0001011 [3] - intra | = 10001011" [6] >ackab [2]-ackbb []-sibfb (1) -ackab [0] -> intrb else if ( porta AND posts) [2] -ackbb. (1)-ible opports postcenable = 00/0/0/1
(1)-ible opports postcenable = 00/0/0/1
(1)-ible opports postcenable = 00/0/0/1
(1)-ible opports postcenable = 00/0/0/1 [5] I not used
[4] but to
default if [5] I not used it [7] Instrued but (2) -> Stbaby if

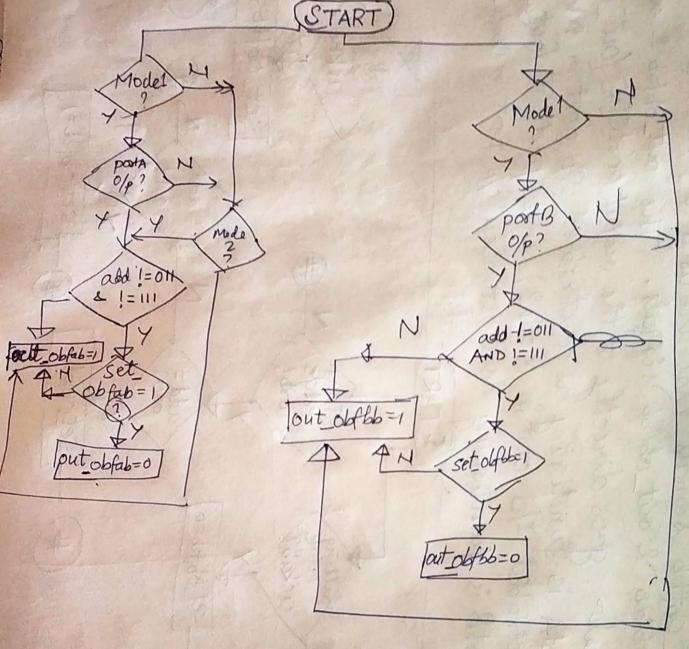
How diagram for generating signals enable signal 12 [7] - obfab 1 % ports
[5] - Ibfa
[3] - intra] 1/0 [6] ackab Whot [4] - Stbab [2] not used [1] but deflt portBenable = "1" postBenable = "0" postcerble = 11/010100011.

-> Flow diagram to generate set obfato and set obfbb signals that are used to generate out\_obfab & out\_obfbb signals. The out\_obfab & out\_obfbb signals goes directly to the output post([7] (out\_obfab) if postA is functioning as a strobbed % post in Model or stoobed I/o post in Mode2, and post C[i] (out\_dofbb) if portB is functioning as a strobed of port in Model. START set\_obtab=o setobfbb=1

Flow diagram to generate out obfab and out obfbb signals in model & model operations.

START

Model 4



(#4)