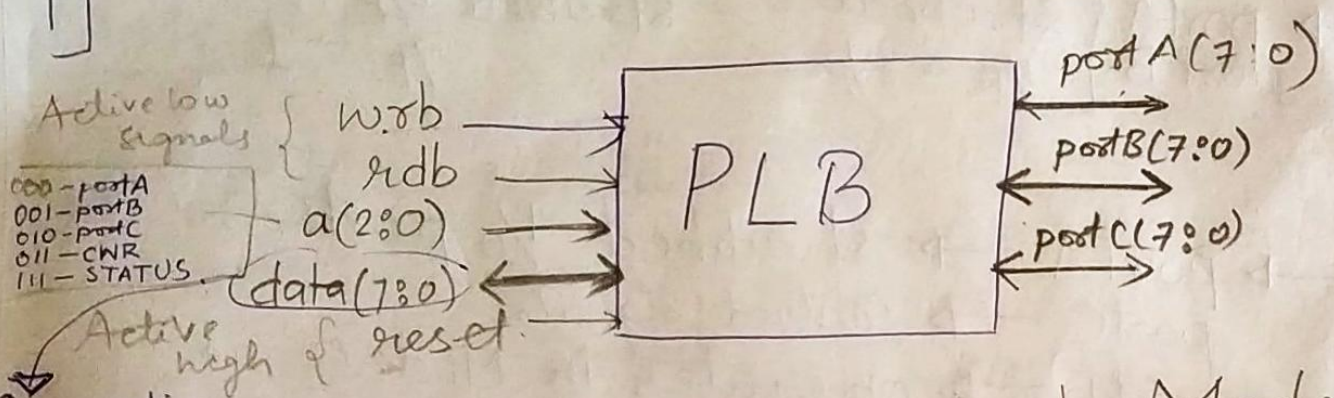
Programmable logic Block for Peripheral Interface.

1]

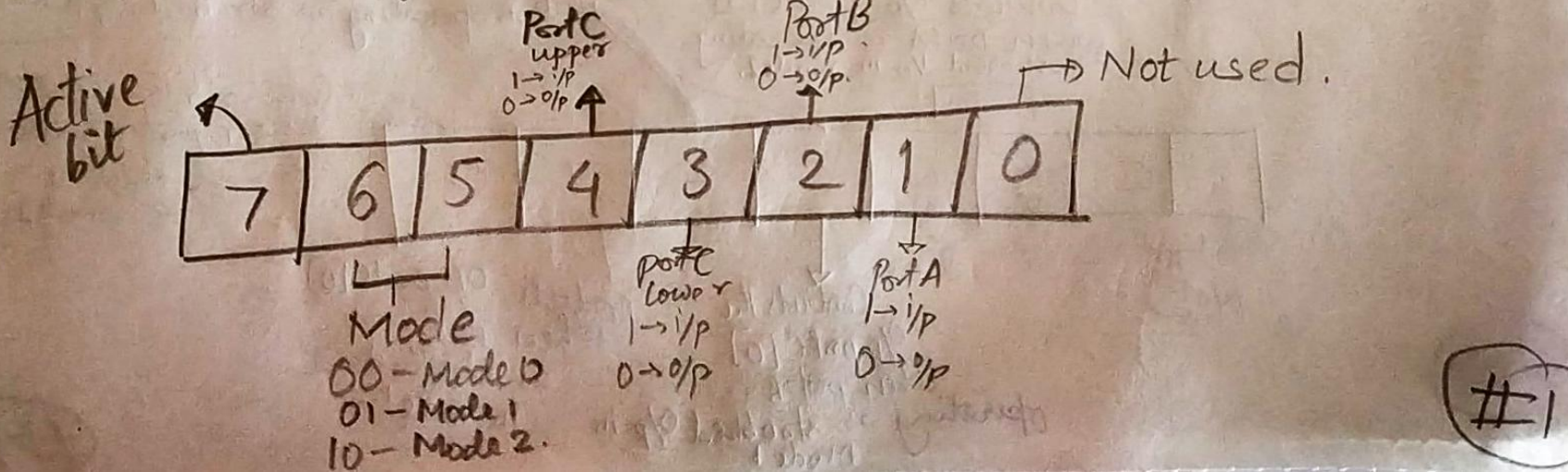


24 I/O pins { A, B, C — portCupper, portClower }

Modes { 0, 1, 2 }

Internal Registers — ②

- ① CWR → determines the functionality & direction of ports
- ② STATUS



#1

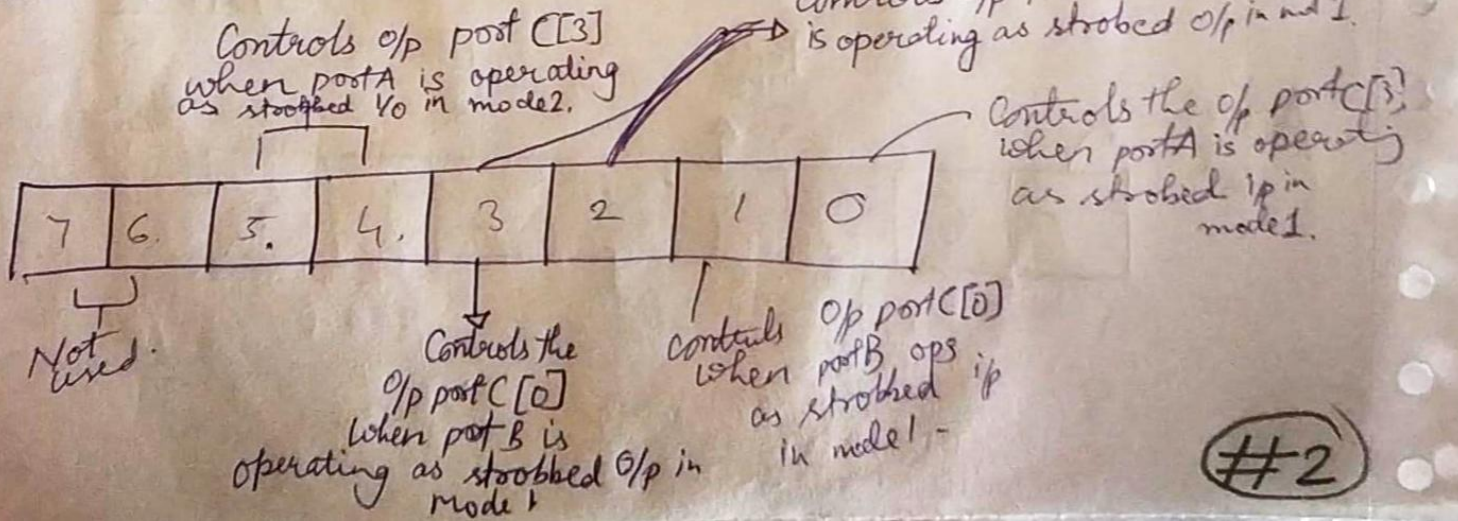
Mode "00" → portA, portB, portC } i/p or o/p → 1 – i/p, 0 – o/p

Mode "01" → portA, portB } strobbed i/p or o/p. strobed o/p – 0, " i/p – 1.

Mode "10" → portA → strobbed I/O port.
portC → control signals
portB → operates in Mode 0 as either i/p or o/p.

STATUS Register

↳ Controls o/p Port C when the PLB is operated in mode 1 and ~~mode 0~~ mode 2.



#2

2] Modes of Operation

Mode 0 → Self explainatory

Mode 1 → ~~Either~~ portA portB → strobbed i/p / o/p.
portC → functions as control ports for portA & portB

101XX__X

00 → both o/p
01 → B-o/p | A-i/p
10 → B-i/p | A-o/p
11 → both i/p

intra → interrupt req for ↑
stbab → loads data into port latch until it is i/p to µP.
ibfa → o/p indicating that i/p latch contains information.

Mode 2 → portA – strobbed I/O.
portB – i/p or o/p (like in Mode 0)
portC – Control ports for portA.

1 1 0 XX_XX

0 – PortB ops as on o/p | PortA → strobbed I/O
1 – " " " " i/p | " " "

3] Microarchitecture Defination for Programmable Peripheral Interface