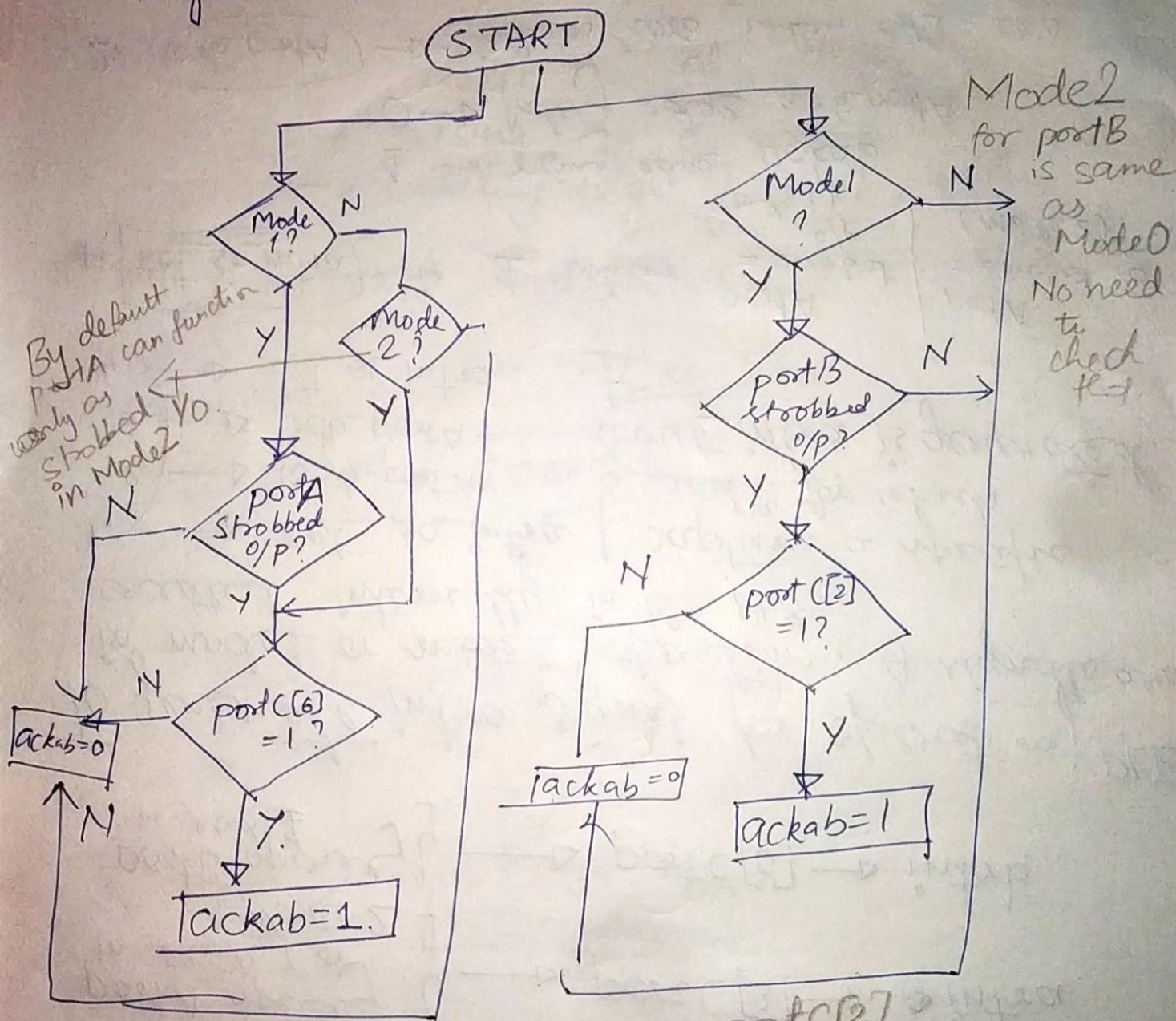


→ Flow diagram to generate ackab & ackbb signals for mode 1 & mode 2 ops.



portC[6]  
↓  
drives the ackab

portC[2]  
↓  
drives the ackbb



For op. of PLB in Mode 1 & Mode 2, the signals intra & intrb need to be generated. #16

portA operating in Mode 1 or Mode 2 }  $\rightarrow$  portC[3]  $\rightarrow$  intra.

portB operating in Mode 1 }  $\rightarrow$  portC[0]  $\rightarrow$  intrb.

To generate intra signal for operation of PLB in mode 1 or mode 2 operation, 4 signals are created internally in the PLB.

1.  $\rightarrow$  set\_so\_intra
  2.  $\rightarrow$  wrb\_postA
  3.  $\rightarrow$  rdb\_postA
  4.  $\rightarrow$  set\_si\_intra.
- } capture a specific cond<sup>n</sup> for which out\_intra is generated.

1. set\_so\_intra  $\rightarrow$  1 when  $\left. \begin{array}{l} \text{portA} \\ = \text{strobed} \\ \text{o/p} \\ (\text{mode 1}) \end{array} \right\} \begin{array}{l} \text{portA} \\ = \text{strobed} \text{ } 1/0 \\ (\text{Mode 2}). \end{array}$

1  $\rightarrow$  rising edge ackab

0  $\rightarrow$  falling edge wrb\_postA

2. wrb\_postA  $\rightarrow$  follows "wrb" when add = 000 (i.e. portA access)

falling edge of wrb\_postA refers to the

" " " wrb for portA access.



### 3. set\_si\_intra

#17

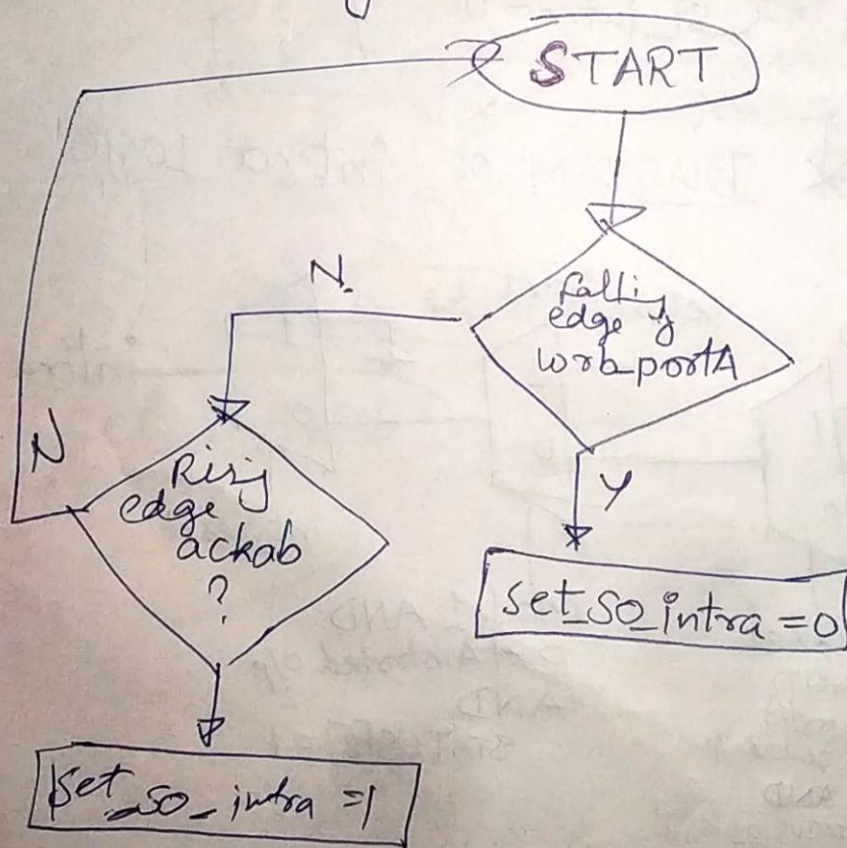
1  $\rightarrow$   $\text{postA} = \text{stbbed i/p}$  (Mode1) OR  $\text{postA} = \text{stbbed}$  (Mode2)  $1/0$

1  $\rightarrow$  rising edge of stbabb

0  $\rightarrow$  falling edge of rdb\_postA

4. rdb\_postA  $\rightarrow$  follows rdb for postA access.

$\rightarrow$  Flow diagram for set\_so\_intra.





→ Flow dia. of set\_si\_intra

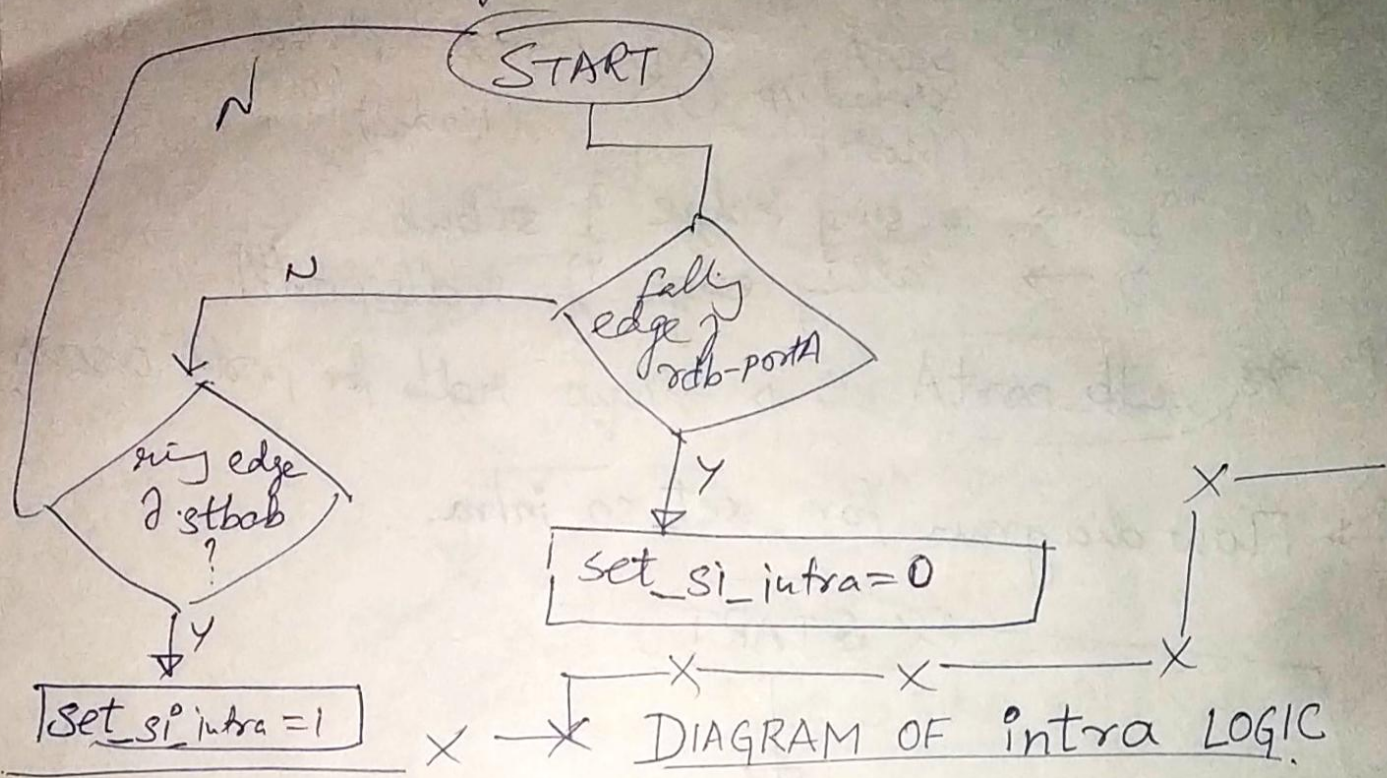
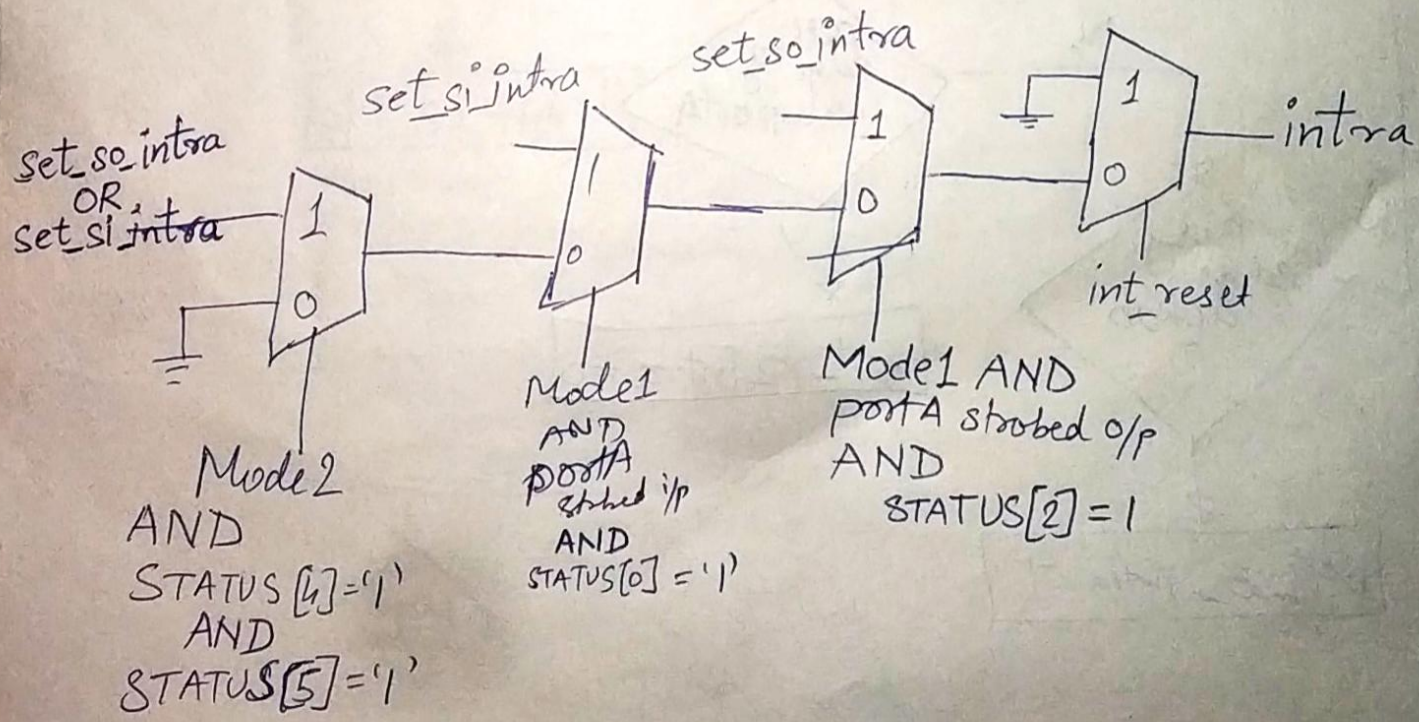


DIAGRAM OF intra LOGIC





→ Flow dia. of set\_si\_intra

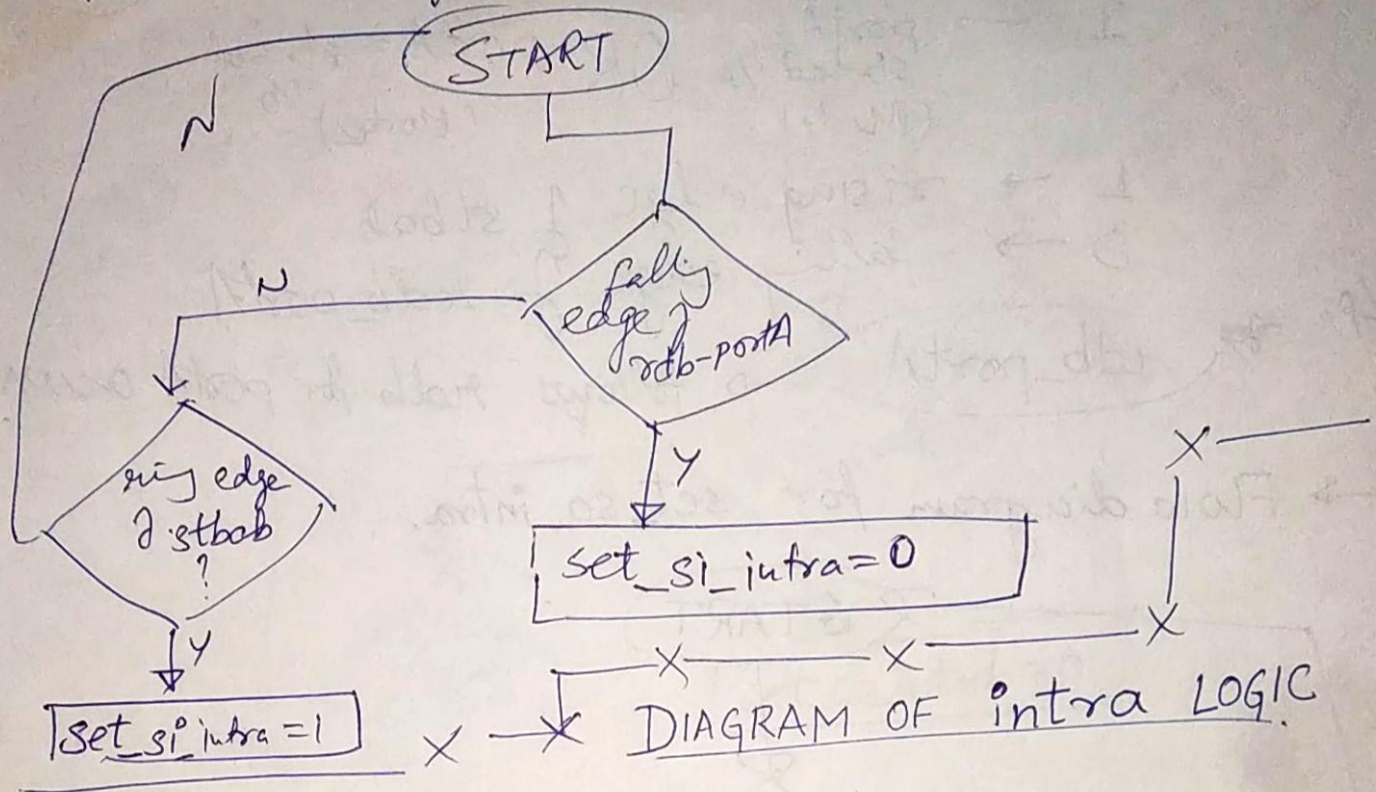
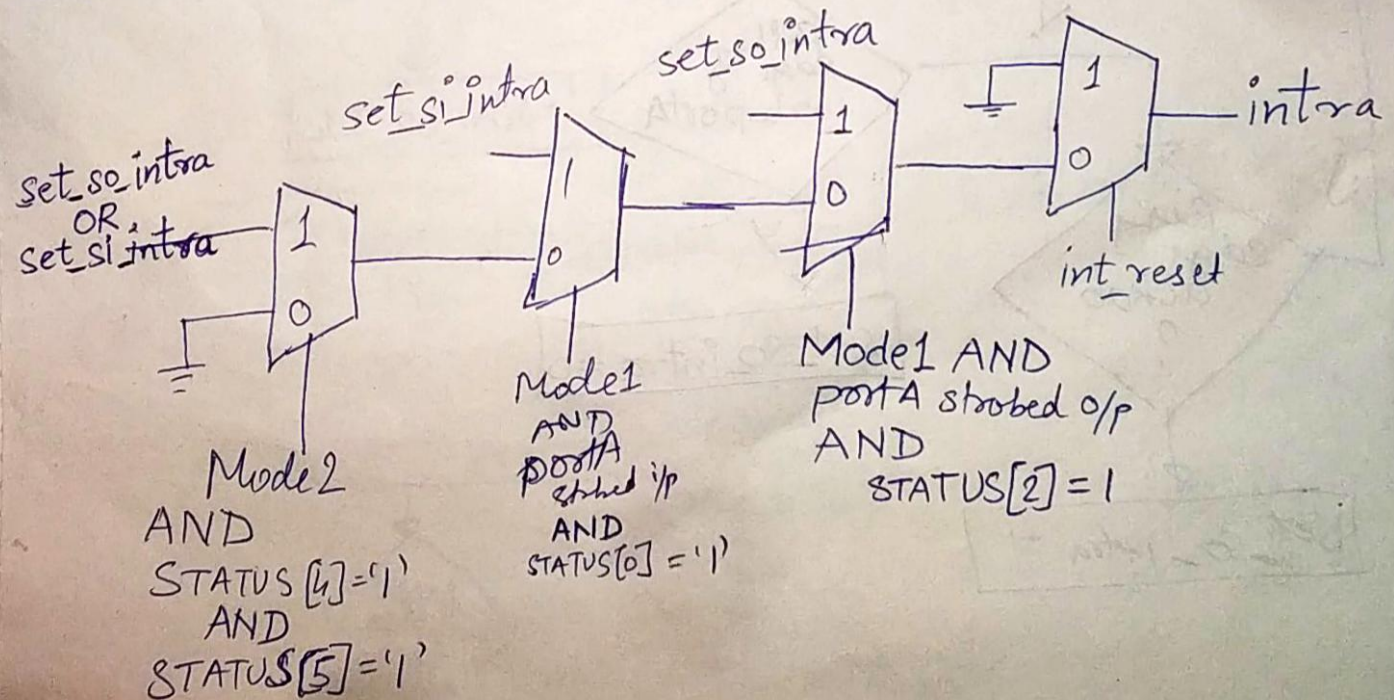


DIAGRAM OF intra LOGIC



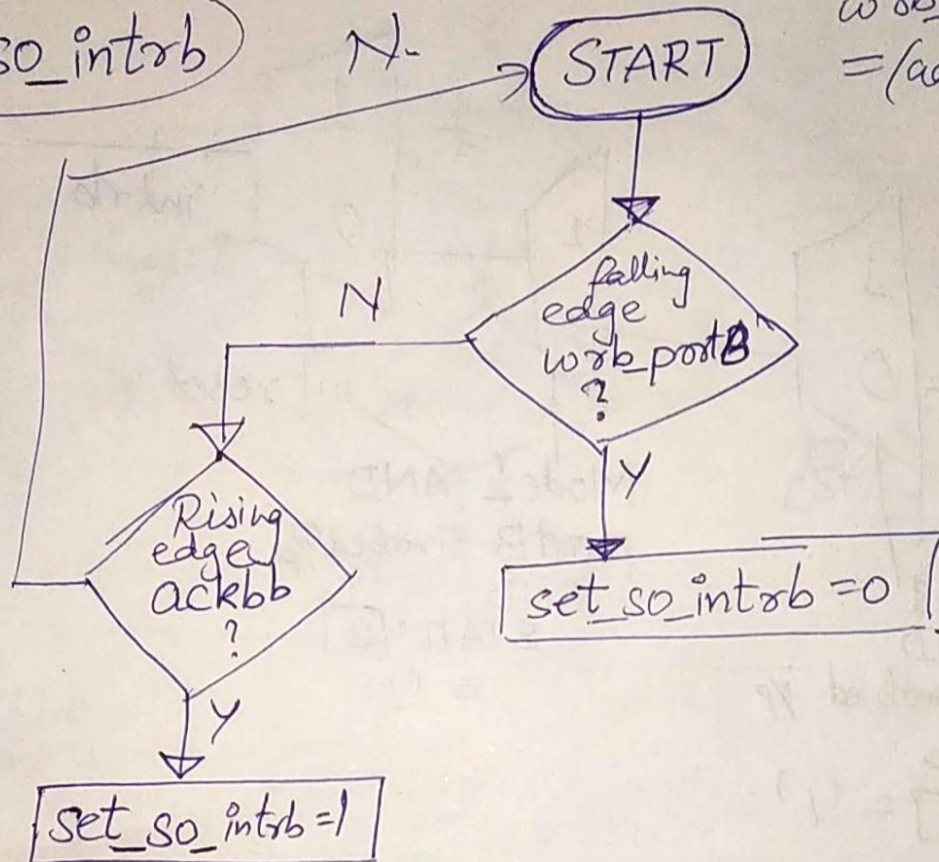


To generate `intrb`, we need the usual stuff

#19

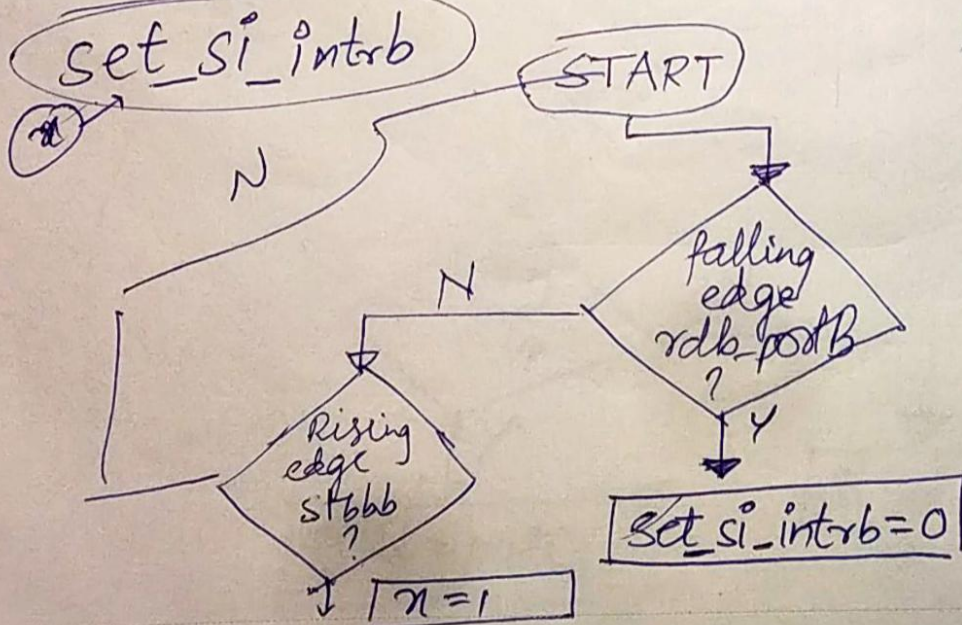
$wrb\_postB = (add == 56001) \& wrb$

set\_so\_intrb



$rdb\_postB = (add = 001) \& rdb$

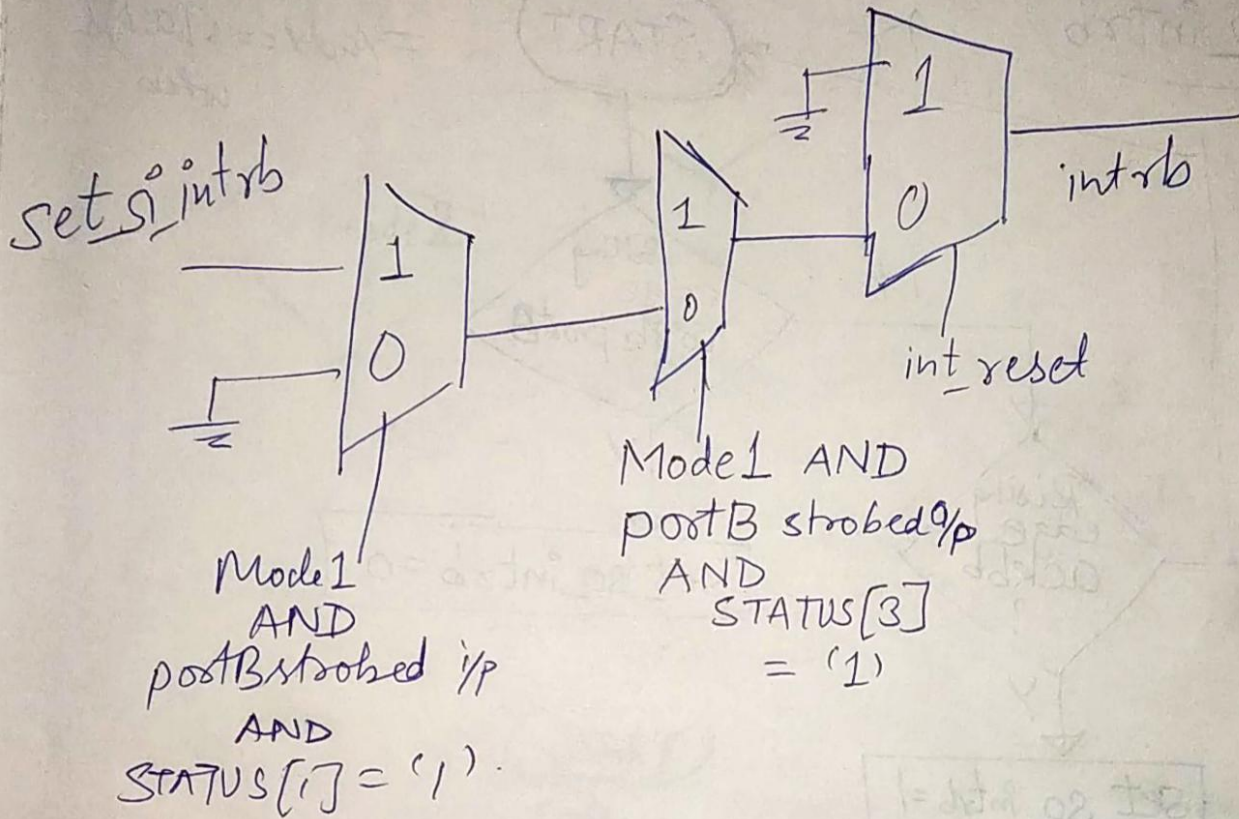
set\_si\_intrb





# intrb logic

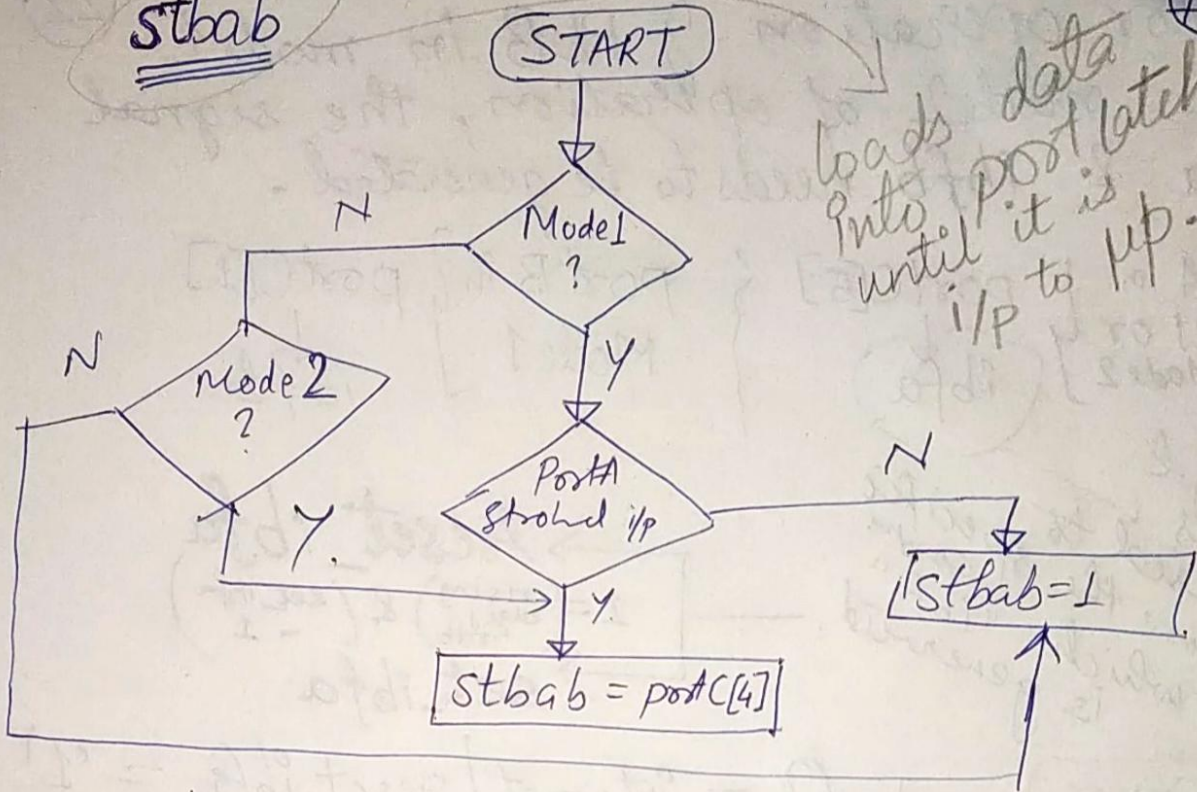
#20



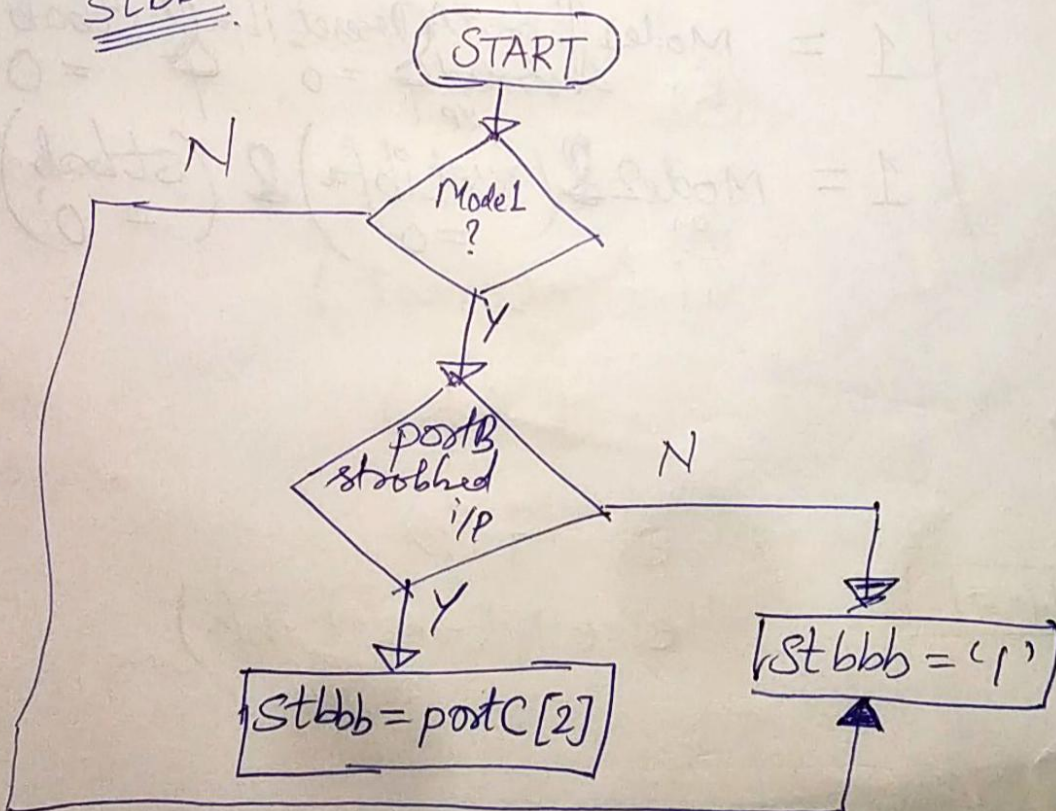


stbab

#21



stbbb



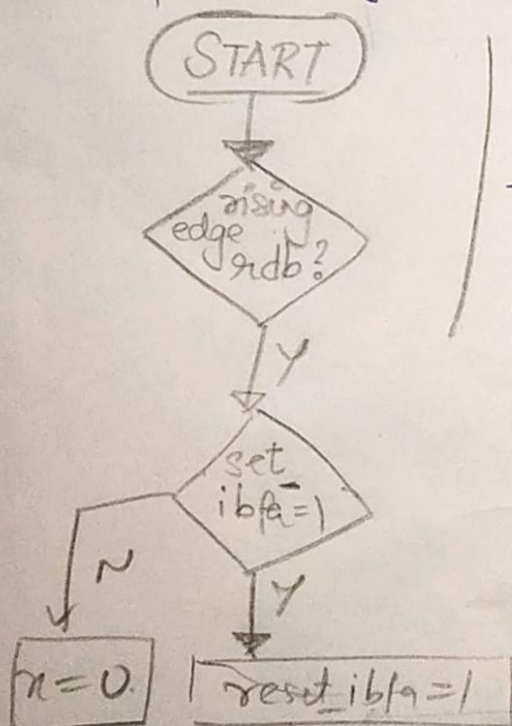


→ For operation of PLB in mode1 and mode2 of operation, the signal  $ibfa$  &  $ibfb$  needs to be generated. (22)

Port A in Mode1 or Mode2 } port C[5] } port B in Mode1 } port C[1]  
 $\downarrow$   $\downarrow$   $\downarrow$   
 $ibfa$   $ibfb$

2 internal signals are used to capture the specific conditions for which "ibfa" is generated.

→ reset\_ibfa  
 $1 = (\text{rising\_edge\_ddb}) \& (\text{reset\_ibfa} = 1)$   
 → set\_ibfa



$0 = \text{int\_reset} / \text{reset\_ibfa} = '1'$   
 $1 = \text{Mode1} \& \text{port A} \& \text{reset\_ibfa} \& \text{stbab}$   
 $\quad \quad \quad \text{stbocd} = 0 \quad \quad \quad \text{stbab} = 0$   
 $\quad \quad \quad \text{if (int\_reset)}$   
 $1 = \text{Mode2} \& (\text{reset\_ibfa}) \& (\text{stbab} = '0')$   
 $\quad \quad \quad \text{if (int\_reset)}$

else if (k)  
 else if (p)  
 else if (reset\_ibfa)