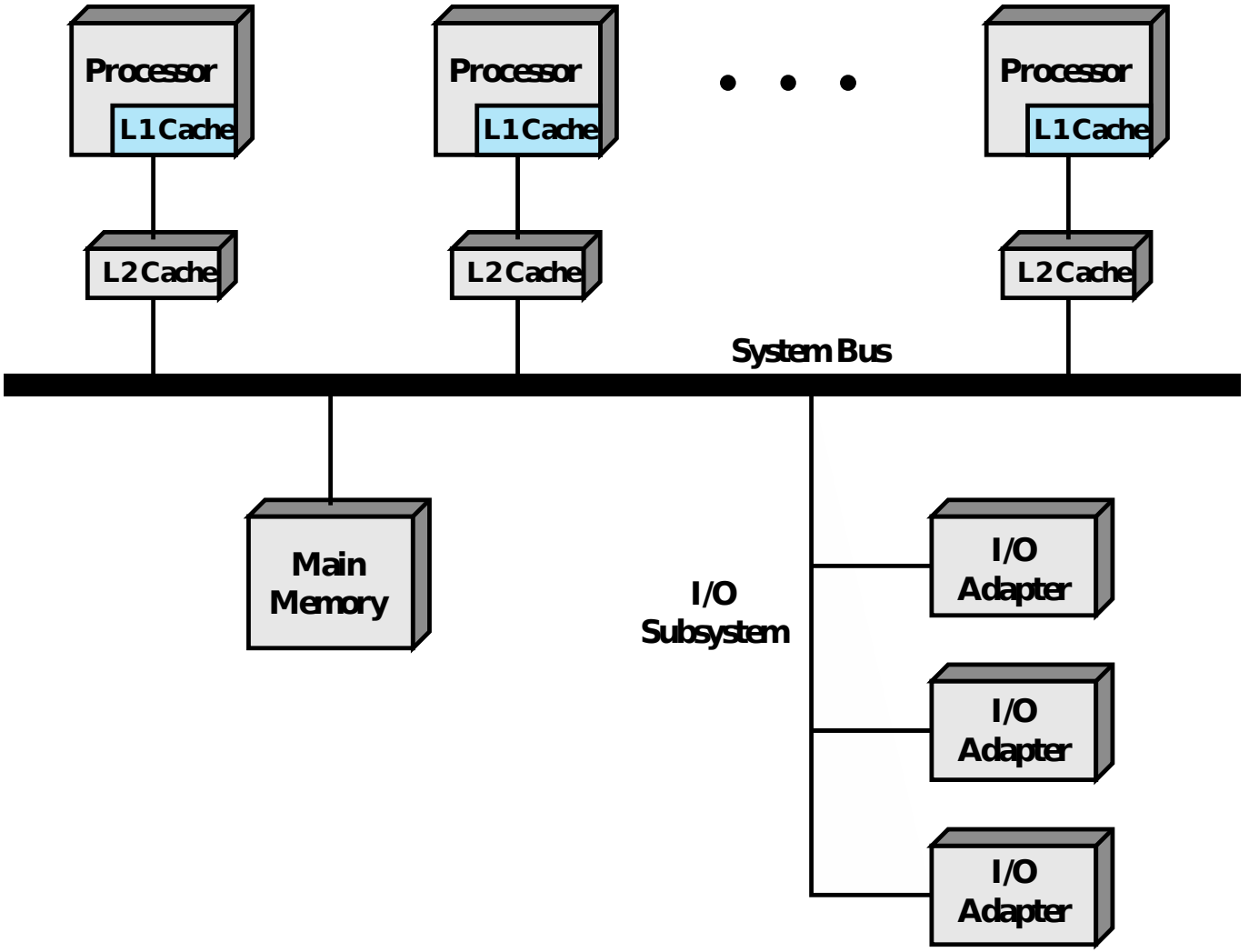


Figure 1.19 Symmetric Multiprocessor Organization

Source :- Operating Systems: Internals and Design Principles

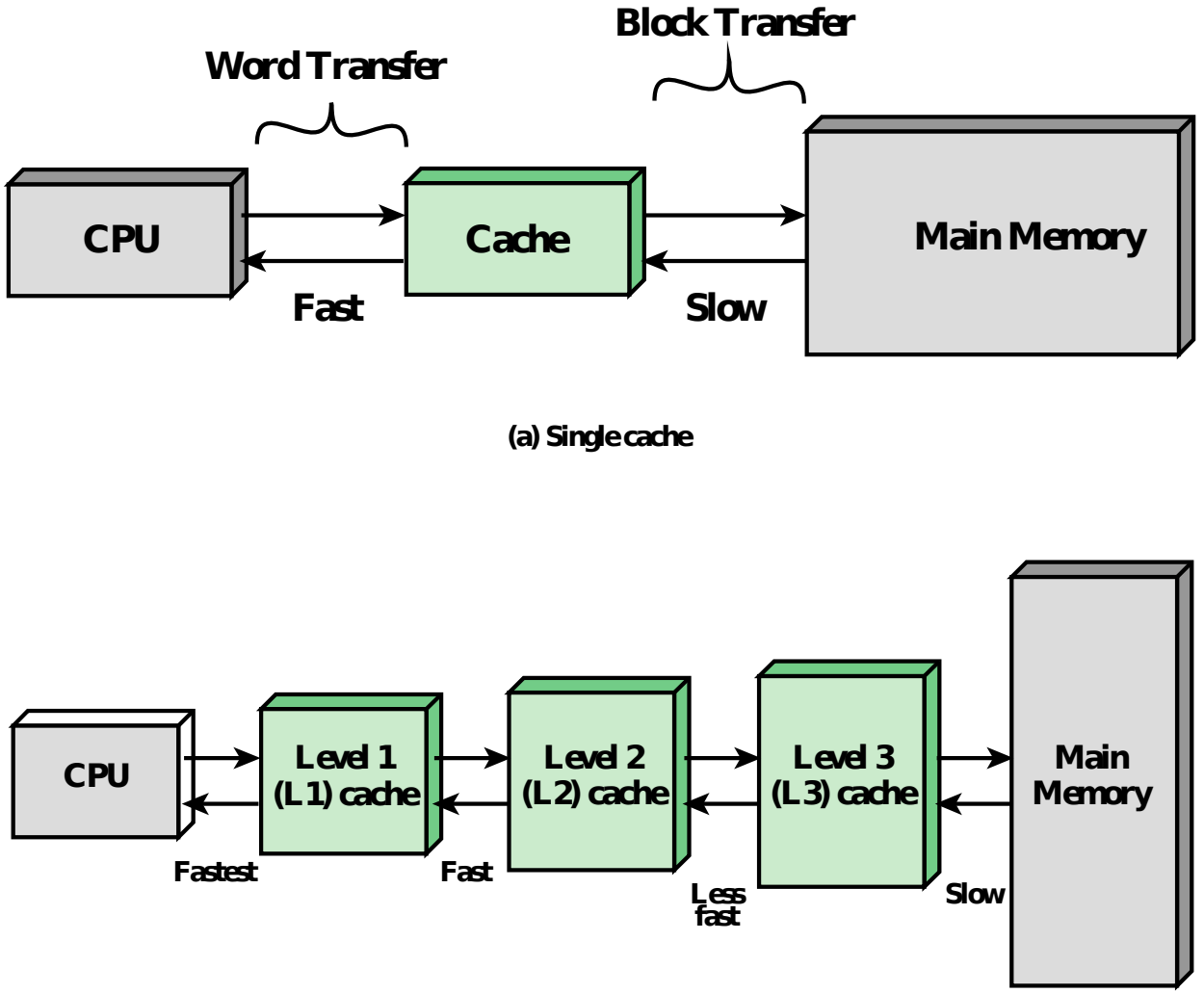
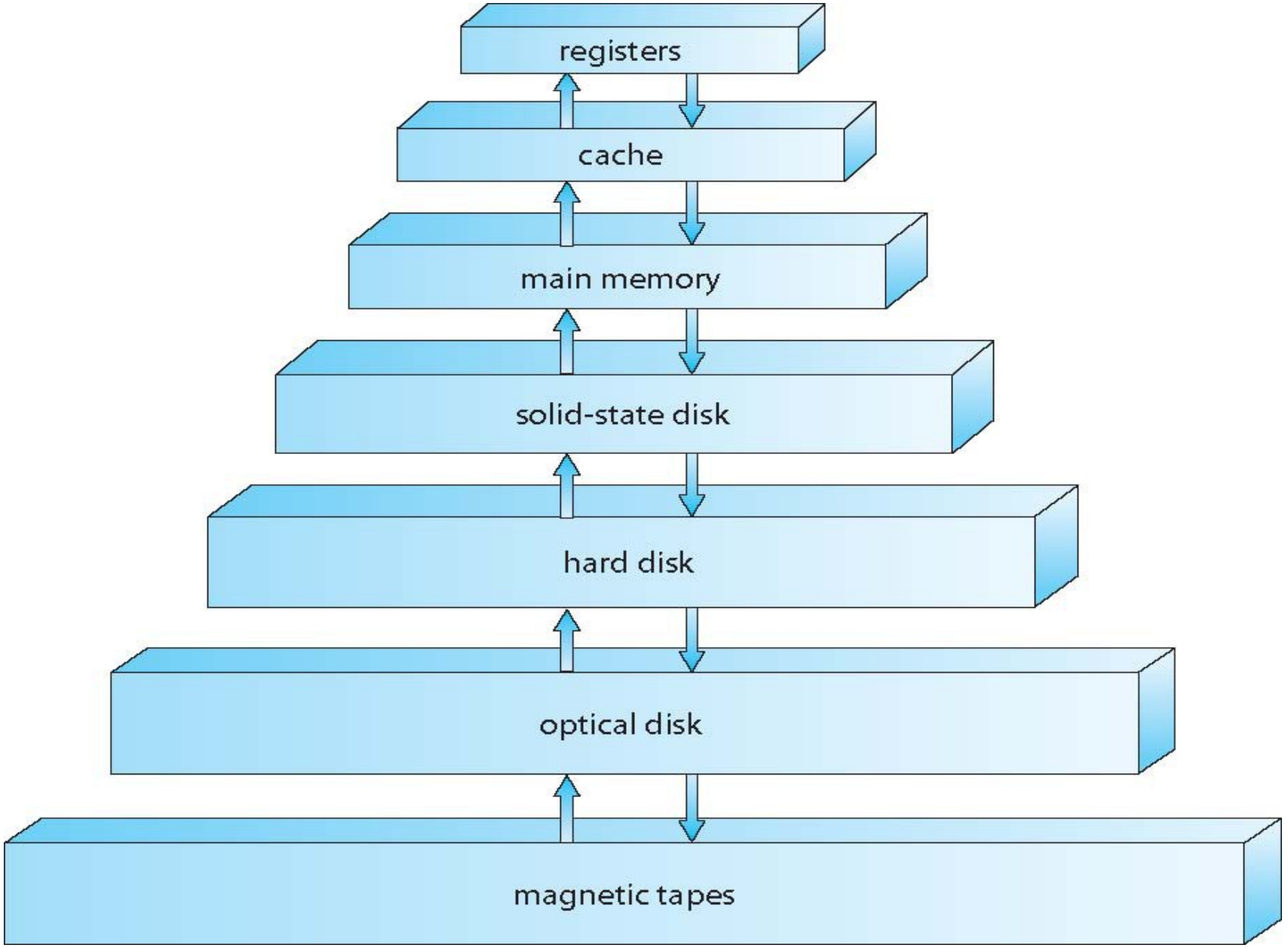


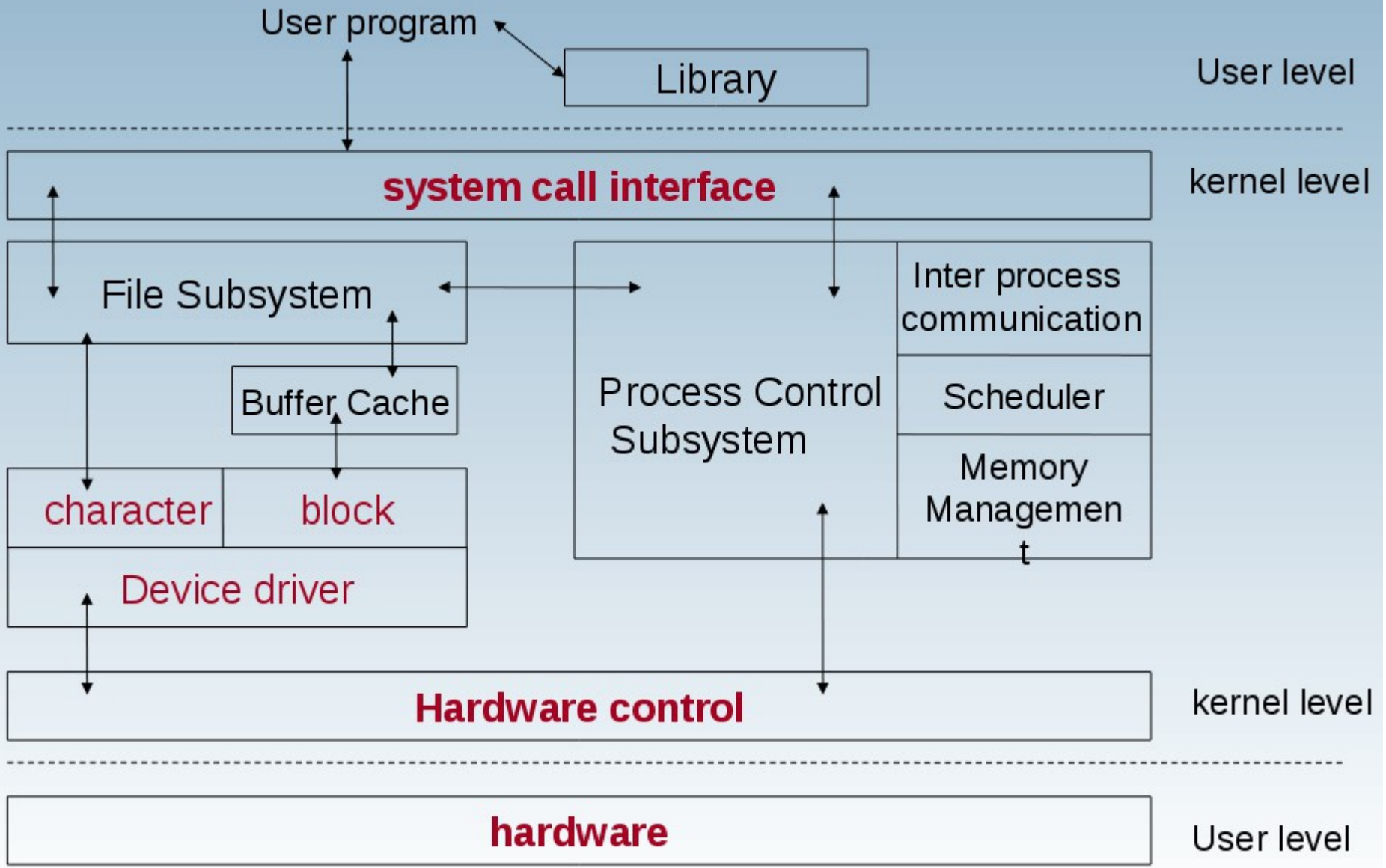
Figure 1.16 Cache and Main Memory

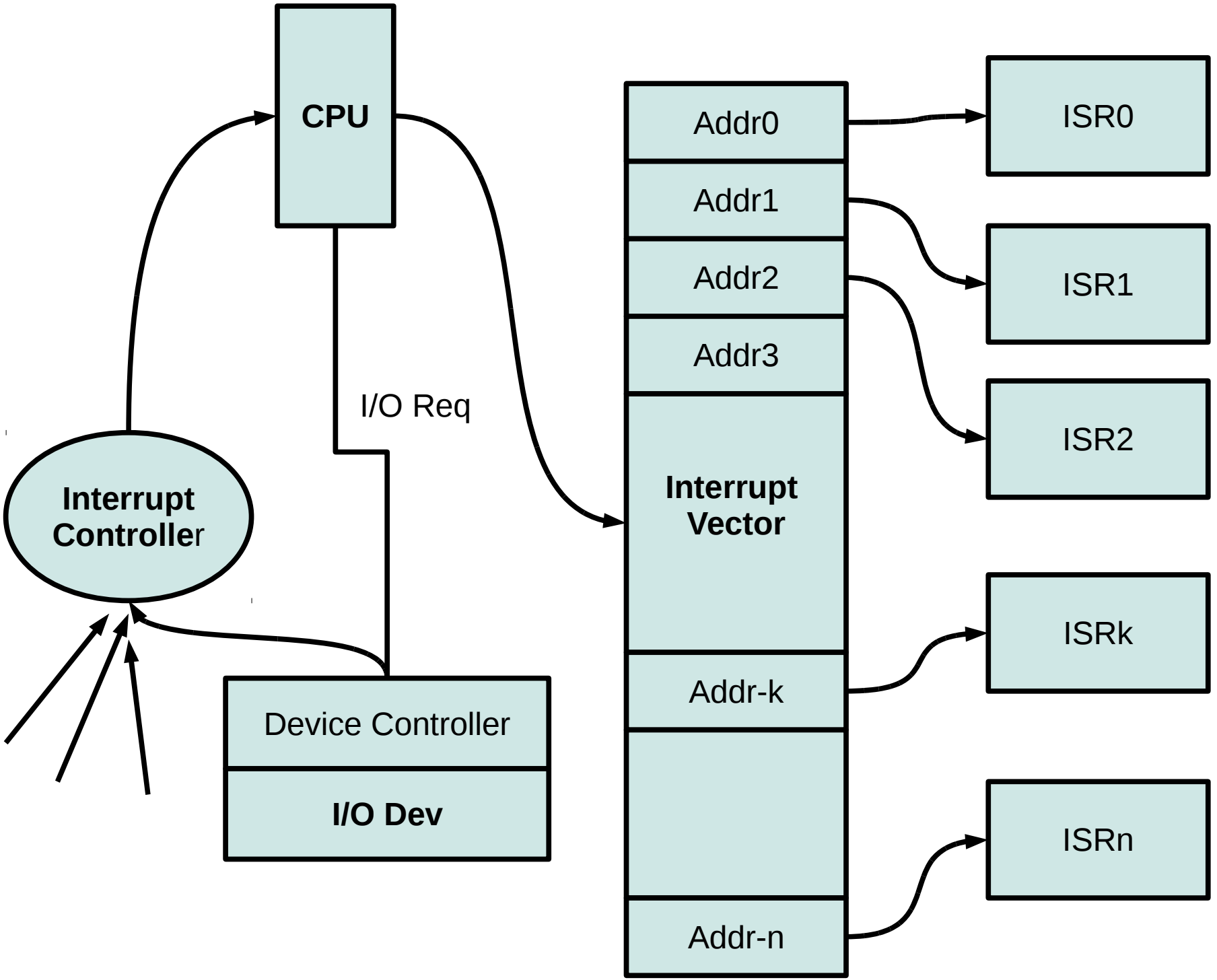
Source :- Operating Systems: Internals and Design Principles

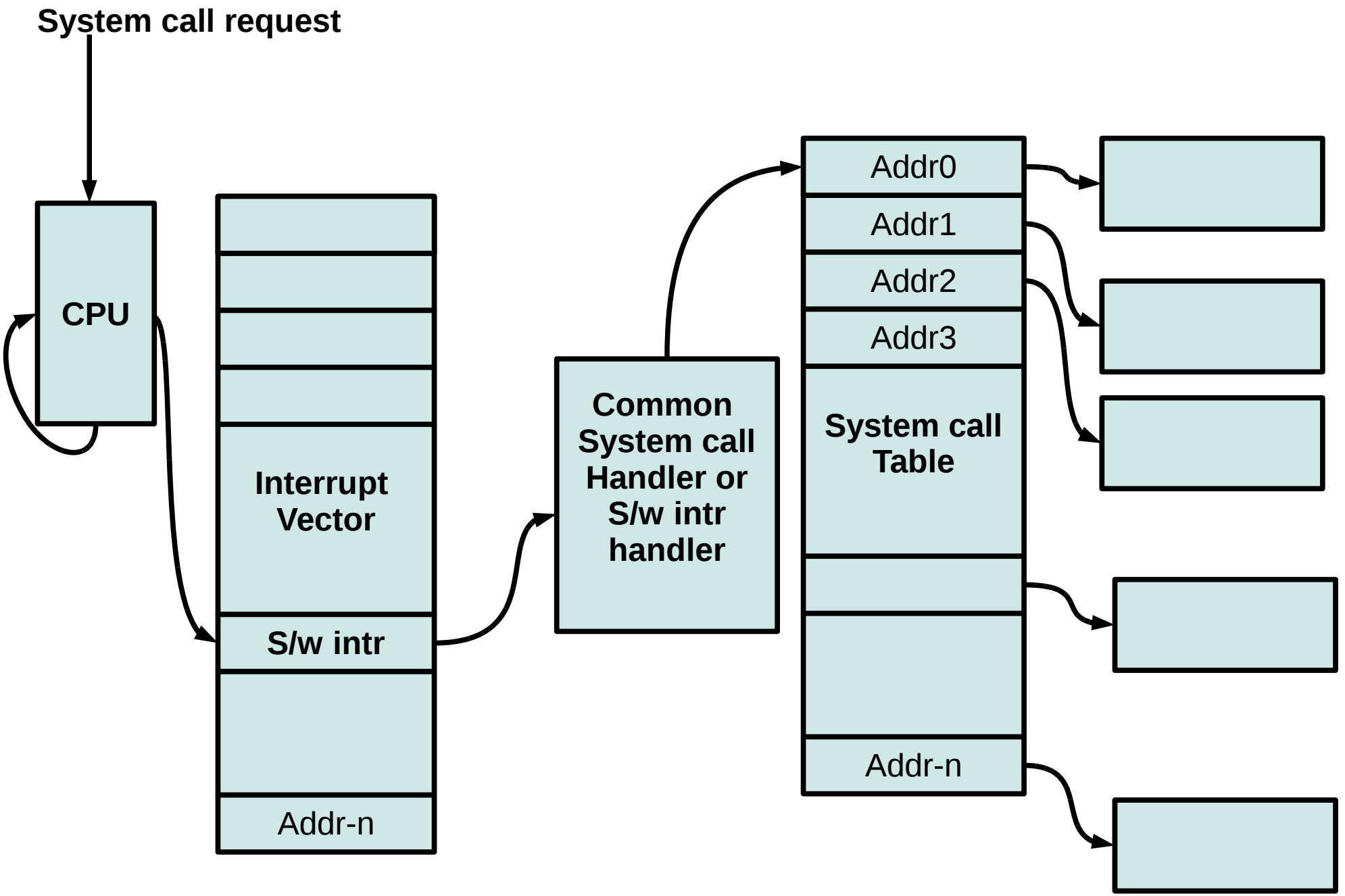


Source :- Operating System Concepts, Galvin

kernel Architecture (UNIX)




CPU
Addr0
Addr1
Addr2
Addr3
Interrupt Vector
Addr-k
Addr-n
ISR0
ISR1
ISR2
ISRk
ISRn
I/O Req
Interrupt Controller
Device Controller
I/O Dev


System call request
CPU
Interrupt Vector
S/w intr
Addr-n
Common System call Handler or S/w intr handler
Addr0
Addr1
Addr2
Addr3
System call Table
Addr-n