Saptarshi Talukdar

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Skills

Digital & FPGA: SystemVerilog, Verilog, Quartus Prime, ModelSim, FPGA Design, Computer Architecture, RISC-V Assembly

Embedded Systems: C/C++, Embedded C, UART/I2C/SPI/PoE, Real-Time Systems, MPLAB X IDE, Python, MATLAB

Circuit Design & PCB: Altium Designer, KiCAD, PCB Layout, Power Electronics, LTSpice, Circuit Analysis, Soldering

Education

University of Toronto **Sept 2023 – May 2027**

*BASc Electrical Engineering, AI Minor – **3.89 CGPA [RBC Tech Scholar in AI]*** *Toronto, Canada*

Coursework: Digital Systems, Computer Organization, Verilog, C/C++, Hardware Design and Communication, Signals and Systems, Circuit Analysis, Semiconductor Devices, Energy Systems, Linear Algebra, Differential Equations

Experience

IEEE Student Branch UofT **Aug 2025 – Present**

ASIC Team Associate *Toronto, Canada*

- Design and verify **custom integrated circuits** using **HDL**, contributing to **architecture, logic, and verification** for projects
- Performed **SPICE simulations** of pre-made XOR blocks and tested **NMOS/PMOS layouts** created in **Magic** and **Siliwiz**
- Collaborate with team to prepare designs for **fabrication**, ensuring **functionality**, **testability**, and adherence to design cycles

Power Line Communication Research, UofT ECE **May 2025 – Aug 2025**

Undergraduate Researcher, Prof. Aleksander Prodic *Toronto, Canada*

- Developed a low-power **Power Line Communication (PLC)** system enabling textile-integrated biosensors for **Myant Inc.**
- Implemented **FPGA**-based **UART**, **Manchester** encoding, and **On-Off Keying** controllers in **SystemVerilog** for data transfer
- Validated conductive fabrics by transmitting **2.5 W** (500 mA at 5 V) across **2.1 m** while maintaining stable PLC communication
- Optimized **bias-tee** and **filtering circuits** to improve noise resilience and sustain data rates up to **1 MBaud**

RSX (Robotics for Space Exploration) **Sep 2024 – May 2025**

Electrical Team Member *Toronto, Canada*

- Designed **200W synchronous boost converter** using **TPS43060** to power rover subsystems, enabling **stable operation**
- Created and assembled **PCB** in **KiCAD**, optimized layout for **thermal** performance, **power efficiency**, **high current** handling
- Developed **isolated PoE injector board** delivering up to **52V at 1.2A** to power **camera** and **antenna** over Ethernet
- Tested and verified **PoE board** under **load conditions**, allowing successful participation in the **University Rover Challenge**

Projects

Vector Processing Unit (VPU) – DE10-Lite FPGA | *SystemVerilog, FPGA, C++, ModelSim* **Jun 2025 – Present**

- Designed an **8×8 systolic array based processor** for fast **INT8 vector/matrix operations** with **32-bit accumulators**
- Implemented a **custom one-hot encoded instruction set** with **32-bit opcodes** for **parallel execution** of complex operations
- Developed a **C++ assembler** to generate **instructions** for **neural network inference**, **DSP**, and **matrix computations**
- Verified all modules using **ModelSim testbenches**, ensuring correct and modular operation across different use cases
- **Project Link and Documentation:** github.com/SattiDaBeaver/Vector-Processing-Unit

Neural Network on FPGA – DE10-Lite FPGA | *SystemVerilog, Embedded C, Python, FPGA, ModelSim* **May 2025 – Jun 2025**

- Implemented a **multilayer perceptron (MLP)** in **SystemVerilog** for **handwritten digit recognition** on **MNIST dataset**
- Deployed a **model** with **4 hidden layers**, **16 neurons each** on the **DE10-Lite FPGA**, achieved **95% classification accuracy**
- Designed **modular neuron architecture** supporting **configurable input size**, **bit width**, and **layer depth** for flexibility
- Verified all modules using **ModelSim testbenches**; generated **Q8.8 fixed-point weights/biases** via **Python scripts**
- Developed a **touchscreen UI** in **Embedded C** to draw digits and send data to the **FPGA**; predictions on a **7-segment display**
- **Project Link and Documentation:** github.com/SattiDaBeaver/Neural-Network-on-FPGA

Modulator for Software-Defined Radio | *ATmega324, Embedded C, Altium, MPLAB X IDE* **Jan 2025 – Apr 2025**

- Built a **modulator subsystem** outputting **in-phase (I)** and **quadrature (Q) signals** from **baseband input** for ECE295
- Implemented **internal call sign transmission** on the **ATmega324**; only team in 4 years of the course to achieve this
- Optimized **DAC** and **signal processing** with **fixed-point arithmetic** at 8 MHz, achieving precise timing on a slow MCU
- Created the **PCB** in **Altium** and programmed the **microcontroller** using **MPLAB X IDE** and **PICkit 4 programmer**
- Project recognized with the **Kepler Most Innovative Design Award** for technical creativity and system performance

Awards and Achievements

RBC Tech Scholars in AI Engineering

- **One of five** third-year engineering students awarded **CAD 25,480** for **academic excellence** and **AI minor** focus

Kepler Most Innovative Design Award (ECE295)

- Recognized for **originality** and **execution**; **only team** in course's 4-year history to successfully transmit internal signal

Top 30 in ECE Department

- Ranked among the **top 30 students** in Electrical and Computer Engineering Department; attended **ECE Awards Dinner**