Saptarshi Talukdar

saptarshi.talukdar@mail.utoronto.ca linkedin.com/in/saptarshi-talukdar github.com/SattiDaBeaver

Skills

Hardware & Design: FPGA, Quartus Prime, Altium Designer, KiCAD, PCB Design, Circuit Design, Digital Electronics

Programming & Software: C/C++, SystemVerilog, Verilog, Python, ModelSim, LTSpice, MPLAB X IDE

Education

University of Toronto **Sept 2023 – May 2027**

BASc Electrical Engineering, ***3.89 CGPA [Dean's Honors List, Top 30 ECE]*** *Toronto, Canada*

Coursework: Computer Organization, Digital Systems, Hardware Design and Comm., Signals and Systems

Experience

Power Line Communication Research, UofT ECE **May 2025 – Present**

Undergraduate Researcher, Prof. Aleksander Prodic *Toronto, Canada*

- Developing a low-power Power Line Communication (PLC) system for textile-integrated biosensors with Myant Inc.
- Designed the interface between biosignal sensors and a PLC transceiver IC using a microcontroller for data handling
- Implemented firmware for master-slave communication to enable reliable sensor data acquisition and transmission
- Tested conductive fiber links for reliability and bandwidth; achieved 166 kbps over 2.1m with 2.5W (5V@500mA) power

RSX (Robotics for Space Exploration) **Sep 2024 – Present**

Electrical Team Member *Toronto, Canada*

- Designed a 200W synchronous boost converter using the TPS43060 to power the rover's subsystems
- Created and assembled the PCB in KiCAD, optimizing layout for thermal performance and high current handling
- Developed an isolated PoE injector board delivering up to 52V at 1.2A to power the camera and antenna over Ethernet
- Tested and verified the PoE board to ensure reliable operation under load conditions for the University Rover Challenge

Projects

Neural Network on FPGA — DE10-Lite | *FPGA, ModelSim, SystemVerilog, C, Python* **May 2025 – Jun 2025**

- Implemented a multilayer perceptron (MLP) in SystemVerilog for handwritten digit recognition on MNIST dataset
- Deployed the model with 1 hidden layer of 16 neurons on the DE10-Lite FPGA, achieving 95% classification accuracy
- Designed modular, parameterized neuron architecture supporting configurable input size, bit width, and layer depth
- Verified all modules in ModelSim using custom testbenches; used Python to generate Q8.8 fixed-point weights/biases
- Developed a touchscreen-based UI in C to draw digits and send data to the FPGA; predictions on a 7-segment display
- **Project Link:** github.com/SattiDaBeaver/Neural-Network-on-FPGA

Modulator for Software-Defined Radio | *ATmega324, Embedded C, Altium, MPLAB X IDE* **Jan 2025 – Apr 2025**

- Built a modulator subsystem that outputs in-phase (I) and quadrature (Q) signals from baseband input for ECE295
- Implemented internal call sign transmission on the ATmega324; only team in 4 years of the course to achieve this
- Designed a high-speed custom DAC for I/Q output, optimized for precision and timing-critical performance
- Created the PCB in Altium and programmed the microcontroller using MPLAB X IDE and PICkit 4 programmer
- Project recognized with the **Kepler Most Innovative Design Award** for technical creativity and system performance

8-bit Processor on DE10-Lite FPGA | *Verilog, C++, Quartus Prime, ModelSim* **Mar 2025 – May 2025**

- Designed and implemented an 8-bit processor with 11 instructions on the DE10-Lite FPGA using Verilog
- Added a 256-bit memory and memory-mapped I/O support for peripheral interaction and system extensibility
- Developed a custom assembler in C++ to convert assembly code into machine code (binary) for the processor
- Simulated the processor in ModelSim and successfully deployed it on the DE10-Lite board for hardware validation
- **Project Link and Documentation:** https://github.com/SattiDaBeaver/SimProc

Awards and Achievements

Kepler Most Innovative Design Award (ECE295)

- Awarded for originality and execution; only team in course's 4-year history to successfully transmit internal signal

Top 30 in ECE Department

- Ranked among the top 30 students in Electrical and Computer Engineering Department; attended ECE Awards Dinner

Dean's Honours List

- Achieved a CGPA of 3.89/4.0, earning a place on the Dean's Honours List for all semesters