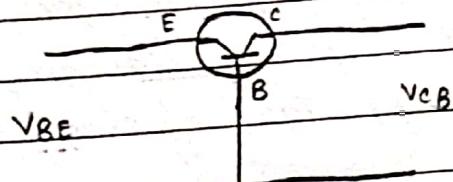


## Common Base Configuration



Current gain =  $\frac{\text{Output current}}{\text{Input current}}$

Input voltage =  $V_{BE}$

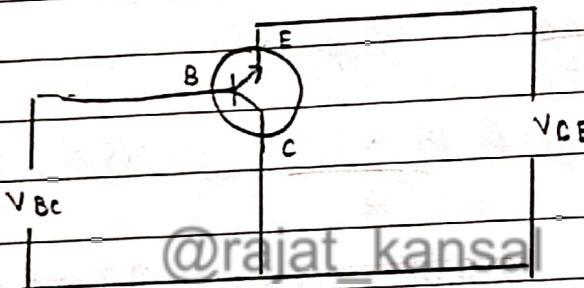
Output voltage =  $V_{CB}$

Input current =  $I_E$

Output current =  $I_C$

Current gain ( $\alpha$ ) =  $\frac{I_C}{I_E}$

## Common Collector Configuration



Input voltage =  $V_{BC}$

Output voltage =  $V_{CE}$

Input current =  $I_B$

Output current =  $I_E$

Current gain ( $\gamma$ ) =  $\frac{I_E}{I_B}$

## Formulas

$$I_E = I_B + I_C$$

$$I_B = \frac{I_E}{1+\beta}$$

$$\alpha = \frac{I_C}{I_E}$$

$$\beta = \frac{I_C}{I_B}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\alpha = \frac{\beta}{\beta+1}$$

Ques: A 230 V, 50 Hz voltage is applied to primary of a 4:1 step down transformer used in bridge rectifier having load resistance of 600 Ω. Assuming diode to be ideal, determine

- (a) DC output voltage
- (b) DC power supplied to load
- (c) PIV
- (d) Output frequency

$$(a) \frac{N_1}{N_2} = \frac{V_1}{V_2}$$

$$V_{\text{rms}} = V_2 = \frac{230}{4} = 57.5 \text{ V}$$

$$V_m = 57.5\sqrt{2}$$

$$V_{\text{dc}} = \frac{2 \times V_m}{\pi} = \frac{2 \times 57.5 \times 1.414}{3.14} = 51.78 \text{ V}$$

$$@ \text{V}_{\text{dc}} = 51.78$$

$$(b) P_{\text{dc}} = \frac{V_{\text{dc}}^2}{R_L} = \frac{(51.78)^2}{600} = 4.46 \text{ W}$$

$$(c) PIV = V_m = 81.3 \text{ V}$$

$$(d) \text{Output frequency} = 2 \nu = 2 \times 50 = 100 \text{ Hz}$$

Ques Find current through series resistance, zener diode and load resistance for circuit given below.

loop ABEFA

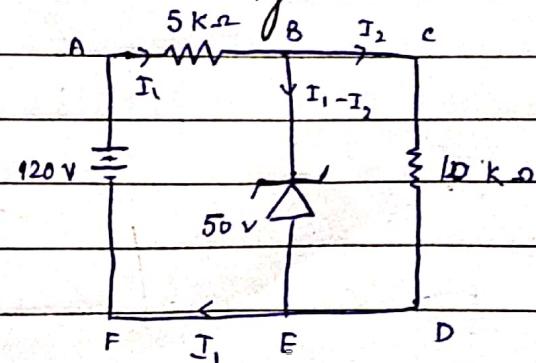
$$5000 I_1 + 50 - 120 = 0$$

$$5000 I_1 = 70$$

$$I_1 = \frac{7}{500}$$

$$= 1.4 \times 10^{-2} \text{ A}$$

$$= 14 \text{ mA}$$



loop BCDEB

$$10000 I_2 = 50$$

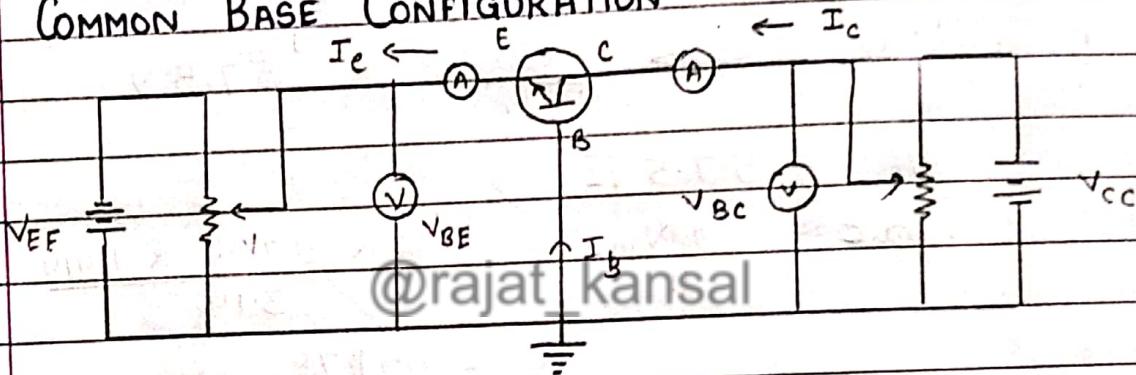
$$I_2 = \frac{50}{10000} = 5 \text{ mA}$$

Current through series resistance =  $I_1 > 14 \text{ mA}$

" " " load resistance =  $I_2 > 5 \text{ mA}$

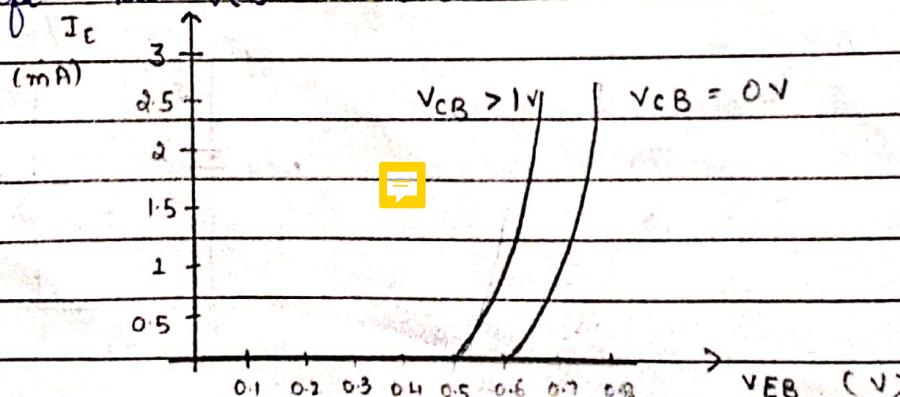
" " " Zener diode =  $I_1 - I_2 > 9 \text{ mA}$

### COMMON BASE CONFIGURATION



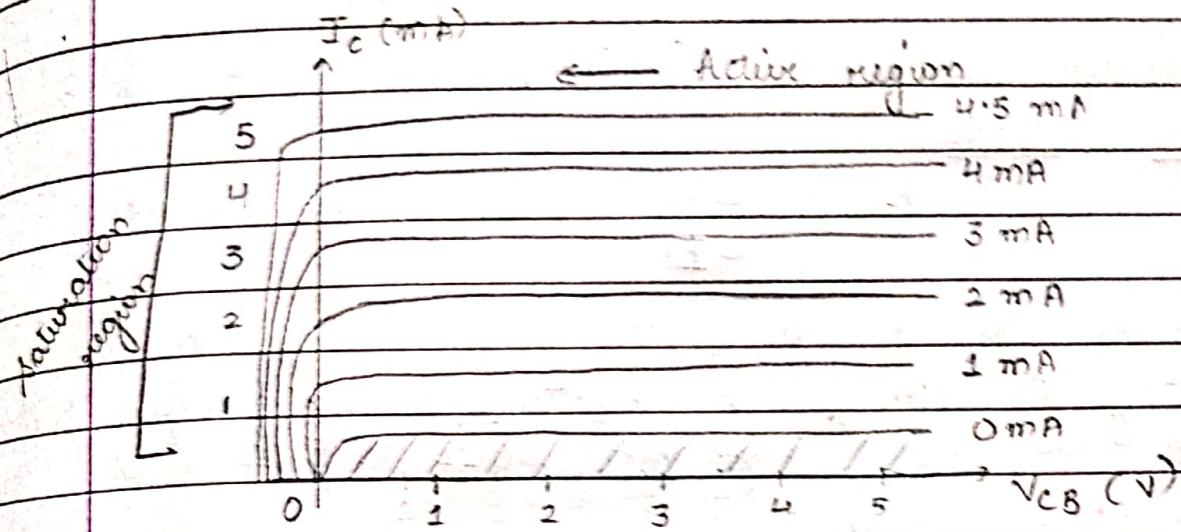
### Input Characteristics

1.  $V_{CB}$  is kept constant at zero volt
2.  $I_e$  is increased from 0 by small increasing  $V_{EB}$
3. Curve is drawn between  $I_e$  and  $V_{BE}$  at constant collector base voltage ( $V_{CB}$ )
4. when  $V_{CB}$  is increased keeping  $V_{EB}$  constant, width of base region will decrease, this results in increase of  $I_e$ . Therefore curve shifts to left as  $V_{CB}$  increase



## Output characteristics

1.  $I_e$  is kept constant by adjusting  $V_{ES}$
2. It can be seen that for a constant value of  $I_e$ ,  $I_c$  is independent of  $V_{CB}$ .



3. Curves are parallel to  $V_{CB}$  axis.  $I_c$  flows even when  $V_{CB} = 0$

4. As emitter-base junction is forward biased,  $e^-$  from emitter are ejected toward base. Due to reverse bias of collector-base junction  $e^-$  flow toward collector  $\rightarrow$  region gives rise to  $I_c$  even when  $V_{CB}$  is zero.

## Early Effect or Base with Modulation

As collector voltage  $V_{CC}$  is made to increase the reverse bias, the space charge width between collector and base is tend to increase with the result that effective width of base decreases. This dependency of base width on collector voltage is known as Early Effect.

## Punch Through

For ext. large voltages, effective base width may be reduce to 0, causing voltage breakdown in transistor, this

phenomena is called punch through.

- \* For higher value of  $V_{CB}$  due to early effect the value of  $\alpha$  increases  
 $\alpha$  changes from 0.98 to 0.985.

### Transistor Parameter (H-Parameter or Hybrid Parameters)

#### 1. Input Impedance

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, \quad V_{CB} = \text{constant}$$

It is defined as ratio of change in emitter voltage to change in emitter current keeping  $V_{CB}$  constant.  
 Typical value of  $h_{ib}$  ranges from  $20\Omega$  to  $50\Omega$ .

#### 2. Output Impedance

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, \quad I_E \text{ constant}$$

It is defined as ratio of change in collector current to change in collector voltage with emitter current constant.

Typical value of  $h_{ob}$  is of order of  $0.1 \Omega$  to  $10 \Omega$ .

#### 3. Forward current gain

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, \quad V_{CB} \text{ constant}$$

It is defined as ratio of change in collector current to emitter current with  $V_{CB}$  constant. Typical value varies from 0.9 to 1.

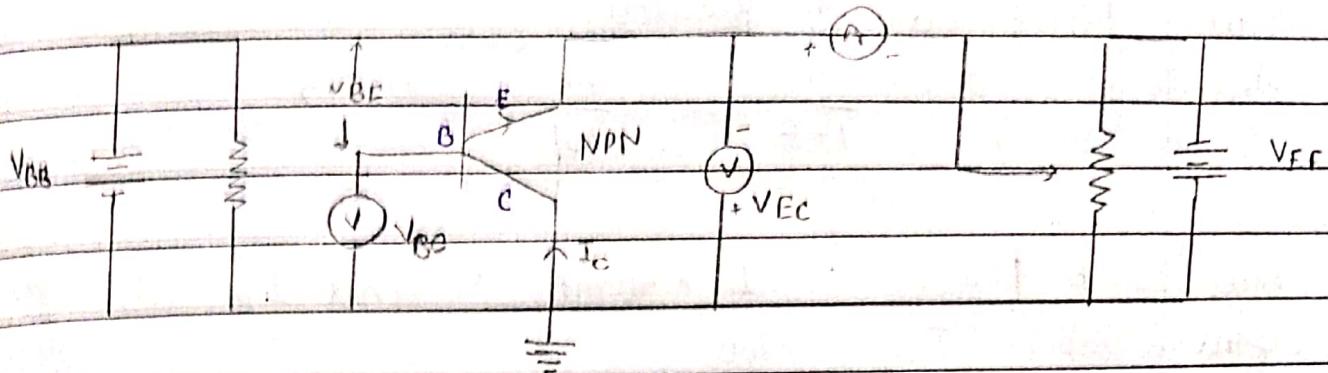
#### 4. Reverse voltage gain

$$h_{rdb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, \quad I_C \text{ constant.}$$

It is defined as ratio of change in emitter voltage to change in collector voltage with constant  $I_C$ .

Typical value of  $\alpha$  is of order of  $10^{-5}$  to  $10^{-4}$

## COMMON COLLECTOR



Q. In common base, emitter current is 10 mA and collector current 9.8 mA. Find base current.

Ans

$$I_e = I_b + I_c$$

$$I_b = 0.2 \text{ mA}$$

Q. In CB, emitter current is 6.28 mA and  $I_c = 6.20 \text{ mA}$ . Determine common base dc current gain.

Ans

$$\alpha = \frac{I_c}{I_e} = \frac{6.20}{6.28} = 0.987$$

Q. CB dc current gain is 0.967.  $I_e = 10 \text{ mA}$   $I_b = ?$

Ans

$$\frac{I_c}{I_e} = 0.967$$

$$I_c = 9.67$$

$$I_b = I_e - I_c = 0.33 \text{ mA}$$

Q. Transistor has  $I_e = 10 \text{ mA}$   $\alpha = 0.98$ . Determine  $I_c, I_b$

$$I_c = \alpha \times I_e = 0.98 \times 10 = 9.8$$

$$I_b = I_e - I_c = 10 - 9.8 = 0.2 \text{ mA}$$

Ques If  $\alpha = 0.97$  Find  $\beta$

Ans  $\beta = \frac{\alpha}{1-\alpha} = \frac{0.97}{0.03} = 32.3$

Ques Find  $\alpha$  if  $\beta = 200$

Ans  $\alpha = \frac{\beta}{1+\beta} = \frac{200}{201} = 0.995$

Ques  $\beta = 100$   $I_c = 40 \text{ mA}$  - Find  $I_e$

Ans  $\frac{I_e}{I_b} = 100$

$$I_b = \frac{40}{100} = 0.4 \text{ mA}$$

$$I_e = I_c + I_b = 40.4 \text{ mA}$$

Ques  $\beta = 150$   $I_c, I_b = ?$   $I_e = 10 \text{ mA}$

Ans  $\alpha = \frac{\beta}{\beta+1}$

$$\frac{I_e}{I_b} = \frac{150}{151}$$

$$I_c = \frac{150 \times 10}{151} = 9.93 \text{ mA}$$

$$I_b = 10 - 9.93 = 0.07 \text{ mA}$$

Q.  $I_b, I_e = ?$   $I_c = 80 \text{ mA}$   $\beta = 170$

Ans  $\frac{I_c}{I_b} = 170$

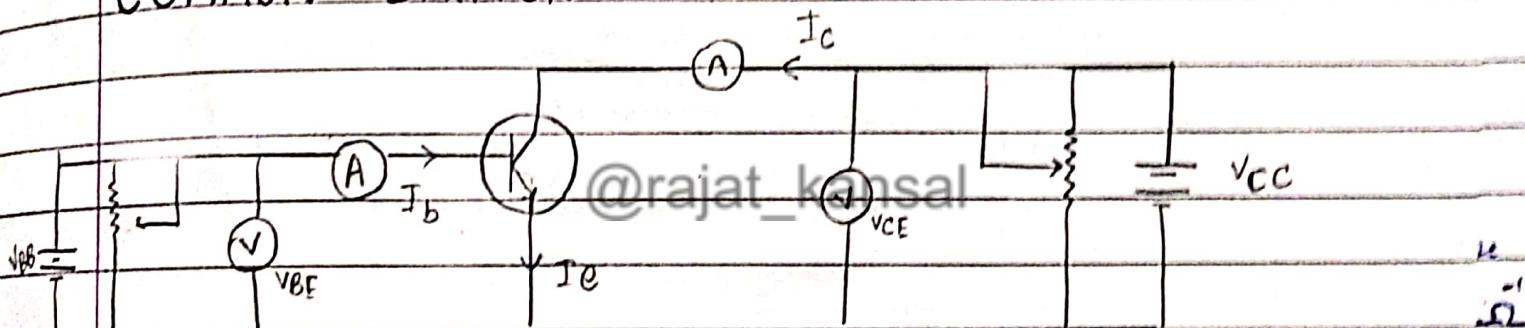
$$I_b = \frac{80}{170} = \frac{8}{17} = 0.47 \text{ mA}$$

$$I_e = 80.47 \text{ mA}$$

# COMPARISON OF COMMON BASE, COMMON EMMITTER, COMMON COLLECTOR

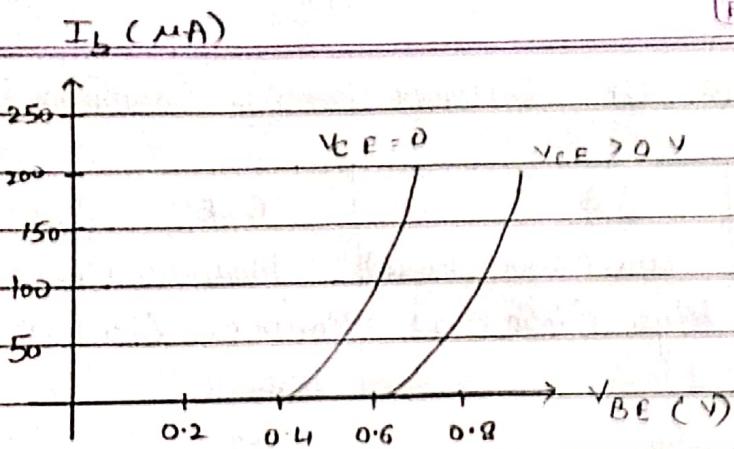
Property	C.B	C.E	C.C
Input resistance	Low (about $100\ \Omega$ )	Moderate (about $750\ \Omega$ )	High ( $750\ K\ \Omega$ )
Output current gain	High ( $450\ K\ \Omega$ )	Moderate ( $45\ K\ \Omega$ )	Low ( $25\ \Omega$ )
Voltage gain	1	High 500	High less than 1
Phase shift b/w Inp and output voltages	$0^\circ$ or $360^\circ$	$180^\circ$	$0^\circ$ or $360^\circ$
Application	For high frequency circuits	For audio frequency circuits	For impedance matching circuits

## COMMON Emitter



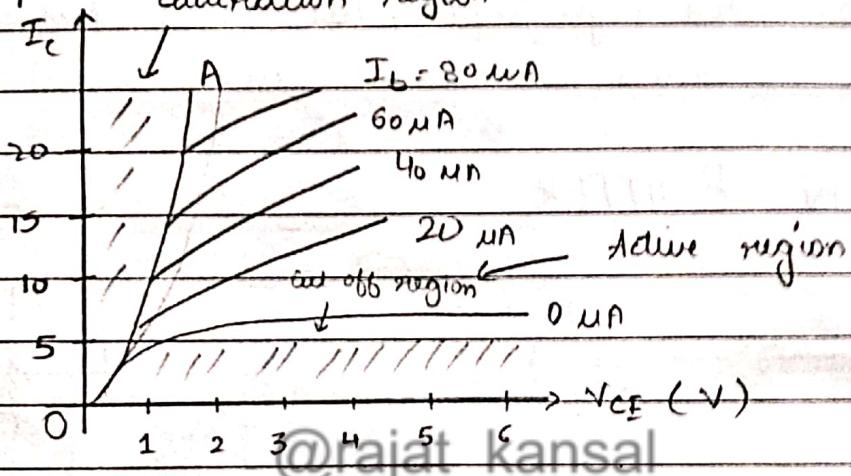
### Input Characteristics

1. Character to emitter voltage is kept constant at 0V.
2. Base current  $I_B$  is increased from 0 by increasing  $V_{BE}$ .
3. When  $V_{CE}$  is 0, emitter-base junction is forward biased.
4. When  $V_{CE}$  is increased, width of depletion region at reverse biased collector-base junction will increase so width of base will decrease.
5. Therefore  $V_{BE}$  should be increased, hence curve shift to right as  $V_{CE}$  is increased.



### Q3f Output characteristics

Saturation region



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$T_b$  is kept constant at suitable value.  $V_{CE}$  is increased from 0 V

Even for larger values of  $V_{CE}$ , a very small change in  $\alpha$  is reflected. When  $\alpha$  is 0.98  $\alpha = 0.985$   
 $\beta$  is 49  $\beta = 66$

A slight inc in  $\alpha$  by about ~~0.5%~~ result in inc in  $\beta$  by about 30%.

→ The region below the curve for  $I_b = 0$ , is called cut off region. In this region, both junction are reverse biased.

→ The central region where curves are uniform in spacing and slope is called active region. In

this region, emitter - base junction is forward biased and C-B junction is reverse biased.

The region of curve of to left of line OA is called saturation region and line OA is called saturation line.

In this region, both junction are forward biased.

### TRANSISTOR PARAMETER

#### 1. Input Impedance.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, V_{CE} \text{ constant}$$

Ratio of change in base voltage to change in base current.

The typical value of  $h_{ie}$  ranges from 500 to 2000  $\Omega$ .

#### 2. Output admittance.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, I_B \text{ constant}$$

Ratio of change in collector current to change in collector voltage, the typical value of  $h_{oe}$  is of order of 0.1 to  $10 \mu S$ .

#### 3. Forward current gain

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, V_{CE} \text{ constant}$$

Ratio of change in collector current to change in base current. Typical value: 30 to 200.

#### 4. Reverse voltage gain

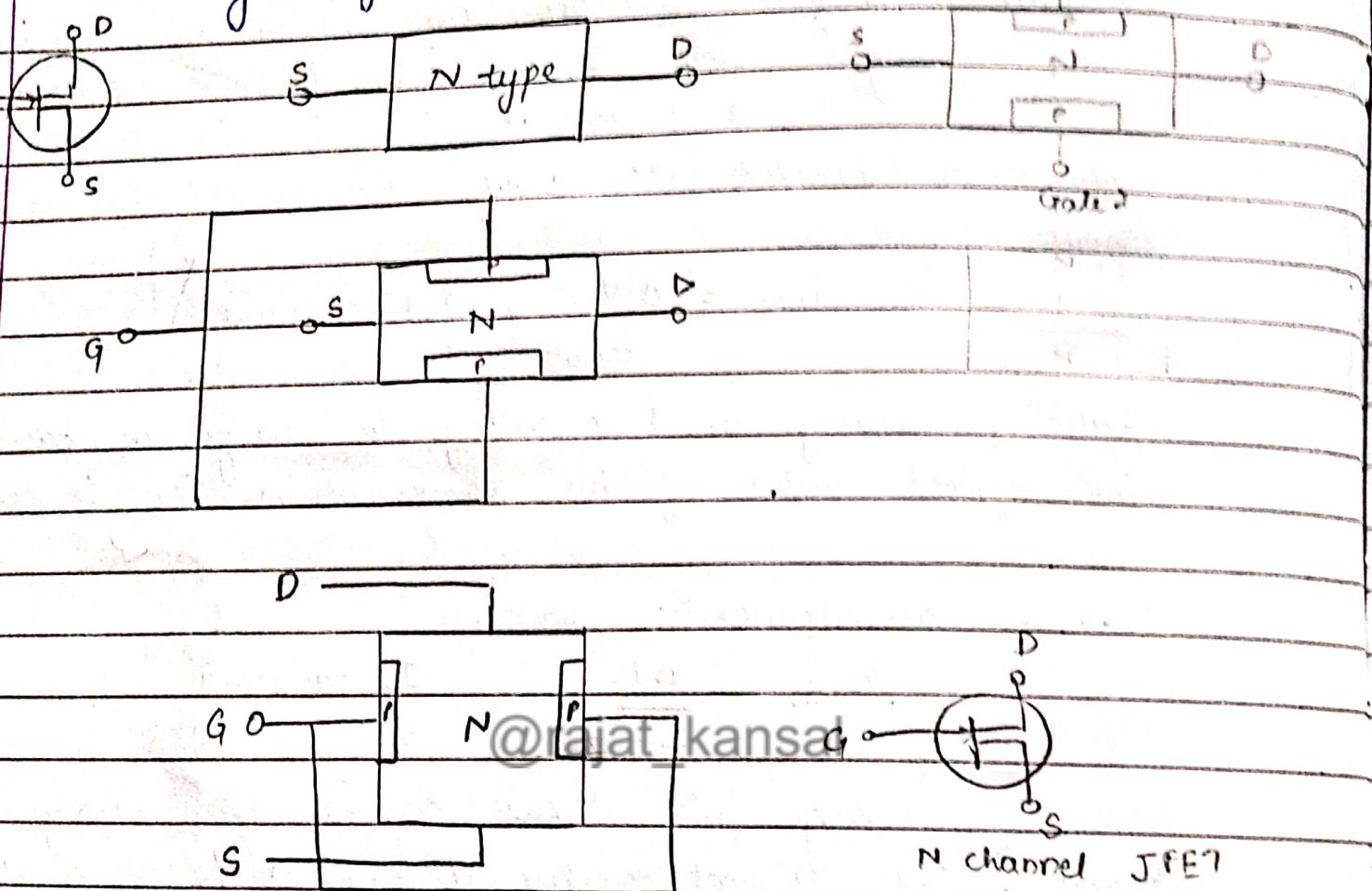
$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_B \text{ constant}$$

Ratio of change in base voltage to change in collector voltage.

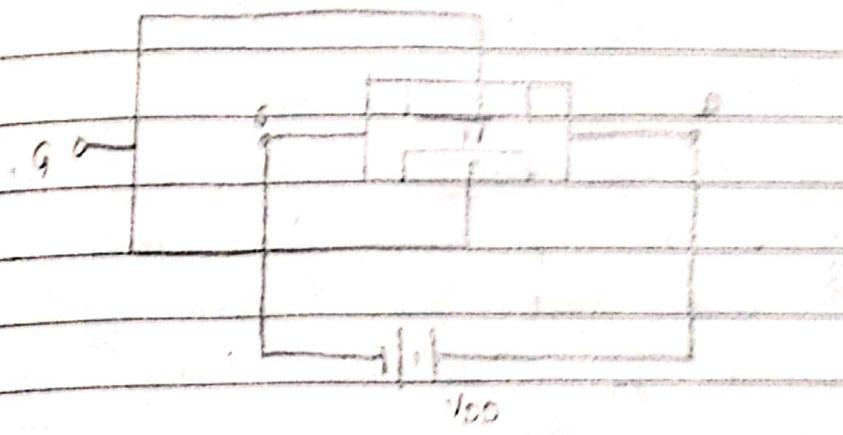
Typical value:  $10^{-5}$  to  $10^{-4}$

## JFET (JUNCTION FIELD EFFECT TRANSISTOR)

In this transistor, the flow of current through conducting region is controlled by electric field.

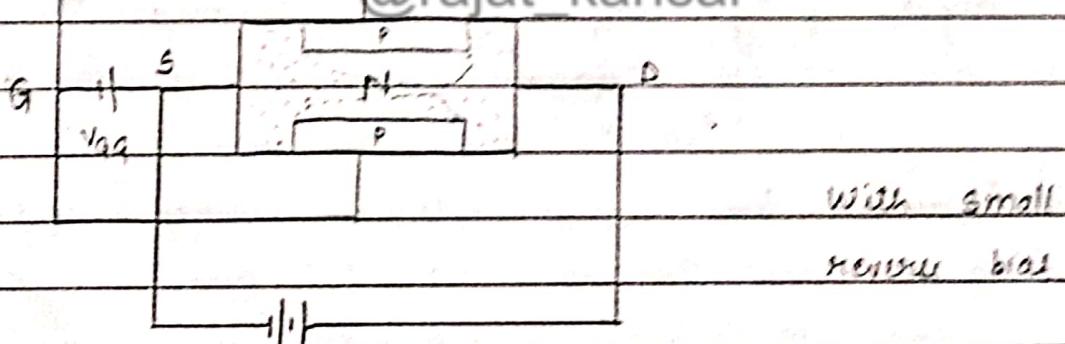


The structure of N channel JFET starts with bar of N-type silicon. This bar behaves like a resistor between its two terminals S and D (S → Source and D → Drain). Heavily doped P type regions are introduced on either side of bar. The p-regions are called gates. Usually two gates are connected together. N-type bar is called channel. P-operate an N-channel JFET by applying +ve voltage to drain with respective source.



Due to this voltage, the majority carriers in boron starts flowing from source to drain. This flow of e<sup>-</sup> makes drain current ( $I_D$ ). The e<sup>-</sup> in the boron have to pass through space between two p-regions. The width of this space can be controlled by varying the gate voltage. i.e. this space is called channel.

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A small <sup>reverse</sup><sub>bias</sub> voltage <sup>VDD</sup> is applied to gate. Because of reverse bias, width of depletion region increases. As n-type boron is lightly doped compare to p-regions, the depletion region extends more into n-type boron. This reduces the width of channel.

Channel is narrower at drain end because amount of reverse bias is not same throughout the length of p-n junction. When current flows through boron, a potential drop occurs across its length.

If reverse gate bias voltage is increased further, the channel becomes narrower at drain end and drain current further reduces. If reverse bias is made large, the depletion region tends to extend into channel and meet. This pinches off current flow. The gate source voltage, at which pinch off occurs is called pinch off voltage.

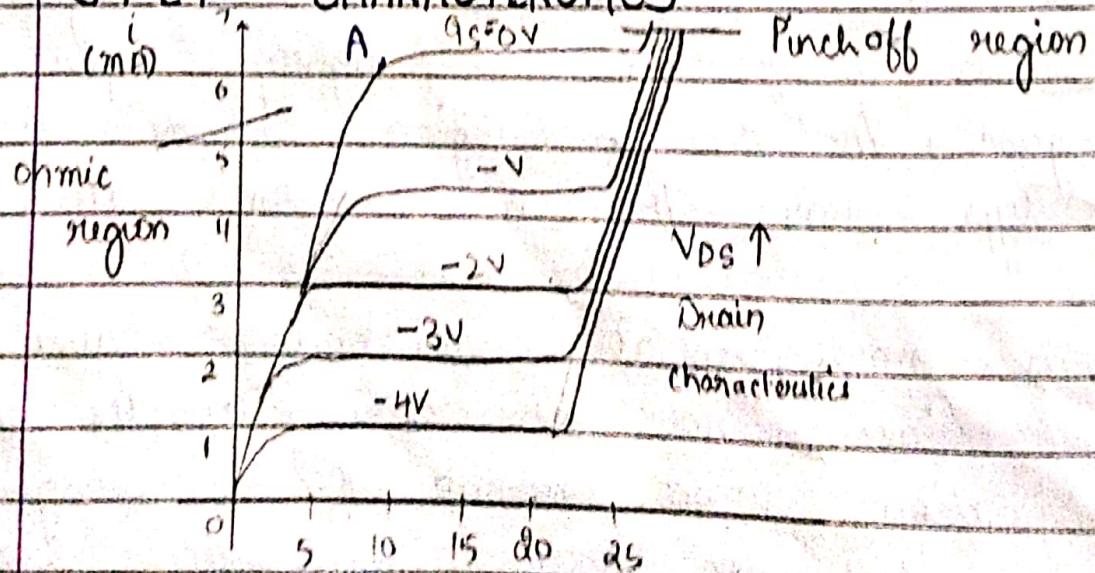
**Source** - is a terminal through which majority carriers enter bar.

**Drain** - is terminal through which majority carriers leave bar.

**Gate** - On both sides on n-type bar, heavily doped p-type regions are formed. These regions are called gates.

**Channel** - The region between source and drain is called channel. The majority carriers move from source to drain through this channel.

## JFET CHARACTERISTICS



For each curve, gate to source voltage ( $V_{GS}$ ) is constant. First step is to consider the curve for zero gate bias in which  $V_{GS}$  is 0. When  $V_{GS}$  is 0, the channel is entirely open but drain current is zero because drain terminal doesn't have majority carriers. When small  $V_{GS}$  voltage is applied, the p bar acts as barrier and  $I_D$  current increases linearly with voltage  $V_{GS}$ . The region left to A is called ohmic region and bar acts as ohmic resistor. As we start increasing  $V_{GS}$ , the channel starts becoming narrow at drain end. The channel is eventually pinched off. The current  $I_D$  no longer increases with increase in  $V_{GS}$ . It approaches a constant saturation level. The voltage  $V_{GS}$  at which channel is pinched off is called pinch-off voltage. The region to right of A is called pinched off region.

For an inc. reverse bias at gate or the breakdown of gate junction occurs at lower value of  $V_{GS}$ . This happens because the effective bias at gate junction is voltage  $V_G$  added to voltage  $V_{GS}$ .

The greater the value of  $V_{GS}$ , lower the value of  $V_{GS}$  is required by the junction to break down. The max saturation drain current is also smaller b/c conducting channel now becomes more narrower. Increase in voltage  $V_{DC}$ , inc reverse bias across gate junction therefore drain current shoots to a high value.

## JFET PARAMETERS

1. Dynamic Drain Resistance ( $r_d$ ) - It is defined as ratio of small change in drain voltage to small change in drain current keeping gate voltage constant.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

Typical value is  $400\text{ k}\Omega$

2. Mutual Conductance or Transconductance ( $g_m$ )

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}, \text{ drain voltage constant}$$

Typical value : range from  $150\mu\text{s}$  to  $250\mu\text{s}$   
 $\downarrow$  Siemens

3. Amplification Factor ( $\mu$ )

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}, I_D \text{ constant}$$

Typical value : can be as high as 100

$$\mu = r_d \times g_m$$

## NUMBER SYSTEM

- x (1) Decimal No. System

Decimal	Binary	Octal	Hexadecimal
0-9	0,1	0-7	0-15
Base $\rightarrow 10$	Base $\rightarrow 2$	Base $\rightarrow 8$	Base $\rightarrow 16$

	Binary	Hexadecimal
0	0	0
1	1	1
2	10	2
3	11	3
4	100	4
5	101	5
6	110	6
7	111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

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# Conversion of any form in decimal

①.  $(1101.011)_2 \xrightarrow{\text{Binary to decimal}} [Binary \text{ to } Decimal]$

$$1 \times 2^0 + 0 \times 2^1 + 1 \times 2^2 + 1 \times 2^3 + 0 \times 2^4 + 1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$$

$$1 + 0 + 4 + 8 + 0 + \frac{1}{4} + \frac{1}{8}$$

$$13 + \frac{d+1}{8} - \frac{104+3}{8} = \frac{107}{8}$$

$$= 13.3$$

[Octal to Decimal]

(2)  $(13.45)_8$

$$3 \times 8^0 + 1 \times 8^1 + 4 \times 8^{-1} + 5 \times 8^{-2}$$

$$3 + 8 + \frac{1}{2} + \frac{5}{16}$$

$$11 + \frac{13}{8} - 11 + 1.62 = \cancel{12.62} \quad 12.62$$

(3)

$(ABC.3A)_{16}$

$$\begin{matrix} & 11 \\ & 1 \\ 2 & B & C & \cdot & 3 & A \end{matrix} \rightarrow 10$$

[Hexadecimal to Decimal]

$$12 \times 16^0 + 11 \times 16^1 + 2 \times 16^2 + 3 \times 16^{-1} + 10 \times 16^{-2}$$

$$12 + 176 + 512 + \frac{3}{16} + \frac{10}{256}$$

$$= 700 + \frac{48+10}{256}$$

$$700 + 0.22 = 700.22$$



Conversion of Decimal to any form

(37)<sub>10</sub> to binary

2	37
2	18 - 1
2	9 - 0 ↑
2	4 - 1
2	2 - 0
1	0

Take LCM by 2 and write remainder

$$(100101)_2$$

(37)<sub>10</sub> to octal

Take LCM by 8 and write remainder

$$\begin{array}{r} 8 \mid 37 \\ 8 \quad 4 \quad 5 \\ \hline (45)_8 \end{array}$$

$(75.37)_{10}$  to binary

$$\begin{array}{r} 2 \mid 75 \\ 2 \quad 37 \quad -1 \\ 2 \quad 18 \quad -1 \\ 2 \quad 9 \quad -0 \\ 2 \quad 4 \quad -1 \\ 2 \quad 2 \quad -0 \\ \hline 1 \quad -0 \end{array}$$

$$1001011 \cdot 01011$$

(Multiply 4-5 times)

$$\begin{array}{l} 0.37 \times 2 = 0.74 \\ 0.74 \times 2 = 1.48 \quad \downarrow \text{Don't take 1 for multiplication} \\ 0.48 \times 2 = 0.96 \\ 0.96 \times 2 = 1.92 \\ 0.92 \times 2 = 1.84 \end{array}$$

$(75.37)_{10}$  to octal

$$\begin{array}{r} 8 \mid 75 \\ 8 \quad 9 \quad -3 \\ \hline 1 \quad -1 \end{array}$$

$$113$$

$$0.37 \times 8 = 2.96$$

$$0.96 \times 8 = 7.68$$

$$0.68 \times 8 = 5.44$$

$$0.44 \times 8 = 3.52$$

$$(113 \cdot 2753)_8$$

$(12)_{10}$  to octal

$$\begin{array}{r} 8 \mid 12 \\ 8 \quad 1 \quad -4 \\ \hline \end{array} \quad (14)_8$$

Convert octal no. to decimal

(1)  $(444)_8$

$$4 \times 8^0 + 4 \times 8^1 + 4 \times 8^2 = 4 + 32 + 256 = (292)_{10}$$

(2)  $(237)_8$   
 $7 \times 8^0 + 3 \times 8 + 2 \times 8^2 = 7 + 24 + 128 = (159)_{10}$

(3)  $(190)_8$   
 $0 \times 8^0 + 2 \times 8 + 1 \times 8^2 = 0 + 16 + 64 = (80)_{10}$

Q.  $(112)_{10}$  to hexadecimal

$$\begin{array}{r} 16 | 112 \\ \quad\quad\quad 7 - 0 \\ \hline \quad\quad\quad (70)_{16} \end{array}$$

$(253)_{10}$  to hexadecimal

$$\begin{array}{r} 16 | 253 \\ \quad\quad\quad 15 - 13 \\ \hline \quad\quad\quad (1513)_{16} \quad (FD)_{16} \end{array}$$

~~(4AB)H~~ Hexadecimal

4AB H to decimal

$(4AB)_{16}$

$$11 \times 16^0 + 10 \times 16 + 4 \times 16^2 = 11 + 160 + 1024 = (1195)_{10}$$

$(23F)_{16}$  to decimal

$$15 \times 16^0 + 3 \times 16 + 2 \times 16^2 = 15 + 48 + 512 = (575)_{10}$$

Convert octal to Binary

$(45)_8$   
 ✓ ↗  
 100 101

$(100101)_2$

Octal  
 $\downarrow$   
 $2^3 = 8$

Repr. in 3 bits

$$(327)_8 \quad \begin{matrix} \downarrow & \downarrow & \downarrow \\ 011 & 010 & 111 \end{matrix} \quad (011010111)_2$$

$$(011010111)_2$$

## # Hexadecimal To Binary

Hexadecimal  $\xrightarrow{16} 2^4 \rightarrow 4\text{ bits}$

$$\Rightarrow (327)_{16} \quad \begin{matrix} \downarrow & \downarrow & \rightarrow \\ 0011 & 0010 & 0111 \end{matrix} \quad (001100100111)_2$$

$\Rightarrow (276)_8$  to binary

$$(010\cancel{1}\cancel{1}\cancel{1}10)_2$$

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$\Rightarrow (2A16)_{16}$  to Binary

$$(0010\cancel{1}\cancel{0}\cancel{0}0001\cancel{0}\cancel{1}\cancel{0})_2$$

## # Convert Binary to Other forms

$\Rightarrow (110\cancel{1}\cancel{1}0\cancel{1}0\cancel{1}0\cancel{1})_2$  to hexadecimal

$$(0110\cancel{1}\cancel{1}0\cancel{1}0\cancel{1}0\cancel{1})_2$$

$$(6135)_{16} \quad (6D5)_{16}$$

$\Rightarrow (110\cancel{1}\cancel{1}0\cancel{1}0\cancel{1}0\cancel{1})_2$  to octal

$$(011\cancel{0}\cancel{1}0\cancel{1}0\cancel{1})_2 \quad (3325)_8$$

## # Convert Hexadecimal To Octal

$$(24)_{16} \quad \begin{matrix} \downarrow & \downarrow \\ 0010 & 0100 \end{matrix}$$

$$(00010\cancel{0}\cancel{1}00)_2$$

$$(044)_8$$

## # Convert Binary To Octal

Q.  $(1100.011)_2$   
 $(001\ 100.011)_2$ ,  $(14.3)_8$

Q.  $(100100.0111)_2$   
 $(100\ 100 \cdot 0111\ 100)_2$ ,  $(44.34)_8$

## # Convert binary to Hexadecimal

$(1100.0110)_2$   
 $(C.6)_{16}$

$(00100100.0111)_2$   
 $(24.7)_{16}$

Ques. 1  $(1001011)_2$  to decimal

$1 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 0 \times 2^4 + 0 \times 2^5 + 1 \times 2^6$   
 $1 + 2 + 8 + 64 = (75)_{10}$

Ques 2  $(105.15)_{10}$  to binary

$\frac{2}{105}$		
$\frac{2}{52} - 1$	$1$	$101001.$
$\frac{2}{26} - 0$		
$\frac{2}{13} - 0$		
$\frac{2}{6} - 1$		
$\frac{2}{3} - 0$		
$1 - 1$		

$0.15 \times 2 = 0.30$   
 $0.30 \times 2 = 0.60$   
 $0.60 \times 2 = 1.20$   
 $0.20 \times 2 = 0.40$   
 $0.40 \times 2 = 0.80$

$(1101001.00100)_2$

Ques 3  $(367.52)_8$  to binary  
 $(011110111.101010)_2$

Ques 4  $(10101111001.0111)_2$  to octal

$(01010111001.011100)_2$   
 $(2571.34)_8$

Ques 5  $(4057.06)_8$  to decimal

$$7 \times 8^0 + 5 \times 8^1 + 4 \times 8^2 + 6 \times 8^3 \\ 7 + 40 + 2048 + \frac{6}{64}$$

$$2095 + 0.09 = (2095.09)_{10}$$

Ques 6  $(378.93)_{10}$  to octal

8	378
8	47 -2
5	-7

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$$0.93 \times 8 = 7.44$$

$$0.44 \times 8 = 3.52$$

$$0.52 \times 8 = 4.16$$

$$0.16 \times 8 = 1.28$$

$(572.7341)_8$

Ques 7  $(010\underline{1111}011.\underline{011111})_2$  to Hexadecimal

001011111011.01111100

$(2FB.7C)_{16}$

Ques 8.  $(3A9E.B0D)_{16}$  to Binary

$(0011101010011110.101100001101)_2$

# BINARY ARITHMETIC

## (1) Addition

$$\begin{array}{r} 0 & 0 & 1 & 1 \\ + 0 & + 1 & + 0 & + 1 \\ \hline 0 & 1 & 1 & 0 \\ & & & \downarrow \\ & & & \text{carry} \end{array}$$

## (2) Subtraction

$$\begin{array}{r} 0 & 1 & 1 & 1 \\ - 0 & - 0 & - 1 & \\ \hline 0 & 0 & 0 & \end{array} \quad \begin{array}{r} 10 \\ \rightarrow 2 \\ - 1 \\ \hline 1 \end{array}$$

## (3) Multiplication

$$\begin{array}{r} 0 & 0 & 1 & 1 \\ \times 0 & \times 1 & \times 0 & \times 1 \\ \hline 0 & 0 & 0 & 0 \end{array}$$

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## (4) Division

$$\begin{array}{r} 0 & 1 & 0 & 1 \\ \div 0 & \div 0 & \div 1 & \div 1 \\ \hline \text{Not defined} & \infty & 0 & 1 \end{array}$$

Q.

$$\begin{array}{r} 1101 \\ + 1111 \\ \hline 11100 \end{array} \quad \begin{array}{r} 1101 \\ \times 1101 \\ \hline 11100 \end{array} \quad 1+1=$$

Q.

$$\begin{array}{r} 1110 \\ - 1001 \\ \hline 0101 \end{array}$$

$$\begin{array}{r}
 & 2 \curvearrowleft \\
 & \downarrow \\
 \begin{array}{r} 0 \\ 1 \\ - \\ 1 \end{array} & 0 & 0 & 0 & 0 \\
 & 0 & 0 & 1 & 1 \\
 & \hline
 & 1 & 1 & 0 & 1
 \end{array}$$

$$\begin{array}{r}
 & 2 \curvearrowleft \uparrow \\
 & \downarrow \\
 0 & (10) \\
 & 1 & 0 & 0 & 0 & 0
 \end{array}$$

$$\begin{array}{r}
 Q. \quad \text{Ans} \quad 1101 \\
 \times 1100 \\
 \hline
 0000 \\
 0000X \\
 11101 \quad XX \\
 1101 \quad X \quad XX \\
 \hline
 10011100
 \end{array}$$

$$\begin{array}{r}
 Q. \quad 11111 \\
 \times 10001 \\
 \hline
 01111 \\
 00000X \\
 00000XX \\
 11111X \\
 \hline
 100001111
 \end{array}$$

$$\begin{array}{r}
 Q. \quad 10000 \\
 \times 101 \\
 \hline
 10000 \\
 0000X \\
 1000XX \\
 \hline
 101000
 \end{array}$$

$$Q. \quad 10 \quad | \quad 110$$

$$\underline{10}$$

$$\underline{10}$$

$$\underline{10}$$

$$\underline{X}$$

$$\begin{array}{r}
 Q. \quad 110 \quad | \quad 11110 \\
 \hline
 101
 \end{array}$$

$$\underline{110}$$

$$\underline{110}$$

$$\underline{110}$$

$$\underline{X}$$

1's Complement

$$1010 \rightarrow 0101$$

2's Complement

$$1010 \rightarrow 0101$$

Add ① to on 1's complement

$$\begin{array}{r} 0101 \\ + 1 \\ \hline \end{array}$$

$$\underline{0110} \rightarrow 2's \text{ complement}$$

Subtraction Using 1's Complement

Q. 1111 - 1010

Smallest no.  $\rightarrow$  1's complement. Add it to other no  
If it has carry add it to answer.

$$1010 \rightarrow 0101$$

$$\begin{array}{r} 1111 \\ - 1010 \\ \hline 0101 \end{array} @rajat_kansal$$

$$0101$$

$$\underline{\textcircled{1}}0100$$

$$+ 1$$

$$\underline{0101} \rightarrow \text{Ans}$$

Q

1010 and 1000

$$1000 \rightarrow \cancel{00} 0111$$

$$1010$$

$$0111$$

$$\underline{0001}$$

$$+ 1$$

$$\underline{0010}$$

$$\text{Ans} \rightarrow 0010$$

## Subtraction Using 2's complement

1111

1010

Smallest no  $\rightarrow$  2's complement. Add it to other no  
if there is carry, discard it

$$1010 \rightarrow 0101 \rightarrow 0110$$

1111

$$+ \underline{0110}$$

$$\underline{\underline{0110}}$$

$$0101 \rightarrow \text{Ans}$$

## BOOLEAN ALGEBRA RULES

### 1. Complement laws :

$$\bar{0} = 1$$

$$\bar{1} = 0$$

$$\text{If } \bar{A} = 0 \text{ then } A = 1$$

### 2. AND Rules

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$$A \cdot 0 = 0$$

$$A \cdot 1 = A$$

$$A \cdot \bar{A} = 0$$

$$A \cdot A = A$$

$$\bar{A} \cdot \bar{A} = \bar{A}$$

## LOGIC GATES

Basic Gate - AND, OR, NOT

Universal Gate - NAND, NOR

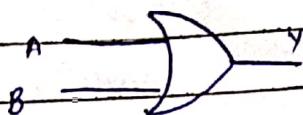
### # AND



$$Y = A \cdot B$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

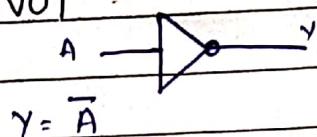
# OR



$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

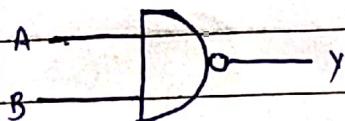
# NOT



$$Y = \bar{A}$$

A	Y
0	1
1	0

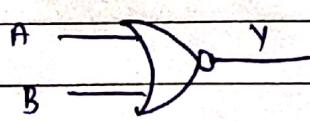
# NAND



$$Y = \bar{A} \cdot \bar{B}$$

A	B	Y
0	0	1
1	0	1
1	1	0

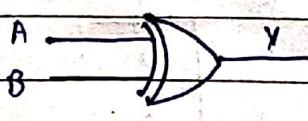
# NOR



$$Y = \bar{A} + \bar{B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

# XOR



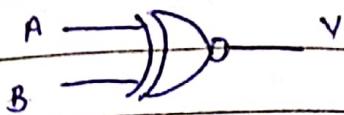
$$Y = \bar{A} \cdot B + A \cdot \bar{B}$$

$$Y_2 = A \oplus B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

eg  
 $A=0 \quad B=1$   
 $1 \times 1 + 0 \times 0 = 1$   
 $1+0 = 1$

XNOR



$$Y = \underline{A \oplus B}$$

$$Y = A \oplus B$$

$\neg A$	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

## Boolean Algebraic laws (Contd.)

### 3. OR laws

$$A + 0 = A$$

$$A + 1 = 1$$

$$A + \bar{A} = 1$$

$$A + A = A$$

### 4. Commutative laws

$$A + B = B + A$$

$$A \cdot B = B \cdot A$$

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### 5. Associative laws

$$(A + B) + C = A + (B + C)$$

$$(A \cdot B) \cdot C = A \cdot (B \cdot C)$$

### 6. Distributive law

$$A \cdot (B + C) = A \cdot B + A \cdot C$$

$$A + (B \cdot C) = (A + B)(A + C)$$

$$(A + B)(A + C) = A \cdot A + A \cdot C + B \cdot A + B \cdot C$$

$$= A + A \cdot C + B \cdot A + B \cdot C$$

$$= A(1 + C) + B(A + C)$$

$$= A + B \cdot A + B \cdot C$$

$$= A + B + BC$$

$$= A + BC$$

$$A + \bar{A}B = A + B$$

$$(A + \bar{A})(A + B)$$

$$\downarrow (A + B) = A + B$$

$$\times [AB + \bar{A}C + BC \cdot 1]$$

$$(AB + (\bar{A} + B)C)$$

$$AB + \bar{A}C + BC \cancel{(A + \bar{A})}$$

$$AB + (\bar{A}C + ABC)(\bar{A}C + \bar{A}BC)$$

$$AB + C(\bar{A} + AB)(\bar{A}C(1 + B))$$

$$AB + C(\bar{A} + AB)(\bar{A}BC)$$

$$AB + \bar{A}C + ABC + \bar{A}BC$$

$$AB + \bar{A}CB + ABC$$

$$AB + BC(\bar{A} + A)$$

X

Q.

$$AB + \bar{A}C + BC = AB + \bar{A}C$$

$$AB + \bar{A}C + BC \cdot 1$$

$$AB + \bar{A}C + BC(A + \bar{A})$$

$$\underline{AB} + \bar{A}C + \underline{BAC} + BC\bar{A}$$

$$ABC(1 + C) + \bar{A}C(1 + B)$$

$$ABC + \bar{A}C$$

De Morgan's Theorem

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

$$\overline{A + B} = \bar{A} \cdot \bar{B}$$

$$\times A[B + \bar{C} [\overline{AB + A\bar{C}}]]$$

$$A[B + \bar{C} [\bar{A}\bar{B} + \bar{A}C]]$$

$$A[B + \bar{A}\bar{B}\bar{C} + \bar{A} \cdot 0]$$

$$A[B + \bar{A}\bar{B}\bar{C}]$$

$$AB + 0 = AB$$

Q.  $A [B + \bar{C} [AB + \bar{A}\bar{C}]]$

$A [B + \bar{C} [\bar{A}B - \bar{A}\bar{C}]]$

$A [B + \bar{C} [(\bar{A} + \bar{B}) \cdot (\bar{A} + C)]]$

$A (B + \bar{C} (\bar{A}\bar{A} + \bar{A}C + \bar{B}\bar{A} + \bar{B} \cdot C))$

$A (B + \bar{C} (\bar{A} + \bar{A}C + \bar{B}\bar{A} + \bar{B}C))$

$A (B + \bar{A}\bar{C} + 0 + \bar{A}\bar{B} + \bar{C} + 0)$

$AB + 0 + 0 + 0 = AB$

Q.  $[A + \bar{B}\bar{C}] \cdot [A\bar{B} + ABC]$

$[\bar{A} \cdot \bar{\bar{B}}\bar{C}] \cdot [A (\bar{B} + BC)]$

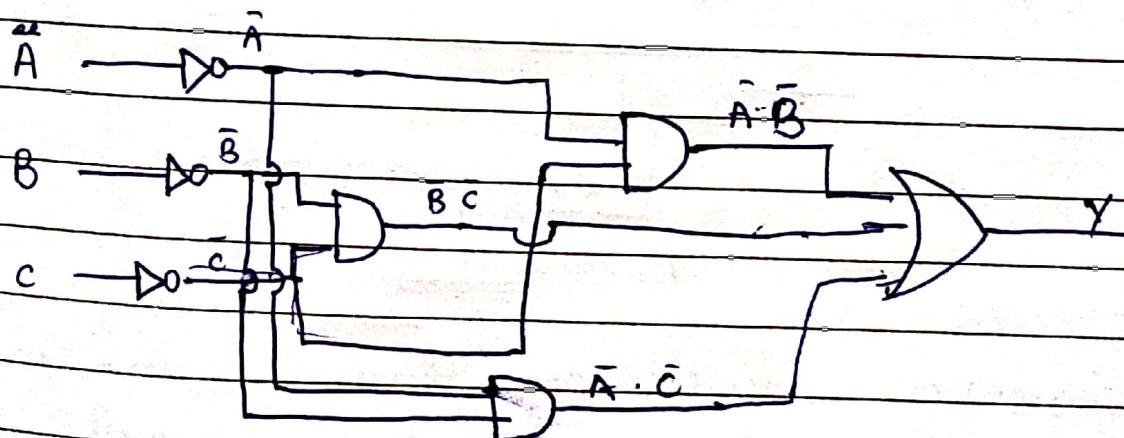
$[\bar{A} \cdot BC] \cdot [A\bar{B} + ABC]$

$\underbrace{\bar{A}A\bar{B}BC}_{0} + \underbrace{\bar{A}ABCBC}_{0} = 0$

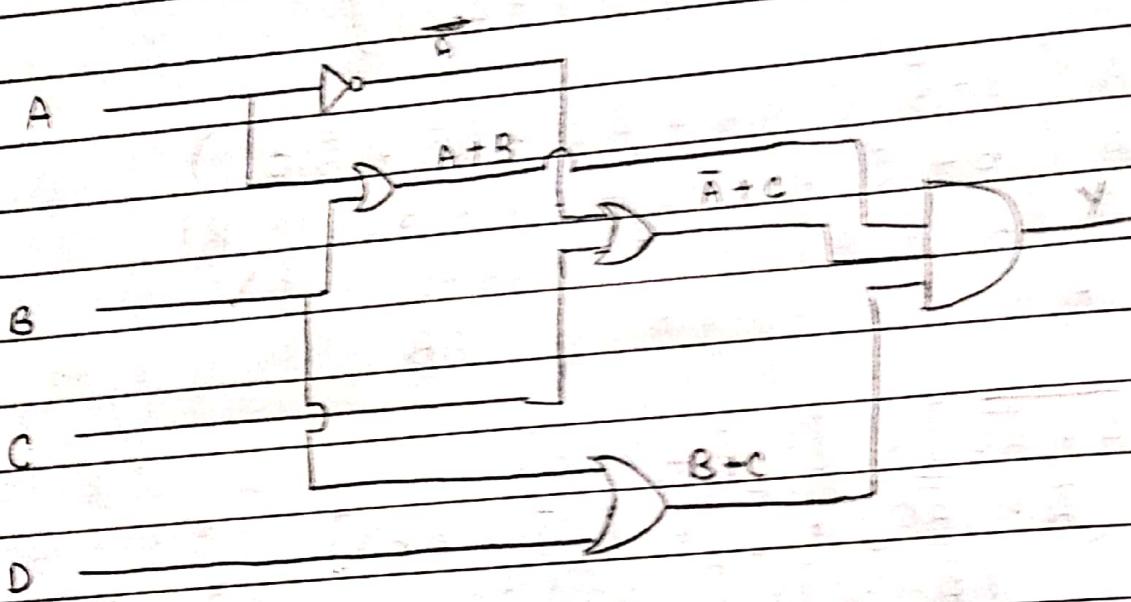
Rita

## RULIZATION OF LOGIC GATES

$$Y = \bar{B}\bar{C} + \bar{A}\bar{C} + \bar{A}\bar{B}$$



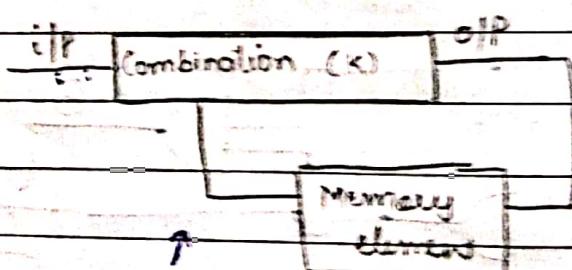
$$Y = (A+B)(\bar{A}+C)(B+D)$$



## INTRODUCTION TO COMBINATION AND SEQUENTIAL LOGIC

if Combination  
(K) @ajat\_kansal

Combinational circuits are those circuit in which output depends only on present input. No memory element is required in this circuit. eg - logic gates



Sequential circuits are those circuits in which output depends on present as well as past input. Memory element is required to store past input. eg - flipflops, counters, shift registers.

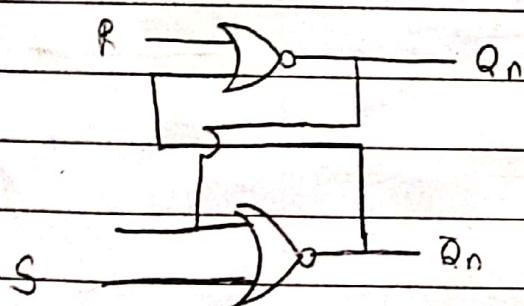
d latch and flip flop.

d latch is an unlock flip flop in which clock is absent.

Flip flop is a clocked device in which output can change its state only ~~at~~ after either +ve or -ve. It can store 1 bit of data so it is also called as 1-bit memory cell.

### RS FLIPFLOP

S	R	Q <sub>n</sub>	$\bar{Q}_n$	Q <sub>n+1</sub>	$\bar{Q}_{n+1}$	Clocked
0	0	0	1			No change
0	1	0	1	0	1	
1	0	0	1	1	0	
1	1	0	1	0	0	(C Invalid)



### IC555 TIMER

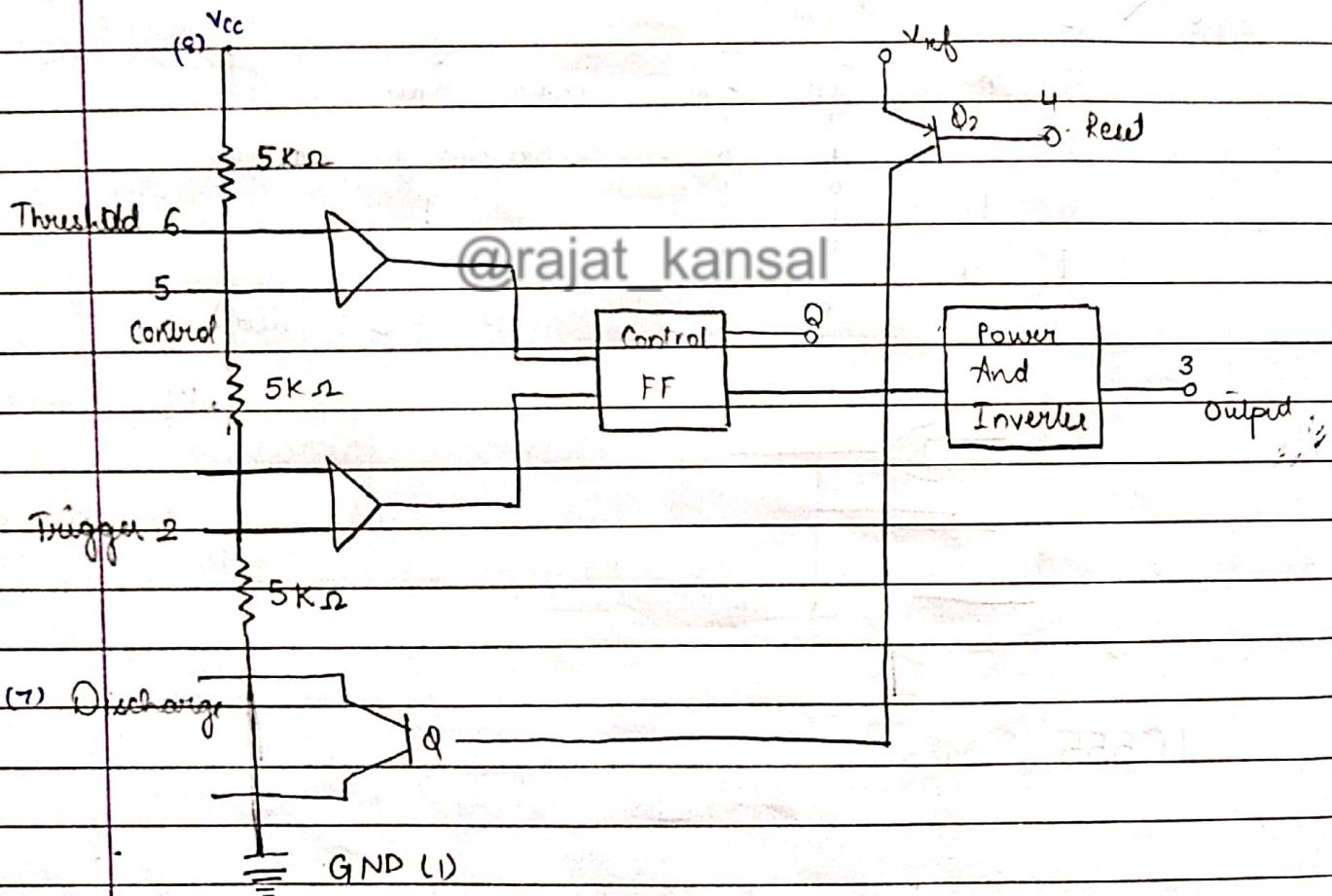
GND	1	8	V <sub>cc</sub>
Trigger	2	7	Discharge
Output	3	555	Threshold
Reset	4	5	Control Voltage

### Application :

Square wave generator, safety alarm, train circuits, traffic lights controller, pulse generator.

⇒ 555 timer operates at dc supply voltage ranging from +5V to +18V. It provides time delay ranging from μs to hours.

### FUNCTIONAL BLOCK DIAG OF IC555



+ve DC power supply is connected to 8 pin, -ve is connected to 1 pin. ~~3.5~~ There 5 kΩ resistors provide potential divider arrangement. It provides volt of  $\frac{2}{3} V_{cc}$  to -ve terminal of upper comparaula and  $\frac{1}{3} V_{cc}$  to +ve terminal of lower

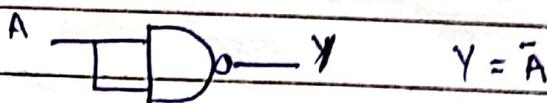
comparator. The +ve input terminal of upper comparator is called threshold terminal. The -ve input terminal of lower comparator is called trigger terminal.

## Designing of Gates using NAND and NOR

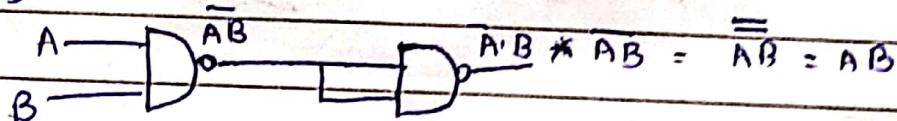
	NAND	NOR
NOT	1	1
AND	2	3
OR	3	2
XOR	4	5
XNOR	5	4

### Using NAND

# NOT



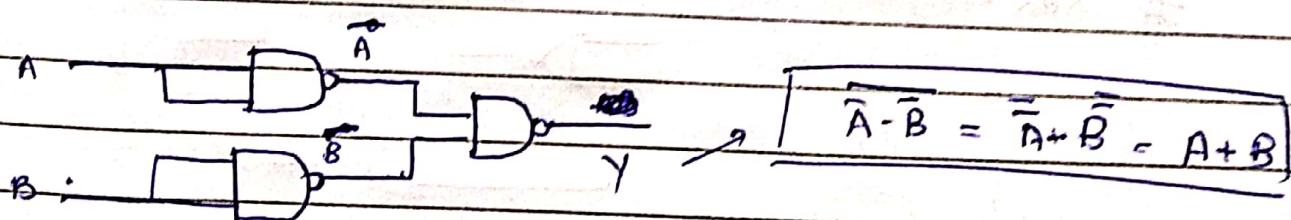
# AND



$$\text{@rajat\_kansal}$$

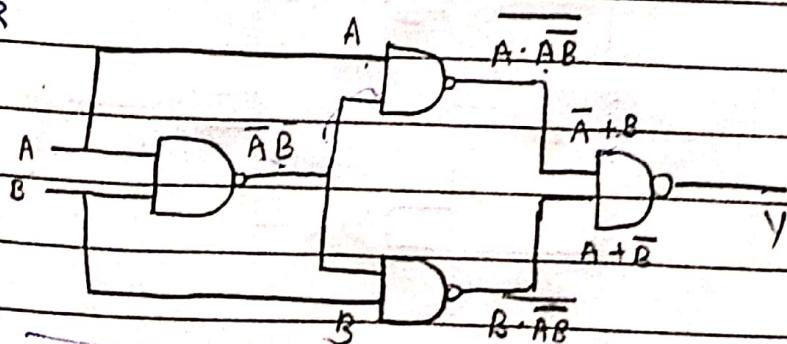
$$A \cdot B \Leftrightarrow \bar{A} \bar{B} = \bar{\bar{A}} \bar{\bar{B}} = AB$$

# OR



$$\bar{A} - \bar{B} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$$

# XOR

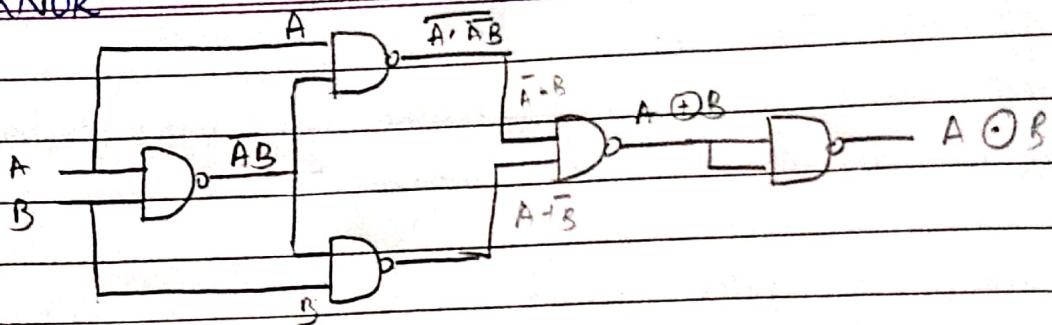


$$\overline{A \bar{B} + \bar{A} B}$$

$$\overline{A \cdot \bar{B}} \cdot \overline{\bar{A} \cdot B}$$

$$(\bar{A} \cdot B) \cdot (\bar{A} + \bar{B})$$

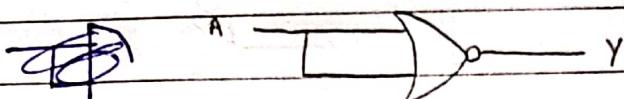
# XNOR



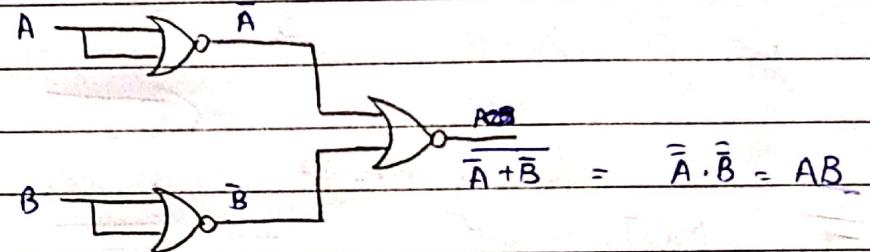
Using NOR

# NOT

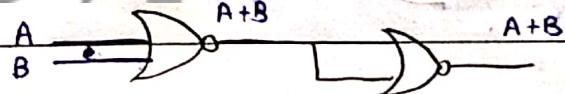
$$Y = \bar{A}$$



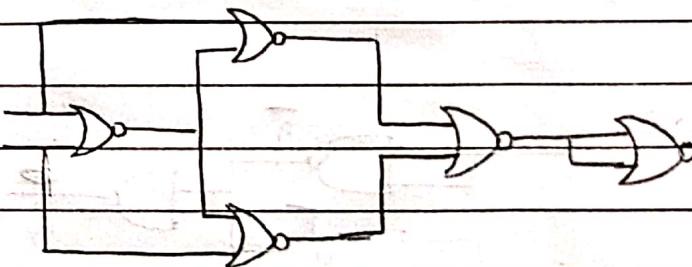
# AND



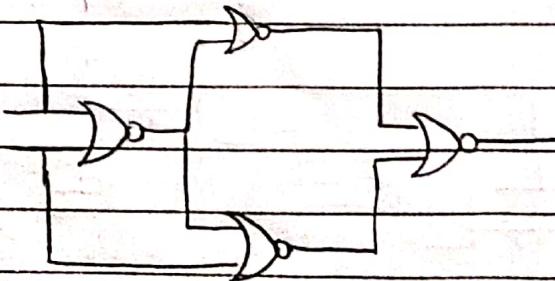
# OR



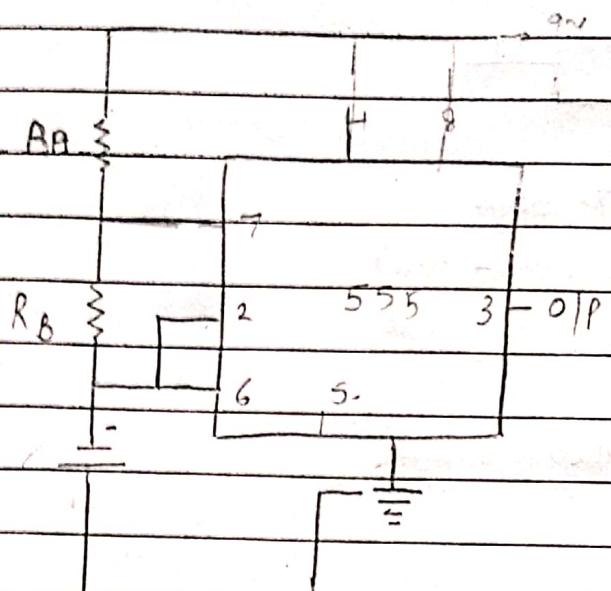
# XOR



# XNOR



# PIN DIAG OF 555



subtract

1000 and 1010

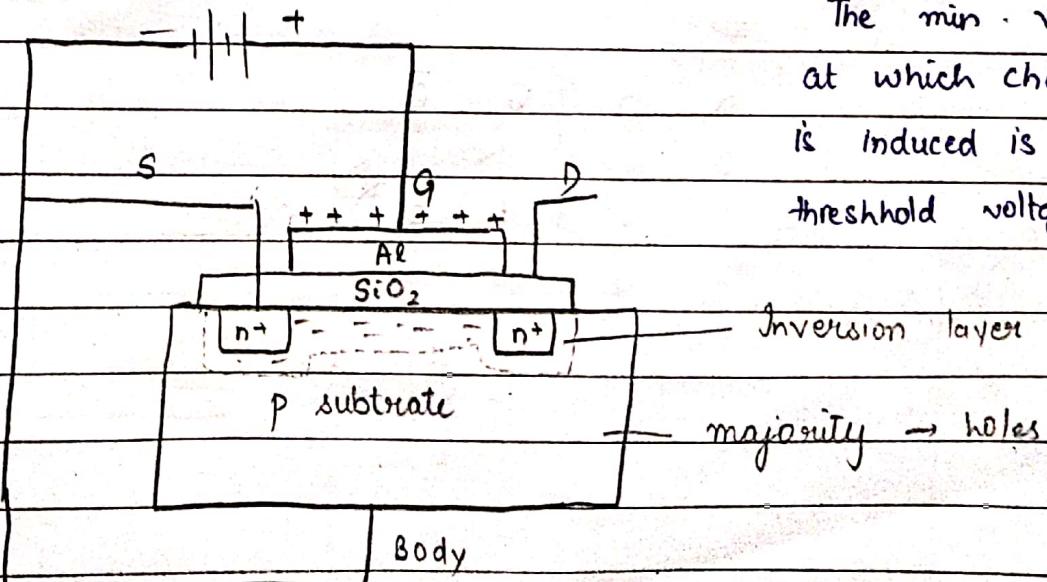
1's comp      ~~011~~ 011

Sub : 1010

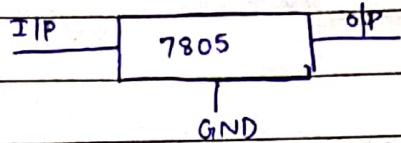
011  
①0001  
+  
0000

$$\begin{array}{r} 011 \\ \underline{+} \\ 1000 \\ + \\ 0000 \end{array}$$

Enhancement MOSFET



## VOLTAGE REGULATOR (7805)

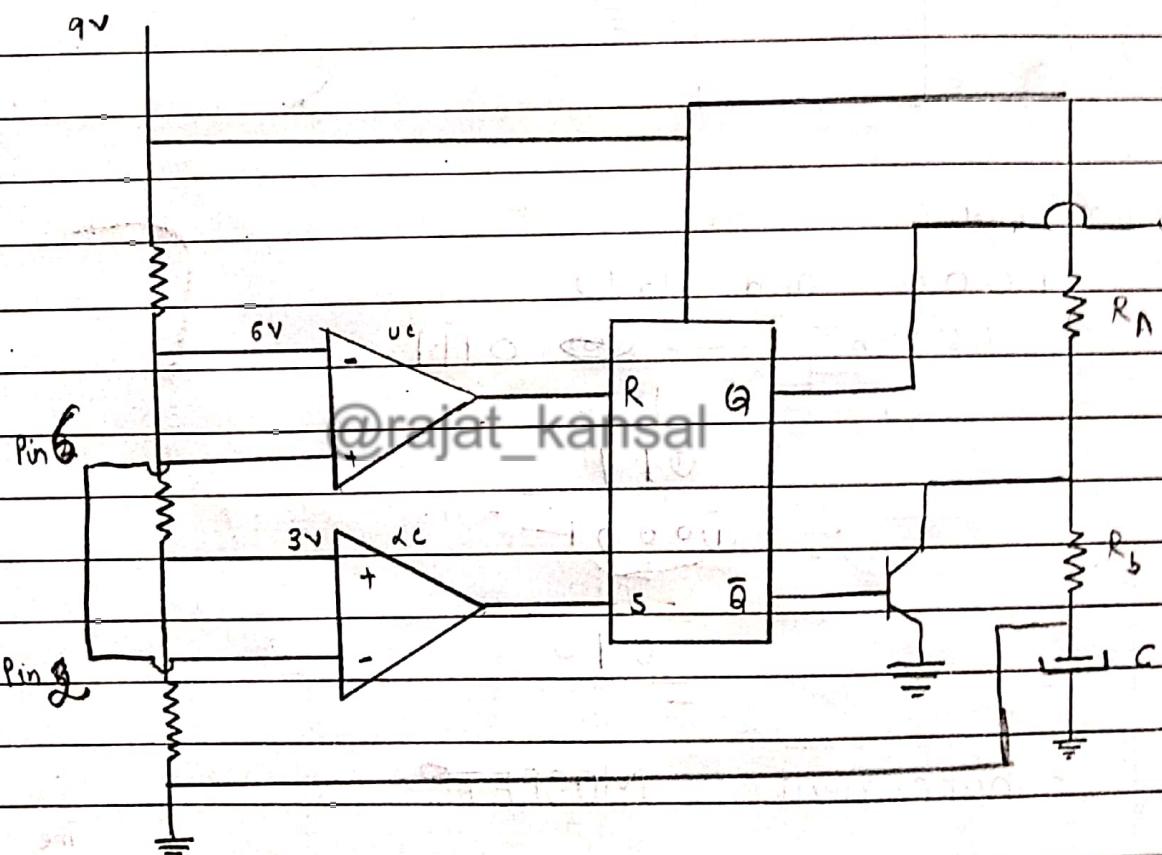


Input voltage -  $7 - 35V$

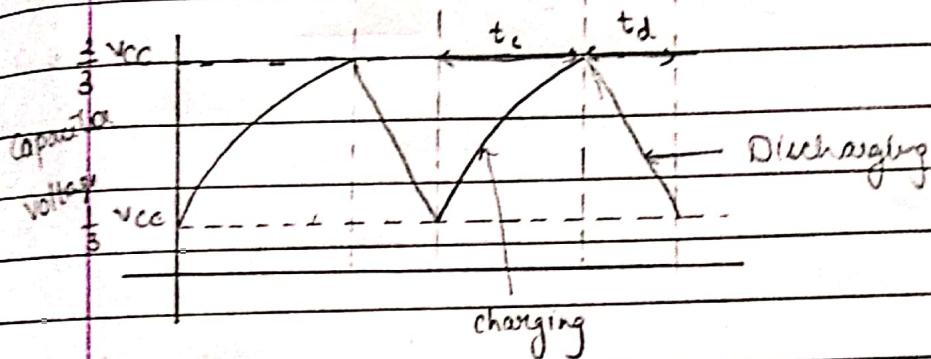
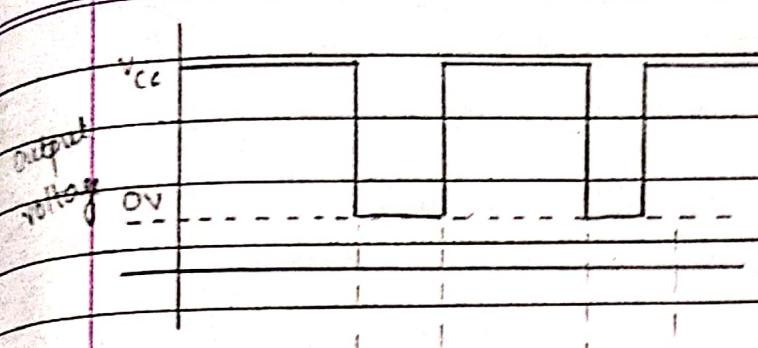
Output voltage - 5 ( $4.8 - 5.2$ )

lost energy in form of heat

555 as Astable Multivibrator



	R	S	Q	$\bar{Q}$
Initial state	0	0	No change	
Setting S=1	0	1	1	0
Setting R=1	1	0	0	1
Setting both R & S = 1	1	1	Illegal	



Charging - time of capacitor  $t_c = 0.693 (R_A + R_B) C$

Discharging - time  $t_d = 0.693 R_B C$

Given  $R_A = 2.2 \text{ k}\Omega$   $R_B = 3.9 \text{ k}\Omega$   $C = 0.1 \mu\text{F}$   $t_c = ?$   $t_d = ?$

$$t_c = 0.693 \times (2.2 + 3.9) \times 10^3 \times 0.1 \times 10^{-6}$$

$$= 0.472273 \times 10^{-3}$$

$$= 4.72273 \times 10^{-4}$$

$$t_d = 0.693 \times 3.9 \times 0.1 \times 10^{-3}$$

$$= 0.27027 \times 10^{-3}$$

$$= 2.7 \times 10^{-4} \text{ s}$$