# Timing and Control

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- The timing for all registers in the basic computer is controlled by a master clock generator.

- The clock pulses are applied to all flip-flops and registers in the system, including the flip-flops and registers in the control unit.

- The clock pulses do not change the state of a register unless the register is enabled by a control signal.

- The control signals are generated in the control unit and provide control inputs for the multiplexers in the common bus, control inputs in processor registers, and microoperations for the accumulator

- There are two major types of control organization:
1. Hardwired Control
2. Microprogrammed Control

Hardwired Control

- In the hardwired organization, the control logic is implemented with gates, flip-flops, decoders, and other digital circuits. It has the advantage that it can be optimized to produce a fast mode of operation. A hardwired control, as the name implies, requires changes in the wiring among the various components if the design has to be modified or changed.

Microprogrammed control

- In the microprogrammed control, any required changes or modifications can be done by updating the microprogram in control memory. . In the microprogrammed organization, the control information is stored in a control memory. The control memory is programmed to initiate the required sequence of microoperations.

Control Unit of a basic computer
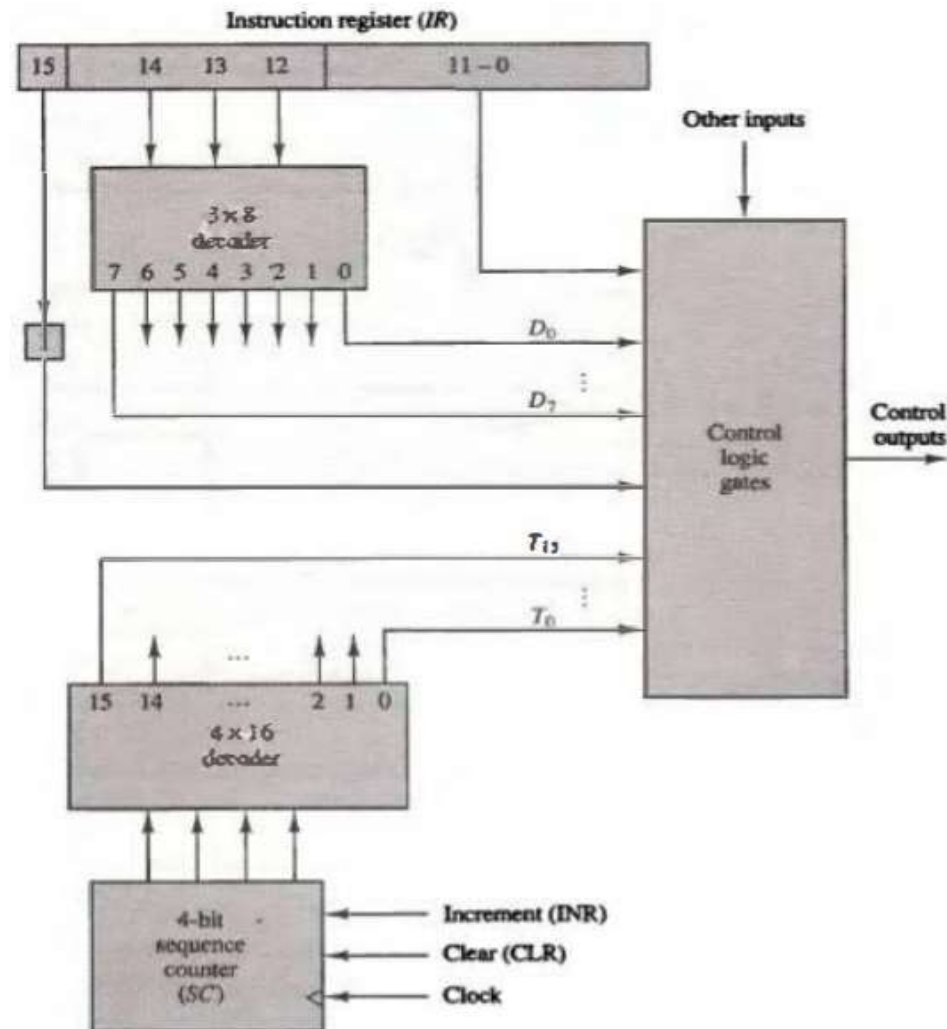
Control Unit of a basic computer

- It consists of two decoders, a sequence counter, and a number of control logic gates. An instruction read from memory is placed in the instruction register (IR) where it is divided into three parts: the I bit, the operation code, and bits 0 through 11.

- The operation code in bits 12 through 14 are decoded with a 3 x 8 decoder. The eight outputs of the decoder are designated by the symbols D0 through D7•

- The subscripted decimal number is equivalent to the binary value of the corresponding operation code. Bit 15 of the instruction is transferred to a flip-flop designated by the symbol I. Bits 0 through 11 are applied to the control logic gates.

- The 4-bit sequence counter can count in binary from 0 through 15. The outputs of the counter are decoded into 16 timing signals T0 through T15•

- The sequence counter SC can be incremented or cleared synchronously. Most of the time, the counter is incremented to provide the sequence of timing signals out of the 4 x 16 decoder. Once in awhile, the counter is cleared to 0, causing the next active timing signal to be To. As an example, consider the case where SC is incremented to provide timing signals T0, T1 T2, T3, and T4 in sequence.

- As an example, consider the case where SC is incremented to provide timing signals T0, Tv T2, T3, and T4 in sequence. At time T4, SC is cleared to 0 if decoder output D3 is active. This is expressed symbolically by the statement D3T4: SC <- 0