



Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
- Computational Fluid Dynamics

PCB Design and Analysis Learning Map

Beginner

Advanced



Beginner

Advanced

IC Package Design and Analysis Learning Map

Beginner



Advanced

IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language



Allegro Package Designer Plus **NEW**



SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



TopXplorer SystemSI for Parallel Bus and Serial Link Analysis



Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM



Clarity 3D Solver **NEW**



Celsius Thermal Solver



Beginner



Advanced

NEW

New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available



Digital Badge Available

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Circuit Modeling, Analog/Mixed-Signal/RF Circuit Design and Simulation

Mixed-Signal Simulation

Mixed-Signal Simulations using Spectre AMS Designer



Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model **NEW**



SimVision for Debugging Mixed-Signal Simulations



AMS/Real Number Modeling

Analog Modeling with Verilog-A



Behavioral Modeling with Verilog AMS



Real Modeling with Verilog-AMS



Real Modeling with SystemVerilog



SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification **NEW**



Virtuoso Schematic Editor



Virtuoso Visualization and Analysis



Virtuoso® ADE Explorer & Assembler Series

S1 ADE Explorer & Single Test Corner Analysis



S2 ADE Assembler & Multi Test Corner Analysis



S3 Sweeping Variables and Simulating Corners



S4 Monte Carlo, Real-Time Tuning & Run Plans



Virtuoso® ADE Verifier Series

S1 Setup, Run, & View Verifier Results



S2 Reference Flow and Analog Coverage Using the Setup Library Assistant



Microwave & RF Design (AWR®)

Microwave Office for RF Designers



5G mmWave Handset System Design – S1 RFIC (Transceiver) Design



Spectre® Simulator Fundamentals Series

S1 Spectre Basics



S2 Large-Signal Analysis



S3 Small-Signal Analysis



S4 Spectre MDL



Design Checks and Asserts



High Performance Spectre Simulation (APS, Spectre X)



Spectre FX Simulator **NEW**



Virtuoso® Spectre® Pro Series

S1 DC Algorithm



S2 Transient Algorithm



Spectre® RF Series

Spectre RF Shooting Newton **NEW**



Spectre RF Harmonic Balance **NEW**

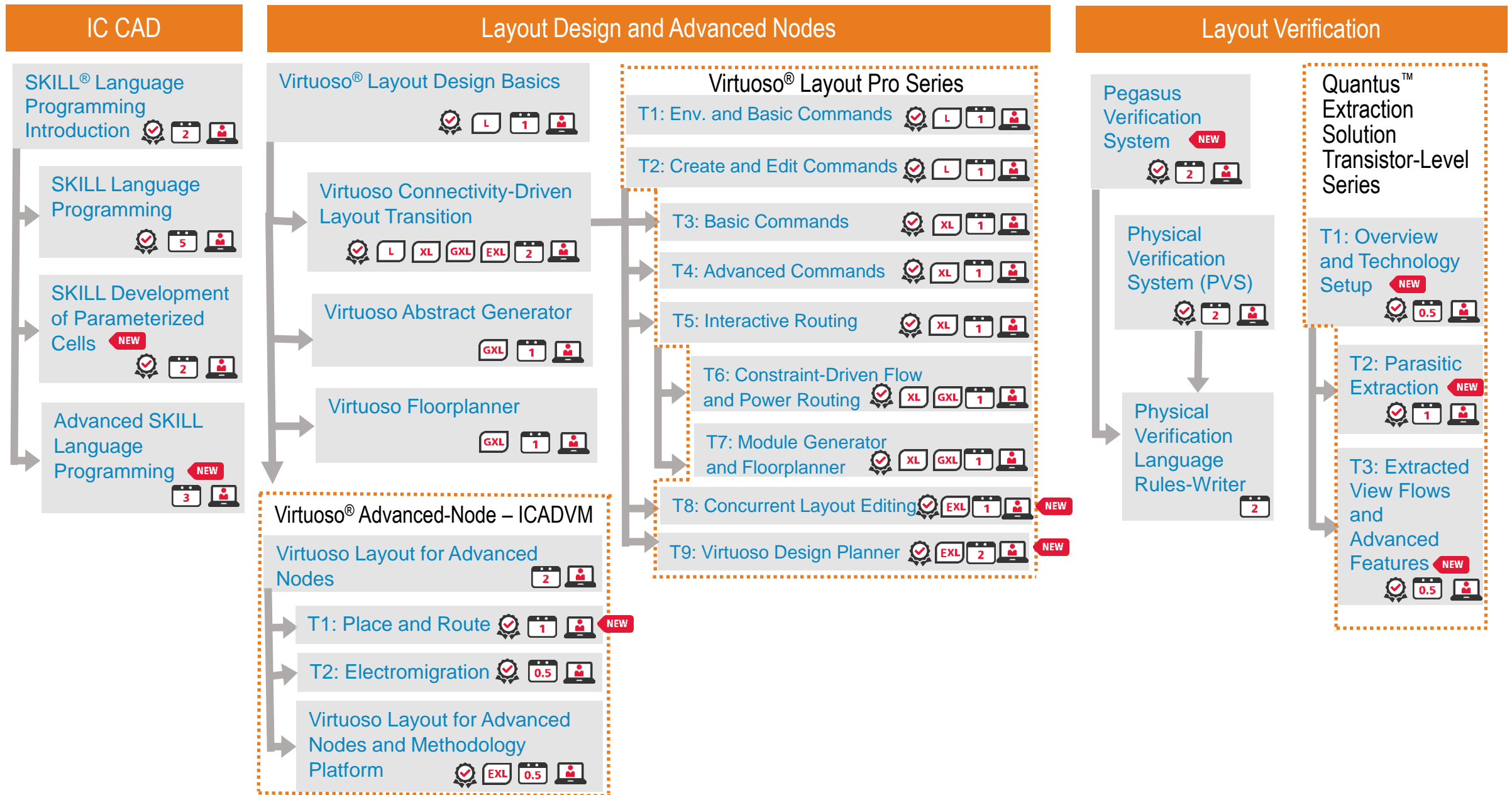


Beginner

Advanced

Beginner

Advanced



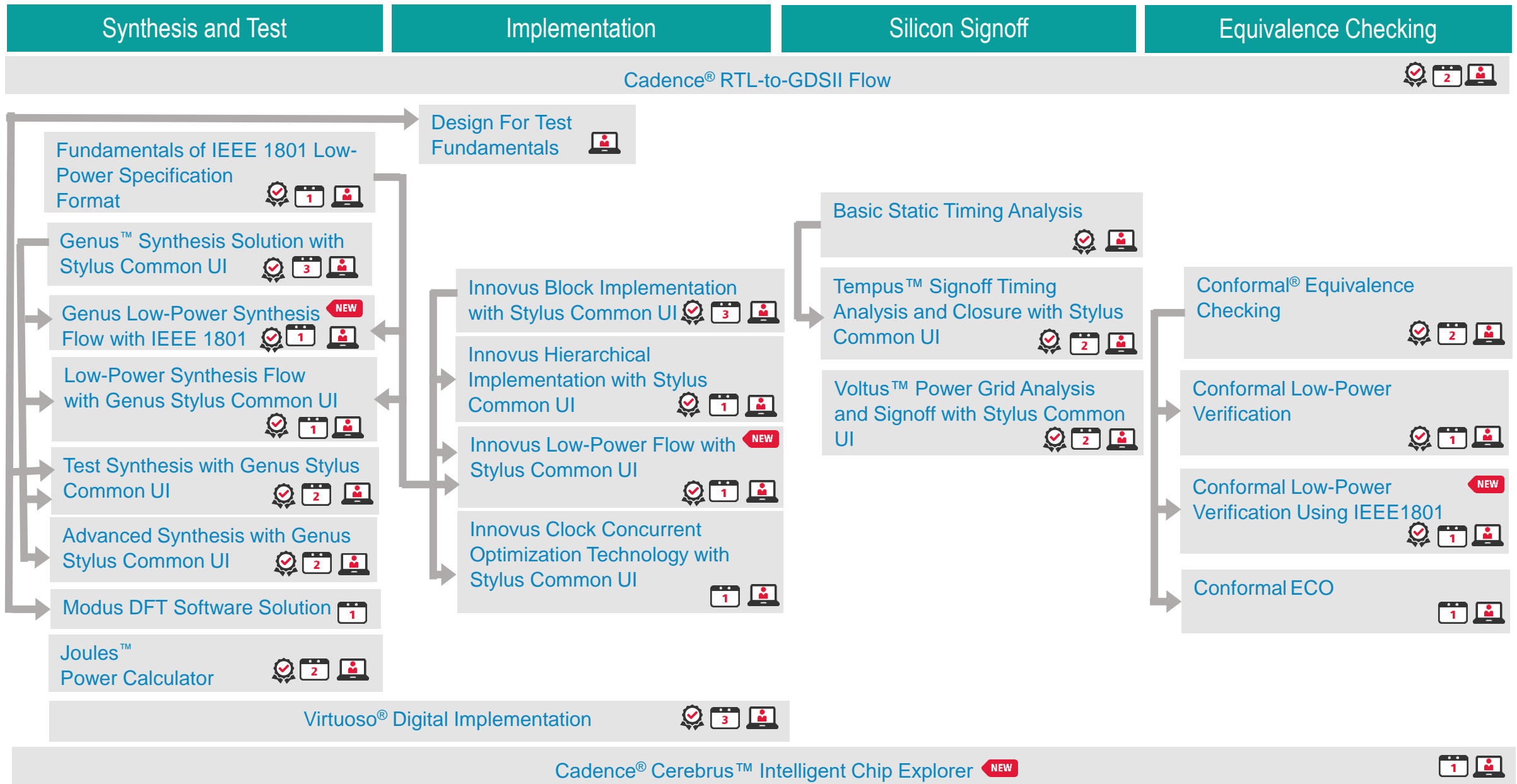
Digital Design and Signoff Learning Map

Beginner

Advanced

Beginner

Advanced

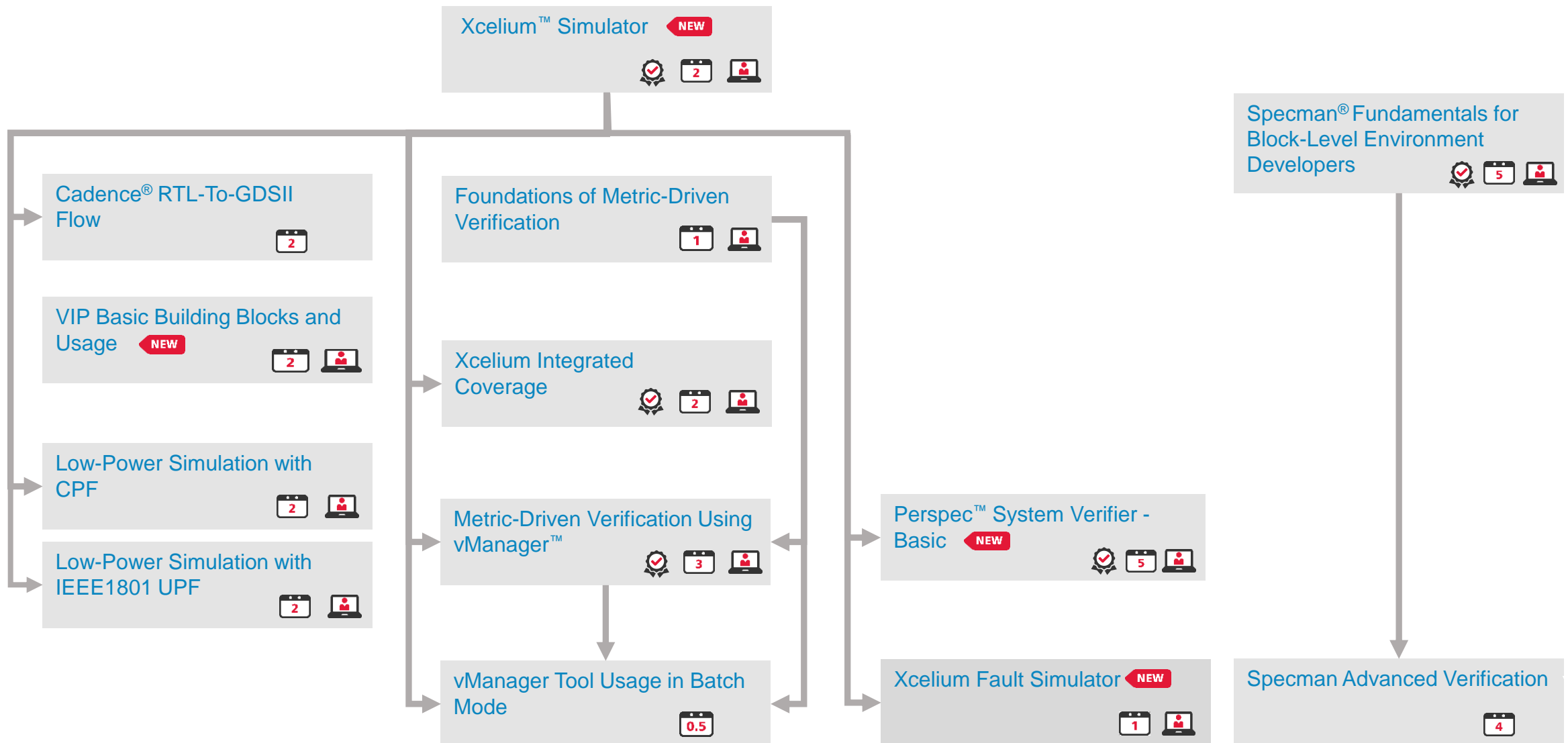


System Design and Verification Learning Map

Beginner

Advanced

Simulation, Coverage and Debug



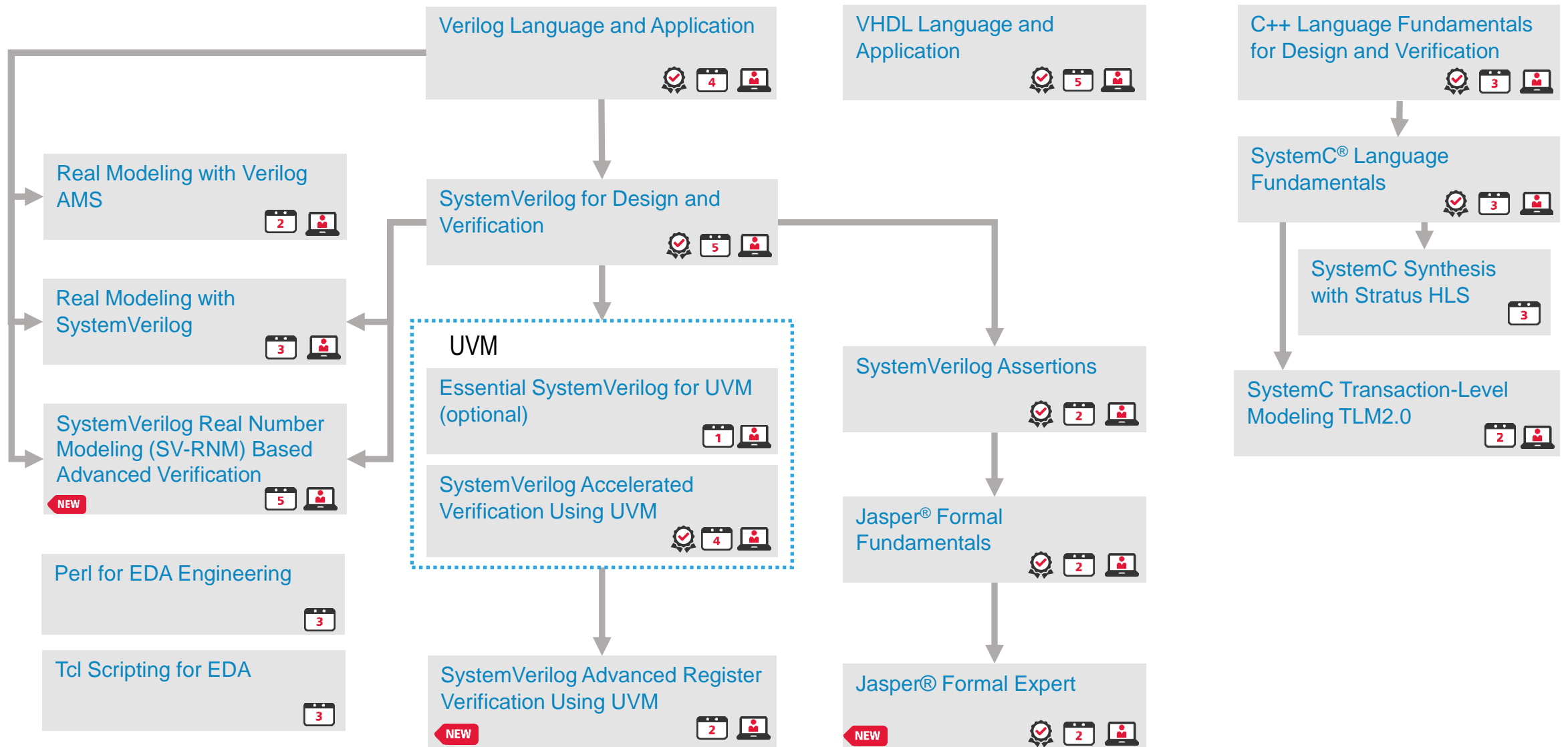
Beginner

Advanced

System Design and Verification Learning Map

Beginner

Design and Verification Languages



Beginner

Advanced

Tensilica Processor IP Learning Map

1 of 2 – see next page



Tensilica Xtensa LX

[Tensilica® Xtensa® LX Processor Fundamentals](#)



ConnX DSP

[Tensilica ConnX BBE16EP Baseband Engine](#)



[Tensilica ConnX BBE32EP Baseband Engine](#)



[Tensilica ConnX BBE64EP Baseband Engine](#)



[Tensilica ConnX 110 and 120 DSP Family](#)



Fusion & FloatingPoint DSP

[Tensilica Fusion F1 DSP](#)



[Tensilica Fusion G3 DSP](#)



[Tensilica Fusion G6 DSP](#)



[Tensilica FloatingPoint DSP Family](#)



HiFi Audio DSP

[Tensilica Audio Codec API](#)



[Tensilica HiFi 2/EP/Mini Audio Engine ISA](#)



[Tensilica HiFi 3 Audio Engine ISA](#)



[Tensilica HiFi 4 DSP](#)



[Tensilica HiFi 5 DSP](#)



[Tensilica Xtensa Audio Framework](#)



Vision DSP

[Tensilica Vision DSP Family](#)



[Tensilica Xtensa Neural Network Compiler v2](#)



[Tensilica DNA 100 Architecture and Programming](#)



New Course



Number of days for instructor-led course



Online Course Available

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Tensilica Xtensa NX

[Tensilica® Xtensa® NX Processor Fundamentals](#)



ConnX DSP

[Tensilica ConnX B10 DSP](#)

NEW



[Tensilica ConnX B20 DSP](#)

NEW



Vision DSP

[Tensilica Vision DSP Family](#)

NEW



[Tensilica Xtensa Neural Network Compiler v2](#)

NEW



[Tensilica Xtensa NX Processor Interfaces](#)



[Tensilica Xtensa NX Hardware Verification and EDA](#)



[Tensilica Instruction Extension Language and Design](#)



[Tensilica System Modeling using XTSC](#)



Computational Fluid Dynamics

Beginner

Advanced

Fidelity		
Turbomachinery	Meshing	Auto Aero

Fine
Marine

Fidelity Turbo: Introduction

3

Fidelity Automesh for
Unstructured Meshing

1.5

Fidelity Flow

1.5

Fine Marine for Beginners

2.5

Fine Marine for Advanced Users

1.75

Beginner

Advanced

NEW

New Course



Number of days for instructor-led course

L

XL

GXL

Tiers of Cadence products used in course



Online Course Available

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