

Assignment - 2
Logic Effort
EE 671 - VLSI Design



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Date of Sub: 11th Sep, 2023

The method of logical effort uses a template inverter as the reference. While using the method, we express –

- all times in units of τ , which is the delay of a template inverter driving an identical inverter, excluding the parasitic delays.
- all capacitances in units of the input capacitance of this inverter
- all transistor widths in units of the width of the n channel transistor in the template inverter.

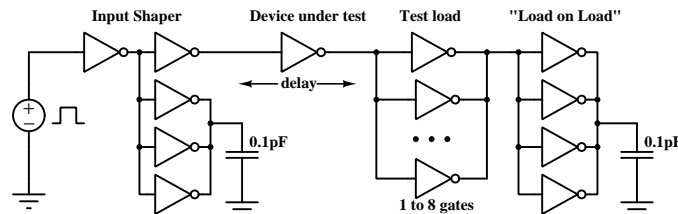
We'll use the inverter designed by you in assignment-1 as the template inverter. We want to measure τ and the parasitic delay p_{inv} for this inverter. To do this, we plot the delay of the inverter when it is loaded with 1, 2, 3 \dots 8 template inverters in parallel. We fit a straight line to the delay data vs the number of load inverters and from the slope and intercept of this line, determine τ and p_{inv}

We define the delay of a logic stage as the time interval between the midpoint of input and output transitions. In practice, this delay is not independent of the rise/fall time of the input. In this simulation, we'll try to use realistic conditions for input wave shapes and output loading.

If we use a voltage source as the input signal, it has zero output impedance and does not represent realistic inputs in a VLSI circuit. Therefore, we buffer a voltage source using loaded inverters and then use the output of the buffer as the input signal.

The delay of the device under test is not independent of the load placed on the inverter(s) being used as the load. (This is because of the coupling through C_{dg} of the transistors of the load inverter and miller effect). Therefore, we should put a realistic load on the inverter(s) being used as the load on the device under test. It is common to use a fan out of 4 in logic design. (Some justification for this will come after we have learnt optimization using logical effort).

Given these considerations, we use the following circuit for evaluation of τ and p_{inv} . It uses only inverters, so it will be convenient if you define your template inverter as a sub-circuit. Then you can instantiate it at multiple places easily.



The circuit has four parts.

1. **Input shaper:** The delay of a logic gate is influenced by the rise and fall times of the input. We would like to apply inputs which have the kinds of rise and fall times typically encountered in actual circuits, rather than the steep pulses provided by ideal voltage sources. Therefore we drive the device under test with pulses passed through a two stage inverter buffer. The first stage is a single template inverter, driving four template inverters which form the second stage. One of the four inverters in the second stage drives the device under test. The other 3 inverters present an additional dummy load to the first stage inverter. These 3 inverters drive a common load of 0.1pF.
2. **Device under test:** This is the template inverter whose delay parameters are being evaluated.
3. **Test load:** The logic gate being tested (an inverter here) will be loaded with 1 to 8 logic gates (identical to it) in parallel, to evaluate the delay as a function of the fan-out. The fanout (b) will be varied from 1 to 8.
4. **Load on Load:** The logic gates acting as load should themselves see a realistic capacitive load. Otherwise their outputs will rise too quickly, putting an unrealistic Miller capacitor load on the device under test. In this problem, we use 4 inverters in parallel driving a final output capacitance of 0.1pf as the load on load.

The delay of the logic gate under test will be measured from 50% of input transition to 50% of the output transition. We shall use the average of delays measured with the input rising and falling as the gate delay. Use the parameterized pulse generator statement suggested in assignment 2.

```
* pulse with time period of Trep, rise and fall times = Trep/20
.param Trep= 5n
.param Trf = {Trep/20.0}
.param Tw = {Trep/2.0 - Trf}
.param hival=1.8
.param loval=0.0
Vpulse pgen 0 DC 0 PULSE({loval} {hival} {Tw} {Trf} {Trf} {Tw} {Trep})
.tran 1pS {3*Trep} 0nS
```

The delays can be measured using meas constructs in the post-processing part of simulation.

```
meas tran invdelay1 TRIG v(dutin) VAL=0.9 RISE=2 TARG v(dutout) VAL=1.65 FALL=2
```

This measures the time between the instants when the voltage at dutin reaches $V_{DD}/2 = 0.9V$ during the second rising transient and when the voltage at dutout reaches $V_{DD}/2 = 0.9V$ during the second falling transient. Similar constructs can be used for evaluating the delay for a falling input.

Simulate the circuit above with different number of inverters (from 1 to 8) as load on the inverter under test. Make sure you give a short enough time step in your .tran statement ($\leq 1ps$) so that you can evaluate delays of the order of tens of ps accurately. (Don't be alarmed if your rise and fall times do not match very closely in this simulation).

As mentioned earlier, the delay here is the average of delays observed for input falling/output rising and input rising /output falling. Plot the delay of the inverter-under-test versus fan-out, fit a straight line to this data and Find the slope and intercept of this line. Using the

slope and intercept, find the values for τ and p_{inv} . Also, report the value of γ , the ratio of the width of p and n channel transistors required to give equal rise and fall times. (This was done in assignment-1).

Use a supply voltage of 1.8V and use the same model file as was used for all the previous assignments.

Model Files

```
.MODEL CMOSN NMOS LEVEL=8 VERSION=3.3.0
+TNOM      = 27          TOX      = 4.1E-9
+XJ        = 1E-7        NCH      = 2.3549E17      VTH0     = 0.3662473
+K1        = 0.5864999    K2      = 1.127266E-3      K3       = 1E-3
+K3B       = 0.0294061    W0      = 1E-7          NLX      = 1.630684E-7
+DVTOW     = 0           DVT1W   = 0           DVT2W    = 0
+DVT0      = 1.2064649    DVT1   = 0.4215486      DVT2     = 0.0197749
+U0        = 273.8094484  UA      = -1.40499E-9    UB       = 2.408323E-18
+UC        = 6.504826E-11 VSAT    = 1.355009E5     A0       = 2
+AGS       = 0.4449958    B0      = 1.901075E-7    B1       = 4.99995E-6
+KETA      = -0.0164863   A1      = 3.868769E-4    A2       = 0.4640272
+RDSW      = 123.3376355  PRWG    = 0.5           PRWB     = -0.197728
+WR        = 1           WINT    = 0           LINT     = 1.690044E-8
**+XL      = 0           XW      = -1E-8
+DWG       = -4.728719E-9 DWB     = -2.452411E-9   VOFF     = -0.0948017
+NFACTOR    = 2.1860065   CIT     = 0           CDSC     = 2.4E-4
+CDSCD     = 0           CDSCB   = 0           ETA0     = 2.230928E-3
+ETAB      = 6.028975E-5  DSUB    = 0.0145467    PCLM     = 1.3822069
+PDIBLC1   = 0.1762787   PDIBLC2 = 1.66653E-3     PDIBLCB  = -0.1
+DROUT     = 0.7694691   PSCBE1  = 8.91287E9     PSCBE2   = 7.349607E-9
+PVAG      = 1.685917E-3 DELTA    = 0.01         MOBMOD    = 1
**+RSH     = 6.7
+PRT       = 0           UTE     = -1.5         KT1      = -0.11
+KT1L      = 0           KT2     = 0.022        UA1      = 4.31E-9
+UB1       = -7.61E-18   UC1     = -5.6E-11     AT       = 3.3E4
+WL        = 0           WLN     = 1           WW       = 0
+WWN       = 1           WWL     = 0           LL       = 0
+LLN       = 1           LW       = 0           LWN      = 1
+LWL       = 0           CAPMOD  = 2
**+XPART    = 0.5
+CGD0      = 8.23E-10     CGS0     = 8.23E-10     CGB0     = 1E-12
+CJ        = 9.466429E-4  PB       = 0.8         MJ       = 0.3820266
+CJSW      = 2.608154E-10 PBSW      = 0.8         MJSW     = 0.102322
+CJSWG     = 3.3E-10     PBSWG    = 0.8         MJSWG    = 0.102322
+CF        = 0           PVTH0    = -2.199373E-3 PRDSW    = -0.9368961
+PK2       = 1.593254E-3 WKETA    = -2.880976E-3 LKETA    = 7.165078E-3
+PU0       = 6.777519    PUA      = 5.505418E-12 PUB       = 8.84133E-25
+PVSAT     = 2.006286E3  PETA0    = 1.003159E-4 PKETA    = -6.759277E-3
+NOIMOD=2.0E+00 NOIA=1.3182567385564E+19
+NOIB=144543.977074592 NOIC=-1.24515784572817E-12 EF=0.92 EM=41000000
*
```

```

*
* flicker noise parameters above added manually from some other process
*
.MODEL CMOSP PMOS LEVEL=8 VERSION=3.3.0
+TNOM      = 27              TOX      = 4.1E-9
+XJ        = 1E-7            NCH      = 4.1589E17      VTH0     = -0.3906012
+K1         = 0.5341312      K2       = 0.0395326      K3       = 0
+K3B       = 7.4916211      W0       = 1E-6          NLX      = 1.194072E-7
+DVTOW     = 0              DVT1W    = 0              DVT2W    = 0
+DVT0      = 0.5060555      DVT1    = 0.2423835      DVT2     = 0.1
+U0        = 115.6894042    UA       = 1.573746E-9      UB       = 1.874308E-21
+UC        = -1E-10         VSAT    = 1.130982E5      A0       = 1.9976555
+AGS       = 0.4186945      B0     = 1.949178E-7      B1       = 6.422908E-7
+KETA      = 0.0166345      A1     = 0.4749146      A2       = 0.300003
+RDSW     = 198.321294      PRWG    = 0.5          PRWB     = -0.4986647
+WR        = 1              WINT    = 0          LINT     = 2.94454E-8
+XL        = 0              XW      = -1E-8          DWG      = -2.798724E-8
+DWB       = -4.83797E-10   VOFF    = -0.095236      NFACTOR  = 2
+CIT       = 0              CDSC    = 2.4E-4          CDSCD    = 0
+CDSCB     = 0              ETA0    = 1.035504E-3      ETAB     = -4.358398E-4
+DSUB      = 1.816555E-3    PCLM    = 1.3299898      PDIBLC1  = 1.766563E-3
+PDIBLC2   = 7.728395E-7    PDIBLCB = -1E-3          DROUT    = 1.011891E-3
+PSCBE1    = 4.872184E10    PSCBE2  = 5E-10          PVAG     = 0.0209921
+DELTA     = 0.01           RSH     = 7.7          MOBMOD   = 1
+PRT       = 0              UTE     = -1.5          KT1      = -0.11
+KT1L      = 0              KT2     = 0.022         UA1      = 4.31E-9
+UB1       = -7.61E-18      UC1     = -5.6E-11      AT       = 3.3E4
+WL        = 0              WLN     = 1          WW       = 0
+WWN       = 1              WWL     = 0          LL      = 0
+LLN       = 1              LW      = 0          LWN     = 1
+LWL       = 0              CAPMOD  = 2          XPART    = 0.5
+CGDO      = 6.35E-10       CGSO    = 6.35E-10      CGBO     = 1E-12
+CJ         = 1.144521E-3    PB      = 0.8468686      MJ       = 0.4099522
+CJSW      = 2.490749E-10    PBSW    = 0.8769118      MJSW     = 0.3478565
+CJSWG     = 4.22E-10       PBSWG   = 0.8769118      MJSWG    = 0.3478565
+CF         = 0              PVTH0   = 2.302018E-3    PRDSW    = 9.0575312
+PK2       = 1.821914E-3     WKETA   = 0.0222457      LKETA    = -1.495872E-3
+PUO       = -1.5580645     PUA     = -6.36889E-11    PUB      = 1E-21
+PVSAT     = 49.8420442     PETA0   = 2.827793E-5    PKETA    = -2.536564E-3
+ NOIMOD=2.0E+00            NOIA=3.574569933176E+18 NOIB=2500
+ NOIC=2.612600202858E-11 EF=1.1388            EM=41000000
*
*
* flicker noise parameters above added manually from some other process
*

```

Ng Spice code

- In the ***test load stage** section, keep removing one comment in order to increase the number of load inverters.

```
1 * Inverter for 23M1117 with 200 + 2 x 17 = 234ps delay.
2
3 *including model files for pMOS and nMOS
4
5 .include models-180nm.txt
6
7 *defining a parameter in order to scale the geometry of pMOS and nMOS
8
9 .param w_p=1.740 w_n=0.595
10 .param l_p=0.18 l_n=0.18
11
12 *defining a circuit component that can be called multiple times
13 *formula used for Area: AD=AS= Wx2Lmin and Perimeter: PD=PS= 2x(W+2Lmin)
14 .subckt inv supply Inp Out
15 MP1 Out Inp Supply Supply cmosp
16 + L={1u*{l_p}} W={{w_p}*1u} AD = {2*{w_p}*{l_p}*{1p}} AS = {2*{w_p}*{l_p}*{1p}}
17   PD = {2*({w_p}+2*{l_p})*1u} PS = {2*({w_p}+2*{l_p})*1u}
18 MN1 Out Inp 0 0 cmosn
19 + L={1u*{l_n}} W={{w_n}*1u} AD = {2*{w_n}*{l_n}*{1p}} AS = {2*{w_n}*{l_n}*{1p}}
20   PD = {2*({w_n}+2*{l_n})*1u} PS = {2*({w_n}+2*{l_n})*1u}
21 .ends
22 vdd supply 0 dc 1.8
23
24 *Input shaper stage
25 Xinv1 supply ck o1 inv
26 Xinv2 supply o1 o2 inv
27 Xinv3 supply o1 o3 inv
28 Xinv4 supply o1 o3 inv
29 Xinv5 supply o1 o3 inv
30 c1 o3 o 0.1p
31
32 *Design under test stage
33 Xinv6 supply o2 o4 inv
34
35 *Test load stage
36 *Xinv7 supply o4 o5 inv
37 *Xinv8 supply o4 o5 inv
38 *Xinv9 supply o4 o5 inv
39 *Xinv10 supply o4 o5 inv
40 *Xinv11 supply o4 o5 inv
41 *Xinv12 supply o4 o5 inv
42 *Xinv13 supply o4 o5 inv
43 *Xinv14 supply o4 o5 inv
44
45 *Load on Load stage
46 Xinv15 supply o5 o6 inv
47 Xinv16 supply o5 o6 inv
48 Xinv17 supply o5 o6 inv
49 Xinv18 supply o5 o6 inv
50 c2 o6 o 0.1p
51
52
53 * pulse with time period of Trep, rise and fall times = Trep/20
54 .param Trep= 5n
55 .param Trf = {Trep/20.0}
```

```

56 .param Tw = {Trep/2.0 - Trf}
57 .param hival=1.8
58 .param loval=0.0
59 Vpulse ck 0 DC 0 PULSE({loval} {hival} {Tw} {Trf} {Trf} {Tw} {Trep})
60 .tran 0.5pS {3*Trep} 0nS
61
62 .control
63 run
64 meas tran invdelay16 TRIG v(o2) VAL=0.9 RISE=2 TARG v(o4) VAL=0.9 FALL=2
65 meas tran invdelay16 TRIG v(o2) VAL=0.9 FALL=2 TARG v(o4) VAL=0.9 RISE=2
66 .endc
67 .end

```

- Simulate the circuit to obtain the delay for the different number of loads and plot the graph:

Number of Inverters	Delay (in ps)		
	Fall Time (ps)	Rise Time (ps)	Average (ps)
0	26.704	27.401	27.0525
1	41.516	41.408	41.462
2	54.494	53.563	54.0285
3	67.091	65.716	66.4035
4	79.644	77.951	78.7975
5	92.188	90.414	91.301
6	104.763	103.116	103.9395
7	117.363	115.980	116.6715
8	129.980	128.946	129.463

Table 1: Delay times, in ps, for different numbers of inverters in parallel

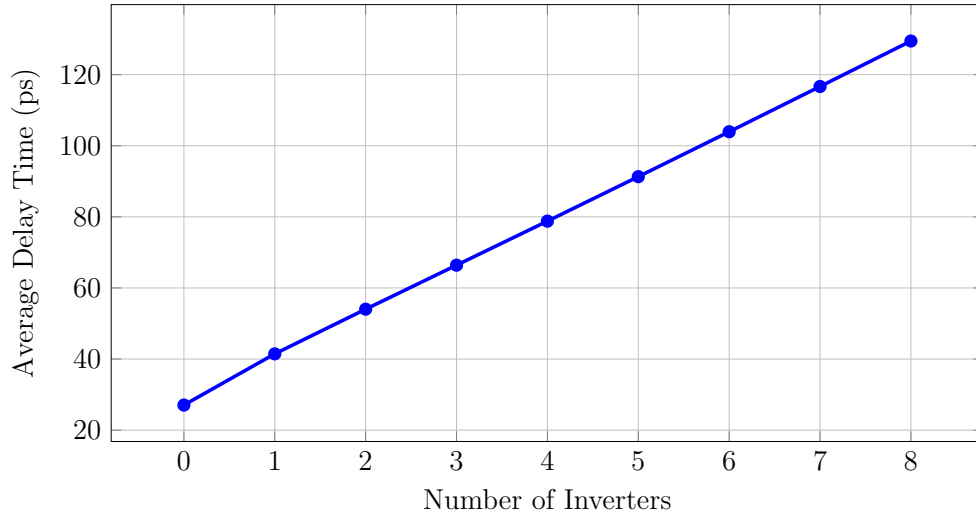


Figure 1: Number of Inverters vs. Average Delay Time

The Delay can be defined as: $D = gbh + p_{inv}$

This whole equation is in units of τ . So the equation would become $D = (gbh + p_{inv})\tau$

The slope of the graph would be: τ

The intercept of the graph would be: τp_{inv}

Finding slope of the graph, for $p_{inv} = 0$, which will get us τ .

$$\tau = \frac{y_2 - y_1}{x_2 - x_1}$$
$$\tau = \frac{66.4035 - 54.0285}{3 - 2}$$
$$\tau = 12.3750 \text{ ps}$$

For number of load inverters = 0, we have $D = p_{inv}\tau$, where $D = 27.0525$.

So, solving the equation for p_{inv} would get us the value of p_{inv} :

$$D = p_{inv}\tau$$
$$27.0525 = p_{inv} * (12.3750)$$
$$p_{inv} = 2.1860$$

For custom inverter of 23M1117,

The width of pMOS inverter = 1.740

The width of nMOS inverter = 0.595

$$\gamma = \frac{1.740}{0.595} = 2.9243$$