# Assignment - 1

## CMOS Logic Design

# EE 671 - VLSI Design



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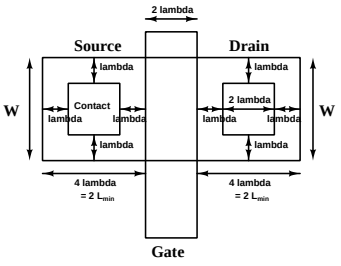
| Date of Sub: | 21st Aug, 2023 |

| Monday | EE 671: VLSI Design | Due on |
|---|---|---|
| Aug. 14, 2023 | Assignment 1 | Aug. 21, 2023 |

We want to design a CMOS inverter using a 180 nm CMOS process. The n and p channel transistors in this process have a channel length of 0.18$\mu$m and a minimum channel width of 0.24$\mu$m. The supply voltage for logic design is 1.8V. Transistor models for this process are attached in a separate file called models-180nm.

Design an inverter in this process with a load capacitance of 0.05pF. In addition to this capacitance, the capacitances associated with the inverter tranistors themselves should be included in the design. For this, the source/drain area and perimeter values (which depend on transistor geometry) should be given to the simulator. These parameters can be calculated as shown in the figure below.

Width of either diffused region is $W$ while its length is $4\lambda$.
Since $\lambda = L_{min}/2, 4\lambda = 2L_{min}$, the Source/Drain area is given by as = ad = $W \times 2L_{min}$.
Source/Drain perimeter is given by:
ps = pd = $2 \times (W + 2L_{min})$.
Thus the capacitances contributed by transistors can be accounted for if we know transistor width and length.




When *as*, *ad*, *ps* and *pd* are specified, the capacitance contributed by these diffused regions is incorporated by the transistor models (and need not be specified separately as a circuit component).

A template file to simulate the inverter is given below. It uses minimum widths for n as well as p channel transistors. Your solution should replace these with appropriate values to meet the delay specification. Notice that the values of area and perimeter of source and drain regions will have to be recalculated when you change the widths.

The .include statement in the template input file given below imports the models from the file models-180nm.

```
* Unit Inverter
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L=0.18U W=0.24U AD = 0.0864P AS = 0.0864P PD = 1.2U PS = 1.2U
MN1 Output Inp 0      0      cmosn
+ L=0.18U W=0.24U AD = 0.0864P AS = 0.0864P PD = 1.2U PS = 1.2U
.ends

vdd supply 0 dc 1.8

*  Device under test
x3  supply Ck dutout inv
```

```
* Load Capacitor
C3 dutout 0 0.05pF

.include models-180nm

*TRANSIENT ANALYSIS with pulse inputs
VCk  Ck   0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS

.control
run
plot 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18 FALL=2
.endc
.end
```

**Q–1** Design a CMOS inverter which gets a rail to rail square wave as the input with rise/fall times of 20 ps. Your inverter should have equal rise/fall times of $200 + 2 \times nn$ ps, where nn represents the last two digits of your roll number.
The design involves the choice of appropriate widths for n and p channel transistors such that it meets the rise/fall time requirements with the given load. Measure the rise/fall times of the output by finding the time taken by the output to traverse between 10% of $V_{DD}$ and 90% of $V_{DD}$.

**Q–2** Use ng-spice to plot the static transfer characteristics of this inverter by using a DC sweep on the input from 0 to $V_{DD}$. Determine the static noise margins for it by drawing tangents with slope = -1.

**Q–3** Using the above inverter as the base design, apply series-parallel rules to design a logic gate which produces $\overline{A \cdot (B + C)}$ at its output. Find the rise and fall times of this gate for the following input combinations:

a) A = '1', B = '0', C = $0 \rightarrow 1$ and C = $1 \rightarrow 0$.
b) A = '1', C = '0', B = $0 \rightarrow 1$ and B = $1 \rightarrow 0$.
c) B = '0', C = '1', A = $0 \rightarrow 1$ and A = $1 \rightarrow 0$.

Take a logic '1' to be $0.9V_{DD}$ and a logic '0' to be $0.1V_{DD}$.

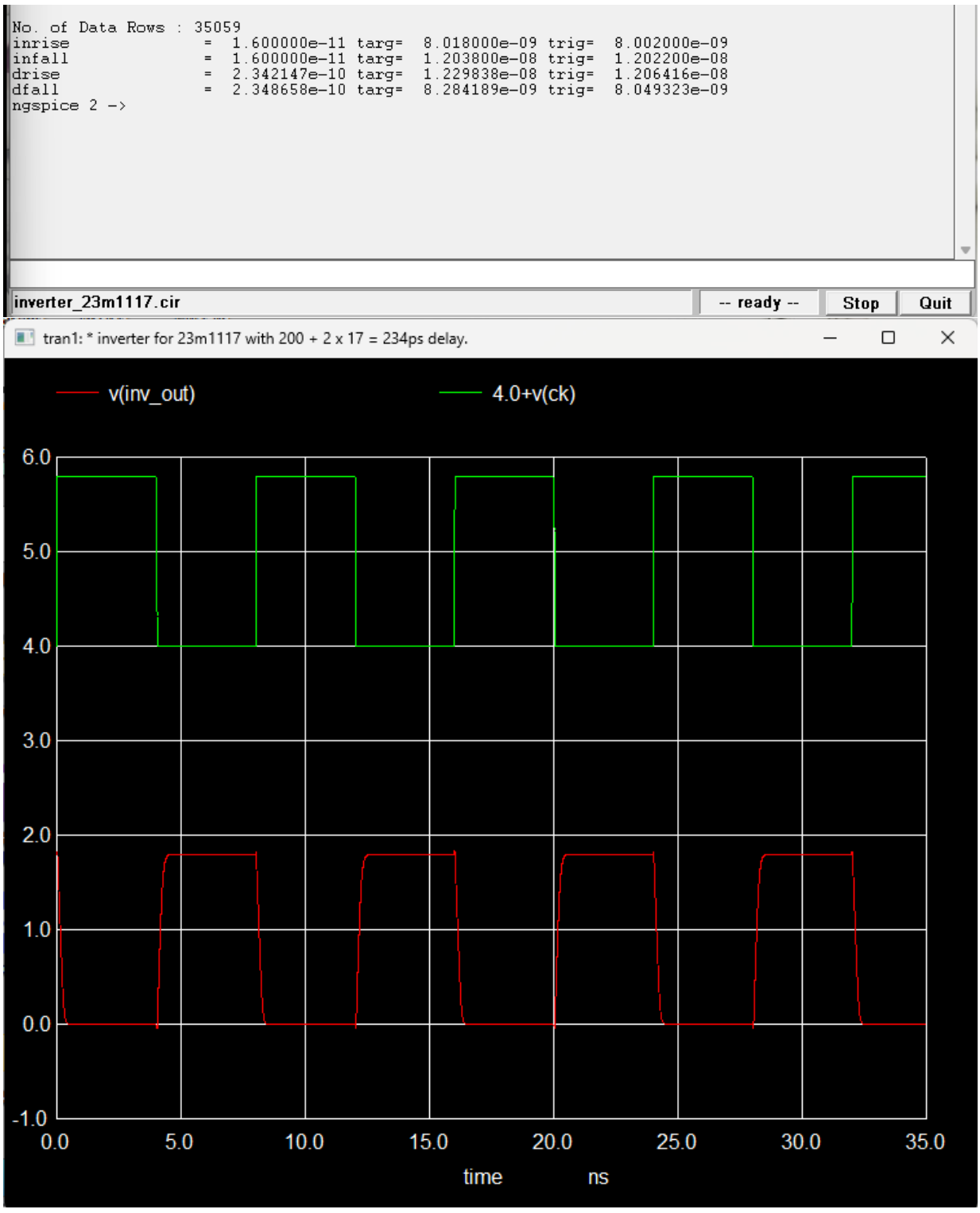
# Q-1 CMOS Inverter

## NgSpice Code

```
* Inverter for 23M1117 with 200 + 2 x 17 = 234ps delay.

*including model files for pMOS and nMOS

.include models-180nm.txt

*defining a parameter in order to scale the geometry of pMOS and nMOS

.param w_p=1.740 w_n=0.595
.param l_p=0.18 l_n=0.18

*defining a circuit component that can be called multiple times
*formula used for Area: AD=AS= Wx2Lmin and Perimeter: PD=PS= 2x(W+2Lmin)
.subckt inv supply Inp Out
MP1 Out Inp Supply Supply cmosp
+ L={1u*{l_p}} W={{w_p}*1u} AD = {2*{w_p}*{l_p}*{1p}} AS = {2*{w_p}*{l_p}*{1p}}
    PD = {2*({w_p}+2*{l_p})*1u} PS = {2*({w_p}+2*{l_p})*1u}
MN1 Out Inp 0      0      cmosn
+ L={1u*{l_n}} W={{w_n}*1u} AD = {2*{w_n}*{l_n}*{1p}} AS = {2*{w_n}*{l_n}*{1p}}
    PD = {2*({w_n}+2*{l_n})*1u} PS = {2*({w_p}+2*{l_n})*1u}
.ends

* Main Supply
vdd supply 0 dc 1.8
*DUT
x1  supply Ck inv_out inv
* Load Capacitor
C1 inv_out 0 0.05pF
*TRANSIENT ANALYSIS with pulse inputs
Vck  Ck   0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)

* transient analysis with 1ps step size untill 35nS with 0nS of delay
.tran 1pS 35nS 0nS
.control
run
plot 4.0+V(Ck) V(inv_out)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(inv_out) VAL=0.18 RISE=2 TARG v(inv_out) VAL=1.62 RISE=2
meas tran dfall TRIG v(inv_out) VAL=1.62 FALL=2 TARG v(inv_out) VAL=0.18 FALL=2
.endc
.end
```

## Output

For pMOS width = 1.740$\mu m$ and nMOS width = 0.595$\mu m$.
Rise Time = 234.21ps
Fall Time = 234.86ps



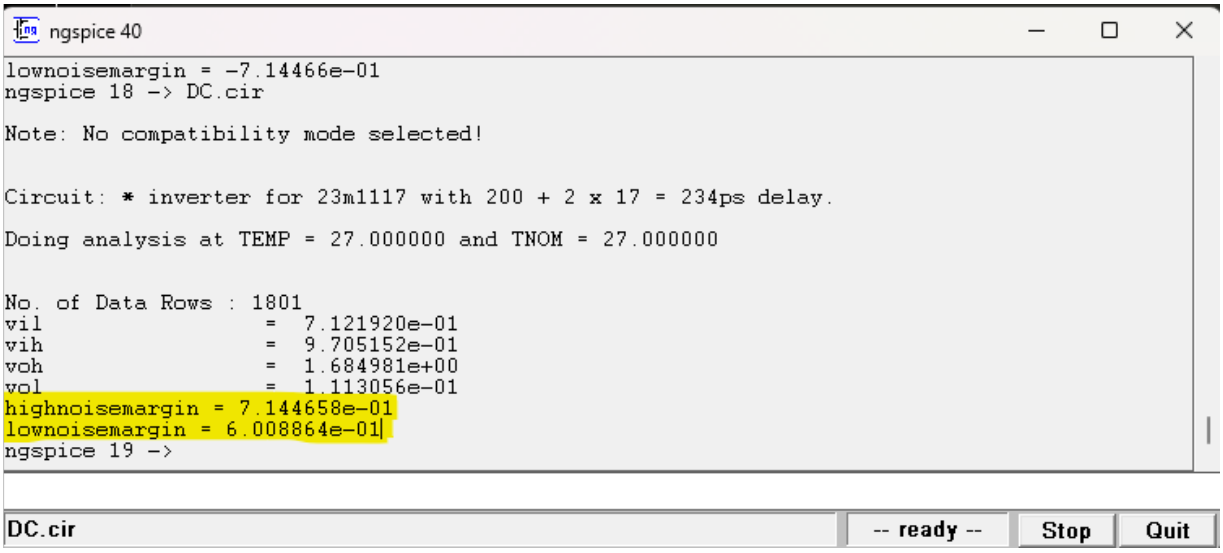
# Q-2 VTC of CMOS Inverter and Noise Margins

## NgSpice code:

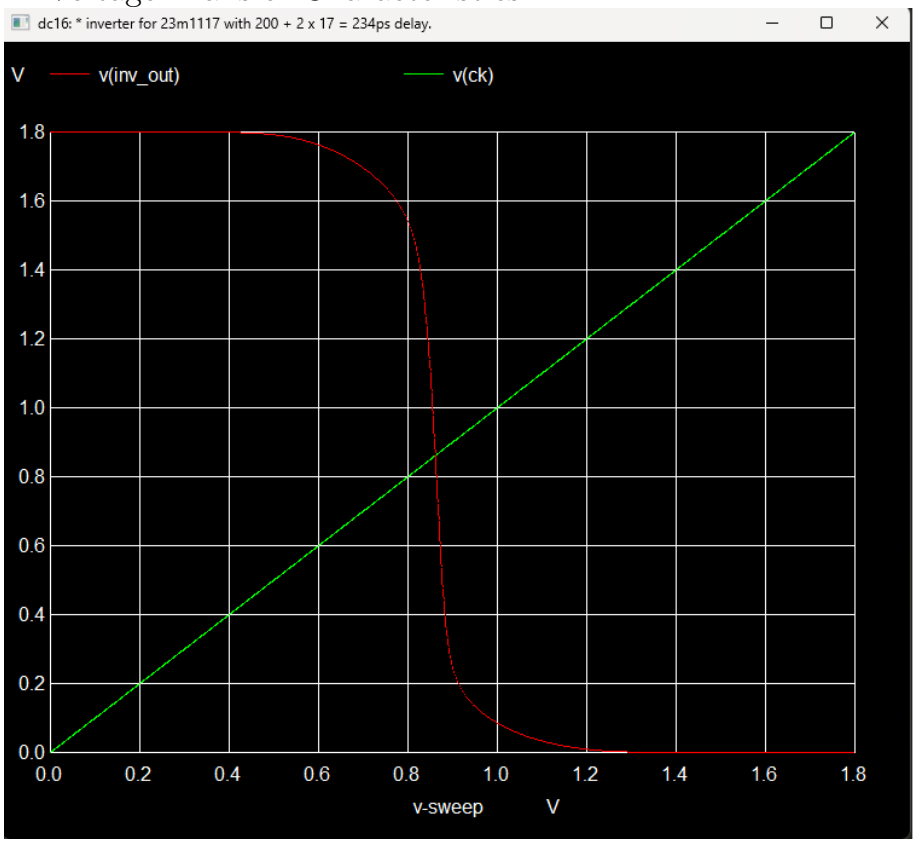
```
* Inverter for 23M1117 with 200 + 2 x 17 = 234ps delay.

*including model files for pMOS and nMOS

.include models-180nm.txt

*defining a parameter in order to scale the geometry of pMOS and nMOS

.param w_p=1.740 w_n=0.595
.param l_p=0.18 l_n=0.18

*defining a circuit component that can be called multiple times
*formula used for Area: AD=AS= Wx2Lmin and Perimeter: PD=PS= 2x(W+2Lmin)
.subckt inv supply Inp Out
MP1 Out Inp Supply Supply cmosp
+ L={1u*{l_p}} W={{w_p}*1u} AD = {2*{w_p}*{l_p}*{1p}} AS = {2*{w_p}*{l_p}*{1p}}
    PD = {2*({w_p}+2*{l_p})*1u} PS = {2*({w_p}+2*{l_p})*1u}
MN1 Out Inp 0      0      cmosn
+ L={1u*{l_n}} W={{w_n}*1u} AD = {2*{w_n}*{l_n}*{1p}} AS = {2*{w_n}*{l_n}*{1p}}
    PD = {2*({w_n}+2*{l_n})*1u} PS = {2*({w_p}+2*{l_n})*1u}
.ends

* Main Supply
vdd supply 0 dc 1.8
*DUT
x1  supply Ck inv_out inv
* Load Capacitor
C1 inv_out 0 0.05pF
*DC Sweep from 0V to 1.8V with 0.1 steps of increments
Vck ck 0 1.8V
.DC VCk 0V 1.8V 1mV
.control
run
plot V(ck) V(inv_out)
*taking the derivative of the output curve to get to the slope of -1 in order
   to find noise margins
let dv = deriv(V(inv_out))

meas dc VIL find V(Ck) when dv=-1 fall=1
meas dc VIH find V(Ck) when dv=-1 rise=1
meas dc VOH find V(inv_out) when V(ck)=VIL
meas dc VOL find V(inv_out) when V(ck)=VIH

let highnoisemargin = VOH-VIH
print highnoisemargin
let lownoisemargin = VIL - VOL
print lownoisemargin

.endc
.end
```

## Output

High noise margin = 714.46mV
Low noise margin = 600.88mV

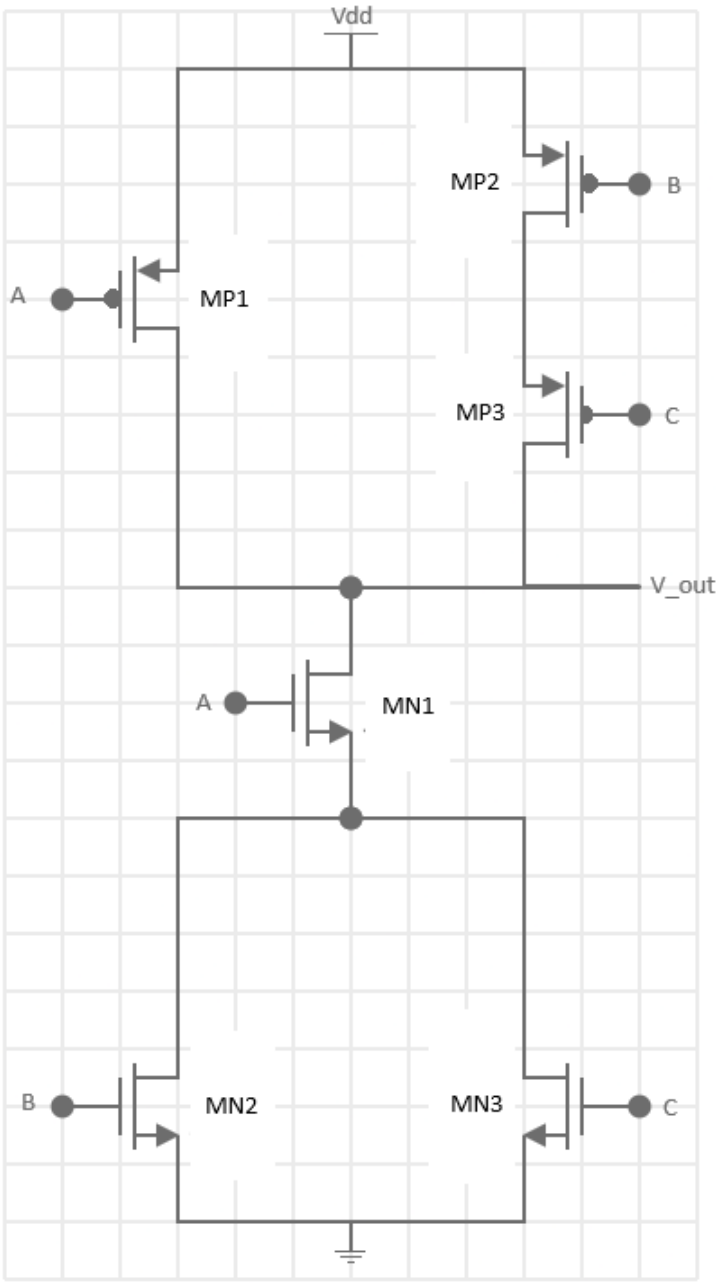



Voltage Transfer Characteristics



## Q-3 CMOS Logic Design of $\overline{A.(B+C)}$

- The geometry of MP1 with input A is left as it is.
- The geometry of MP2 and MP3 with input B and C respectively, scaled to 2 times of the CMOS inverter's pMOS width.
- The geometry of MN1, MN2 and MN3 with input A, B, and C respectively, scaled to 2 times of the CMOS inverter's nMOS width.



## 1) A=1, B=0, C → DC Pulse Input

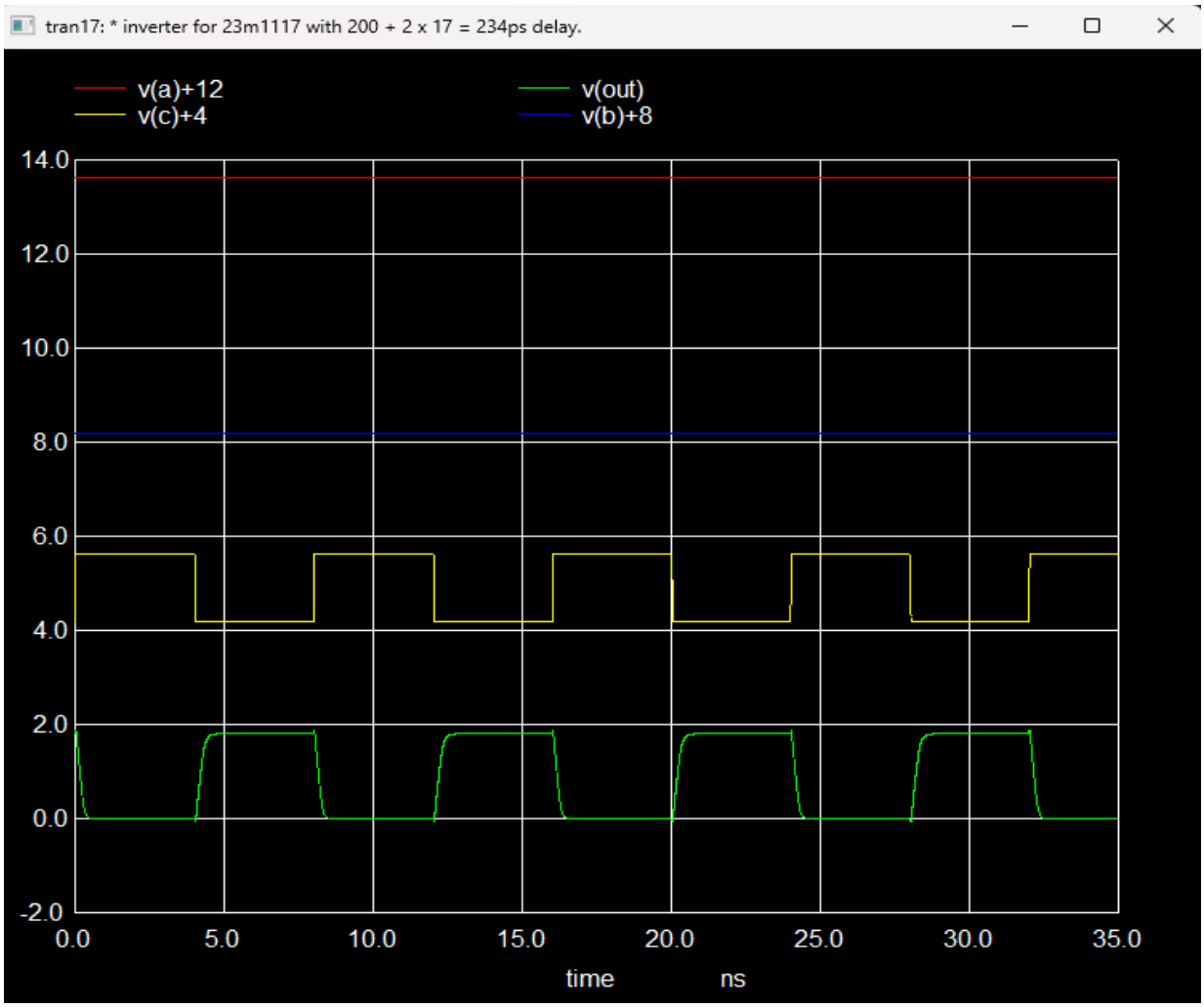
```
* Inverter for 23M1117 with 200 + 2 x 17 = 234ps delay.
*including model files for pMOS and nMOS
.include models-180nm.txt
*main supply
Vdd vdd 0 DC 1.8V

*inputs A = 1, B = 0, and C = Pulse input
Va A 0 dc 1.62V
Vb B 0 dc 0.18V
Vc C 0 DC 0 PULSE(0.18 1.62 0nS 20pS 20pS 4nS 8.0nS)

*defining a parameter in order to scale the geometry of pMOS and nMOS
.param w_p=1.740 w_n=0.595
.param l_p=0.18 l_n=0.18

*MP1 with input A, not scaled!
MP1 out A Vdd Vdd cmosp
+ L={1u*{l_p}} W={{w_p}*1u} AD = {2*{w_p}*{l_p}*{1p}} AS = {2*{w_p}*{l_p}*{1p}}
    PD = {2*({w_p}+2*{l_p})*1u} PS = {2*({w_p}+2*{l_p})*1u}

*MP2 and MP3 with input B and C respectively, scaled to 2 times of the CMOS
   inverter's pMOS width.
MP2 N1 B Vdd Vdd cmosp
+ L={1u*{l_p}} W={{w_p}*2u} AD = {2*2*{w_p}*{l_p}*{1p}} AS = {2*2*{w_p}*{l_p
   }*{1p}} PD = {2*(2*{w_p}+2*{l_p})*1u} PS = {2*(2*{w_p}+2*{l_p})*1u}
MP3 out C N1 N1 cmosp
+ L={1u*{l_p}} W={{w_p}*2u} AD = {2*2*{w_p}*{l_p}*{1p}} AS = {2*2*{w_p}*{l_p
   }*{1p}} PD = {2*(2*{w_p}+2*{l_p})*1u} PS = {2*(2*{w_p}+2*{l_p})*1u}

*MN1, MN2 and MN3 with input A, B, and C respectively, scaled to 2 times of the
    CMOS inverter's nMOS width.
MN1 Out A N2 N2 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}
MN2 N2 B 0 0 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}
MN3 N2 C 0 0 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}

*load capacitor
C3 out 0 0.05pF

*TRANSIENT ANALYSIS with pulse inputs
.tran 1pS 35nS 0nS
.control
run
plot V(out) V(A)+12 V(B)+8 V(C)+4
meas tran drise TRIG v(Out) VAL=0.18 RISE=2 TARG v(out) VAL=1.62 RISE=2
meas tran dfall TRIG v(out) VAL=1.62 FALL=2 TARG v(out) VAL=0.18 FALL=2
.endc
.end
```

Rise time = 300ps, and Fall time = 256ps

ngspice 40

```
Node                                   Voltage
----                                   -------
vdd                                        1.8
a                                         1.62
b                                         0.18
c                                         0.18
out                                    1.79999
n1                                         1.8
n2                                     1.38894
vc#branch                                    0
vb#branch                                    0
va#branch                                    0
vdd#branch                        -4.00156e-09


No. of Data Rows : 35059
drise                =  3.004081e-10 targ=  1.237838e-08 trig=  1.207798e-08
dfall                =  2.567697e-10 targ=  8.322196e-09 trig=  8.065427e-09
ngspice 23 ->
```

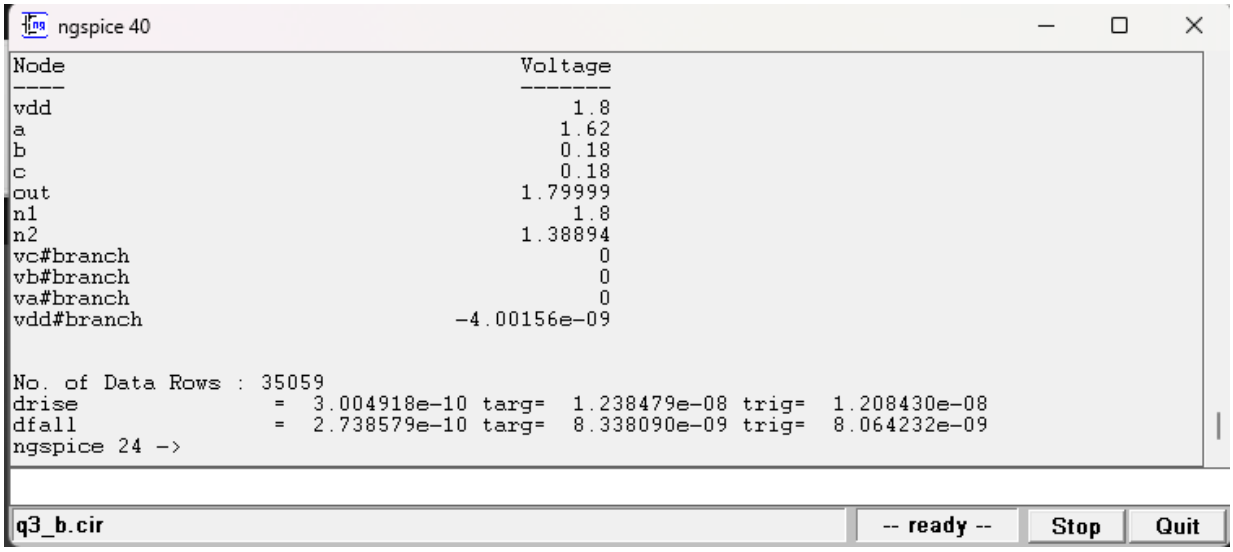
q3.cir -- ready -- Stop Quit

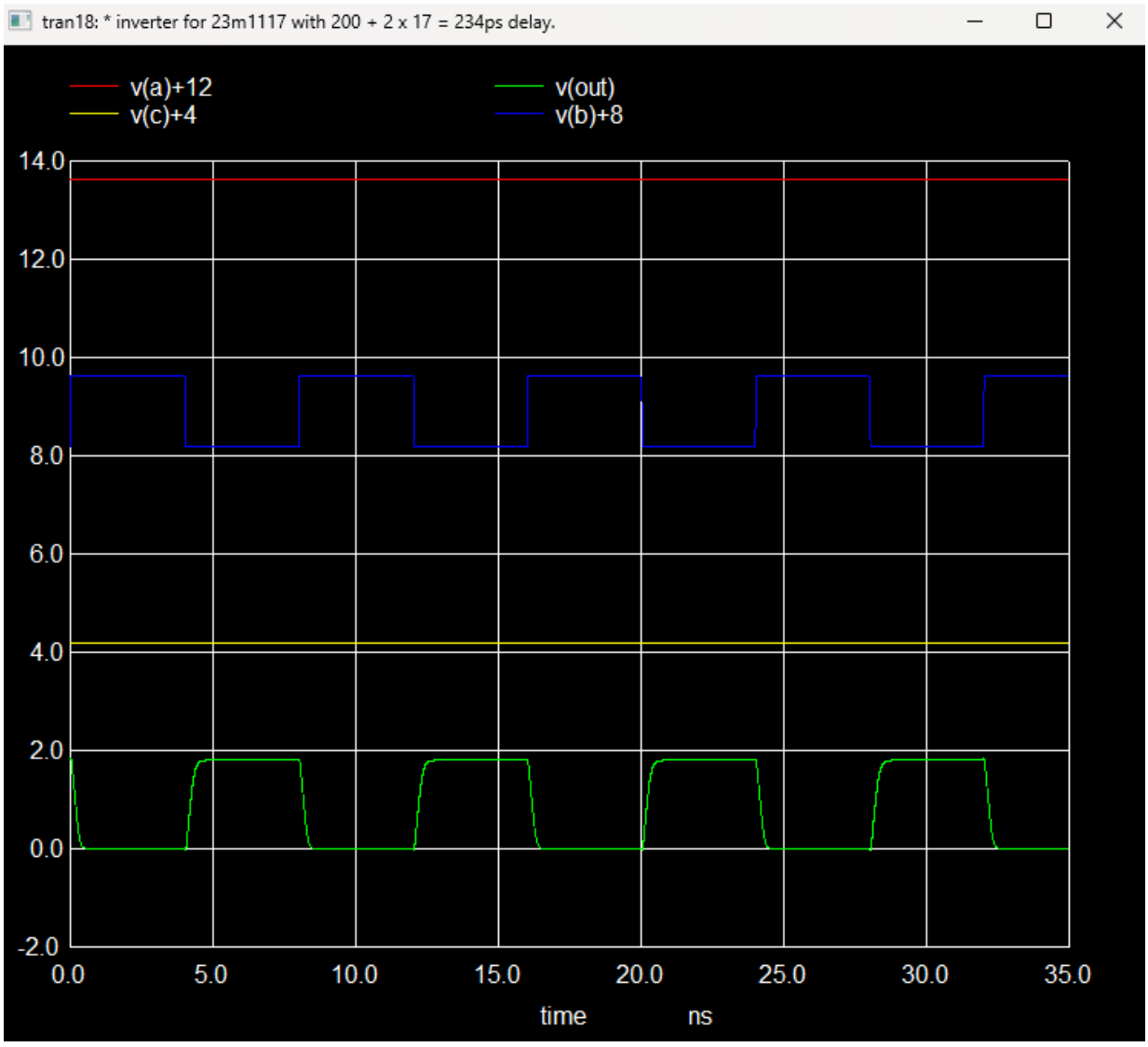


## 2) A=1, B → DC Pulse Input, C=0

```
* Inverter for 23M1117 with 200 + 2 x 17 = 234ps delay.
*including model files for pMOS and nMOS
.include models-180nm.txt
*main supply
Vdd vdd 0 DC 1.8V

*inputs A = 1, B = Pulse input, and C = 0.
Va A 0 dc 1.62V
Vb B 0 dc 0 PULSE(0.18 1.62 0nS 20pS 20pS 4nS 8.0nS)
Vc C 0 DC 0.18V

*defining a parameter in order to scale the geometry of pMOS and nMOS
.param w_p=1.740 w_n=0.595
.param l_p=0.18 l_n=0.18

*MP1 with input A, not scaled!
MP1 out A Vdd Vdd cmosp
+ L={1u*{l_p}} W={{w_p}*1u} AD = {2*{w_p}*{l_p}*{1p}} AS = {2*{w_p}*{l_p}*{1p}}
    PD = {2*({w_p}+2*{l_p})*1u} PS = {2*({w_p}+2*{l_p})*1u}

*MP2 and MP3 with input B and C respectively, scaled to 2 times of the CMOS
   inverter's pMOS width.
MP2 N1 B Vdd Vdd cmosp
+ L={1u*{l_p}} W={{w_p}*2u} AD = {2*2*{w_p}*{l_p}*{1p}} AS = {2*2*{w_p}*{l_p
   }*{1p}} PD = {2*(2*{w_p}+2*{l_p})*1u} PS = {2*(2*{w_p}+2*{l_p})*1u}
MP3 out C N1 N1 cmosp
+ L={1u*{l_p}} W={{w_p}*2u} AD = {2*2*{w_p}*{l_p}*{1p}} AS = {2*2*{w_p}*{l_p
   }*{1p}} PD = {2*(2*{w_p}+2*{l_p})*1u} PS = {2*(2*{w_p}+2*{l_p})*1u}

*MN1, MN2 and MN3 with input A, B, and C respectively, scaled to 2 times of the
    CMOS inverter's nMOS width.
MN1 Out A N2 N2 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}
MN2 N2 B 0 0 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}
MN3 N2 C 0 0 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}

C3 out 0 0.05pF


*TRANSIENT ANALYSIS with pulse inputs


.tran 1pS 35nS 0nS
.control
run
plot V(out) V(A)+12 V(B)+8 V(C)+4
meas tran drise TRIG v(Out) VAL=0.18 RISE=2 TARG v(out) VAL=1.62 RISE=2
meas tran dfall TRIG v(out) VAL=1.62 FALL=2 TARG v(out) VAL=0.18 FALL=2

.endc
.end
```

Rise time = 300ps, and Fall time = 273ps



## 3) A→ DC Pulse Input, B=0, C=1

```
* Inverter for 23M1117 with 200 + 2 x 17 = 234ps delay.
*including model files for pMOS and nMOS
.include models-180nm.txt
*main supply
Vdd vdd 0 DC 1.8V

Va A 0 dc PULSE(0.18 1.62 0nS 20pS 20pS 4nS 8.0nS)
Vb B 0 dc 0.18
Vc C 0 DC 1.62V

*defining a parameter in order to scale the geometry of pMOS and nMOS

.param w_p=1.740 w_n=0.595
.param l_p=0.18 l_n=0.18

*MP1 with input A, not scaled!
MP1 out A Vdd Vdd cmosp
+ L={1u*{l_p}} W={{w_p}*1u} AD = {2*{w_p}*{l_p}*{1p}} AS = {2*{w_p}*{l_p}*{1p}}
    PD = {2*({w_p}+2*{l_p})*1u} PS = {2*({w_p}+2*{l_p})*1u}

*MP2 and MP3 with input B and C respectively, scaled to 2 times of the CMOS
   inverter's pMOS width.
MP2 N1 B Vdd Vdd cmosp
+ L={1u*{l_p}} W={{w_p}*2u} AD = {2*2*{w_p}*{l_p}*{1p}} AS = {2*2*{w_p}*{l_p
   }*{1p}} PD = {2*(2*{w_p}+2*{l_p})*1u} PS = {2*(2*{w_p}+2*{l_p})*1u}
MP3 out C N1 N1 cmosp
+ L={1u*{l_p}} W={{w_p}*2u} AD = {2*2*{w_p}*{l_p}*{1p}} AS = {2*2*{w_p}*{l_p
   }*{1p}} PD = {2*(2*{w_p}+2*{l_p})*1u} PS = {2*(2*{w_p}+2*{l_p})*1u}

*MN1, MN2 and MN3 with input A, B, and C respectively, scaled to 2 times of the
    CMOS inverter's nMOS width.
MN1 Out A N2 N2 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}
MN2 N2 B 0 0 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}
MN3 N2 C 0 0 cmosn
+ L={1u*{l_n}} W={{w_n}*2u} AD = {2*2*{w_n}*{l_n}*{1p}} AS = {2*2*{w_n}*{l_n
   }*{1p}} PD = {2*(2*{w_n}+2*{l_n})*1u} PS = {2*(2*{w_n}+2*{l_n})*1u}

*load capacitor
C3 out 0 0.05pF

*TRANSIENT ANALYSIS with pulse inputs
.tran 1pS 35nS 0nS
.control
run
plot V(out) V(A)+12 V(B)+8 V(C)+4
meas tran drise TRIG v(Out) VAL=0.18 RISE=2 TARG v(out) VAL=1.62 RISE=2
meas tran dfall TRIG v(out) VAL=1.62 FALL=2 TARG v(out) VAL=0.18 FALL=2
.endc
.end
```

Risetime = 309ps, and Fall time = 256ps

ngspice 40

```
Node                                   Voltage
----                                   -------
vdd                                        1.8
a                                         0.18
b                                         0.18
c                                         1.62
out                                        1.8
n1                                         1.8
n2                                   1.3919e-06
vc#branch                                    0
vb#branch                                    0
va#branch                                    0
vdd#branch                         -2.52791e-09


No. of Data Rows : 35059
drise                =   3.092396e-10 targ=  1.238499e-08 trig=  1.207575e-08
dfall                =   2.567755e-10 targ=  8.306370e-09 trig=  8.049594e-09
ngspice 25 ->
```

q3_c.cir | -- ready -- | Stop | Quit