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Institute Of Infrastructure Technology Research and Management (IITRAM)

(An Autonomous University established By Government of Gujarat)

DIGITAL SYSTEMS

BASIC SRAM CELL

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Introduction

Memory is the portion of a computer or other system that store binary data. In a computer, memory is accessed millions of times per second, so the requirement for speed and accuracy is paramount, Very fast semiconductor memory is available today in modules with several GB of capacity. These large –memory modules use exactly the same operating principles as smaller units, so we are using smaller ones for illustration.

Basic memory operation

Addressing is the process of accessing a specified location in memory. Since a memory stores binary data, data must be put into the memory and data must be copied from the memory when needed. The **write** operation puts data into a specified address in the memory, and the **read** operation copies data out of a specified address in the memory. The addressing operation, which is part of both the write and the read operations, selects the specified memory address.

Data units go into the memory during a write operation and come out of the memory during a read operation on a set of lines called the ***data bus***. For a write or a read operation, an address is selected by placing a binary code representing the desired address on a set of lines called the *address bus.* The address code is decoded internally, and the appropriate address is selected.

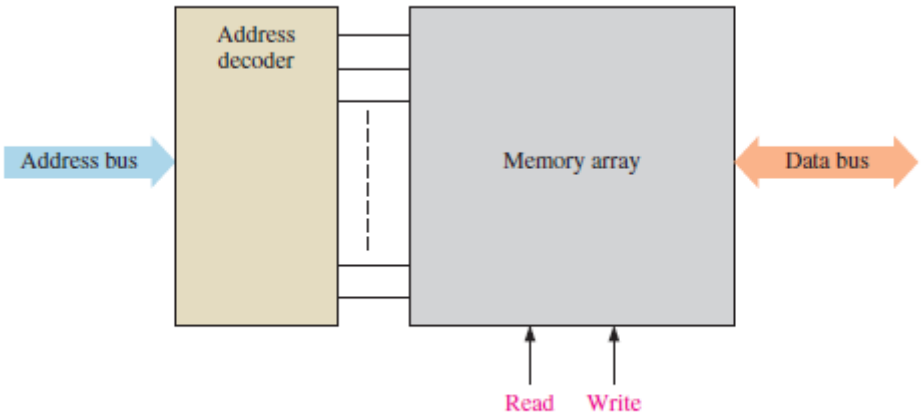


Figure (1)

The write operation

A simplified write operation is illustrated in Figure (2). To store a byte of data in the memory, a code held in the address register is placed on the address bus. Once the address code is on the bus, the address decoder decodes the address and selects the specified location in the memory. The memory then gets a write command, and the data byte held in the data register is placed on the data bus and stored in the selected memory address, thus completing the write operation. When a new data byte is written into a memory address, the current data byte stored at that address is overwritten (replaced with a new data byte).

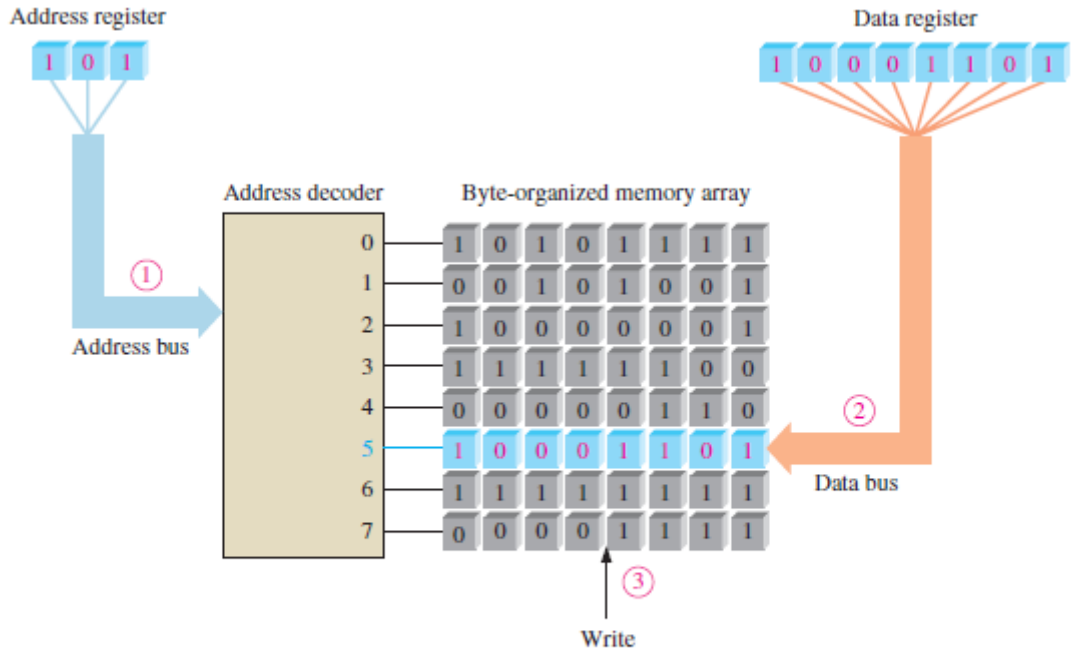
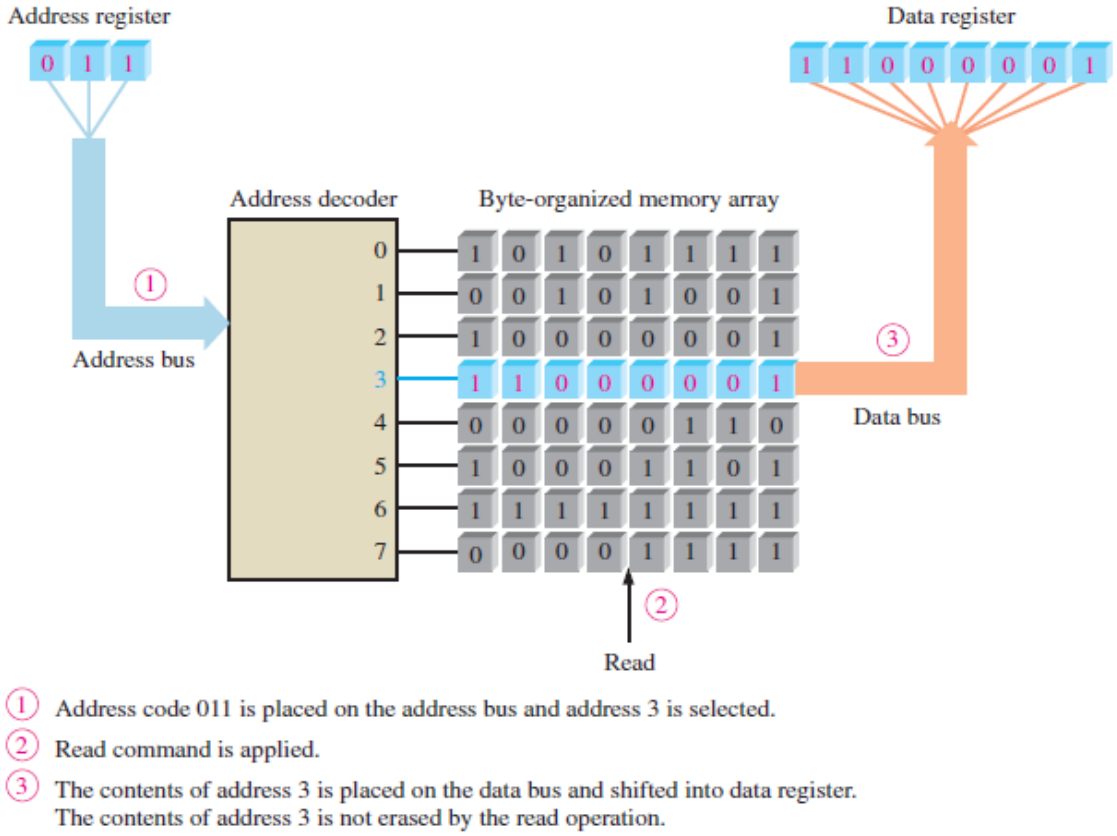


Figure (2)

The Read Operation

A simplified read operation is illustrated in Figure (3). Again, a code held in the address register is placed on the address bus. Once the address code is on the bus, the address decoder decodes the address and selects the specified location in the memory. The memory then gets a read command, and a "copy" of the data byte that is stored in the selected memory address is placed on the data bus and loaded into the data register, thus completing the read operation. When a data byte is read from a memory address, it also remains stored at that address. This is called *non-destructive read*.



1. Address code 011 is placed on the address bus and address 3 is selected.
2. Read command is applied.
3. The contents of address 3 is placed on the data bus and shifted into data register. The contents of address 3 is not erased by the read operation.

Figure (3)

RAMs and ROMs

The two major categories of semiconductor memories are the RAM and the ROM.

RAM (random-access memory) is a type of memory in which all addresses are accessible in an equal amount of time and can be selected in any order for a read or write operation. All RAMs have both *read* and *write* capability. Because RAMs lose stored data when the power is turned off, they are **volatile** memories.

ROM (read-only memory) is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation as in the RAM. The ROM, like the RAM, is a random-access memory but the term *RAM* traditionally means a random-access *read/write* memory. As ROMs retain stored data even if power is turned off, they are **non-volatile** memories.

The Random-Access Memory (RAM)

A RAM is a read/write memory in which data can be written into or read from any selected address in any sequence. When a data unit is written into a given address in the RAM, the data unit previously stored at that address is replaced by the new data unit. When a data unit is read from a given address in the RAM, the data unit remains stored and is not erased by the read operation. This non-destructive read operation can be viewed as copying the content of an address while leaving the content intact. A RAM is typically used for short-term data storage because it cannot retain stored data when power is turned off.

Different Types of RAM

The two major categories of RAM are the *static RAM* (SRAM) and the *dynamic RAM* (DRAM). **SRAMs** generally use latches as storage elements and can therefore store data indefinitely *as long as dc power is applied.* **DRAMs** use capacitors as storage elements and cannot retain data very long without the capacitors being recharged by a process called **refreshing.** Both SRAMs and DRAMs will lose stored data when dc power is removed and, therefore, are classified as volatile memories. Data can be read much faster from SRAMs than from DRAMs. However, DRAMs can store much more data than SRAMs for a given physical size and cost because the DRAM cell is much simpler and more cells can be crammed into a given chip area than in the SRAM. The basic types of SRAM are the *asynchronous SRAM* and the *synchronous SRAM* with a burst feature. The basic types of DRAM are the *Fast Page Mode DRAM* (FPM DRAM), the *Extended Data Out DRAM* (EDO DRAM), the *Burst EDO DRAM* (BEDO DRAM), and the *synchronous DRAM* (SDRAM). These are shown in Figure (4).

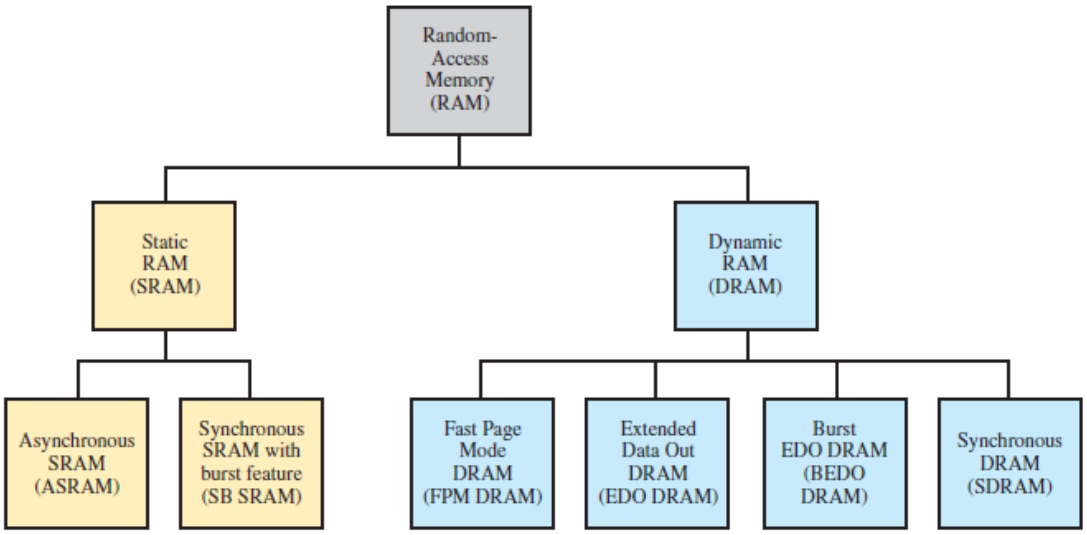


Figure (4)

Static RAMs (SRAMs)

All SRAMs are characterized by latch memory cells. As long as dc power is applied to a **static memory** cell, it can retain a 1 or 0 state indefinitely. If power is removed, the stored data bit is lost.

A typical SRAM latch memory cell is shown in the figure (5). Figure (5) shows a basic SRAM latch memory cell. The cell is selected by an active level on the Select line and a data bit (1 or 0) is written into the cell by placing it on the Data in line.

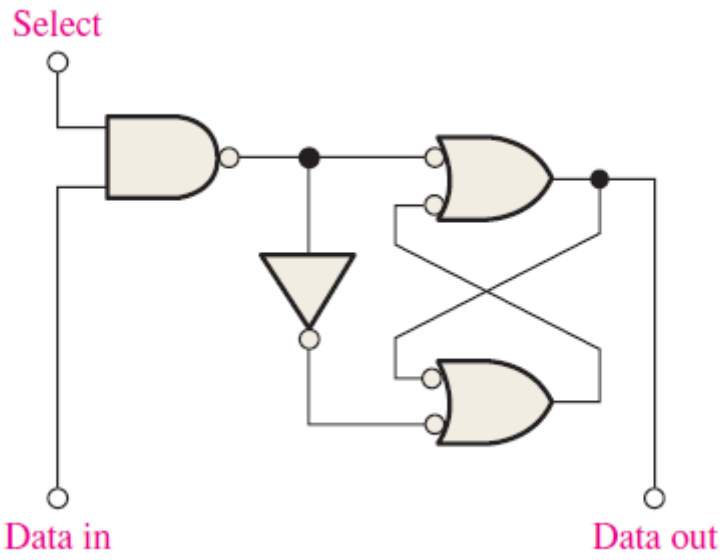
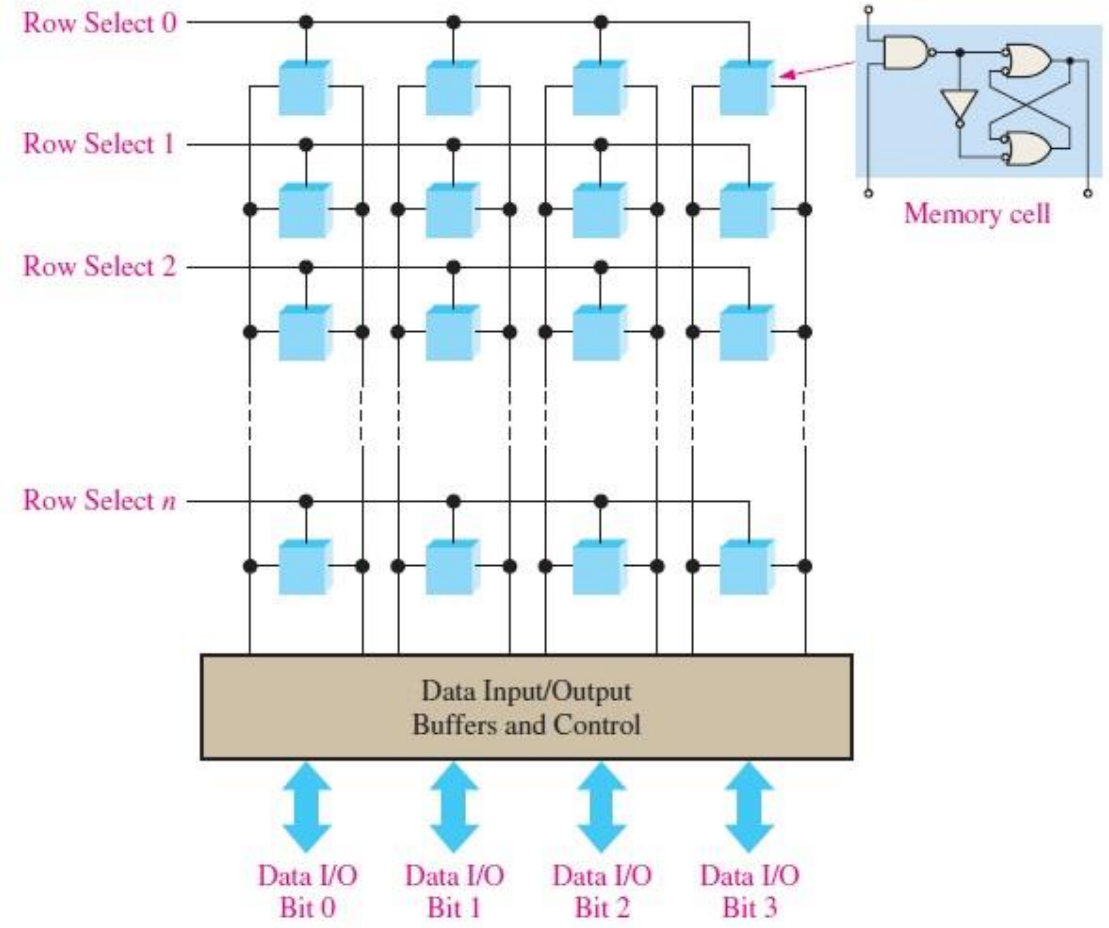


Figure (5)

Static Memory Cell Array

The memory cells in a SRAM are organized in rows and columns, as illustrated in Figure (6) for the case of an *n* * 4 array. All the cells in a row share the same Row Select line. Each set of Data in lines go to each cell in a given. To write a data unit, in this case 4 bits, into a given row of cells in the memory array, the Row Select line is taken to its active state and four data bits are placed on the Data I/O lines. The Write line is then taken to its active state, which causes each data bit to be stored in a selected cell in the associated column. To read a data unit, the Read line is taken to its active state, which causes the four data bits stored in the selected row to appear on the Data I/O lines.



Figure(6)

In figure (7) is shown the basic SRAM cell assembled on Perf board. Which is powered by a 9V battery. Using a 7805 Voltage regulator, 9V is turned into 5V to give the input because mounted ICs need 5V to run.

Figure (7)

Conclusion:

With the help of NAND and NOR gate ICs, a basic SRAM cell is formed, which is the smallest building unit for SRAMs having very big capacity. With this element , only 1 bit of data write operation is shown.

References:

Digital fundamentals (Thomas L. Floyd)