

8-bit Carry Save Multiplier

Design with and without

Pipelining

Table of Contents

Brief Summary table

Unpipelined CSM

- Schematic
- Layout
- Area of CSM Layout
- Input Combinations – Functionality testing
- Maximum operating frequency of CSM

(SPICE simulation showing the frequency of operation without pipelining)

Pipelined CSM

- Schematic
- Maximum operating frequency of CSM
(RC-extracted layout)

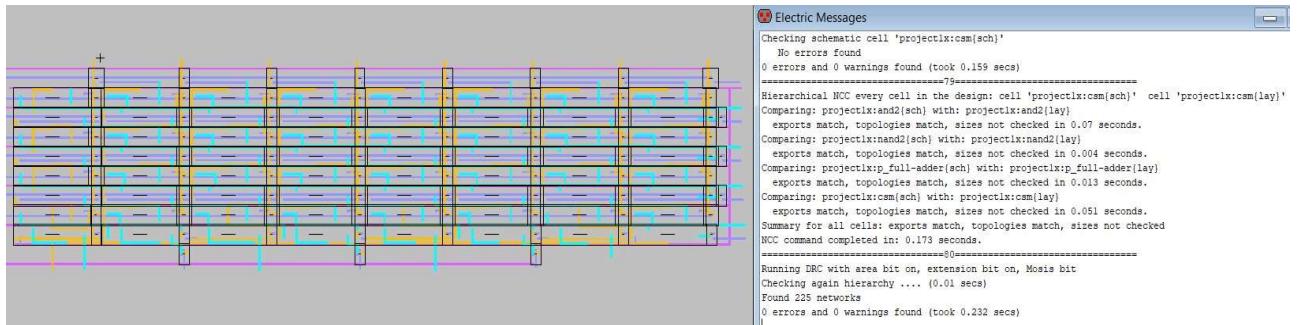
(SPICE simulation showing the frequency of operation with pipelining)

Spice Simulations Vector Merge Sqrt and Ripple Adder

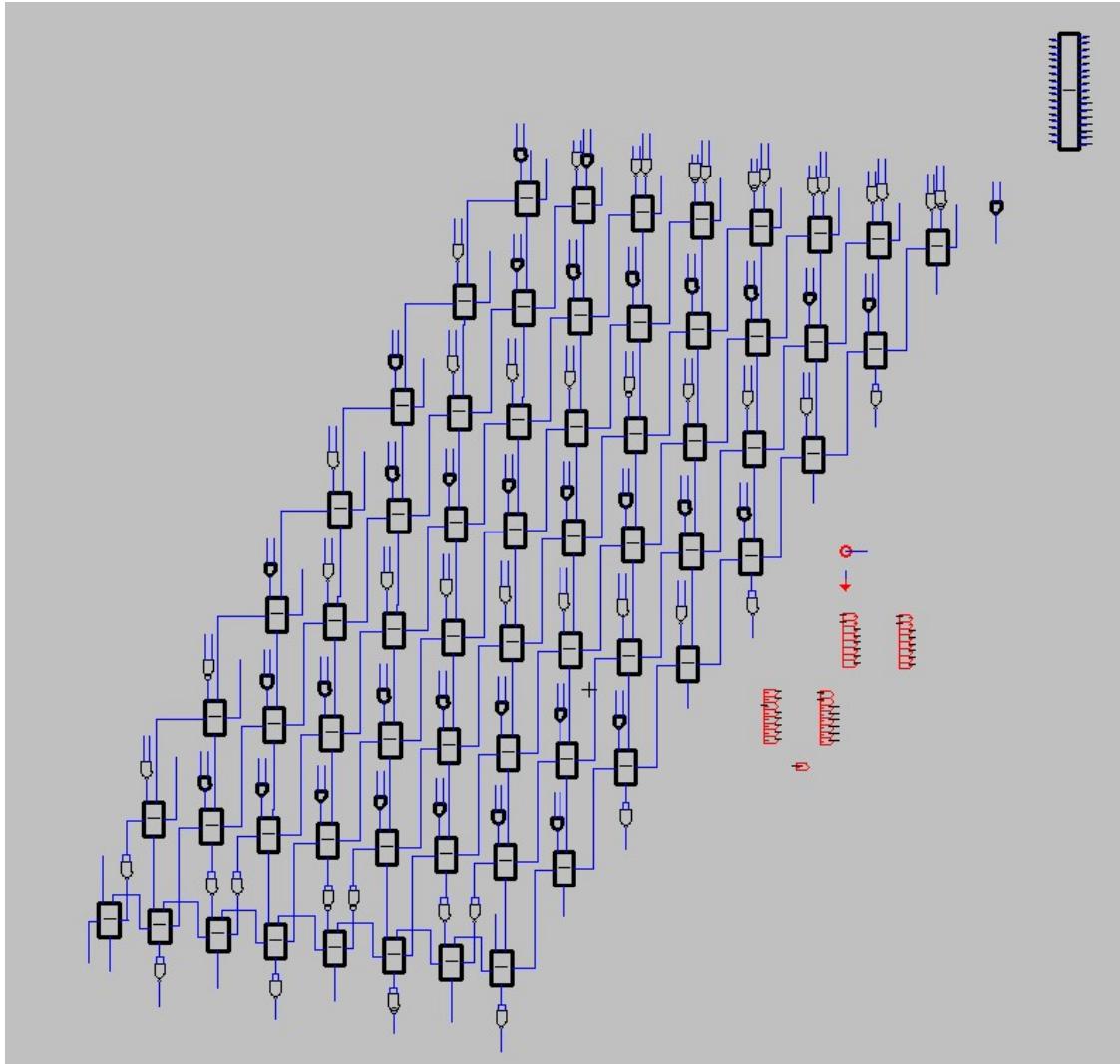
Brief Summary Table

DRS and LVS Status	Clean
Area of CSM Layout (In micro-meter square)	194.61171125
Number of test patterns used for functionality testing of CSM	8
Maximum Clock Frequency without pipelining for Schematic	2.76E+09 Hz
Maximum Clock Frequency without pipelining for Layout (RC – extracted)	1.56E+09 Hz
Maximum Clock Frequency with pipelining for Layout (RC – extracted)	5.03E +09 Hz

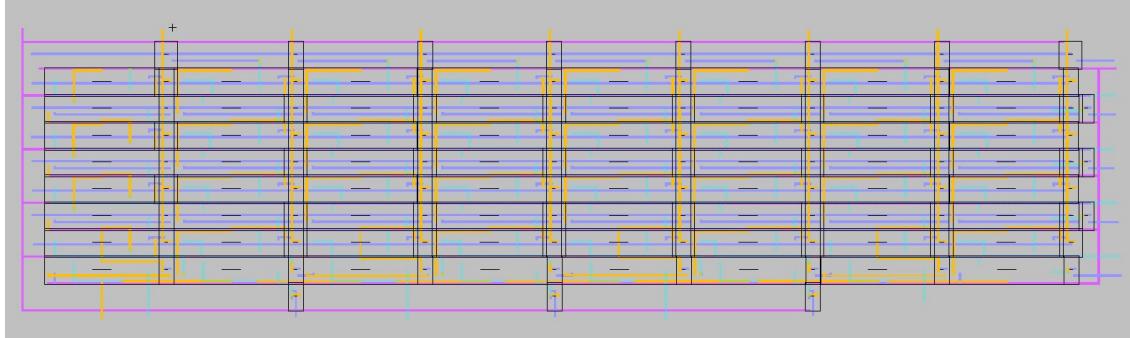
DRS and LVS Clean



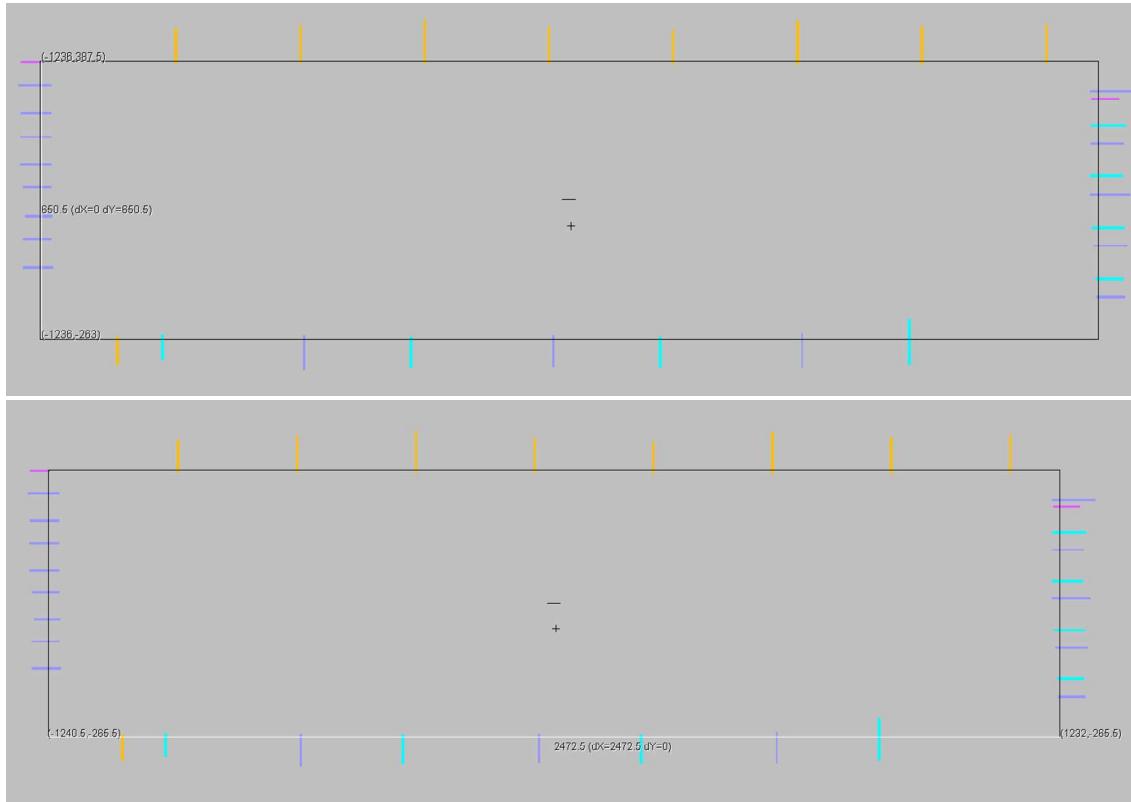
Unpipelined CSM Schematic



Unpipelined CSM Layout



Area of CSM Layout



$$\text{Width} = 2472.5 * (\text{lambda})$$

$$\text{Height} = 650.5 * (\text{lambda})$$

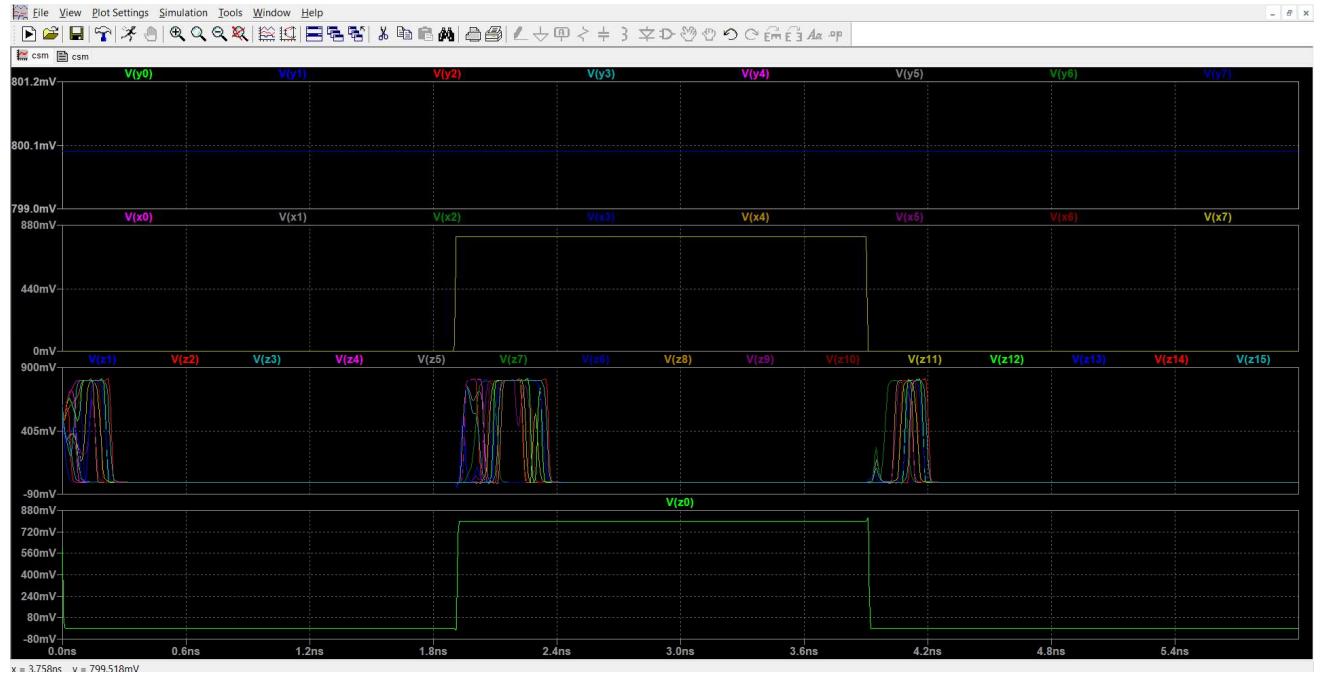
$$\text{Area of CSM Layout} = 2472.5 * 650.5 * (11 \text{ nm} * 11 \text{ nm})$$

$$\text{Area of CSM Layout} = 194.61171125 \mu\text{m}^2$$

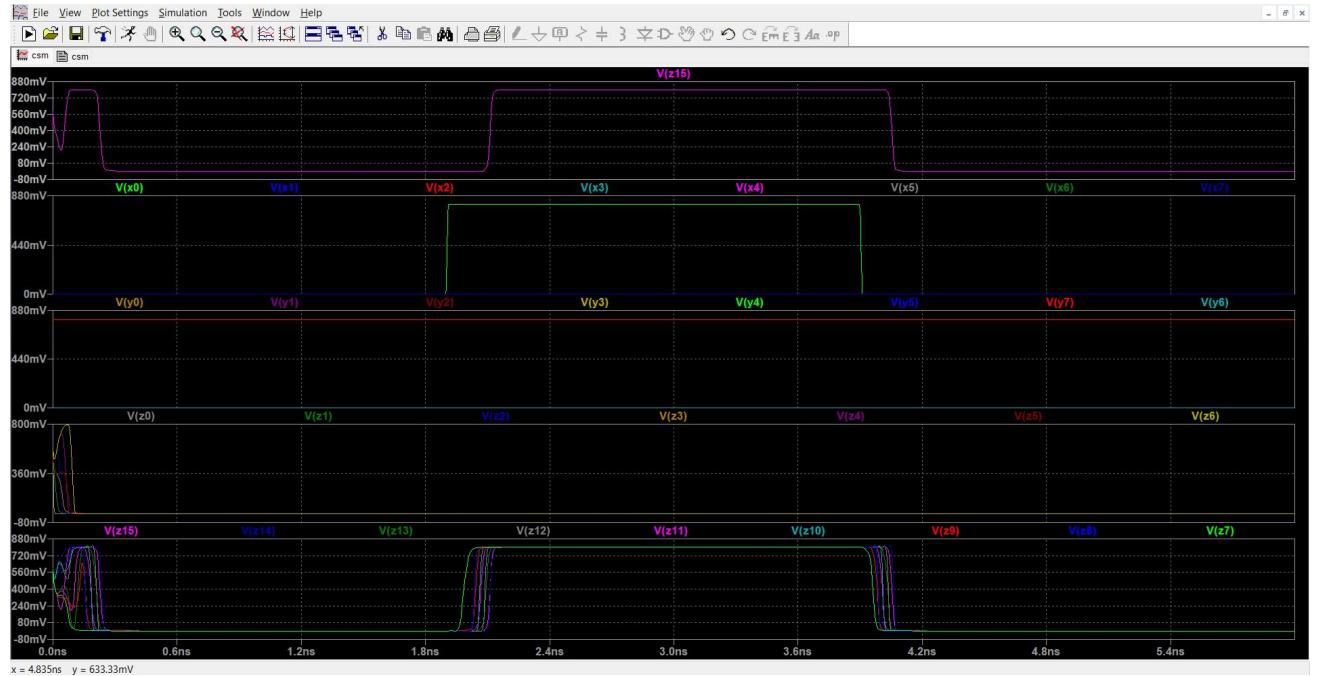
Functionality Testing (Input Combinations) Table

A (dec)	A (binary)	B (dec)	B (binary)	S (dec)	S (binary)	Functionality
-1	11111111	-1	11111111	1	0000000000000001	True
1	00000001	-128	10000000	-128	1111111100000000	True
17	00010001	28	00011100	476	0000000111011100	True
21	00010101	53	00110101	1113	0000010001011001	True
-11	11110101	-11	11110101	121	0000000001111001	True
127	01111111	-128	10000000	-16256	1100000010000000	True
-128	10000000	-1	11111111	128	0000000010000000	True
-69	10111011	119	01110111	-8211	110111111101101	True

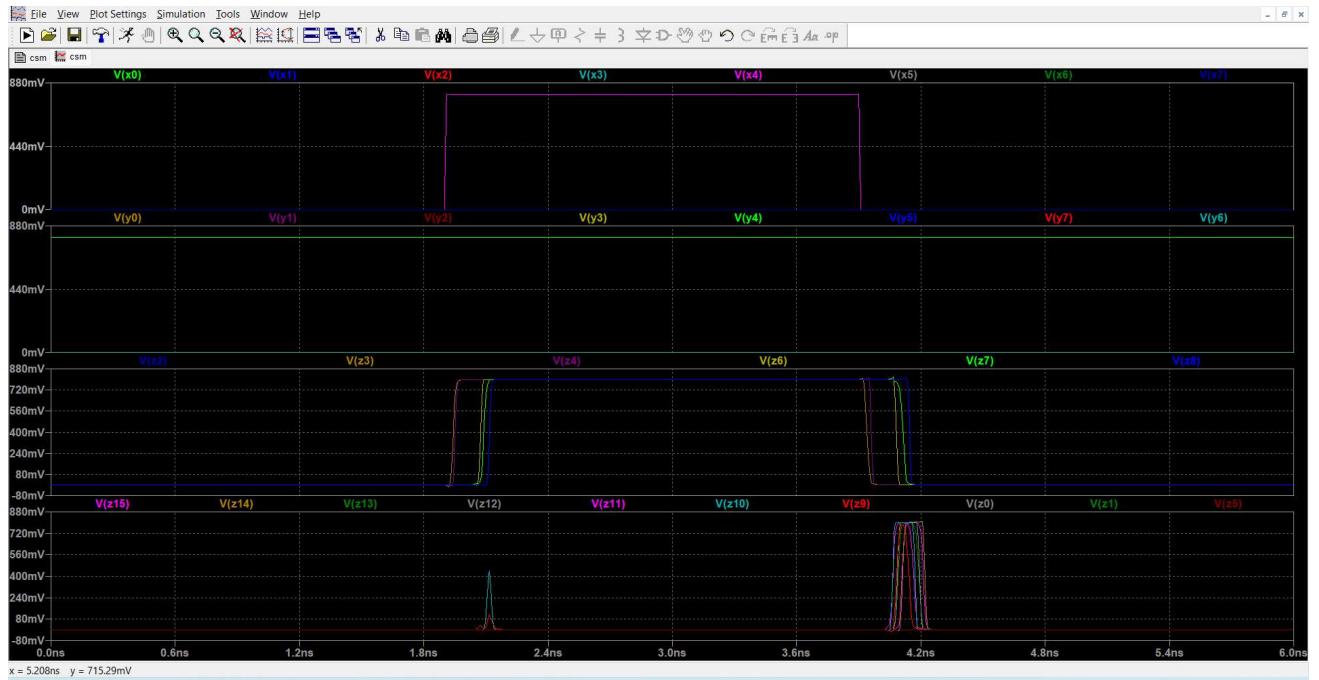
Case-1: A = -1, B = -1



Case-2: A = 1, B = -128



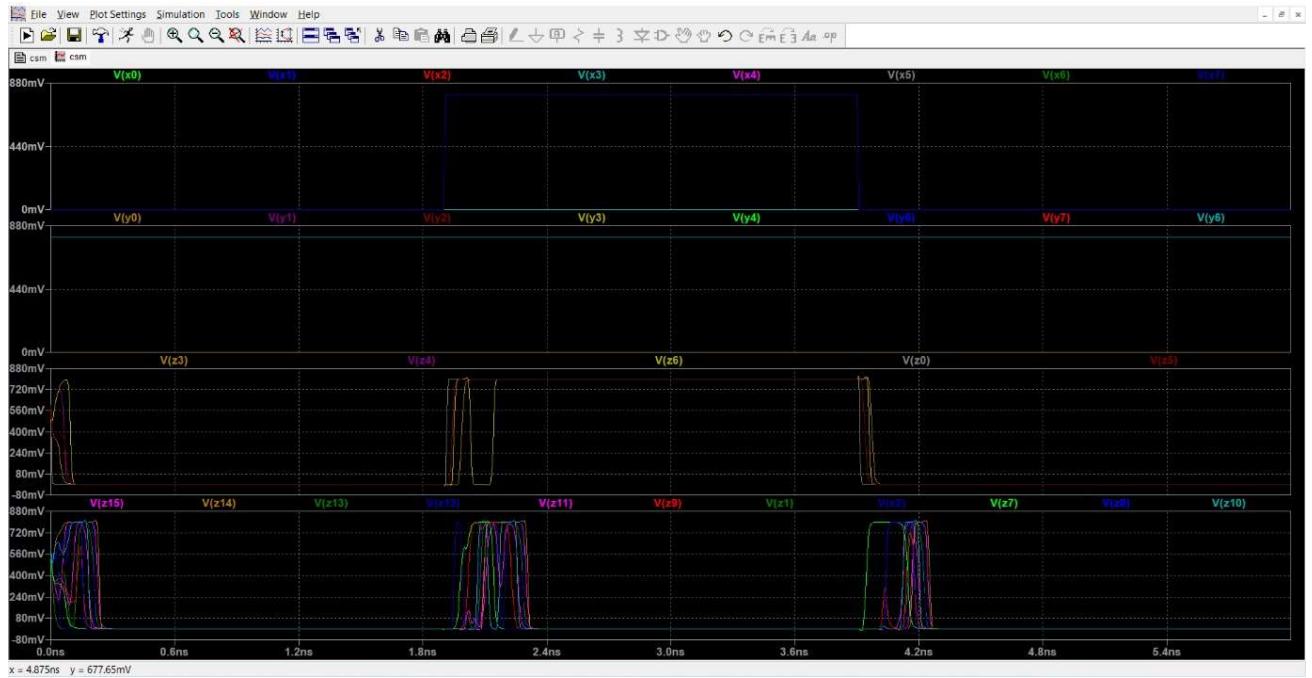
Case-3: A = 17, B = 28



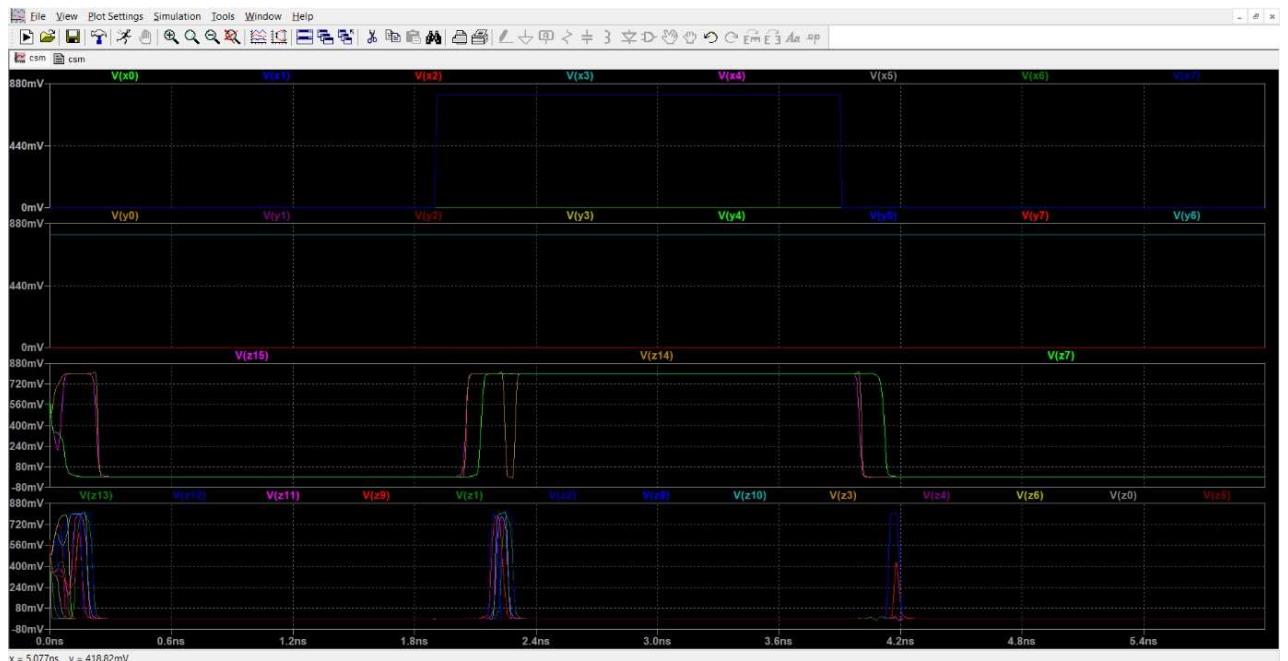
Case-4: A = 21, B = 53



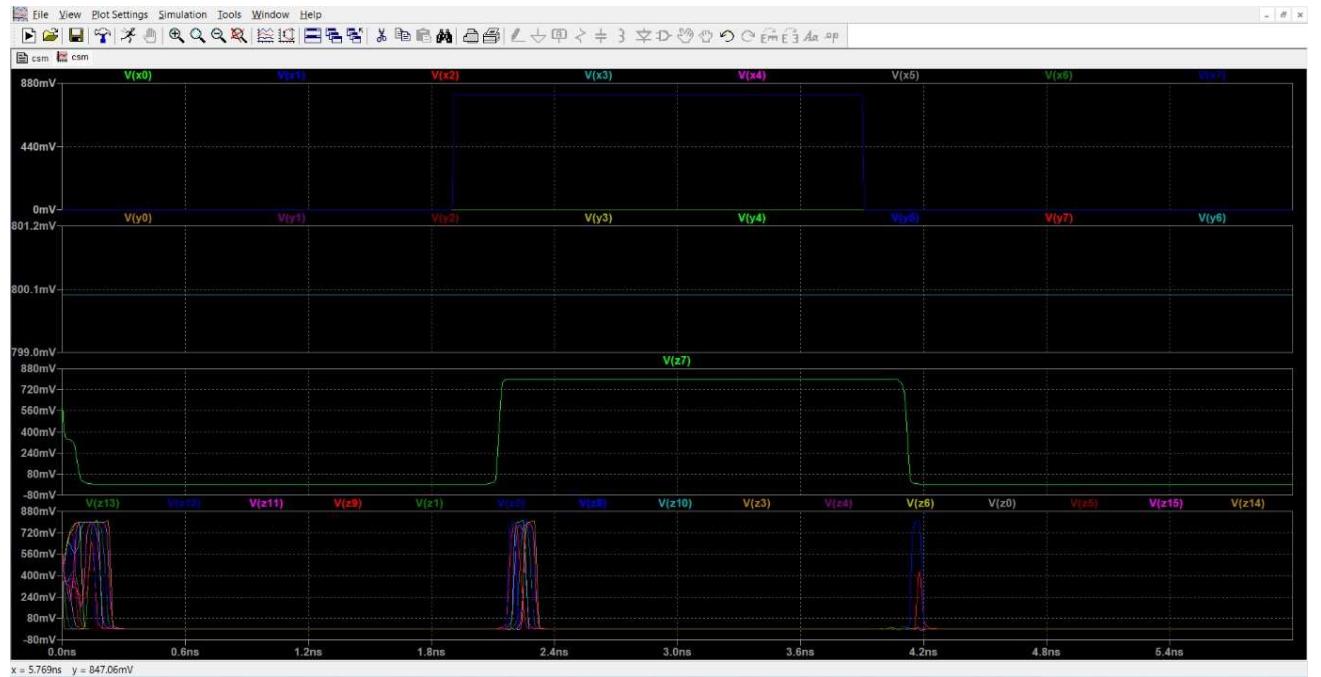
Case-5: A = -11, B = -11



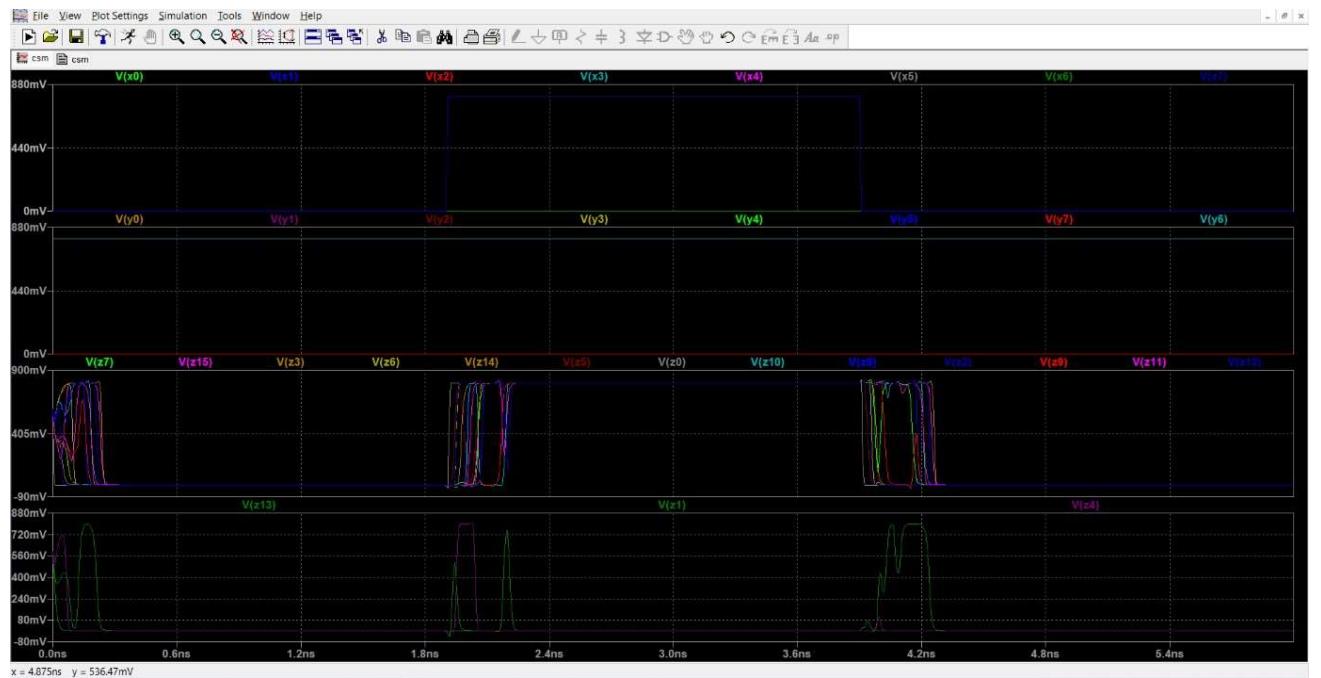
Case-6: A = 127, B = -128



Case-7: A = -128, B = -1

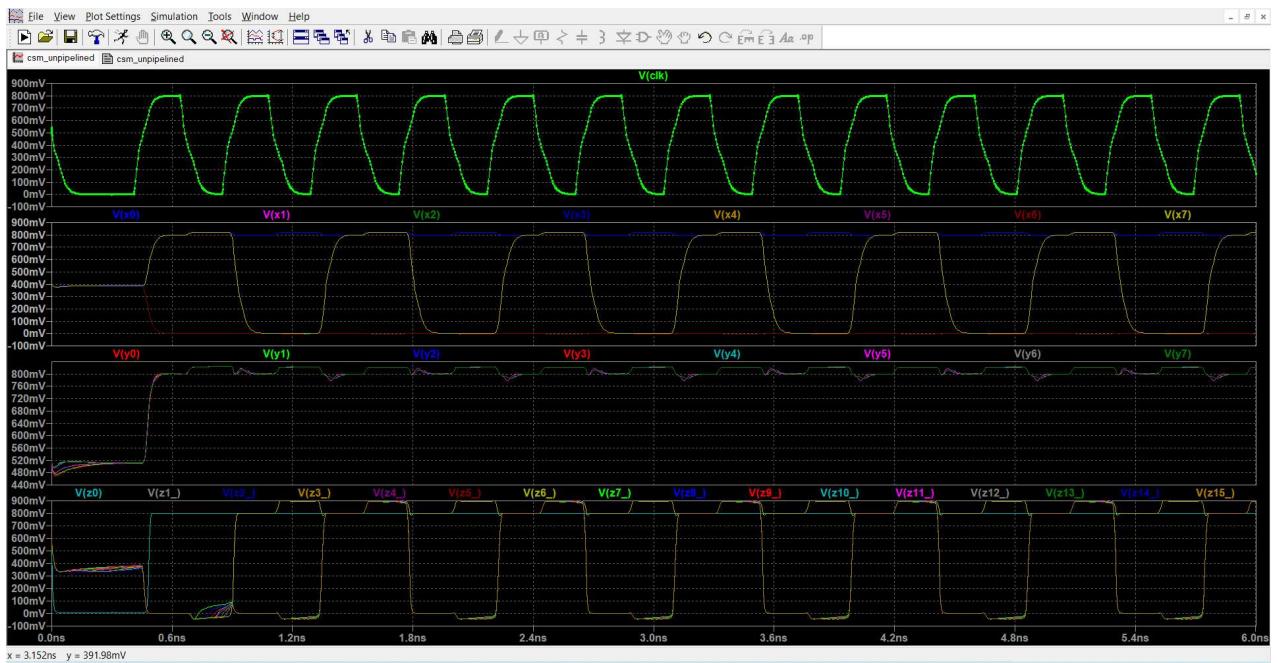


Case-8: A = -69, B = 119

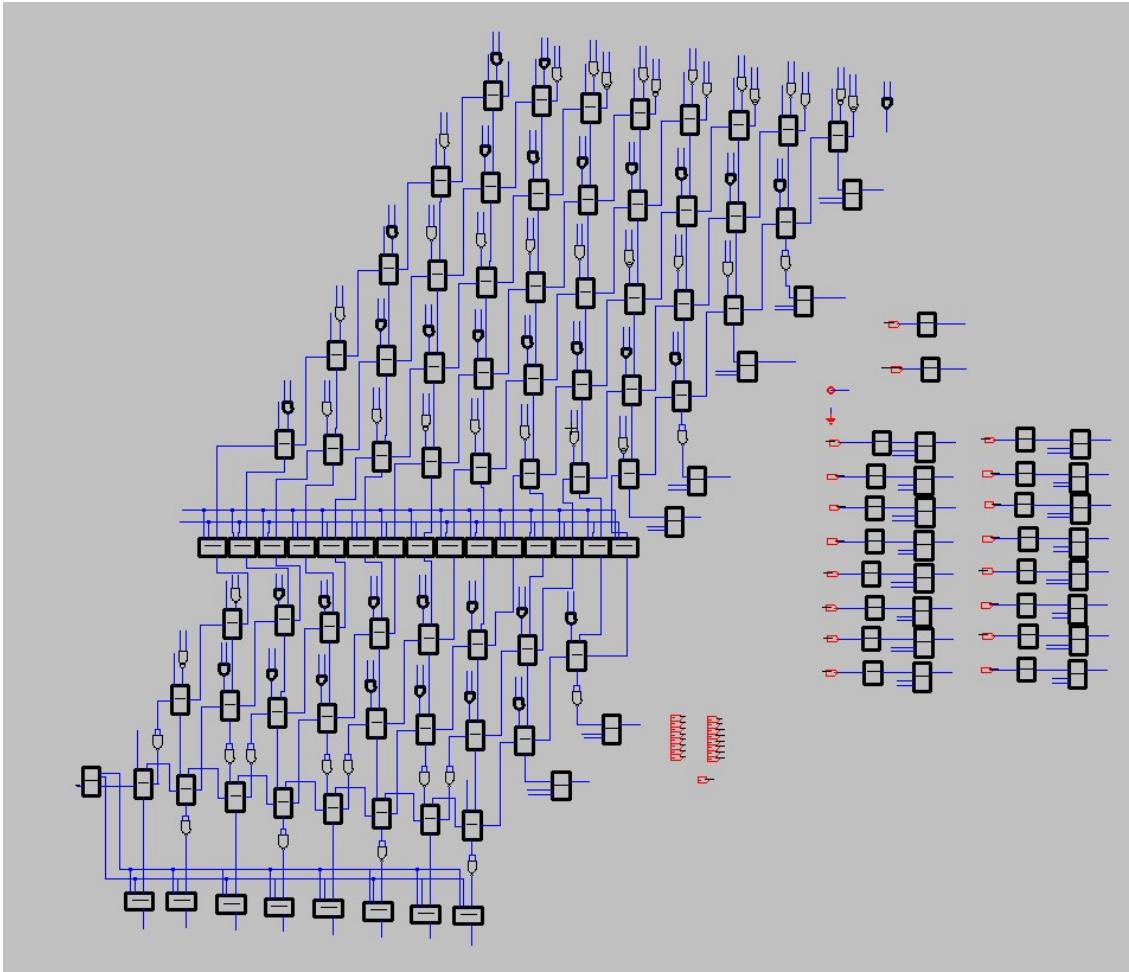


Maximum Operating Frequency of CSM

	Maximum clock frequency (Units:Hz)
Unpipelined CSM (schematic)	2.76E+09
Unpipelined CSM (layout)	1.56E+09

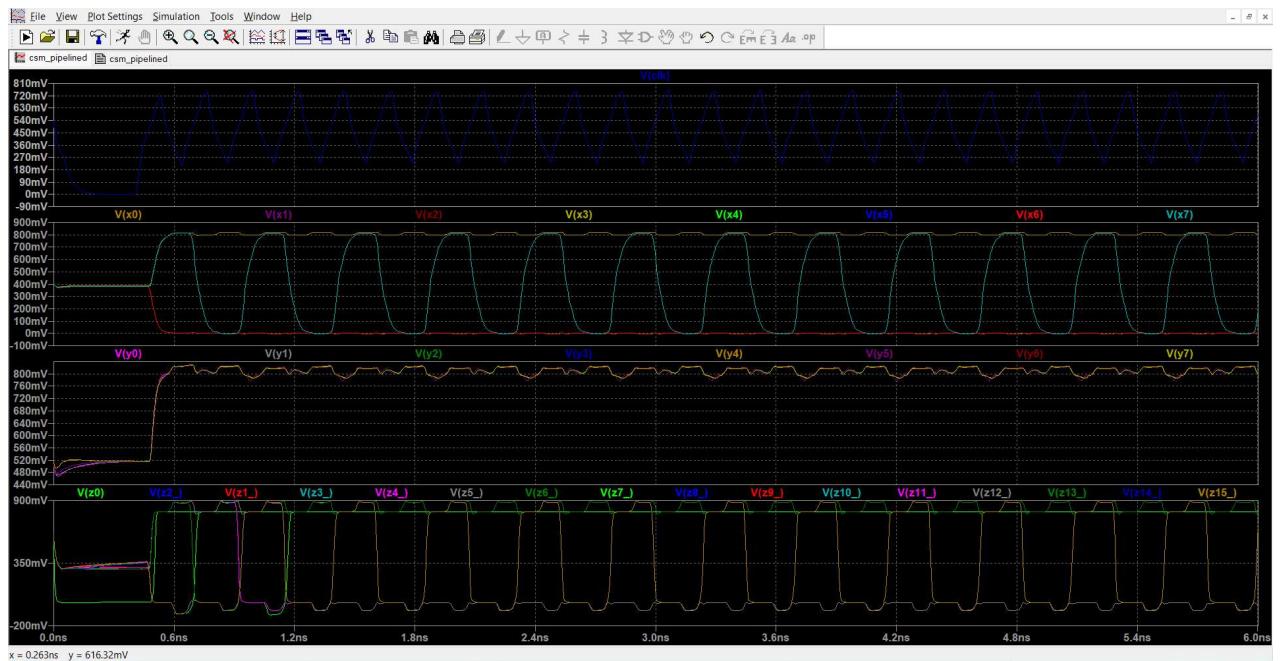


Pipelined CSM Schematic

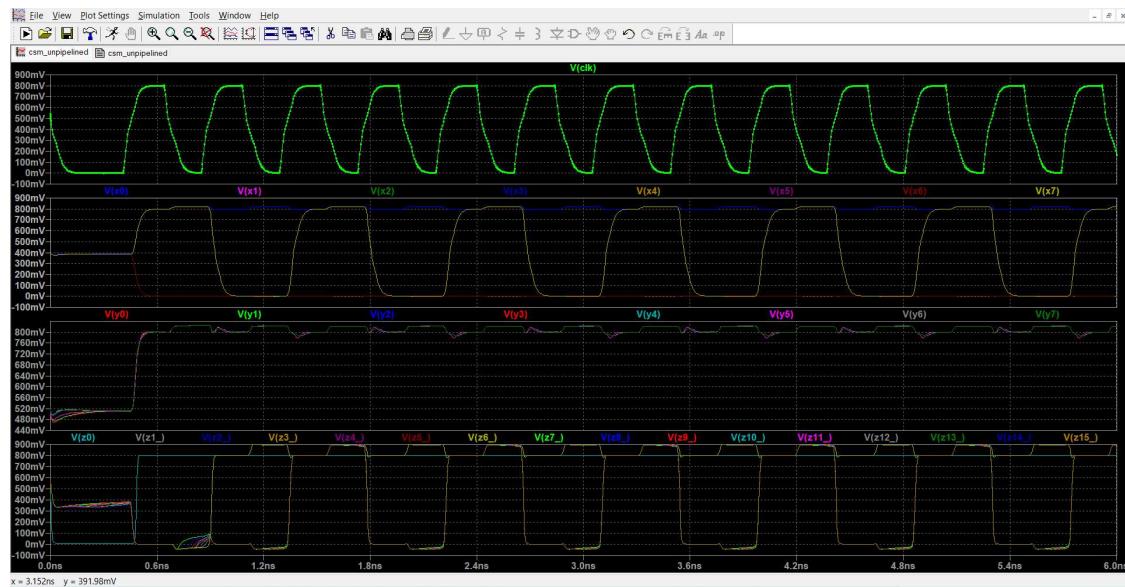


Maximum Clock Frequency with Pipeline (RC-extracted layout)

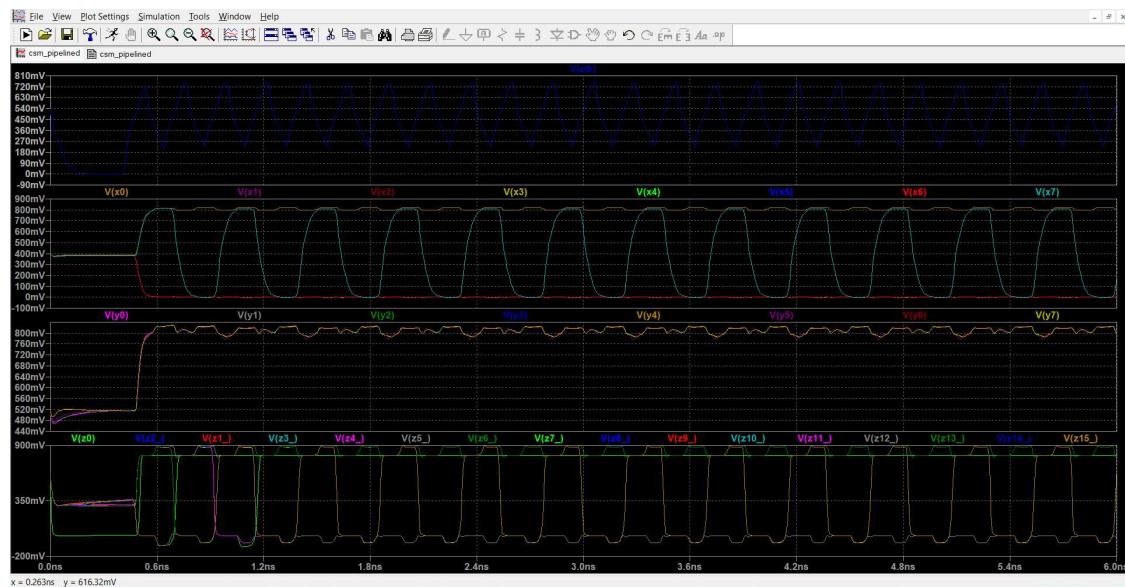
Max Clock Frequency = 5.03E+09 Hz



Comparison between Clock Frequency Spice Simulations of Unpipelined CSM and Pipelined CSM (Without Pipeline)

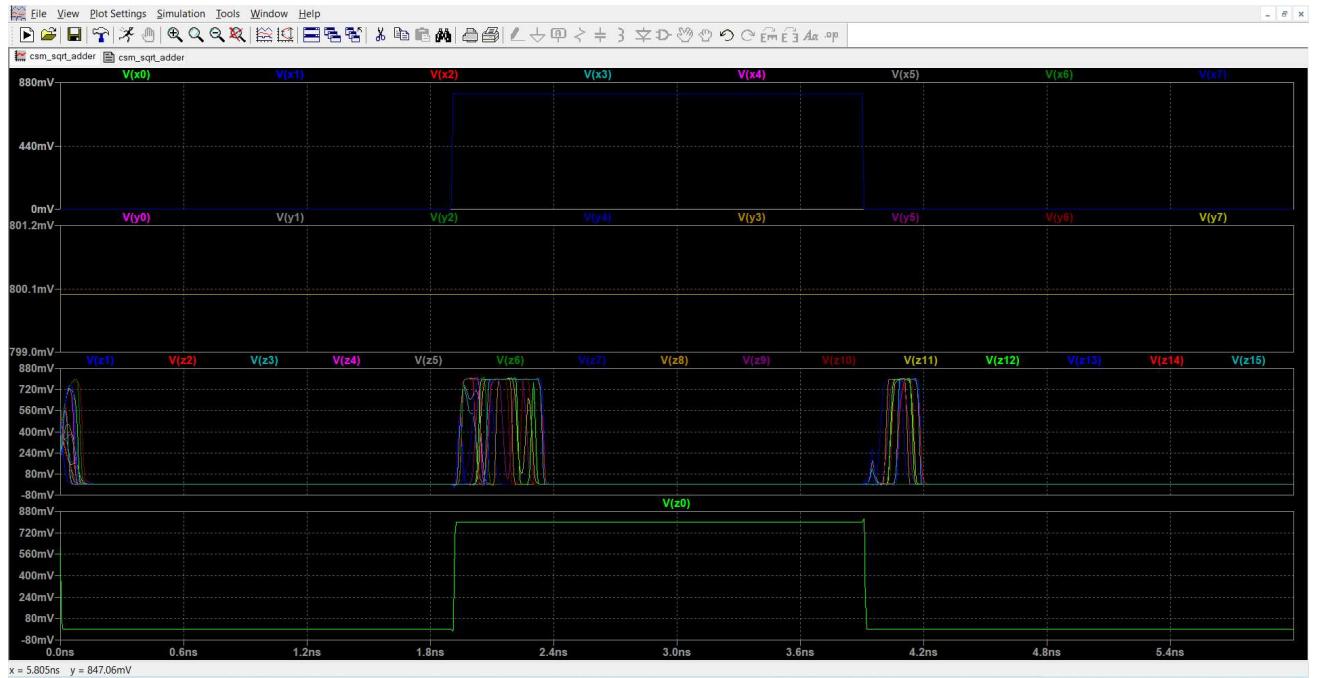


(With Pipeline)

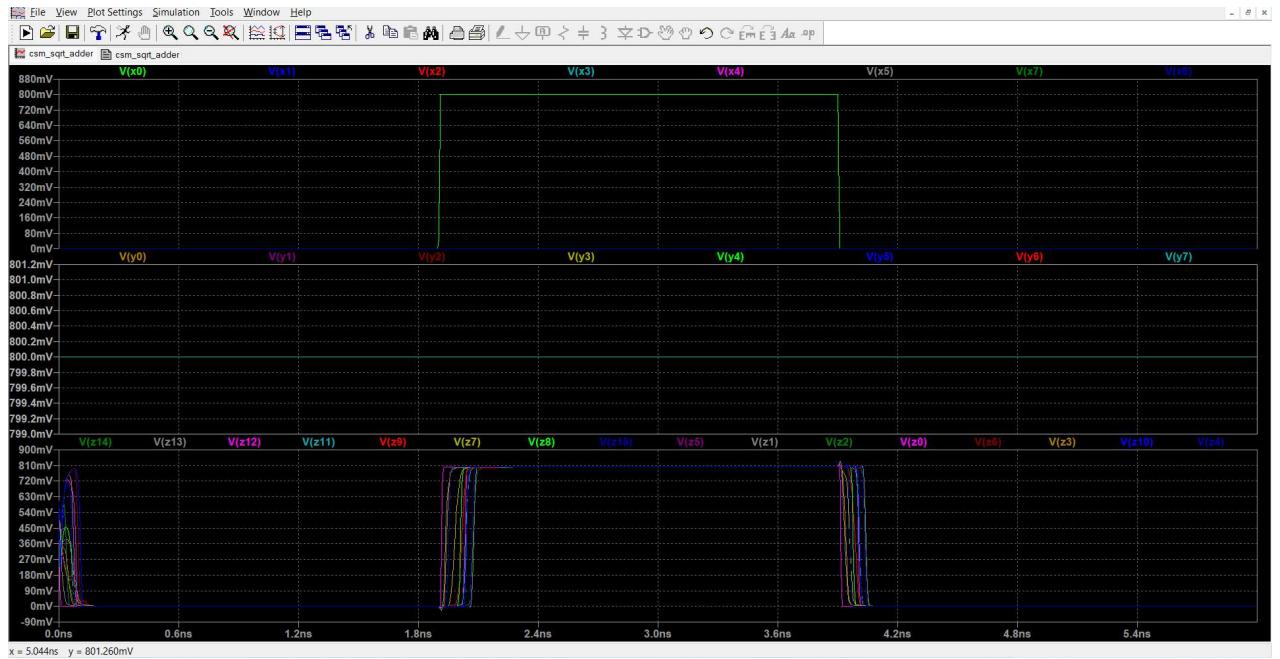


Spice Stimulations Vector Merge Sqrt and Ripple Adders

Case-1: A = -1, B = -1



Case-2: A = -1, B = 1



A (dec)	A (binary)	B (dec)	B (binary)	S (dec)	S (binary)	Sqrt Carry Delay	Ripple Carry Delay
1	00000001	-1	11111111	-1	1111111111111111	1.64E-10	2.07E-10
1	00000001	-128	10000000	-128	1111111100000000	1.67E-10	2.09E-10
17	00010001	28	00011100	476	0000000111011100	2.12E-10	4.67E-11
21	00010101	53	00110101	1113	0000010001011001	2.09E-10	2.14E-10
-11	11110101	-11	11110101	121	0000000001111001	2.36E-10	2.40E-10
127	01111111	-128	10000000	-16256	11000000010000000	1.65E-10	1.48E-10
-128	10000000	-1	11111111	128	00000000010000000	2.22E-10	2.24E-10
-1	11111111	-1	11111111	1	00000000000000001	9.69E-12	9.71E-12