Week 5

Codefest: Going down to physical/transistors (or CLBs) level

ECE 410/510
Spring 2025

Challenge #18

Overview and context:
The goal for this week is to take your HW accelerator design described in a high level HW description language (challenge #15) and to turn it into a physical design by using open-source EDA tools.

Learning goals:

- Synthesize the HW description you generated last week into a physical design description (transistor-level and/or FPGA)
- Install and learn how to use the OpenLane tools.

Suggested tasks:

1. Read through the OpenLane 2 "Newcomers" intro at https://openlane2.readthedocs.io/en/latest/getting_started/newcomers/index.html
2. Getting started with OpenLane 2
    - To check out an example of an OpenLane 2-based flow right in your browser, try the Google Colab™ notebook at https://colab.research.google.com/github/efabless/openlane2/blob/main/notebook.ipynb
    - To set up OpenLane 2 on your computer, check out the Getting Started guide at the following link: https://openlane2.readthedocs.io/en/latest/getting_started/index.html
3. Pick an example design, your own, or one generate by vibe-coding.
4. Try to obtain the maximum operating frequency for your ASIC design.
5. Alternative:
    - Use AMD's Vivado Design Suite to synthesize your design for an FPGA.
    - https://www.amd.com/en/products/software/adaptive-socs-and-fpgas/vivado/vivado-buy.html
    - Obtain the maximum operating frequency for your FPGA design.
6. Use the maximum operating frequency of your design to get a first estimate of the throughput of your accelerator chiplet.