

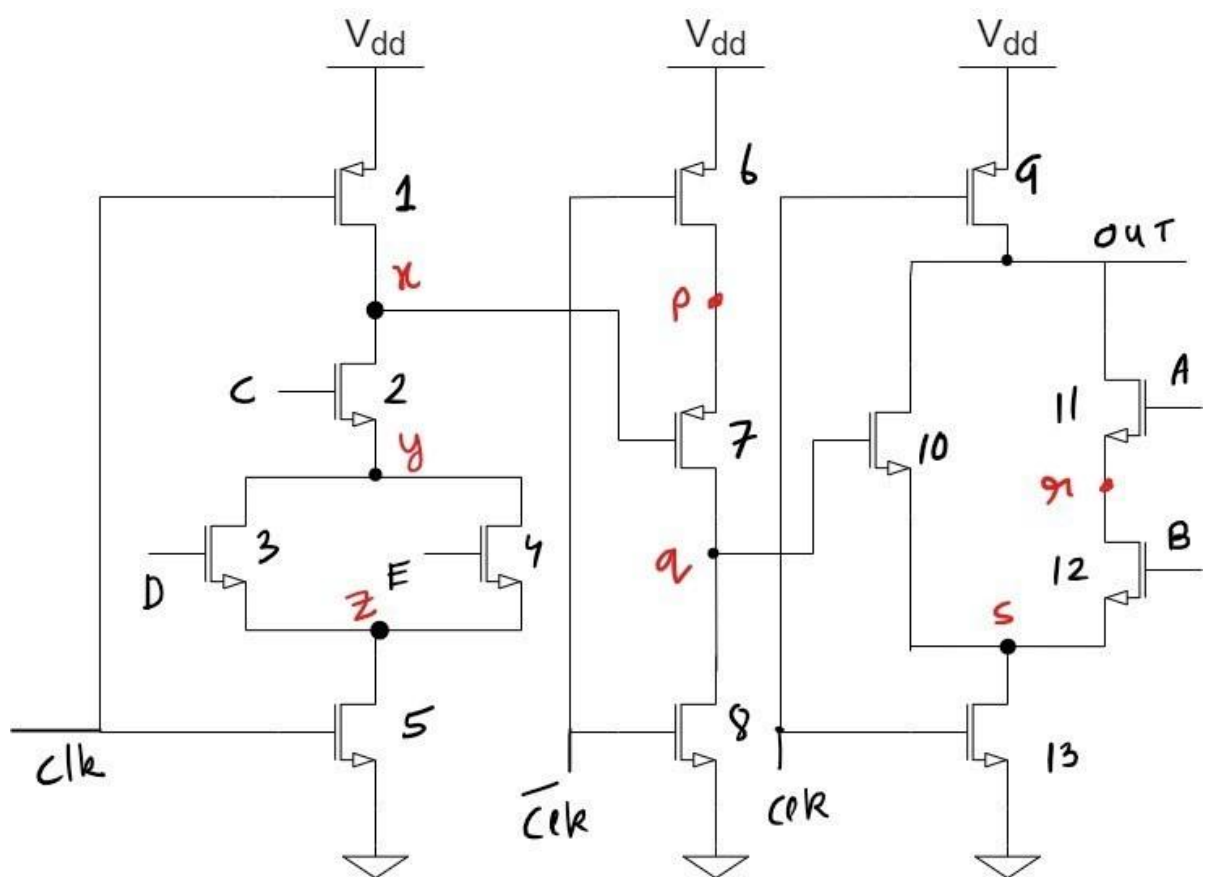
# Design & Layout of Dynamic CMOS logic circuit

BY SATYAKI CHAKRAVORTY

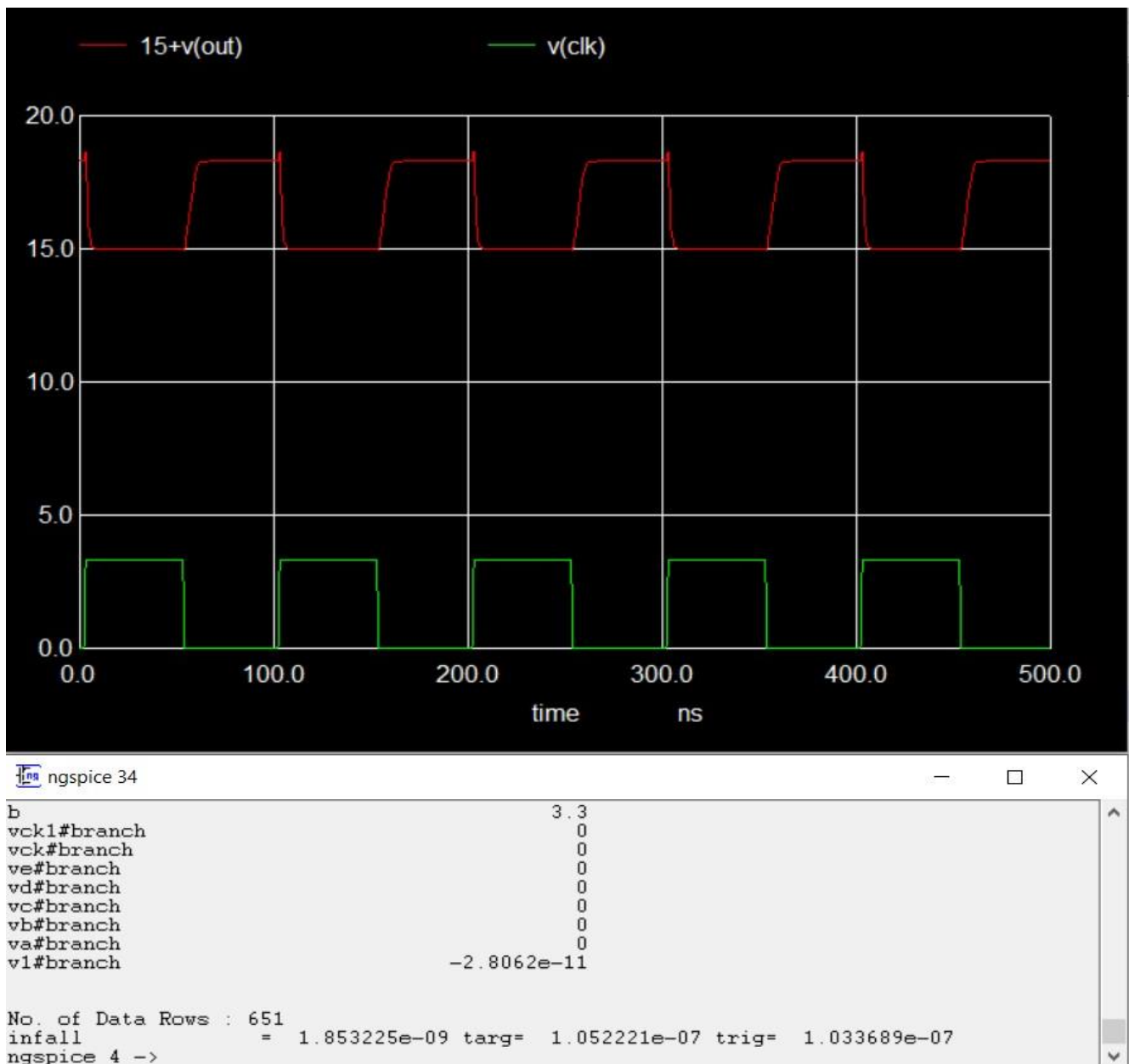
Given logic:  $(AB + C(D+E))'$

Dynamic style used: Zipper Style

## Circuit Diagram



## PRE-LAYOUT SIMULATION

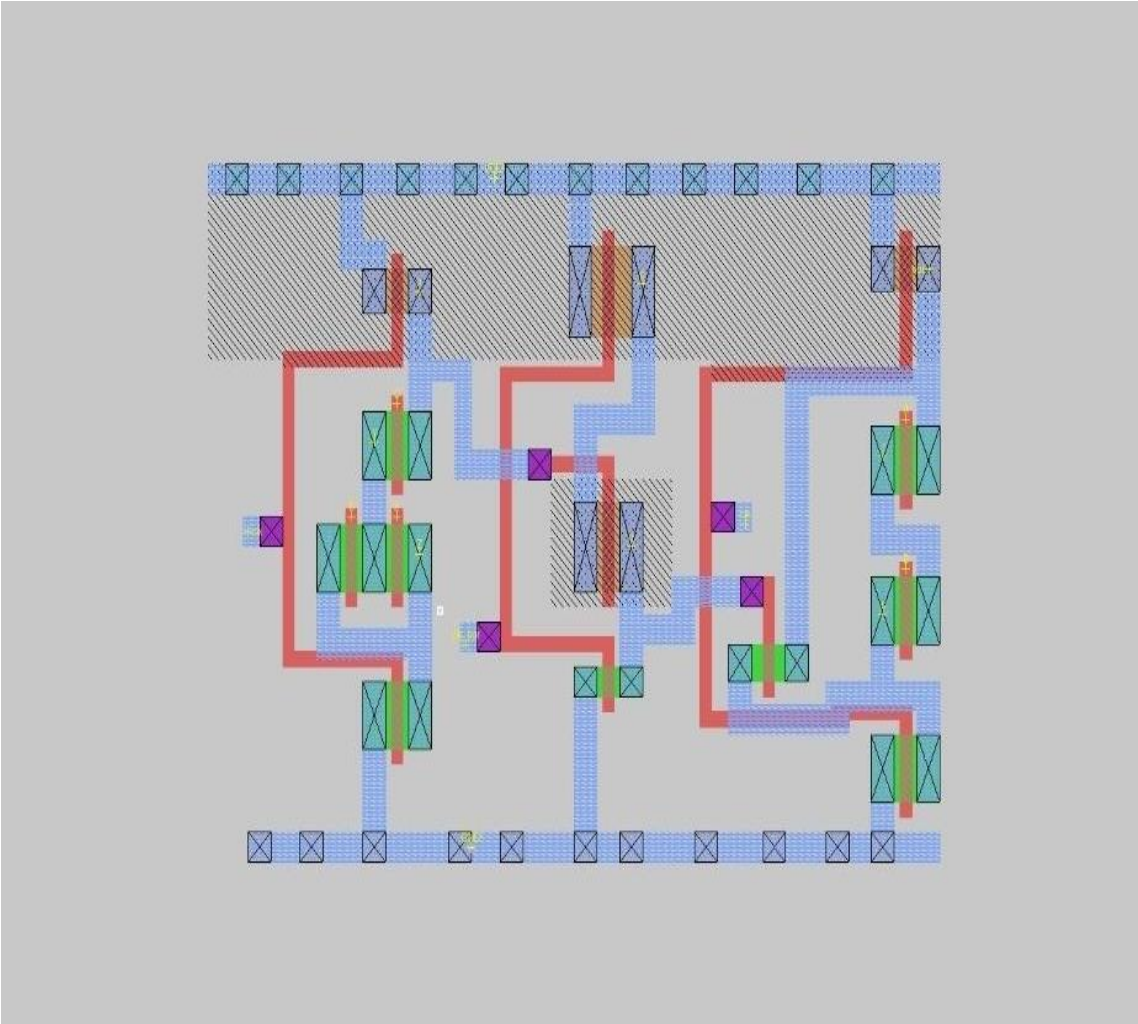


**For Max frequency of operation, input vector chosen:**

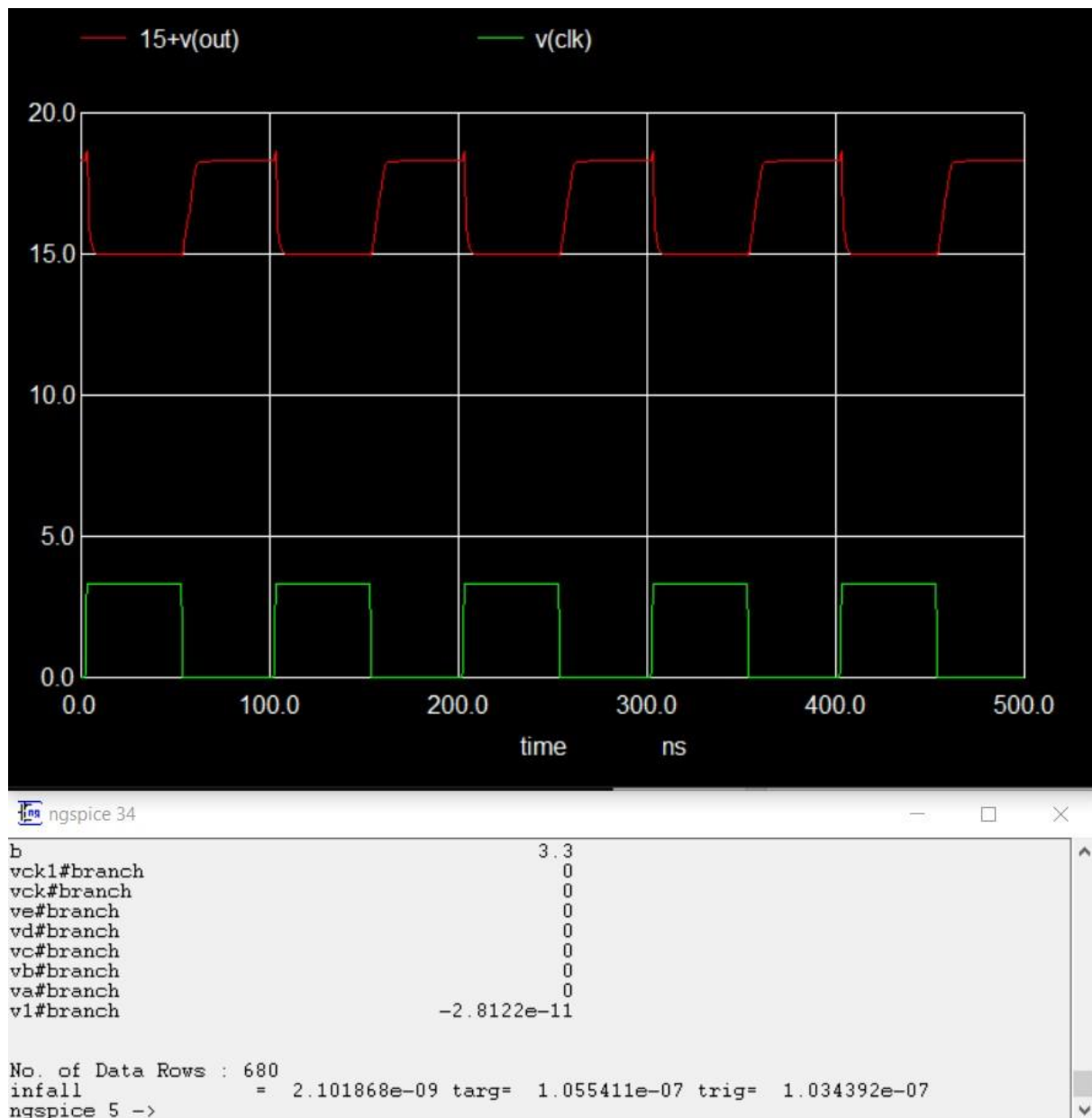
**A=1, B=1, C=0, D=x, E=x as this corresponds to the worst-case condition.**

$$\text{Max Freq} = 1/\text{infall} = \mathbf{539.6 \text{ MHz}}$$

LAYOUT OF THE CIRCUIT



## POST-LAYOUT SIMULATION



**For Max frequency of operation, input vector chosen:**

**A=1,B=1 , C=0, D=x , E=x as this corresponds to the worst case condition.**

$$\text{Max Freq} = 1/\text{infall} = \mathbf{475.7826 \text{ MHz}}$$

**Thus, We can operate at a higher frequency for the pre-simulation case.**