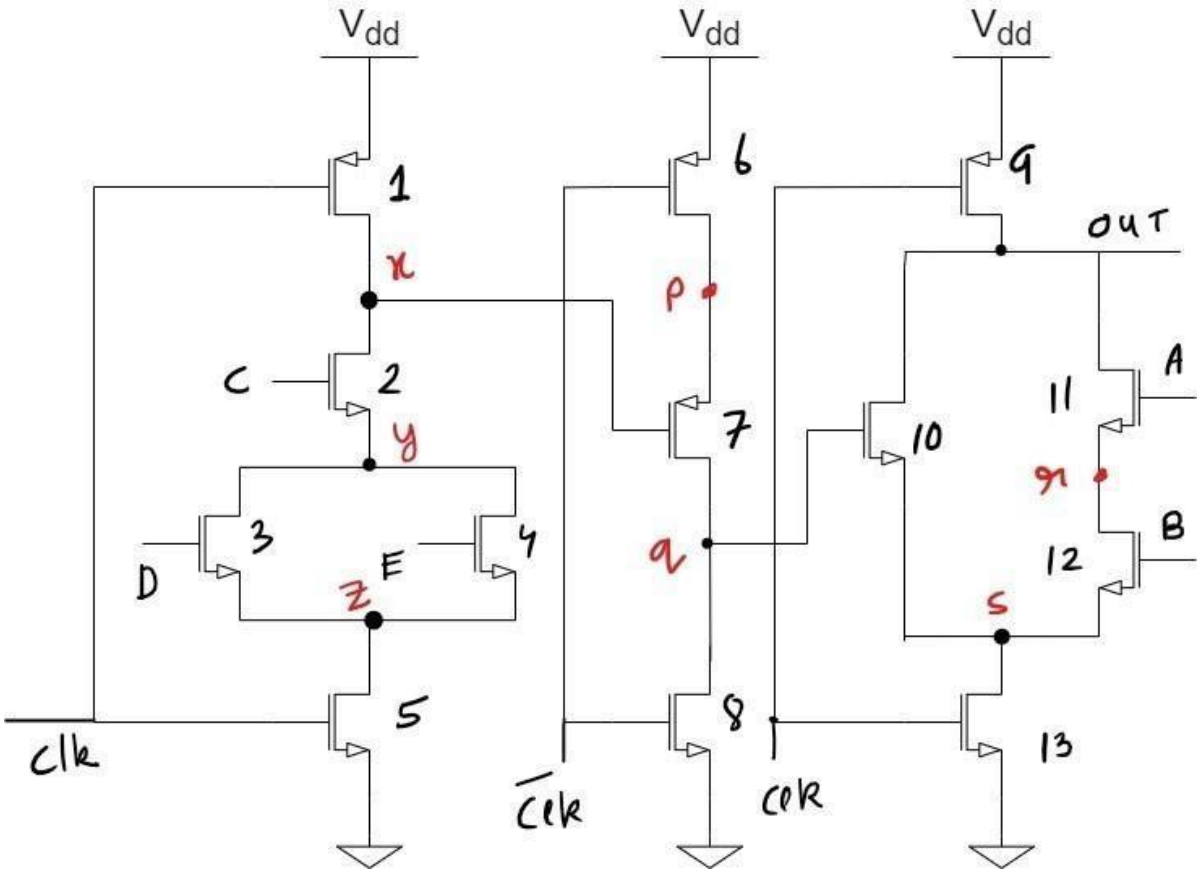
Design & Layout of Dynamic CMOS logic circuit

BY SATYAKI CHAKRAVORTY

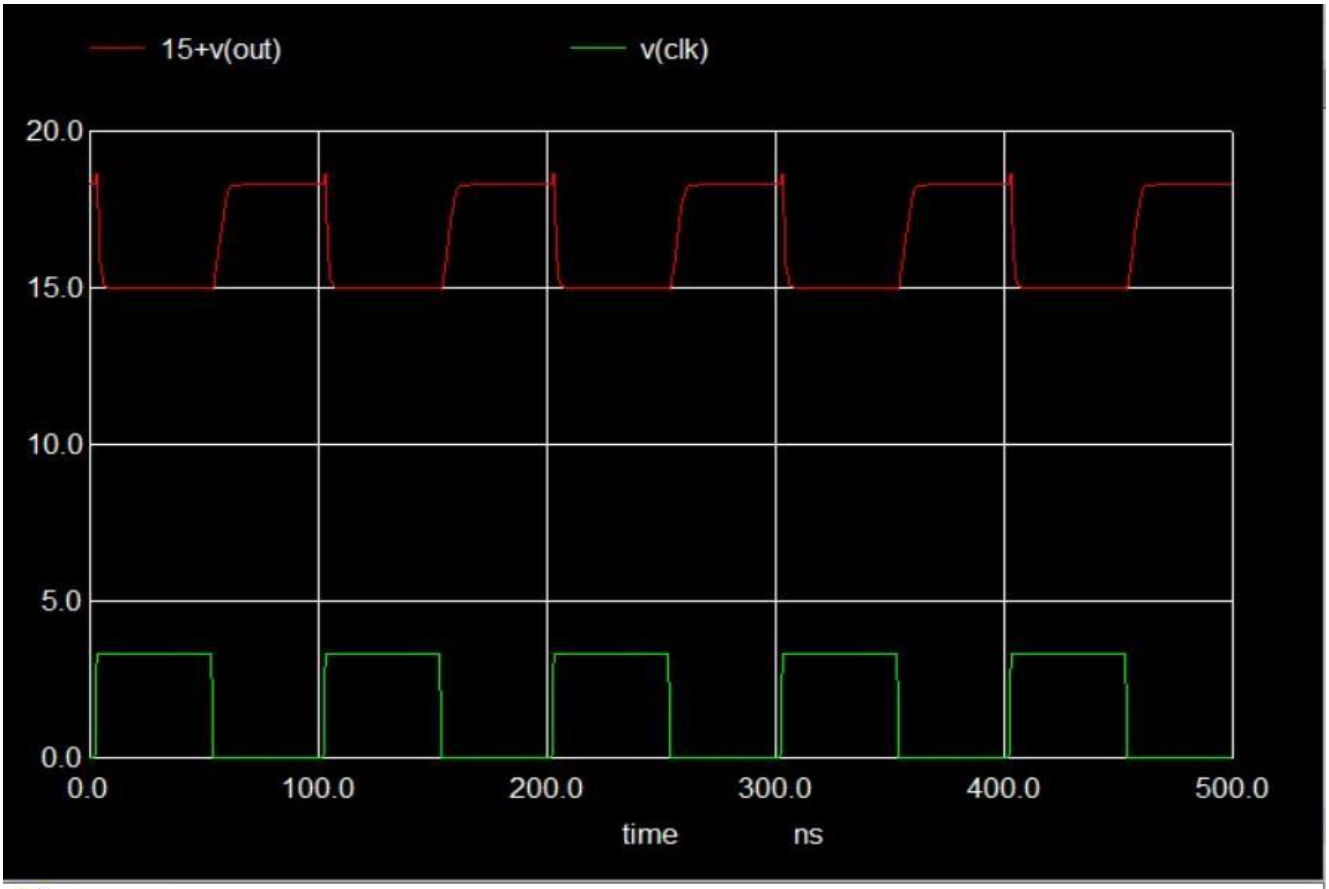
Given logic: (AB+C(D+E))'

Dynamic style used : Zipper Style

Circuit Diagram



PRE-LAYOUT SIMULATION



ngspice 34

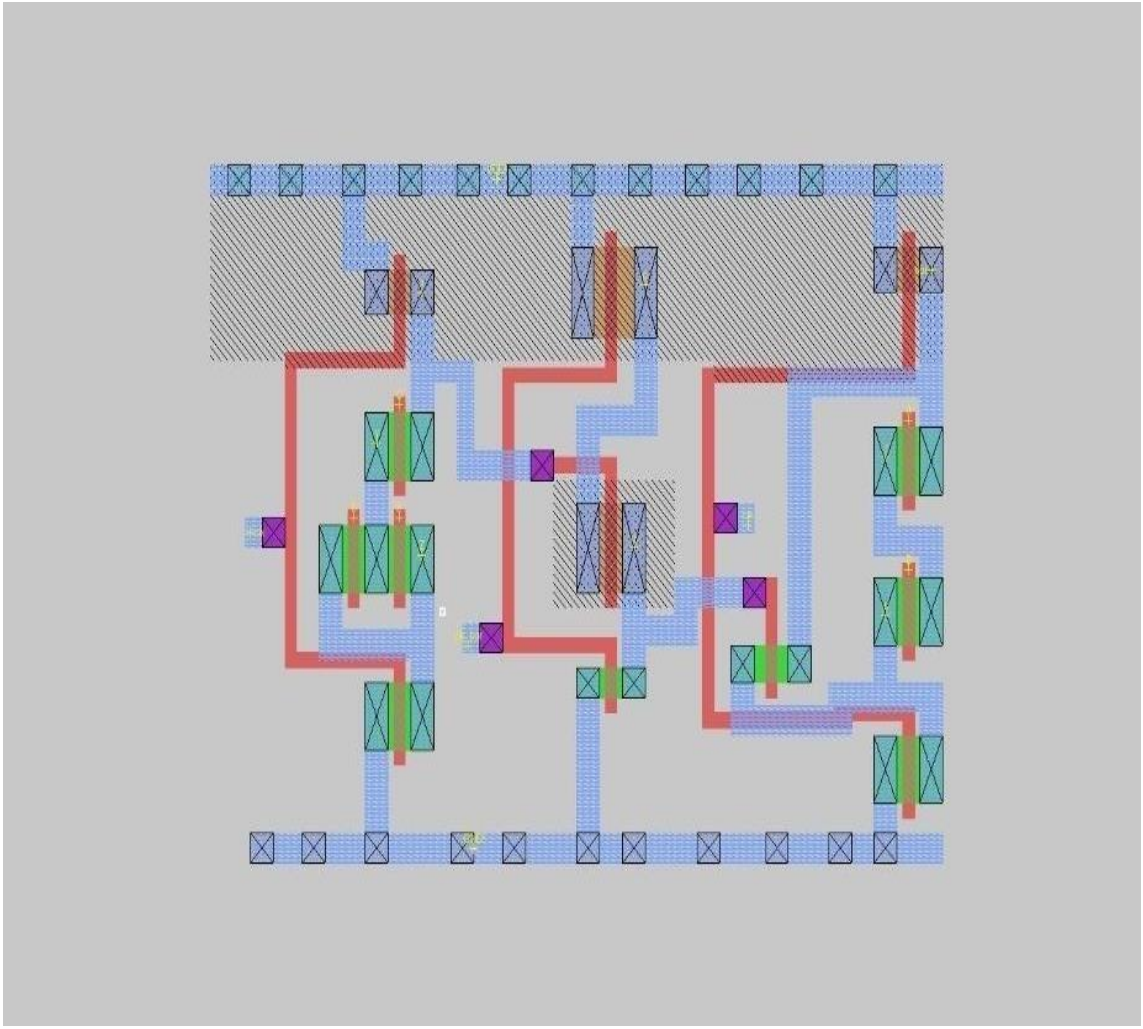
```
b                                    3.3
vck1#branch                            0
vck#branch                             0
ve#branch                              0
vd#branch                              0
vc#branch                              0
vb#branch                              0
va#branch                              0
v1#branch                      -2.8062e-11

No. of Data Rows : 651
infall              =  1.853225e-09 targ=  1.052221e-07 trig=  1.033689e-07
ngspice 4 ->
```

For Max frequency of operation, input vector chosen:

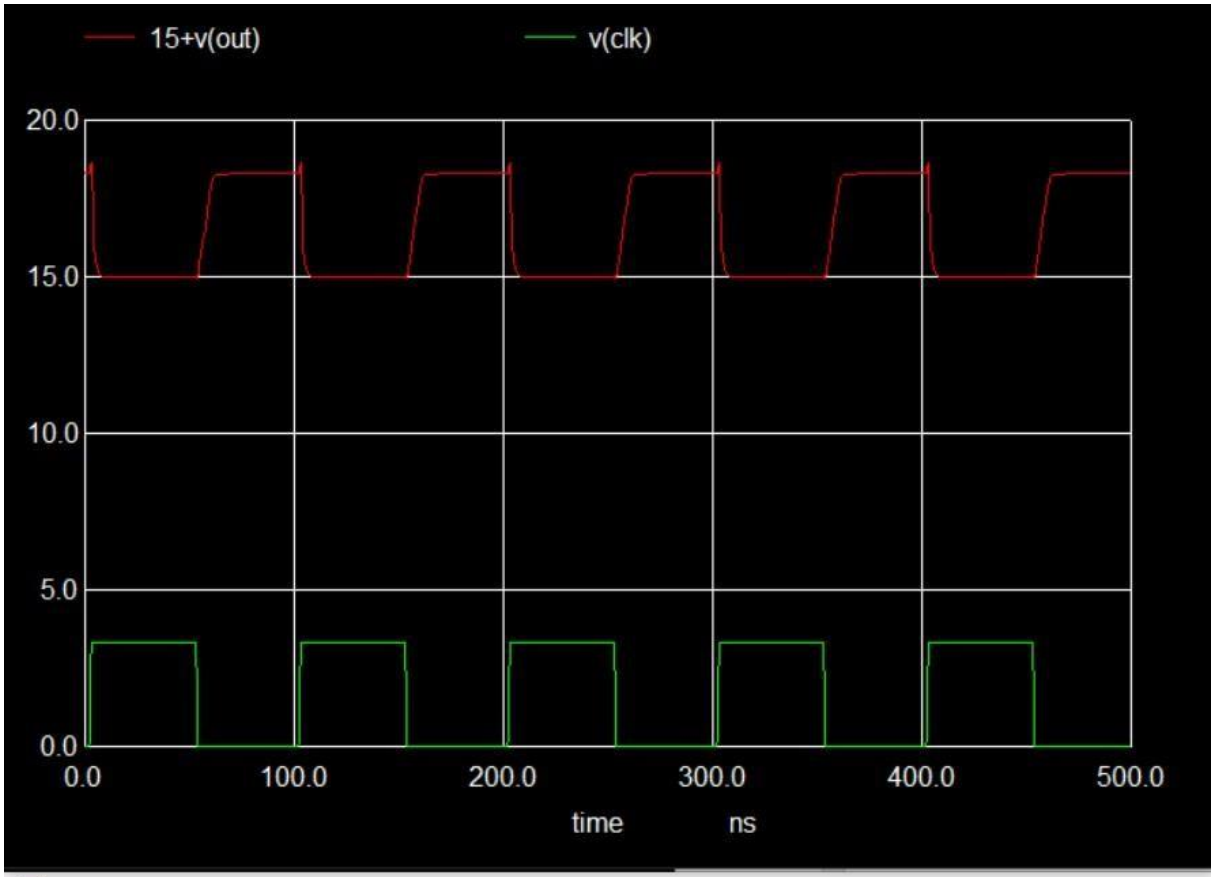
A=1, B=1, C=0, D=x, E=x as this corresponds to the worst-case condition.

Max Freq = 1/infall = 539.6 MHz

LAYOUT OF THE CIRCUIT



POST-LAYOUT SIMULATION



ngspice 34

```
b                                    3.3
vck1#branch                            0
vck#branch                             0
ve#branch                              0
vd#branch                              0
vc#branch                              0
vb#branch                              0
va#branch                              0
v1#branch                      -2.8122e-11


No. of Data Rows : 680
infall                =  2.101868e-09 targ=  1.055411e-07 trig=  1.034392e-07
ngspice 5 ->
```

For Max frequency of operation, input vector chosen:

A=1,B=1 , C=0, D=x , E=x as this corresponds to the worst case condition.

Max Freq = 1/infall = 475.7826 MHz

Thus, We can operate at a higher frequency for the pre-simulation case.