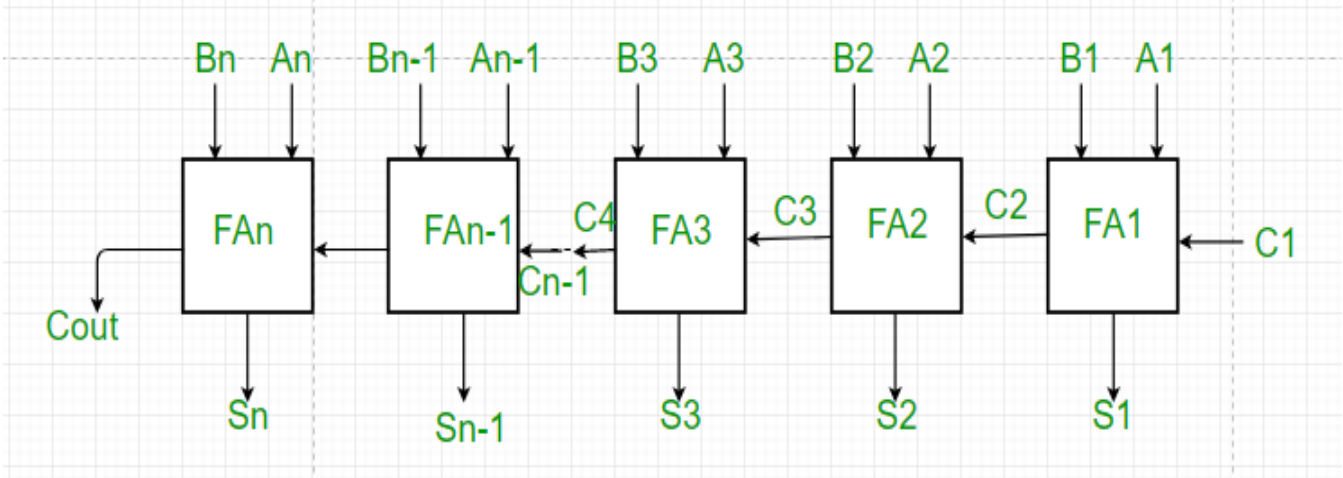
4 - Bit Parallel Adder/Subtractor

Parallel Adder –

A single full adder performs the addition of two one bit numbers and an input carry. But a **Parallel Adder** is a digital circuit capable of finding the arithmetic **sum** of two binary numbers that is **greater than one bit** in length by operating on corresponding pairs of bits in parallel. It consists of **full adders connected in a chain** where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain.
An n bit parallel adder requires n full adders to perform the operation.



Working of parallel Adder –

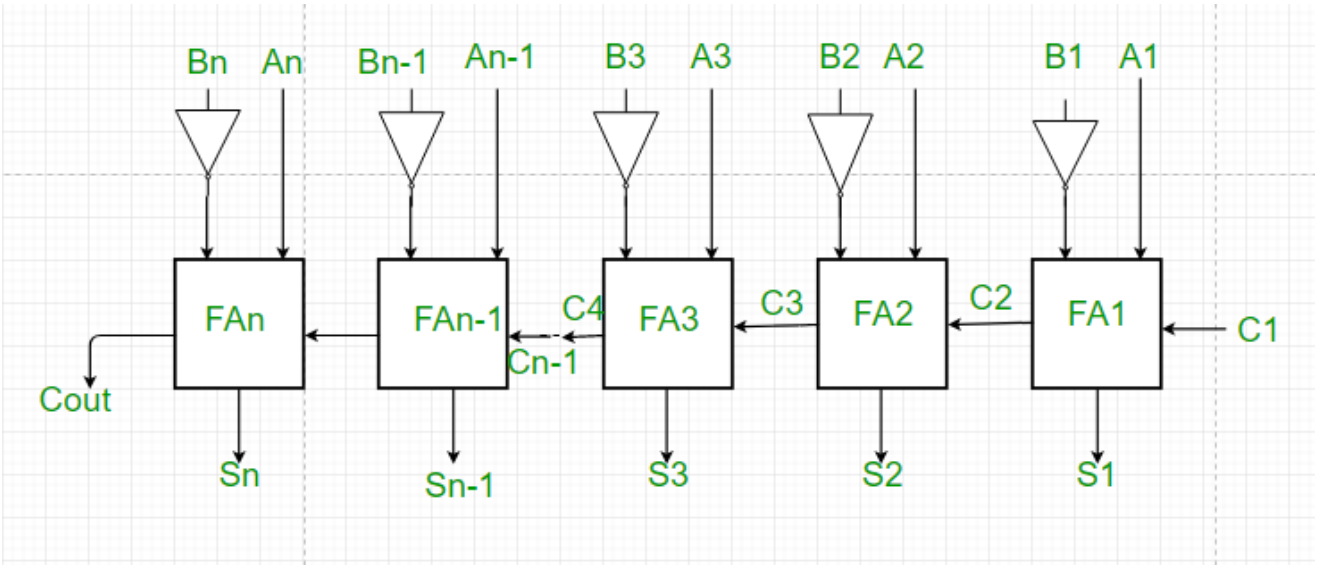
1. As shown in the figure, firstly the full adder FA1 adds A1 and B1 along with the carry C1 (which is 0 for the case of adding two bits) to generate the sum S1 (the first bit of the output sum) and the carry C2 which is connected to the next adder in chain.
2. Next, the full adder FA2 uses this carry bit C2 to add with the input bits A2 and B2 to generate the sum S2(the second bit of

the output sum) and the carry C3 which is again further connected to the next adder in chain and so on.

3. The process continues till the last full adder FA_n uses the carry bit C_n to add with its input A_n and B_n to generate the last bit of the output along last carry bit C_out.

Parallel Subtractor –

A Parallel Subtractor is a digital circuit capable of finding the arithmetic difference of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel. The parallel subtractor can be designed in several ways including combination of half and full subtractors, all full subtractors or all full adders with subtrahend complement input.



Working of Parallel Subtractor –

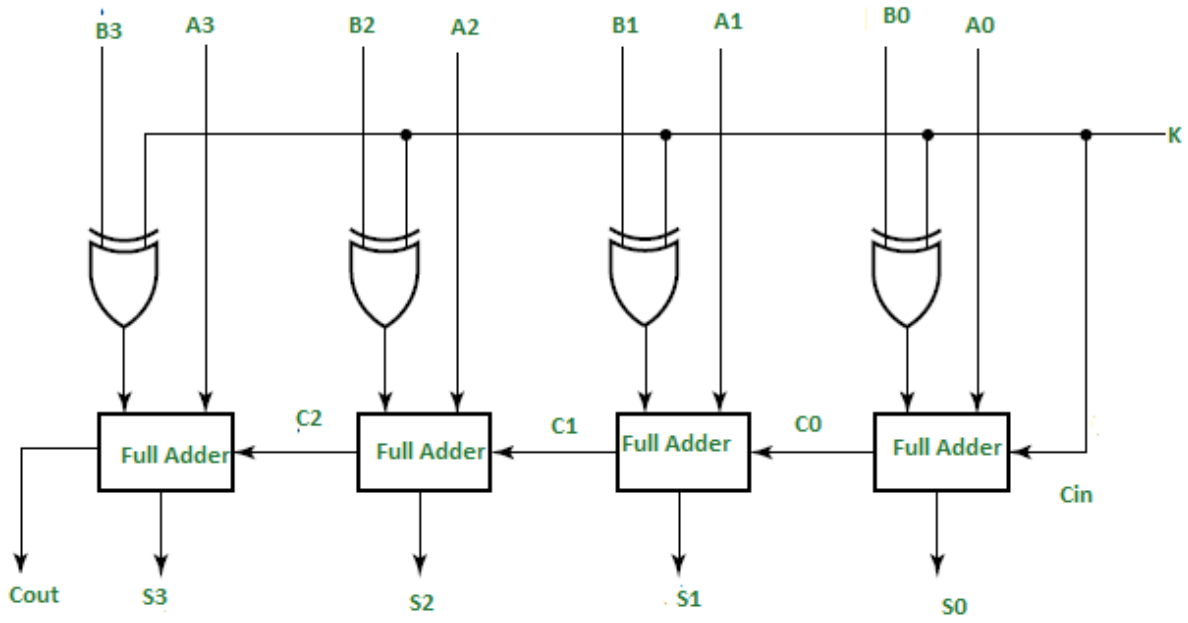
1. As shown in the figure, the parallel binary subtractor is formed by combination of all full adders with subtrahend complement input.
2. This operation considers that the addition of minuend along with the 2's complement of the subtrahend is equal to their subtraction.
3. Firstly the 1's complement of B is obtained by the NOT gate and 1 can be added through the carry to find out the 2's complement of B. This is further added to A to carry out the arithmetic subtraction.
4. The process continues till the last full adder FA_n uses the carry bit C_n to add with its input A_n and 2's complement of B_n to generate the last bit of the output along last carry bit C_out.

In Digital Circuits, A **Binary Adder-Subtractor** is one which is capable of both addition and subtraction of binary numbers in one circuit itself. The operation being performed depends upon the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Unit).
Lets consider two 4-bit binary numbers A and B as inputs to the Digital Circuit for the operation with digits

A0 A1 A2 A3 for A

B0 B1 B2 B3 for B

The circuit consists of 4 full adders since we are performing operation on 4-bit numbers. There is a control line K that holds a binary value of either 0 or 1 which determines that the operation being carried out is addition or subtraction.



Example:

Lets take two 3 bit numbers A=1011 and B=0101 and input them in the full adder with both values of control lines.

For K=0:

B0(exor)K=B0 and C0=K=0

Thus from first full adder

= A0+B0

= 1+1

= 10,

S0=0

C1=1

Similarly,

S1=0 with C1=1

S2=0 with C2=1, and

S3=0 with C3=1

Thus,

A = 1011 =11

B = 0101 = 5

Sum = 10000 = 16

For K=1

B0(exor)K=B0' and C0=k=1

Thus from first full adder

= A0+B0(exor)K+1

= A0+B0’+1

= 1+0+1

= 10,

S0=0 and C1=1

Similarly,

S1=1 and C1=1

S2=1 and C2=0

S3=0 and C3 = 1

In 2’s complement method of subtraction, if C3=1 then it is discarded bit, and answer is the four bits obtained.

And if C3 = 0 then the answer is the 2’s complement of obtained sum which is a negative number.

Thus,

A = 1011 = 11

B = 0101 = 5

Difference = 0110 = 6.

Advantages of parallel Adder/Subtractor –

1. The parallel adder/subtractor performs the addition operation faster as compared to serial adder/subtractor.
2. Time required for addition does not depend on the number of bits.
3. The output is in parallel form i.e all the bits are added/subtracted at the same time.
4. It is less costly.

Disadvantages of parallel Adder/Subtractor –

1. Each adder has to wait for the carry which is to be generated from the previous adder in chain.
2. The propagation delay(delay associated with the travelling of carry bit) is found to increase with the increase in the number of bits to be added.

Links/Resources :

https://www.geeksforgeeks.org/4-bit-binary-adder-subtractor/
https://www.geeksforgeeks.org/parallel-adder-and-parallel-subtractor/
https://www.electrical4u.com/parallel-adder-or-subtractor/

-Report by, Satyam Kumar