Parity Generator and Parity Check

A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word.

What is Parity Bit?

The parity generating technique is one of the most widely used error detection techniques for the data transmission. In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s.

Hence, ***parity bit*** is added to the word containing data in order to make number of 1s either even or odd. Thus it is used to detect errors , during the transmission of binary data .The message containing the data bits along with parity bit is transmitted from transmitter node to receiver node.

At the receiving end, the number of 1s in the message is counted and if it doesn't match with the transmitted one, then it means there is an error in the data.

The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always zero. Such error detecting and correction can be implemented by using Ex-OR gates

Even Parity Generator

In **even parity** bit scheme, the parity bit is '**0**' if there are **even number of 1s** in the data stream and the parity bit is '**1**' if there are **odd number of 1s** in the data stream.

Let us assume that a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuits and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

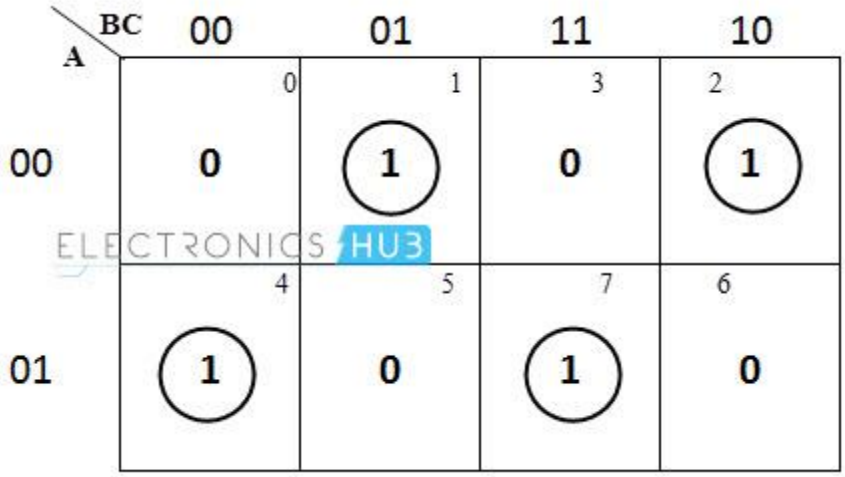
The figure below shows the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

0 0 0 – In this input binary code the even parity is taken as '0' because the input is already in even parity, so no need to add even parity once again for this input.
0 0 1 – – In this input binary code there is only a single number of '1' and that single number of '1' is an odd number of '1'. If an odd number of '1' is there, then even parity generator must generate another '1' to make it

as even parity, so even parity is taken as 1 to make the 0 0 1 code into even parity.
0 1 0 – This bit is in odd parity so even parity is taken as 1 to make the 0 1 0 code into even parity.
0 1 1 – This bit is already in even parity so even parity is taken as 0 to make the 0 1 1 code into even parity.
1 0 0 – This bit is in odd parity so even parity is taken as 1 to make the 1 0 0 code into even parity.
1 0 1 – This bit is already in even parity so even parity is taken as 0 to make the 1 0 1 code into even parity.
1 1 0 – This bit is also in even parity so even parity is taken as 0 to make the 1 1 0 code into even parity.
1 1 1 – This bit is in odd parity so even parity is taken as 1 to make the 1 1 1 code into even parity.

The K-map simplification for 3-bit message even parity generator is shown below.



From the above truth table, the simplified expression of the parity bit can be written as

$$P = \bar{A}\,\bar{B}\,C + \bar{A}\,B\,\bar{C} + A\,\bar{B}\,\bar{C} + A\,B\,C$$

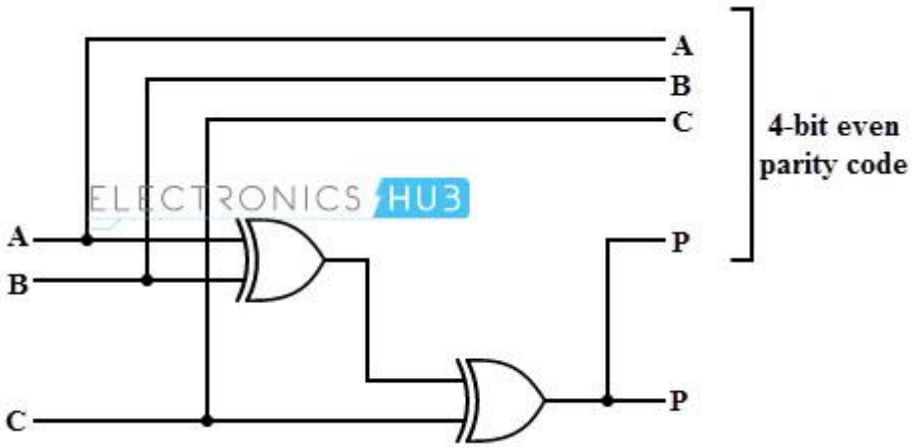
$$= \bar{A}\,(\bar{B}\,C + B\,\bar{C}) + A\,(\bar{B}\,\bar{C} + B\,C)$$

$$= \bar{A}\,(B \oplus C) + A\,(\overline{B \oplus C})$$

$$P = A \oplus B \oplus C$$

The above expression can be implemented by using two Ex-OR gates.

The logic diagram of even parity generator with two Ex – OR gates is shown below.



The three bit message along with the parity generated by this circuit which is transmitted to the receiving end where parity checker circuit checks whether any error is present or not.

To generate the even parity bit for a 4-bit data, three Ex-OR gates are required to add the 4-bits and their sum will be the parity bit.

Odd Parity Generator

In **odd parity** bit scheme, the parity bit is '**1**' if there are **even number of 1**s in the data stream and the parity bit is '**0**' if there are **odd number of 1s** in the data stream.

Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.

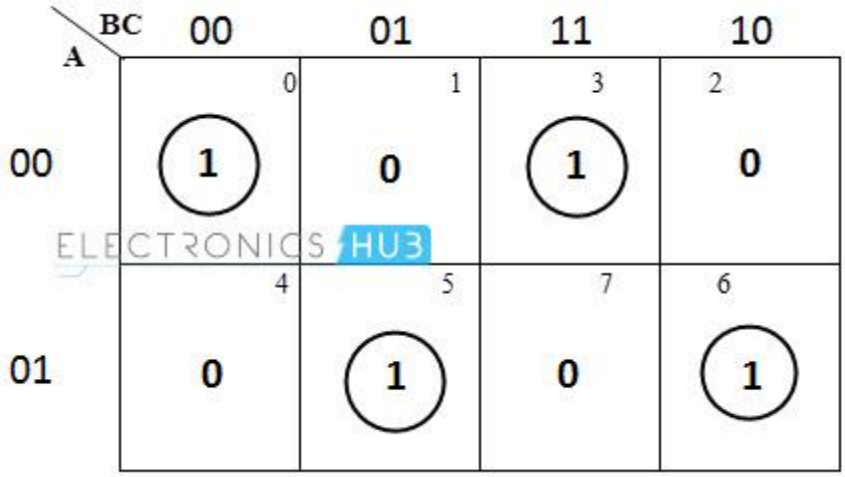
In the given truth table below, 1 is placed in the parity bit in order to make the total number of bits odd when the total number of 1s in the truth table is even.

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

0 0 0 – In this input binary code the odd parity is taken as '1' because the input is in even parity.
0 0 1 – This binary input is already in odd parity, so odd parity is taken as 0.
0 1 0 – This binary input is also in odd parity, so odd parity is taken as 0.

0 1 1 – This bit is in even parity so odd parity is taken as 1 to make the 0 1 1 code into odd parity.
1 0 0 – This bit is already in odd parity, so odd parity is taken as 0 to make the 1 0 0 code into odd parity.
1 0 1 – This input bit is in even parity, so odd parity is taken as 1 to make the 1 0 1 code into odd parity.
1 1 0 – This bit is in even parity, so odd parity is taken as 1.
1 1 1 – This input bit is in odd parity, so odd parity is taken as o.

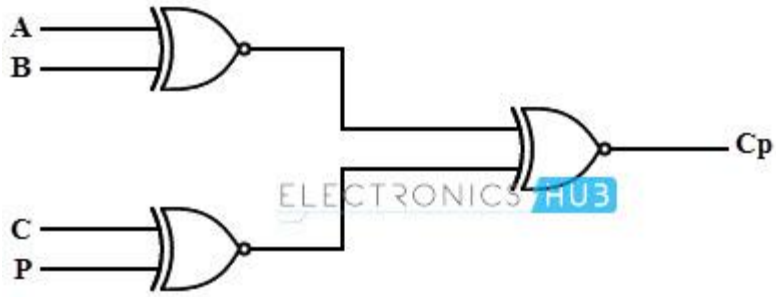
The truth table of the odd parity generator can be simplified by using K-map as shown.



The output parity bit expression for this generator circuit is obtained as

$$P = A \oplus B \text{ Ex-NOR } C$$

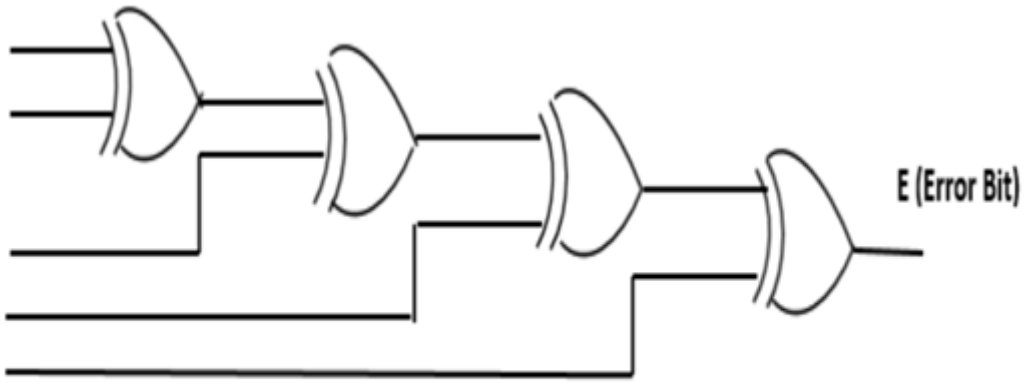
The above Boolean expression can be implemented by using one Ex-OR gate and one Ex-NOR gate in order to design a 3-bit odd parity generator.



Parity Check

It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as even parity checker, the number of input bits must always be even.

When a parity error occurs, the 'sum even' output goes low and 'sum odd' output goes high. If this logic circuit is used as an odd parity checker, the number of input bits should be odd, but if an error occurs the 'sum odd' output goes low and 'sum even' output goes high.



Even Parity Checker

In even parity checker if the error bit (E) is equal to '1', then we have an error. If error bit E=0 then indicates there is no error.

Error Bit (E) =1, error occurs

Error Bit (E) =0, no error

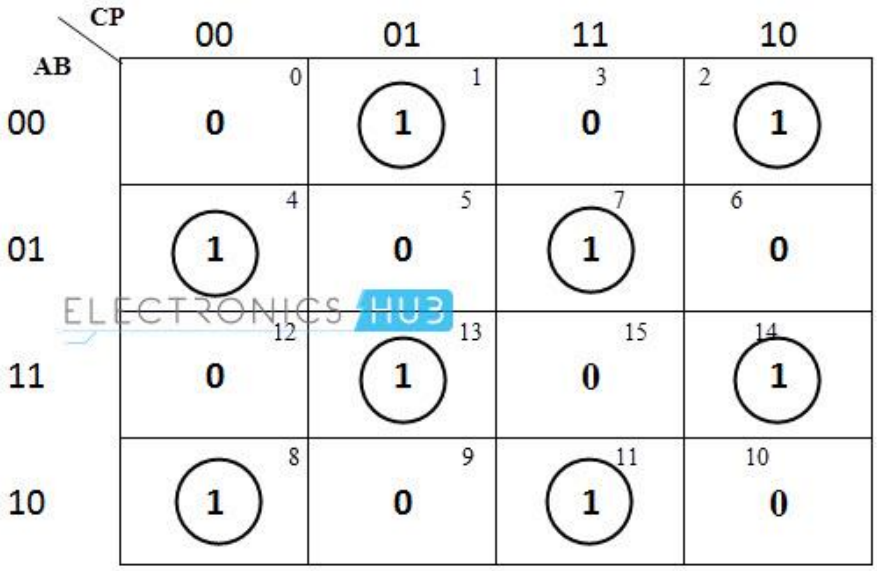
Consider that three input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s.

If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check).

The below table shows the truth table for the even parity checker in which PEC = 1 if the error occurs, i.e., the four bits received have odd number of 1s and PEC = 0 if no error occurs, i.e., if the 4-bit message has even number of 1s.

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

The above truth table can be simplified using K-map as shown below.



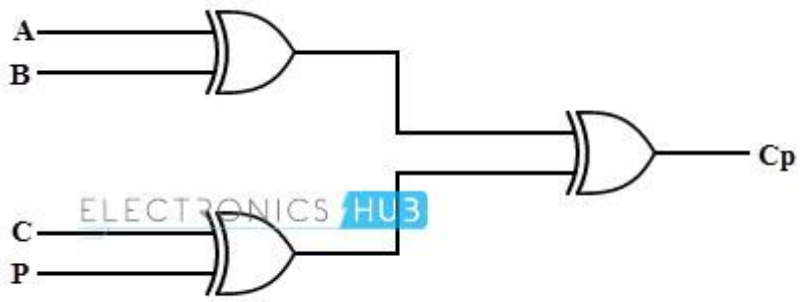
$$PEC = \bar{A}\,\bar{B}\,(\bar{C}\,D + C\,\bar{D}) + \bar{A}\,B\,(\bar{C}\,\bar{D} + C\,D) + A\,B\,(\bar{C}\,D + C\,\bar{D}) + A\,\bar{B}\,(\bar{C}\,\bar{D} + C\,D)$$

$$= \bar{A}\,\bar{B}\,(C \oplus D) + \bar{A}\,B\,(\overline{C \oplus D}) + A\,B\,(C \oplus D) + A\,\bar{B}\,(\overline{C \oplus D})$$

$$= (\bar{A}\,\bar{B} + A\,B)\,(C \oplus D) + (\bar{A}\,B + A\,\bar{B})\,(\overline{C \oplus D})$$

$$= (A \oplus B) \oplus (C \oplus D)$$

The above logic expression for the even parity checker can be implemented by using three Ex-OR gates as shown in figure. If the received message consists of five bits, then one more Ex-OR gate is required for the even parity checking.



Odd Parity Checker

In odd parity checker if an error bit (E) is equal to '1', then it indicates there is no error. If an error bit E=0 then indicates there is an error.

Error Bit (E) =1, no error

Error Bit (E) =0, error occurs

Consider that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit

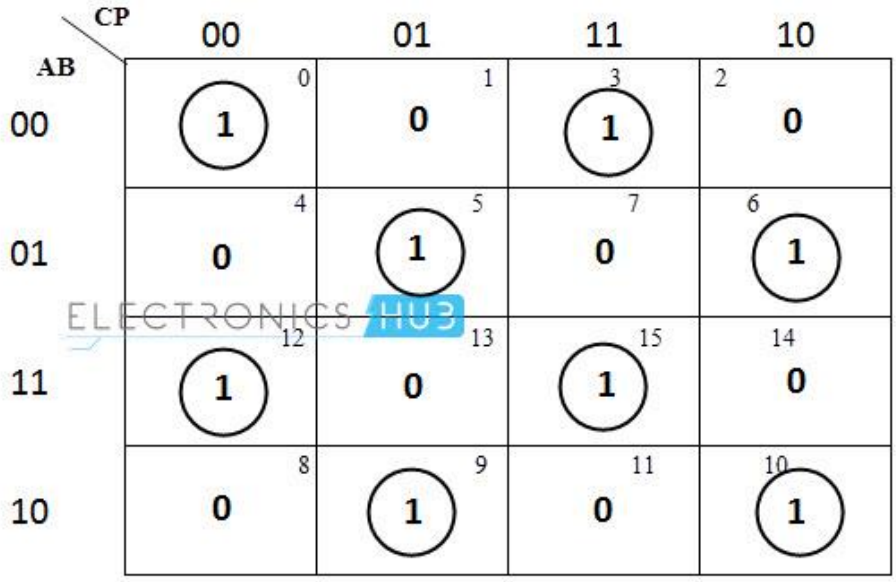
receives these 4 bits and checks whether any error are present in the data.

If the total number of 1s in the data is odd, then it indicates no error, whereas if the total number of 1s is even then it indicates the error since the data is transmitted with odd parity at transmitting end.

The below figure shows the truth table for odd parity generator where **PEC =1** if the 4-bit message received consists of **even number of 1s** (hence the error occurred) and **PEC= 0** if the message contains **odd number of 1s** (that means no error).

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

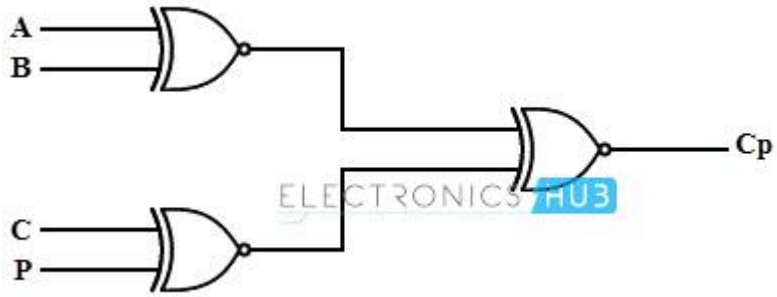
The expression for the PEC in the above truth table can be simplified by K-map as shown below.



After simplification, the final expression for the PEC is obtained as

PEC = (A Ex-NOR B) Ex-NOR (C Ex-NOR D)

The expression for the odd parity checker can be designed by using three Ex-NOR gates as shown below.

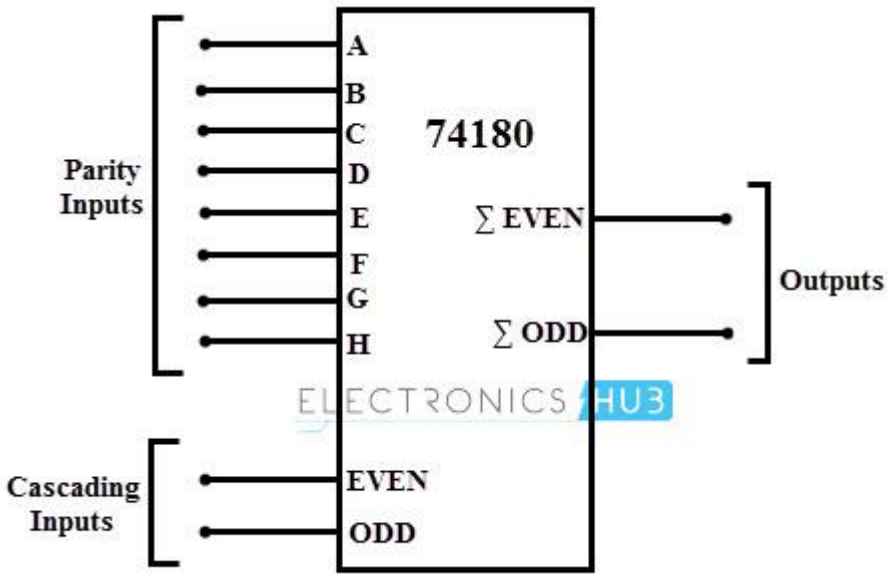


Parity Generator/Checker ICs

There are different types of parity generator /checker ICs are available with different input configurations such as 5-bit, 4-bit, 9-bit, 12-bit, etc. A most commonly used and standard type of parity generator/checker IC is 74180.

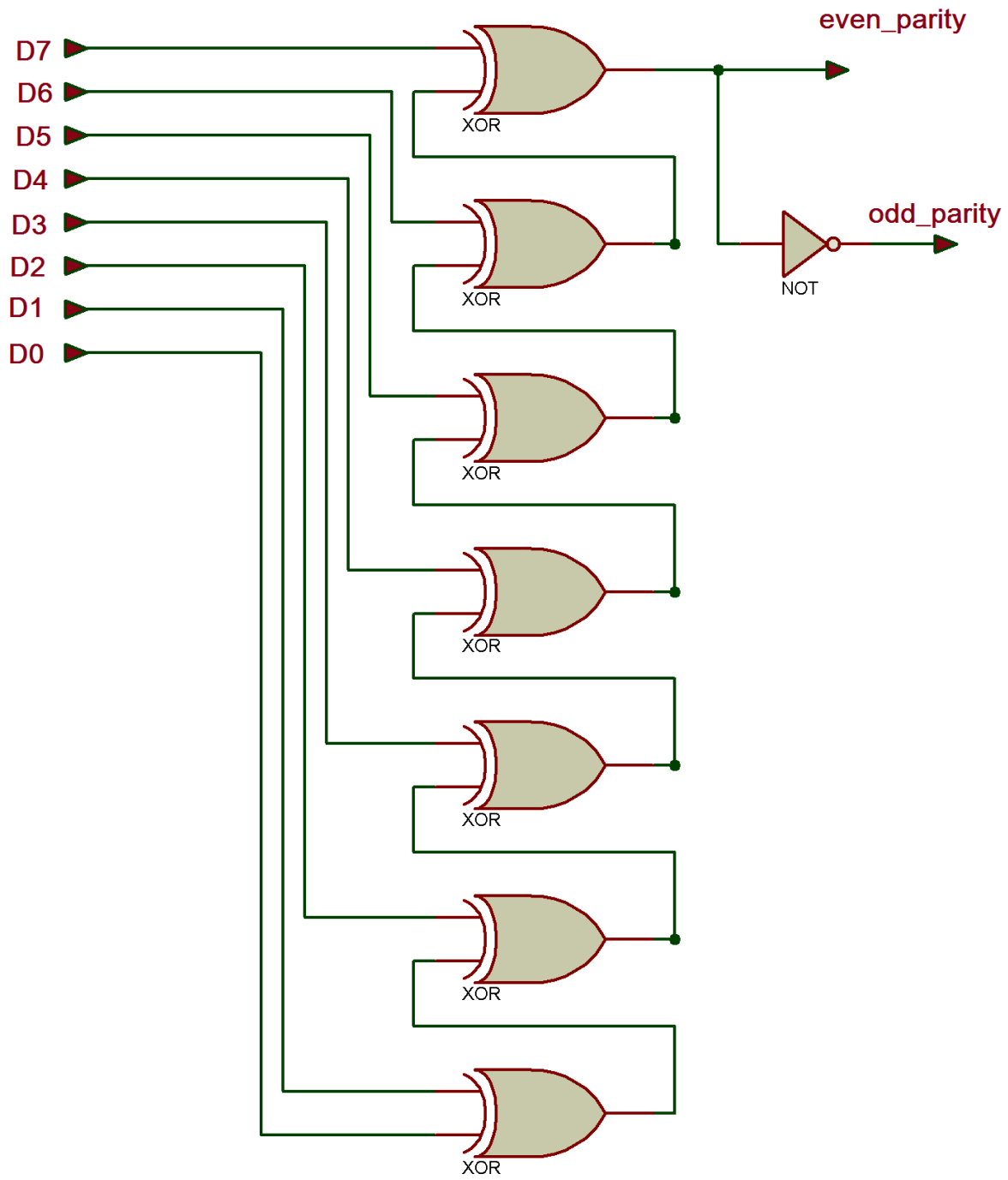
It is a 9-bit parity generator or checker used to detect errors in high speed data transmission or data retrieval systems. The figure below shows the pin diagram of 74180 IC.

This IC can be used to generate a 9-bit odd or even parity code or it can be used to check for odd or even parity in a 9-bit code (8 data bits and one parity bit).



This IC consists of eight parity inputs from A through H and two cascading inputs. There are two outputs even sum and odd sum. In implementing generator or checker circuits, unused parity bits must be tied to logic zero and the cascading inputs must not be equal.

The 8 Bit Parity Generator Circuit



Truth Table

D7	D6	D5	D4	D3	D2	D1	D0	Even_parity	Odd_parity
1	0	1	1	0	0	1	0	0	1
1	1	0	0	1	0	0	0	1	0
1	1	1	1	1	0	1	1	1	0
1	0	1	1	1	1	1	0	0	1
0	0	1	0	1	0	1	0	1	0
0	1	1	1	0	1	0	1	1	0
0	1	0	1	0	0	1	1	0	1

Note : All 256 combinations of D_0 to D_7 are not shown here. Just a few examples are shown.

We can draw the both Even and Odd Parity Circuits in a single circuit.

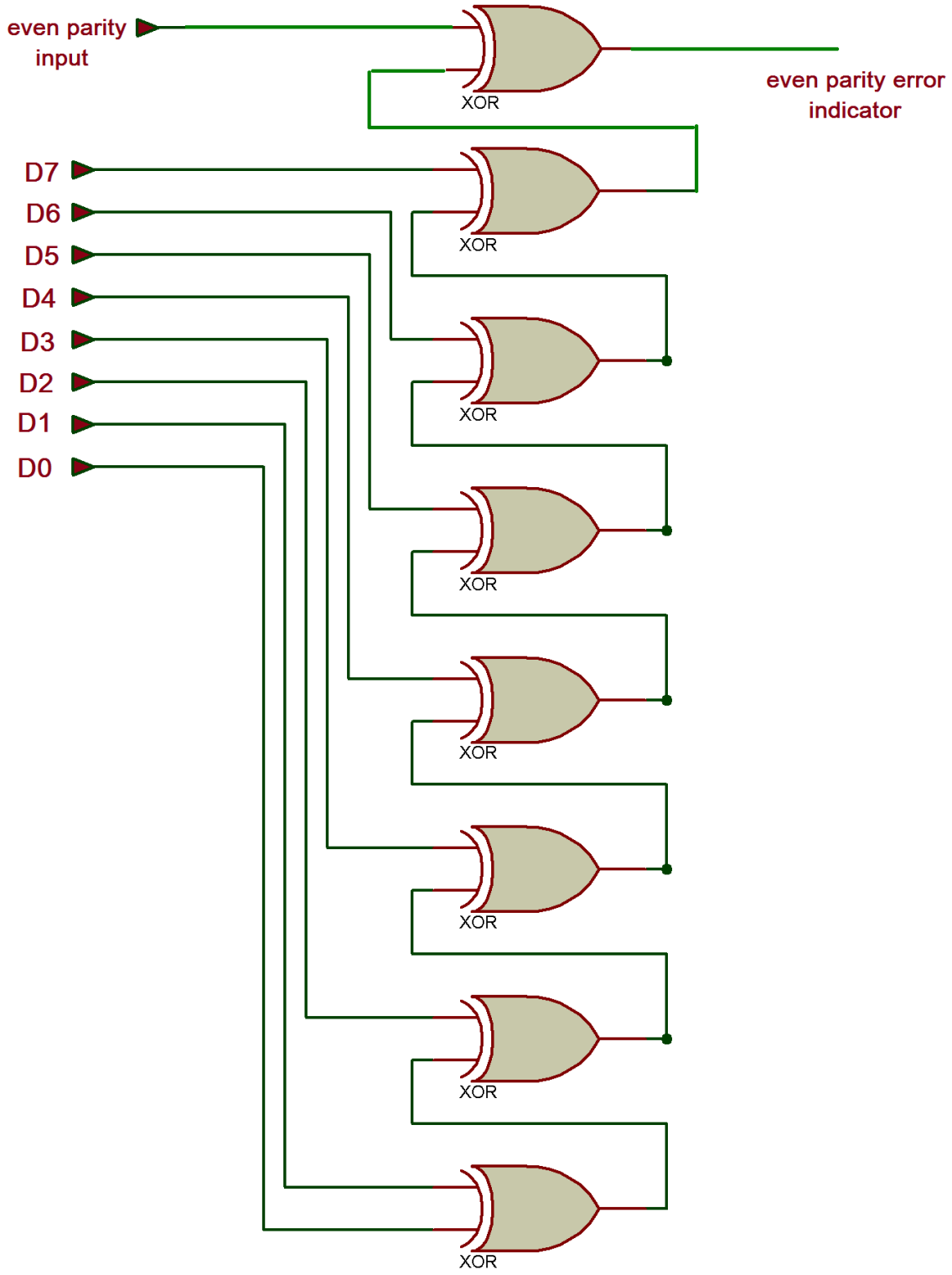
We assume an Enable variable, say M which decides whether the circuit will behave as an Even or an Odd Parity Circuit.

Let's assume that when M = 0 then the circuit is an Odd Parity Generator Circuit, and when M = 1 then the circuit is an Even Parity Generator Circuit.

On simplifying the K maps for both the functions we get the logic functions :

$$P = \overline{M \oplus D\_0 \oplus D\_1 \oplus D\_2 \oplus D\_3 \oplus D\_4 \oplus D\_5 \oplus D\_6 \oplus D\_7}$$

The 8 Bit Parity Checker Circuit



Truth Table

D7	D6	D5	D4	D3	D2	D1	D0	Parity input	Error
1	0	1	1	0	0	1	0	1	1
1	1	0	0	1	0	0	0	1	0
1	0	1	1	1	0	1	1	1	1
1	0	1	1	1	1	1	0	0	0
0	0	1	0	1	0	1	0	1	0
0	1	1	1	0	1	0	1	0	1
0	1	0	1	0	0	1	1	1	1

Similarly with the same logic that of Parity Generator Circuit, we can implement the Parity Checker Circuit on the same circuit.

We assume an Enable variable, say M which decides whether the circuit will behave as an Even or an Odd Parity Circuit.

Let's assume that when M = 0 then the circuit is an Odd Parity Generator Circuit, and when M = 1 then the circuit is an Even Parity Generator Circuit.

On simplifying the K maps for both the functions we get the logic functions :

$$P = \overline{M \oplus D\_0 \oplus D\_1 \oplus D\_2 \oplus D\_3 \oplus D\_4 \oplus D\_5 \oplus D\_6 \oplus D\_7 \oplus P\_in}$$

Advantages of Parity

- Simplicity
- Easy to use

Limitations

The parity checker won't be able to detect if there are errors in more than '1' bit and the correct of data is also not possible, these are the main disadvantages of the parity checker.

Applications of Parity

- In digital systems and many hardware applications, this parity is used
- The parity bit is also used in Small Computer System Interface (SCSI) and also in Peripheral Component Interconnect (PCI) to detect the errors

Links and Resources :

https://www.electronicshub.org/parity-generator-and-parity-check/

https://www.elprocus.com/what-is-parity-generator-and-parity-checker-types-its-logic-diagrams/

https://www.electrical4u.com/parity-generator/

-Report by *Satyam Kumar*