BTEC: Electronic Devices and Circuit

Improving Personal Performance and Lessons Learnt

Written by:

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Report aim

The following report discusses the initial two BTEC assessments that were done, with the main points of discussion revolving around the information and benefits that were gained, with said benefits being split into two sections, practical benefits, which involve the knowledge gained, skills learnt, and techniques developed, while the second section being the behavioral benefits, which revolve around time management abilities and effective communications skills, with both of which not only being discussed, but also are given potential points that of improvement that could be utilized the subsequent times these skills have to be utilized. Additionally, the report discusses the health and safety points procedures that were followed during the practical work within the assessments. Finally, the report discusses and suggest potential improvements to the development process for the circuits that were made throughout both assessments, with the main focus revolving around the simulation, construction, and testing procedures while also reflecting on how simulated values compare to measurements. Overall, the report is given as a personal performance review throughout the two stated assessments and how the knowledge gained throughout them could be utilized for further study or later on during one's professional career.

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Gained knowledge

Semiconductor theory:

Semiconductor applications and elements:

Although it was not discussed heavily during either report, semiconductors and the theory behind them have played an important role in most of the research and the evidence provided in what was written in the first assessment, as both the transistors and diodes rely on them for their function, and exploring their properties through the practical experiments was extremely important. Now, a semiconductor is an element that has a valency of four, giving it the property of being neither and insulator nor a conductor, but rather lying between the two, this in consequence means that the elements can be manipulated much more easily in comparison to elements with higher or lower valences to either become positive or negatively charged. The elements that are mostly utilized as semiconductors are Carbon, Germanium, and Silicon as they have a valency of four while also being able to conduct and insulate well at reasonable temperature unlike other elements which contain the same number of electrons in their valence shell such as Tin.

Types of semiconductors:

Intrinsic: *An intrinsic semiconductor refers to a semiconductor that is "pure", in that all of the elements and bonds that it contains are fully made up of semiconductive elements. However, intrinsic semiconductors are generally not utilized for practical applications, which is the case since due to the fact that since an entire bond of intrinsic semiconductors would be made of the same elements, this consequently means there are no major charge carriers such as free electrons or holes within the crystal as the elements would have the perfect number of electrons in order for each element to fully bond until its valence shell is full. In hindsight, this means that the only thing determining the material's conductivity is the temperature as at high temperatures, electrons would possess an adequate magnitude of energy as to move from one place to another, with the opposite happening at low temperature, in that at absolute zero, a semiconductor is considered to be a perfect insulator. Thus, this means that an intrinsic semiconductor is not very reliable, causing it to not be widely utilized in industrial manufacturing applications.*

Extrinsic: *In contrast to intrinsic semiconductors, extrinsic ones are semiconductors that have been doped with impurity, meaning that an external element that is not a semiconductor has been added to them in order to influence the carriers within the semiconductor's crystal as a way of controlling its overall charge. There are two types of extrinsic semiconductors, N-Type and P-Type, N-Type semiconductors are ones that have been doped with elements that contain a valency of 5, with the most common ones used being Arsenic and Phosphorus, this causes a free electron that acts as a negative charge to be in the material's crystal as the number of electrons within either elements outweighs what the possible number of electrons that can be taken by it from an element with a valency of 4. The same exact process occurs with P-Type semiconductors, with the difference lying in the fact that the doping element has a valency of 3 and the materials being utilized are generally Aluminum, Boron, and Indium, and what this does is that the number of electrons given by doping element is not sufficient to give 4 silicon atoms, consequently causing one of them to have a spot that could be free for an electron, which is also known as a hole and acts as a positive charge. When the concentration of doping elements increases, the overall number of either free electrons or holes increases, consequently meaning that the majority carriers would either become the free electrons or the holes, thus making the electrons within a semiconductor push away or into a moving electrical charged when invoked, however, while at equilibrium, they nonetheless remain neutral.*

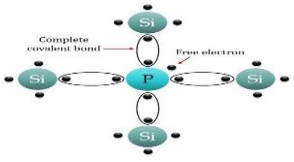


Figure 1 N-Type semiconductor

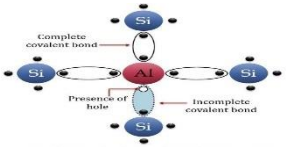


Figure 2 P-Type semiconductor

Diodes:

Definition and theory:

Diodes were a major part that was explored during the first assignment as both the types and the theory behind diodes has been discussed. A diode is a whole is a device that permits the flow of current from one direction but blocks it from the other except when the voltage given to the diode is much larger than the breakdown voltage, and in that case, the diode would permit the flow of current during reverse bias but it would explode. When it comes to the intricacies of how diodes work, it is does so through the use of semiconductors , in that the reverse end of the diode is fitted with an N-Type extrinsic semiconductor while the forward is fitted with a P-Type extrinsic semiconductor, while between the two, an area known as the depletion region can be seen, which simply contains atoms with no excess electrons or holes . This way, whenever a voltage is passes through the diode in forward bias, said voltage would push the holes seen in the P-Type semiconductor towards the depletion region as opposite charges repel each other (positive voltage and positive holes), while the electrons from the N-Type semiconductor are pushing towards the depletion region as well in order to get to the positive voltage, this way, the depletion

region is minimized to the point where current can pass through it. With that being said, the opposite process occurs when a current attempts to pass through a diode in reverse bias, in that the negative charges from the N-Type semiconductor would be attracted to the positive voltage that is trying to get through the diode and the holes in the other side of the diode are being repelled, and due to this, the depletion region would increase in size, consequently preventing current from passing through.

Types of diodes:

Signal: *The signal diode is the most common type of diode seen on the market, it has a forward voltage of 0.7V and is mainly utilized for circuits with relatively low power consumption of around 100mA , with their main applications being rectifier switches and current limiters.*

Power: *Power switches are very similar to that of signal switches, with both of which having a forward voltage of 0.7V and having the same properties with the main difference being that a power diode is used for high voltage applications such as DC PCUs and chargers.*

LED: *An LED, also known as a Light Emitting Diode, is a diode that has a forward voltage of 1.8V and has the property of emitting light whenever it is utilized in forward bias. Its main applications are for emitting lights whether in major circuits or relatively simple prototyping applications.*

Zener: *A Zener diode has a forward voltage of 0.7V as well, but it also has the property of being able to function in reverse bias, in that even if the voltage provided in reverse biased exceeds the maximum, the diode does not malfunction or break, but rather it enters the Zener region and conducts normally. And as such, Zener diodes are only utilized in voltage regulations in professional or industrial applications.*

Transistors:

Definition and applications: *A transistor is an electronic device which constitutes a block of semiconductors and possesses three pins. Said component is one the most utilized components in electronic circuitry, with its main applications being signal current or voltage amplification and acting as an electrical switch that does not require mechanical or physical contact to serve its function.*

Types and their theory:

BJT: *A BJT (abbreviation of Bipolar Junction Transistor) is a transistor that utilizes both free electrons as well as holes in order to achieve its function. It uses three pins called the Collector, Base, and Emitter. There are two types of BJT transistor, an NPN and a PNP, however, the one that would be discussed is the NPN transistor. Within an NPN transistor, the collector and emitter are made using an N-Type semiconductor, while the base – the pin found in the middle – is made out of a P-Type semiconductor. The main voltage that passes through the transistor is the VCE (Collector to Emitter), however, the VCE voltage cannot pass through unless VBE (Base to Emitter) minimum voltage has been applied. In that the base blocks the flow of current between the collector and emitter, however, if the minimum voltage of 0.7V were to be applied to the base in forward bias, the depletion region created by the base would shrink and connect to the emitter, causing current to flow from the base to the emitter and therefore charge carriers from the collector are also able to pass through. This also means that the emitter's current would be the sum of the Collector's current as well as the Base's ($I_E = I_B + I_C$).*

FET: *A FET is the second major family of transistors (abbreviation of Field Effect Transistors), and in contrast to that of BJT, FETs only utilizes either holes or free electrons to carry useful charges, and not both of them simultaneously as seen in BJT. Additionally, FET utilizes pins known as the Gate, Source, and Drain, which are equivalent to the Base, Collector, Emitter (in the same order). Overall, there are two main subtypes of FETs, which JFET (Junction Field Effect Transistor) and MOSFET (Metal Oxide Semiconductor Field Effect Transistor), which are the ones that are going to be discussed in the following section, both of which are going to be ones with an N-Type majority or function rather than a P-type.*

JFET: *A JFET is a FET of transistors that permits the flow of current in its inactive state, basically meaning that that the electrical switched would be on by default. When looking at an N-JFET's composition, which is a JFET with the N-Type majority, it is made up of a big channel in that middle that utilized N-Type semiconductors which connects the Drain and Source pins, and additionally, two small P-Type regions are on either side of the transistor, with one of them being connected to the Gate. This basically means that whenever the gate is in forward bias, the P-Type region would push in towards the middle of the transistor, and in consequence, restricting the flow of current through the N-Type channel and even stopping it if the voltage applied through the gate were to be high enough.*

D and E MOSFET: *The "MOS" within MOSFET refers to the oxidizing layer found at the Gate of the transistor, which acts as an insulator preventing the flow of current to go into the Gate unless it is charged. A MOSFET has an additional two subtypes, with them being D-MOSFET and E-MOSFET (standing for Depletion and Enhancement), with the first of which that is going to be discussed is the N-channel D-MOSFET. When it comes to its construction, the N-channel D-MOSFET has a channel on its side which connects the Drain and Source pins known as the bridge, and in between them lies the Metal Oxide layer which insulates the gate, additionally, right to the side of the gate is an area that contains P-Type semiconductive material. Similar to a JFET transistor, a D-MOSFET allows for the flow of current when the gate has not been charged, but when the Gate is forward biased, the holes from the area to the side of the bridge become attracted, therefore moving towards the bridge and restricting the flow of current. However, in addition to restricting, a D-MOSFET is also able to enhance the flow of current in the circumstance that the Gate is reverse biased, in which case, the bridge (which contains free electrons) is repelled towards the P-Type area, this causes the bridge to expand and therefore more current to flow through. When it comes to the other type of MOSFETs, the E-MOSFET, it contrasts the D-MOSFET in that it is off by default, in that the change in its composition makes it so there are simply areas of N-Type material surrounding the Drain and Source pins, but a bridge connecting the two is nonexistent. In terms of function, what this does is that it only allows the transistor to utilize the Enhancement mode that was discussed during the D-MOSFET as providing a forward bias voltage to the gate simply creates the bridge that connects to the two pins.*

P-Type transistors: *All of the aforementioned transistors that were explained utilized N-Type semiconductor as their majority carrier, however, there is an alternate type of each of the discussed transistor in which it utilizes a holes as their majority carriers. The difference that this makes is that N-Type material was utilized, it will be a replaced with P-Type and vice versa for areas where P-Type material was used, this consequently also changes the charge required in order to perform forward or reverse biased. In that a P-Type BJT transistor, known as PNP, would require a negative charge rather than a positive one in order for it to function in reverse bias, with the same concept being applied for the P-Type alternate of for any of the discussed transistors. It should be stated that N-Type transistors are rarely replaced by P-Type as they can both serve the same function and electrons working as the majority carriers are generally more flexible and mobile in comparison to holes.*

Operational amplifiers:

Function and application:

An operational amplifier – also called an op-amp – is an IC-based device that – as the name might suggest – is used in amplifying its input signal and is known for having extremely high output to input ratios. In addition to that, an op-amp possesses differential inputs, meaning it contains two input pins, that get their voltages compare, with the purpose of such operation being to determine whether the output signal is going to be simply amplified or amplified and shifted by 180°.

Inverse and non-inverse states:

As stated, depending on the differential inputs, the output of the op-amp could be inversed by 180°, which is one of the main functionalities that an operational amplifier is utilized for. This means that during non-inversing amplification, the output would simply be amplified while still retaining the same phase shift, while during inversing amplification, the output would be "upside-down", in that if the input signal were to be on the positive edge, it will be amplified and on the negative edge when outputted. The way that this is done in terms of the circuitry, is that for non-inversing amplification, the inversing pin is grounded through a resistor connecting to ground and another which goes to the output pin creating a closed feedback loop, while the non-inversing pin is simply connected to the power supply. On the other hand, the circuitry utilized to shift the signal required for the non-inversing pin of the IC to be grounded through a resistor, while the inversing pin connects to two resistors, one being from the power supply, with the other going to the output pin which also creates a closed feedback loop.

Gain properties:

When it comes to the gain of the operational amplifier, it slightly differs during inversing and non-inversing operation. With inversing, Gain is given as -1(Vout/Vin), with the minus indicating that it is 180° out of phase, while on the other hand, during non-inversing operation, the gain is given as (Vout/Vin)+1, with the addition of 1 being due to the fact that gain during non-inversing amplification can never be smaller than one.

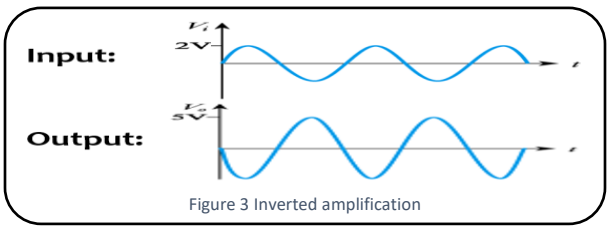


Figure 3 Inverted amplification

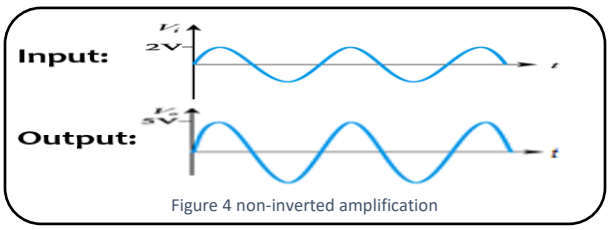


Figure 4 non-inverted amplification

Logic gates:

Logic gate definition: *Logic gates are digital components made up of transistors, diodes, and resistors, and utilize a Boolean expression in determining whether or not to output a HIGH or LOW signal. What this means is that the components only output either the minimum – which is zero – or the maximum voltage they can provide, with the same being said about their input, in that the actual value of the input does not matter, but rather it only checks if there is a signal or not, from there, it placed values of the stated inputs into a Boolean expression and depending on its answer, it will provide either a HIGH or LOW output. Logic gates are major building blocks in any computational application that requires a given logic in order to run an algorithm such as microprocessors and microcontrollers.*

Logic gate families:

What are logic families: *Logic families are the intricacies in which logic gates are constructed internally, with the main difference between one logic family and another lying in the methodology utilized in reaching the same function, in that each of which have their own characteristics in terms of strength and weaknesses. There are many families and subtypes available, specifically 8, however, the ones thar are most popular on the market and which were explored the most during the two assessments were the CMOS and TTL family.*

Transistor-Transistor logic: *The Transistor-Transistor Logic family (stated as TTL) utilize BJT transistors in its construction of logic gates rather than using FET transistors, this assists in that both amplification and logic gating function of the logic gate can be done simultaneously by the transistor, hence the name. The main characteristics of the TTL family is that it has relatively low propagation of 1.5 to 30ns, decent noise immunity, and can fan out to 10 different logic gates.*

Complementary Metal Oxide Semiconductor: *As the name might suggest, the Complementary Metal Oxide Semiconductor (abbreviated as CMOS) utilized MOSFET transistors for their function. The main characteristic of this family stems from the complimentary manner in which its transistor function, in that whenever a transistor turns off, the other turns on. In comparison to TTL, the CMOS family has extremely good noise immunity, can have a fan out that exceeds TTL by 5 times, however, there is a very big tolerance for its propagation at around 1 to 210ns*

Types of logic gates:

NOT: *The not gate is the only one terminal logic gate, its outputs is the opposite of its input as it utilizes the Boolean expression* $\overline{A} = Y$

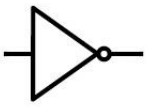
AND: *The AND gate outputs a HIGH signal only when all its input terminals are also at HIGH, utilizing the Boolean expression* $A \cdot B = Y$

OR: *The OR gate would output a HIGH signal if one of its input terminals are HIGH due to its Boolean expression being* $A + B = Y$

XOR: *The XOR gate would only output a HIGH signal if the sum of its HIGH input terminals is an odd number, with its Boolean expression being given as* $A + B = Y$

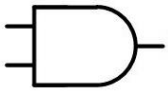
The "Not" logic gates: *The Not logic gates are an alternative type of logic that check for the same Boolean expression as their normal type but output the opposite of it and are available for each of the aforementioned logic gates except for the NOT gate. An example of which would be the NAND gate, A Not AND gate which has the Boolean expression of* $\overline{A \cdot B} = Y$*, in that this logic gate will output a HIGH signal whenever its input signals are not fully, which is the exact opposite to that of the AND gate. In drawing, these gates are identified using a circle drawn in front of the output terminal.*

NOT



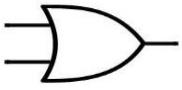
A	Y
0	1
1	0

AND



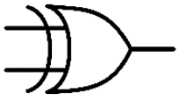
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

XOR



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Flip flops:

Flip flop definition and application:

Flip flops are electronic devices that come in the form of ICs, with their main function being to retain given signals and store them within a memory and due to that, their usage stems from computer engineering as they are mostly found within computational circuitry as such circuits are the ones that require memory retention for their function such as the RAM drives found within a computer. Flip flops mainly utilize logic gates in order to operate, which includes its input and output functions, thus meaning that it is also a digital device that is only able to understand and output HIGH or LOW signals.

Types of flip flops:

SR flip flops: *SR flip flops are the foundation for any other type or flip flop as the functions found within SR flip flops perform the basic and fundamental aspects of what is required from a flip flop. The SR flip flop has 4 major pins other than its Vcc and GND pins, with them being, Set, Reset, Q, and QB. When it comes to the connections, the way this is done is by utilizing two two-input NAND gates, with one terminal from each being connected to a signal input terminal and the other being connected to the other NAND gates output.*

SET: *The set pin acts as the activation pin for the flip flop, in that whenever the set pin is given a HIGH value, the flip flop's main output signal becomes HIGH as well. However, the main characteristic of flip flops can also be seen through the set pin, in that if the set pin were to go back to LOW, the output would retain the set pin's initial value and remain HIGH.*

RESET: *The reset pins acts as a way to counteract the effects of the set pin, in that if the reset pin were to be HIGH while the output still maintains the initial HIGH signal, the output will be reset and go back to its initial value of LOW. It should also be noted that the reset pin would have no effect on the device if it were to be activated when the output is already at LOW.*

Q & QB: *The Q and QB pins are the output sources for the flip flop, the reason to which there are two of them is that QB (pronounced as Q bar) outputs the opposite signal to that of the Q pin. In that is the set pin were to become HIGH, Q will be HIGH, while QB will be LOW. The stated features allows for further versatility in utilizing flip flops as it can be used in circuits to perform necessary functions.*

Additional flip flops: *In addition to SR flip flops, the other types are D-Type flip flops, and JK flip flops. As stated earlier, the SR flip flop contains all the fundamental features that other flip flop types utilize, with such features being the Set, Reset, Q, and QB pins, as such, when analyzing D-Type and JK flip flops, only their defining characteristics would be explained in order to avoid repetition.*

Clock pin: *The clock pin is a common feature found within both JK and D-Type flip flops. The function of the pin is to toggle the Q pin whenever clock reaches its rising edge, meaning that if the clock pin were to become HIGH and Q is LOW, Q will become HIGH, from there, if clock goes back to being LOW, this will not have an effect on the output pin, but rather, the output pins only toggle when the clock pin's signal gets to its rising edge (Q changes its state only when clock becomes HIGH). This function is extremely important especially in automating the flip flop's operation by utilizing the clock pin with the use of a signal with a given frequency.*

D-Type flip flops: *The main feature of the D-Type flip flop comes from its Data pin, a pin that reflects its own signal onto the Q pin, however, it only does so when the clock pin reaches its rising edge. This means that the Q pin follows the same signal that can be seen in the Data pin, however, said signal would not be visible to the Q pin unless the clock signal reaches its rising edge. In that if Q is LOW, and the Data pin becomes HIGH, nothing will change until clock becomes HIGH as well, and from there, if the Data pin becomes LOW, Q will become LOW only whenever clock reaches its rising edge once again, and Q would retain its LOW value even if clock reaches its rising edge once again but only if the Data pin remains LOW as well as Q would only follow the Data pin.*

Major issue with SR and D-Type flip flops: *A major issue that should be noted with SR and D-Type flip flops is the fact that whenever both the Set and Reset pins are provided a HIGH signal at the same time, the flip flop's output pin will go into an "invalid" state that causes outputted signal would be unpredictable, which – especially in major practical applications – could cause significant issues to the functionality of the circuit.*

JK flip flops: *The JK flip flop adds an additional two pins to the IC, with them being the J and K pins. The main functionality of said pins is the exact same as Set and Reset, with J acting as the Set pin and K as the reset pin. However, the main difference between the two lies in the fact that in the circumstance that both pins are given a HIGH signal, the output pins would not go into an invalid state, but rather, the output of the flip flop would simply toggle, hence resolving the stated major issue found within SR and D-type flip flops. The intricacies in which this is done is by utilizing two three-input NAND gates rather than a 2 input AND gates as seen in the other flip flops, with the connection being mostly the same, with the addition of the third terminal, which is connected to each gate's output pin.*

Active LOW and HIGH flip flops: *The discussed flip flops and analysis done for each was explained with the use of an Active HIGH flip flop in mind, which is a flip flop where its output pins is effected on the rising edge of clock, set, and reset pins, however, there also is an alternative type to each of the stated flip flops that works as an Active LOW. Active LOW flip flops also change Q's initial value, in that Q would initially be HIGH, and if set were to go its falling edge, it will turn to LOW.*

Sequential counters:

What are sequential counters: *A sequential counter is an electronic circuit that involves the use of flip flops in order to transmit or save signals by cycling through various states depending on the clock pin's current iteration. The following simply briefs on the types of sequential counters discussed, however, in depth analysis is given in the "Analysis of developed circuits" section.*

Shift registers: *A shift register is a type of sequential counter that generally uses D-Type flip flops allows for the movement of data from one direction to another in a linear manner, in that data either flows from the left to the right or vice versa. Shift registers are generally utilized in either storing or moving data through computer hardware and calculators.*

Asynchronous counters: *An asynchronous counter is a type of sequential counter that does not transmit a unified clock signal to all of its flip flops. The states it forms are continuously changing rather than simply going from one direction to another. Theses types of sequential counters generally utilize JK flip flops and are mostly used in frequency dividers and timers.*

Practical skills learnt

Utilizing CAD programs:

One of the main skills that were developed during the period of both assessment was the ability to effectively utilize CAD programs. This was done through the use of a program called Proteus in order to create and simulate the electrical circuits that we were going to build during the practical session and as a way of comparing theoretical simulated values with actual measurements. The importance in developing this skill lies in the fact that CAD nowadays is an essential part of any engineer's tool kit whether or not that it is in electronics due to its reliability and efficiency of use as it is a much simpler and faster method of testing something in comparison to making an actual prototype of it, not to mention the many issues that could when building prototypes that could provide inaccurate results.

Using electrical measuring equipment:

Utilizing electrical measuring equipment is an essential skill that any electrical engineering should have as being able to get measurements is essential for prototyping, testing, and maintaining, as a way to make sure a circuit is going to function or is functioning as required. This skill was developed a lot during the practical sessions as in multiple occasions, measuring the voltage using an a multimeter or an oscilloscope was a necessity to get parameters to complete the required calculations.

Practically working on circuits:

A major part of the prior assessments was practical work that was done as a way of further exploring the electronic devices and circuits, and during which, the skill of practically working with electronic components was further developed, especially when considering that which was done prior to the assessments was not practical but rather theoretical or drawn only, and even though that was done in great amounts, experiencing potential issues that could occur during practical circuit development gives an idea to what could be expected when working with bigger circuits and the overall feel of working with physical components, which are both necessary development when it comes to eventually working with bigger and more complex circuits during a person's professional career.

Practical work in using applied mathematics:

Although apart of the curriculum currently being done alongside electronics is Applied Mathematics, all of which that is being done there is theoretical, whereas here, utilization of actual values from measurements done through the use of measurements equipment has been done, thus providing an idea of the nuances and potential inconsistencies that will be faced when utilizing actual measured values. This additionally assists in putting values on paper into perspective in real life as measuring values and utilizing them in calculation gives a better understanding of their magnitude. The stated development of applied mathematical skills is essential in a multitude of fields and especially in engineering. The way it was done was mainly through calculation that were done in order to get the amplitude, frequency, time period as well as the equations utilized in finding the gain for the operational amplifier circuits.

Drawing interpreting electrical diagrams:

Another skill that was further developed was during the two assessment was the ability to draw and interpret electrical circuit diagrams and layouts. The importance of the skill is significant especially in any engineering field, in that even though interpreting electrical diagrams and drawings might be something specific to electronics, the ability to read drawing notations and visualizing a technical drawing is extremely important in engineering as a whole. The main areas in which the stated skill has been developed throughout each assessment was interpreting the drawings provided within the assignment briefs and also drawing diagrams and breadboard circuit layout for the prototypes that were made during the practical sessions.

Techniques utilized

Minimizing logic circuits using Karnaugh map

A very important technique that was learned and developed throughout the second assessment was solving and utilizing Karnaugh maps, which is a table that utilized in order to simplify Boolean algebraic expression which are used for logic gate circuitry. The way a Karnaugh map works is that it contains the values from a truth table but in a certain order and format, from there, if any HIGH values are next to each other in a straight and are in quantities of powers of two, their Boolean expression can be combined in order to minimize the overall expression, which consequently assists in simplifying a combinational logic gate circuit by decreasing the number of logic gates required while still maintaining the functionality as the initial circuit. Utilizing a technique to minimize circuitry such as the Karnaugh Map is extremely important especially when making products from an industrial standpoint, as although the exclusion of 2 or logic gates might negligible, it can be extremely profitable from a large scale manufacturing's point of view.

Utilizing universal logic gates for minimization

Universal logic gates refer to specifically the NAND and NOR gates, and they are called as such since – due to their mathematical phenomena – they are able replicate the functionality of each logic gate, in that the functionality of an OR gate could be replicated using a set of NAND gates only that are connected in a particular manner, with the same being the case for any other logic gate. This technique was utilized within the second assessment in order to minimize the amount of logic gates required in order to simplify a logic gate that has been minimized using a Karnaugh map, the circuit was initially a combinational logic circuit that contained two NOT gates, two AND gates, and an OR gate, and after it has been converted, the circuit constituted of 9 NAND gates. Although the overall number of logic gates might be higher since converting a single gate to NAND gates only requires multiple NAND gates, from a manufacturing perspective, utilizing a circuit with NAND gates only is more efficient as it is relatively easier to manufacture circuits that contain only a single type of logic gate, which consequently decreases the capital and operating expenditures in large scale production.

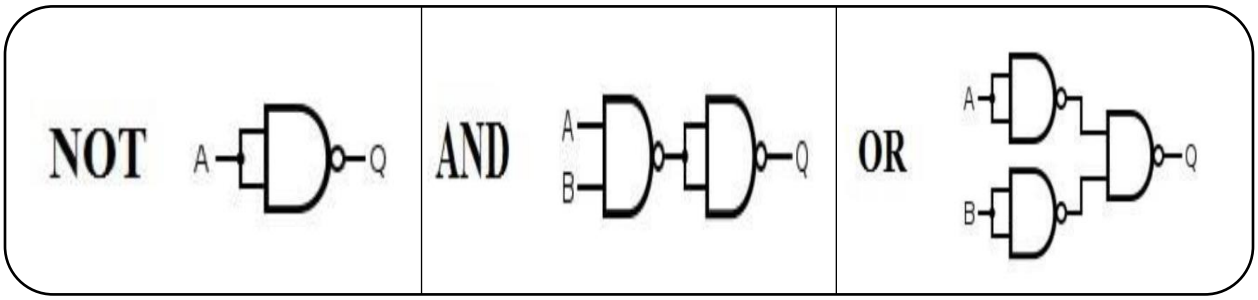


Figure 4 NOT, AND, OR gates to NAND gate equivalent

Asynchronous up counting to up/down counting

One of the major techniques that were implemented throughout the second assessment was converting an upwards counting asynchronous counter to be able to function both as an upwards and as a downwards counter. The way this was done was through the use of adding a combinational logic gate circuit in between each of the flip flops, with said combinational logic gate circuit constituting of 2 AND gates connected to an OR gate. In addition to that, another power source is added which provides two signals, one going through a NOT while the other is unchanged. When it comes to the logic gate circuit connection, one of the AND gate's input terminals are connected to Q and the other is to the inverted signal from the additional power source, while the other AND gate is connected to QB and the unchanged additional power source. which leads to a NOT gate, with the circuit ending with the AND gate's outputs going to the stated OR and the OR gate's output going to the subsequent flip flop's Clock pin. Overall, what the combinational logic gate circuit does is that depending on the signal provided from that additional power source which is controlled by the switch, it will either let a signal pass through to the second flip flop whenever Q is HIGH or whenever QB is HIGH. For instance, if the switch were to be closed, and the non-inverted signal from the power source is HIGH, then the AND gate connected to QB would be HIGH whenever QB is also HIGH since it is the only terminal remaining as the other one is HIGH From the non-inverted signal, thus, whenever QB is HIGH, it will be the signal sent to the second flip flop, and if Q is HIGH, then nothing would be sent since the other terminal from its AND gate is getting a LOW signal from the inverted signal, consequently flipping the order at which signals are being sent since QB is the opposite to that of Q, therefore making it possible to control if the counter is going to count upwards or downwards with the use of the stated switch. The reason to which the stated technique is extremely important is due to the fact that it minimizes that circuitry by a significant amount, in that if not for it, then two separate circuits would have to be made and connected, with one being dedicated to upwards counting and the other to downwards counting, which would have increased the capital and operating expenditures as well as the time consumption per circuit by an extremely significant amount.

Health and safety

Safety precautions

Keep the working area clean: *Keeping the working area clean refers to two different things, keeping the area tidy and keeping it clean from dust. Keeping the area tidy is a significant point that must be followed as having a cluttered area could lead to a variety of safety risks, some of which being that a cluttered area could lead to fire-related hazards in, that a conductive object could be kept in proximity to a power supply, which could consequently lead to it burning another object, and therefore causing a fire, additionally, in cluttered spaces some items could be mistaken for others, which could lead to the usage of devices in applications they are not appropriate for, leading to potential malfunction risks. When it comes to keeping the area clean from dust, it is a point that is often forgotten even though it carries major safety risks, with the reason to which being that dust in high enough quantities could jam certain electronic components, additionally, dust could act as an insulator, and – again – in high enough quantity, this could cause components to malfunction or short circuit, potentially leading to them exploding.*

Keep drinks away from the working area: *Keeping drinks away is a common safety precaution that has to be taken when working with any electronic devices to avoid any potential of spillage occurring. The main reason that this should be avoided is that if a drink were to be spilled onto a circuit, it could potentially connect two of its terminals together, which in most circumstances leads to a short circuit and for devices that were utilized to burn or explode as the current is being redirected spontaneously. Additionally, if water were to be spilled, even if the aforementioned issue did not occur, it could lead to the material utilized for the devices to rust, although this would most likely not cause major safety issues, it would nevertheless cause long-term functionality issues.*

Expect all circuits and devices to have voltage running through them: *A useful precaution or mindset to have when working with electronics is to always expect any circuit or device plugged into a board to have live current passing through them, which forces the person to always check the power to see whether or not that is the case. This helps in making sure to never touch a circuit unless it has been ensured that there is no risk of electrical shock in doing so.*

Personal Protective Equipment

Static wristband: *A static electricity band is a band is utilized in areas where sensitive components are being dealt with, which – in this circumstance – would be the ICs that were used for the operational amplifier and flip flops. The way the band functions is that it has a metal wire with a clip which is then either grounded or connected to another conductive object such as a metal table, from there, it is simply worn by the person working on the components on their wrist, this way, any static electricity created would sim ply transfer to the place that was just clipped. The importance of utilizing a static waistband is that in the circumstance that static electricity was generated, contact with ICs or other sensitive components could cause them to blow up and possibly harm the person.*

Figure 5 Static wristband

Insulation gloves: *The use of insulation gloves is rather self-explanatory, with their use being to simply prevent possible shock from occurring by touching wires connected to a power supply or a conductive material that m ight be conducting electricity through it. However, it should be noted that insulation gloves were not utilized when building the prototype circuits, but rather they were nearby in the circumstance that live electricity with high voltage would have to be handled, that is the case since insulation gloves are generally thick and working with them on relatively small circuits would be extremely inconvenient.*

Figure 6 Insulating rubber gloves

Emergency actions

Fire: *Due to the workspace nature of an electronics lab, fires are a common emergency that could occur due to the multitude of electronic devices and power supplies available that could malfunction and explode. As such, if a fire were to break out within the laboratory, the initial actions that should be taken would be to turn off the main power supply of the lab, as this could prevent the source of the fire from causing more issues. From there, a fire extinguisher should immediately be used and emergency escapes should be opened, however, it should be noted that water should never be used under any circumstances on electrical components as it could cause them to short circuit, explode, and worsen the situation. Additionally, before using the fire extinguisher, it should be checked to make sure that it is of type C, which is a type of fire extinguisher that utilizes a nonconductive extinguishing agent.*

Serious electrical shock: *In the circumstance that a person receives a serious electrical shock, the initial reaction from most people nearby would be try and help them by moving them away from the hazard, however, this should not be done under any circumstance since current from their body could shock the person trying to assist them at very similar intensities. As such, the first thing that should be done would be wearing insulating gloves, moving the person away from the electrical hazard to stop them from receiving more current, turning off the power in order to ensure that no one else is at risk, and then calling emergency services. Additionally, a bandage should be applied to the shocked area as it could be experiencing third degree burns and bandaging it would decrease the chance of the person receiving a blistering skin. Furthermore, if any signs of a lack in breathing is noticed, CPR should be performed but only by certified or trained people as performing improper CPR could lead to lung injuries or fractures in the rib cage.*

Behavioral skills developed

Brief

The subsequent section of the report will be discussing the behavioral skills that had to be utilized throughout both the first and second assessments in order to produce the required circuits and overall results in an efficient in terms of time management as well as the effective communication between the student and the supervisor as to ensure the final results are up to standard. Additionally, the section will also discuss how the stated behavioral skills as well as the aforementioned knowledge and skills could be utilized in further studies and personal improvement.

Time management

Importance of time management: *In its essence, time management refers to the planning of time utilization effectively to get a certain task done in both an appropriate time and order. Managing a project or a task's time appropriately leads to heightened focus on the ongoing and subsequent tasks without accidentally straying too far from the main objective as managing a project's time means to prioritize tasks accordingly. If done right and without over or underestimation of the required time per task, time management ensures that tasks will be done in a period of time that can be considered to be more than sufficient, consequently leading to an overall better quality of work as tasks would be done with quality and efficiency in mind rather than simply trying to get the work done. As such, a clear distinction should be made between time management and simply putting in deadlines for certain tasks, since it should be noted that although it would be more beneficial overall to complete the project quickly, putting in tight and concrete deadlines would lead to a decrease in motivation and morale due to trying to work quickly in order to meet said deadline, potentially leading to burnout, thus causing work to be slower and of less quality.*

Time management throughout both assessments: *Throughout both assessments, I personally would say that time management was somewhat as I was able to finish tasks in a sufficient time and without having to go through any significant issue in terms of meeting deadlines in an appropriate time. The reason to which is that the way the time was handled was that research on the activities was required to be done for each section, from there, simulations were to be done and the practical experiments were to be conducted, then the same procedure was repeated for each new section that required practical experimentation, which – in terms of order – was great as it allowed for us to understand the devices and their circuitry and then confirm our research through the practical experiments, which helps in further understanding the device's circuitry. When it comes to the deadlines and the time margin provided for them, they were more sufficient for both assessments. However, a major issue that can be concluded from the way that time management was handled is that the time that was provided for research-related sections was the same – and sometimes shorter – in comparison to time provided for building schematics simulation and practical experimentation, while personally I think it should have been the other way around as research sections take requires both understanding the topic which required to be researched and to also thoroughly explain it in the report, both of which requiring a lot more time than creating schematics and simulation or building circuits on a breadboard.*

Potential improvements of time management: *As stated, time management was somewhat throughout both assessment was somewhat efficient, however, it still included some major flaws. And as stated, the main issue that was faced due to time management time management inefficacy was improper time allocation for research sections as it was very little relative to the time allocated for simulation and experimentation. This issue could simply be resolved by increasing the time for research sections and decreasing the time for simulating schematics and practical experiments. This could be specifically implemented by adding the number of circuits and schematics that would be made during each practical-dedicated session, this way, more time would be freed up which could then be used for research. This way, a time-consuming section such as research can be done thoroughly and comfortably without rushing it as to ensure that all the information given is accurate, while although building circuits does require attention and time in order to do correctly, the task is relatively simply as theoretical understanding from the research section and simulation should significantly assist during the practical stage of the assessment. Additionally, the circuit schematics that were drawn were with us during the practical section, meaning all that was required to be done is simply follow them, therefore the section did not require as much time as it was actually given. Furthermore, another issue that could be improved is providing a margin rather than a set time for the deadline, this way, work could be done more comfortably, as well as that, this avoid planning fallacy, which is the inaccurate estimation of the time required to complete a certain task.*

Approximate time management for both assessments								
Process	**Weeks**							
	Week 1	Week 2	Week 3	Week 4	Week 5	Week 6	Week 7	Week 8
Research								
Simulation								
Construction								
Testing								

Optimal time management								
Process	**Weeks**							
	Week 1	Week 2	Week 3	Week 4	Week 5	Week 6	Week 7	Week 8
Research								
Simulation								
Construction								
Testing								

Effective communication and research abilities

Importance of effective communication and communication skills: *Communicating effectively with others – especially your supervisor – leads to a more productive process within all of the required sections, which in this case includes the simulation, development, and construction of electronic circuits. Being able to effectively communicate also assists in interpreting information said by the supervisor which ensures that the tasks being done are up to the required standard. Additionally, effective communication assists in improving morale and motivation to work as being able to communicate accordingly means to be able to understand each other to reach a given goal, consequently motivating someone to improve and exceed expectations. However, should not simply be done verbally but rather also through text using communication platforms such as Microsoft teams, WhatsApp, or Discord, however, it should obviously be notated that when doing so it should be done respectively and at appropriate times. That is the case since in the case since if a point was no understood clearly, being able to communicate through said platforms should ensure that time is not wasted, and that work can be done effectively.*

Importance of personal research: *Although understanding through communicating with peers or supervisors is certainly important, being able to depend on oneself and research on the topics that are required to be understood is an important skill that should not be underestimated, since in the circumstance that getting in contacting with someone that could be of assistance is not an option, then researching through the use of the internet and books would become a necessity, and being able to interpret information form documentations effectively would considerably assist in doing so to the point where it could be more reliable then asking a supervisor as information online are widely available, easy to get, and generally go into much more detail. However, it is important to identify the difference to what might be opinion to that of a fact, as not anything that is found on the internet can be immediately considered true unless it is either well documented and multiple resources mention it or if it is stated by a reliable source such as a known author or company. Overall, personal research is able to develop self-confidence*

Communication between peers and supervisors: *For the majority of the time, I personally feel that the way communication was handled between by the supervisors was relatively poor, which was the case for two significant reasons. The first of which being the lack of theoretical explanation, in that in the circumstance that something did not work, only the practical solution was shown and explained, and without explaining the theoretical significance behind the change made, the actual solution would not be understood, meaning it is not ensured that the issue does not occur again, however, even when asked more than once, hesitance was shown in explaining the theory. The other reason being that text or indirect communication was negligible excluding one or two times, in that it was necessary to meet the supervisors in person in order to ask questions about*

the assessments, which generally hindered the flow of work and overall productivity. With that being said, supervisors nonetheless were able to assist and explain the assessment sufficiently to a point where depending on them was not necessary and personal research all that was required with the exception for a few circumstances. On the other hand, I feel like my personal communication was sufficient as it allowed me to interpret the necessary information from the resources provided by supervisors and the assignment briefs while also being able to communicate with peers effectively in order to assist one another in the development processes.

Potential improvements: *As stated, the main two issues were the lack of theoretical explanation on certain issues and mistakes that were made as well as the lack of external communication outside of the institution even when done appropriately. Although the stated issues are not ones that can be controlled by us, there are nevertheless recommendation that could be implemented in order to potentially improve the way that communication was handled overall. Said recommendations being to try and be more communicative with the supervisors as to try and understand more of the theoretical significance behind mistakes that were made from them. As well as that, specific times should be organized with consultancy of our supervisors for external or indirect communication with them.*

Using skills developed for further studies

Awareness of benefit: *Being eager to learn and improve is an essential aspect of personal development and growth, and way in which a person could enhance that is by learning from any hardships that were went through and utilizing and retaining the skills learned throughout practical experiences, and a perfect example of which being the two assessments being discussed in this report. The main importance lies in the fact that whatever skill or knowledge it may be that has been learned, it will be beneficial whether directly or indirectly, in that it may prove to be of assistance as a skill that provides another gateway of performing a certain task, or on the other hand, it could be a skill that assists generally in both personal and professional life.*

Use of behavioral skills: *As shown, the behavioral skills that were mainly utilized and developed throughout both assessments were time management and communication, which were developed by having to constantly manage our time throughout both of the given assessment as well as continuously trying to communicating with our supervisor as well as our peers in order to achieve the required tasks. Although the stated skills are not directly related to electronic or engineering skills, they are nonetheless extremely important going forward in fields either related to engineering and mechatronics or ones that are not. In that a skill such as being able to effectively communicate with a superior or a coworker or being able to manage the timeline of a project efficiently and effectively are both necessary skills for a person's everyday life or when working in projects of real significance and importance with financial consequences relating to work inefficiency.*

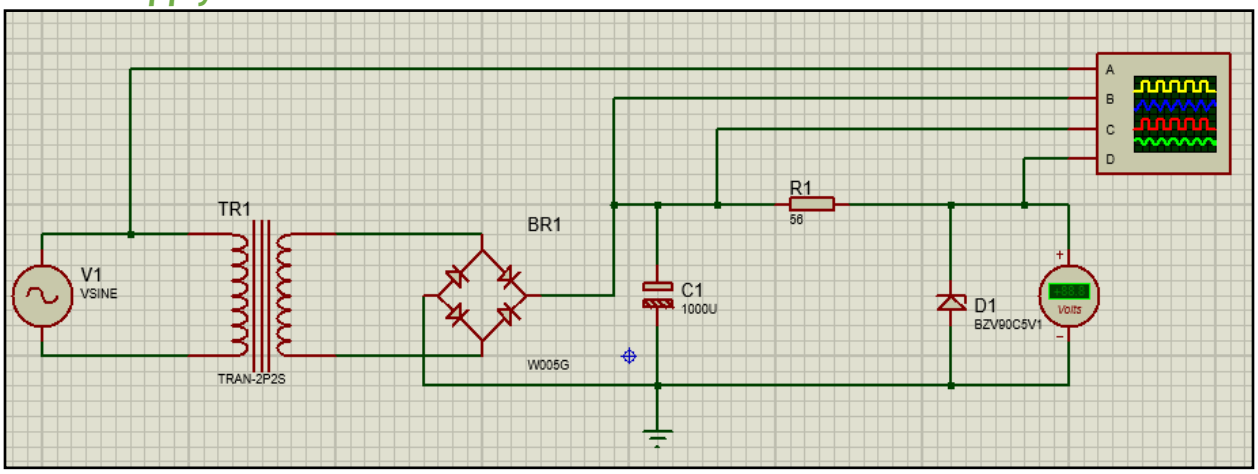
Use of knowledge and practical skills: *All of the stated knowledge and practical skills that were gained throughout both assessments are what can be considered active skills, which are skills that are used in certain circumstances when they are required in carrying out a given task. In that the theoretical aspect of semiconductors within devices can be used as a way of knowing the intricacies of each device, which consequently assists in solving issues and problems that could potentially hinder their performance or functionality. While practical skill and knowledge of different devise and their applications may assist in developing circuits in further study, in that devices such as transistors and diodes are utilized in almost every electrical circuit, operational amplifiers be used in amplifying the voltage or in specific circumstances in which inverting the waveform is required, and finally, logic gates and flip flops are fundamental components of computer circuitry and computer engineering as they assist in performing computational functions and storing memory. In addition to that, other practical skills such as using CAD drawing and simulation programs being extremely useful skills and could be utilized in a multitude of fields going forward when it comes to designing models or drawing schematics even if they are not related to electronics, in that the skill of being able to use CAD is important on its own. Moreover, practically doing applied mathematics is very important to experience as it gives an example of how research during further education or real projects would be like. Furthermore, building actual circuits prepares for the variety of issues that could be encountered when building circuits in real life in comparison to doing so digitally, as it is a very important to skill when working on actual projects.*

Analysis of the developed circuits

Brief:

The following section will discuss and analyze the electronic circuits that were developed throughout both assessments while additionally suggesting potential improvements to the development process for each circuit. The main areas of the development process involved simulating, constructing, and testing the circuits, hence they are going to be the main areas of discussion throughout the following section.

Power supply circuit



Circuit analysis: *The shown circuit represents the common circuitry utilized in converting an AC to DC within a power supply. The way in which the circuit works can be split into four different sections, with the first of which being a transformer which is simply utilized in order to decrease the initial voltage going through the circuit from the power plug. From there, a full-bridge rectifier is utilized, a component made up of four diodes that is able to blow the flow of current when it returns, which assists in blocking the flow of current from returning during the negative phase of the cycle, consequently emitting the entirety of the negative signal, resulting in a pulsating current. After which, the current run through a capacitor, charging the capacitor with a given amount for a short period of time which is then released back into the circuit, with the stated process causing a decrease in the pulsating currents intensity, causing the signal to be smoother. Finally, the last phase of the circuit is for the current to pass through a Zener diode in reverse bias, causing the voltage to be regulated due to a Zener diode's properties, which is the final step required in order to fully smoothen out the pulsating signal and result in a Direct Current.*

Circuit development:

Simulation: *Proteus was used as the program of choice when simulating the circuit, due to the power supply circuit being the first circuit from the initial assignment, it was also the first time that Proteus was utilized, as such, it took quite a bit of time to run and get to know the program, however, from there, the simulation process began by placing the AC power supply and oscilloscope onto the drawing board and then placing and connecting the components from left to right. After which, when the simulation itself was started, for an unknown reason the second signal – which is meant to be the one after full bridge rectifier – provided a signal that looked as if the signal came after the capacitor, with the reason going unresolved due to time constraints.*

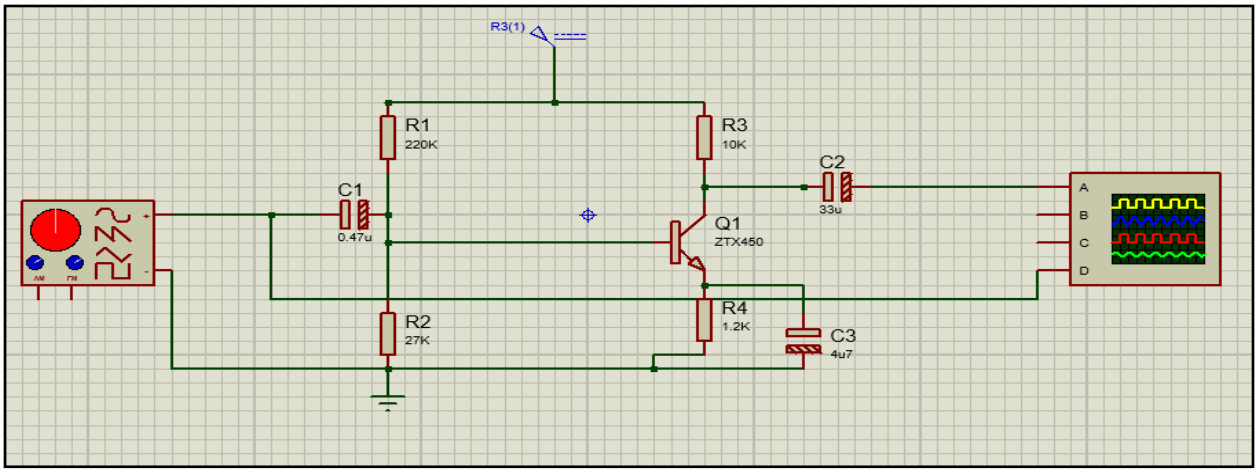
Construction: *During the construction process, following the exact same components as that which were used in the simulation was not possible due to the lack of a mini transformer, as such, however, due to the transformer not being a necessary component since the power supply that was used could generated low enough voltages for the circuit, the way the transformer was replaced was by simply decreasing the voltage from the power supply to one that would be appropriate for the circuit. Otherwise, the construction process went smoothly without any other issues, with a breadboard being the board and the construction process starting from the full bridge rectifier and then working slowly towards the right of the circuit diagram.*

Testing and comparison to simulation: *After the circuit has been constructed, Male-Male were placed after each major component of the circuit (power supply, full-bridge rectifier, capacitor, and Zener diode) in order to connect the clip from the*

oscilloscope and test the circuit. From there, the way the circuit was tested was by initially setting the amplitude and the time period appropriately and then calculating the amplitude and frequency of each signal using the formulas $A = \frac{(Height \times V_{div})}{2}$ *and* $Length \times T_{div}$. *Overall, compared to the simulation, the values gotten were relatively, with only few inconsistencies that were to be expected, with the only major difference being the issue that was gotten with the second signal wave signal providing a smoothed output rather than a pulsating signal, which is an issue that was not encountered during testing, which probably means that the issue was a visual issue that stemmed from the utilized software.*

Development improvement: *When it comes to the simulation process, a potential improvement that could have been made was to provide us with a rundown of the CAD software that we were going to use, such as a diagram that explains the User Interface and what were the major buttons or menus that we had to look out for. Additionally, for the construction process, further planning should have been made in order to ensure that all the required components were available prior to starting the assignment itself. Finally, for the testing process, although there are not any necessary improvements that have to made, testing varying capacitor values in order to see how each could effect the final output of the circuit could have been an added layer of testing that would be interesting.*

Transistor amplifier circuit



Circuit analysis: *The shown circuit represents that of an amplifying transistor circuit. Other than that, the other components that were utilized within the circuit were three capacitors and four resistors, one capacitor and two resistors being at the input, one collector and resistor before the collector pin, and one collector and resistor at the output after the emitter terminal.*

Circuit development:

Simulation: *Due to the transistor amplifier circuit being only the second circuit to be made for the assessments, some issues were still faced during the simulation process related to inexperience with using the simulator program that was being utilized (Proteus), which led to being slightly behind on time. However, other than that, no problems were faced during the simulation process, with the simulation diagram being drawn by going from the function generator on the left to the oscilloscope on the right.*

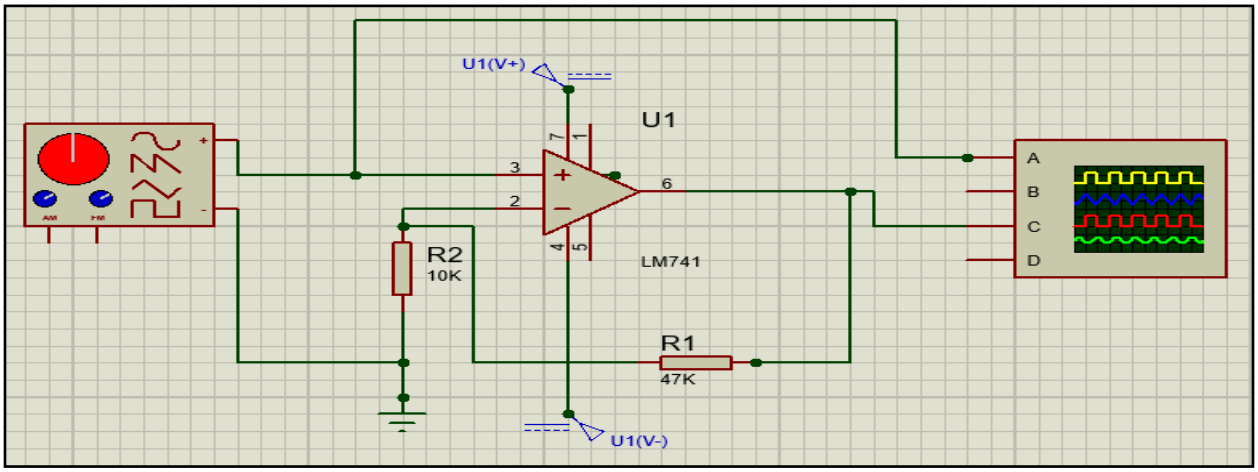
Construction: *During the construction process, the transistor was the first component to initially be placed onto the breadboard, with the wiring then branching out from it. This was done in order to make the construction process simpler as it would be easier to place all the components without under or overestimating the number of breadboard pins required.*

Testing and comparison to simulation: *The main areas in which the circuit was tested was through calculating the amplitude of the value before and after amplification in order to calculate the overall gain of the circuit. However, due to the stated difference in resistor and capacitors, a major difference was found between the simulation and actual measurements, and although a difference were to be expected, it should not have been as significant as it actually was, with led to the belief that the issue stems from the simulator rather than the difference in components, as said difference was rather small.*

Development improvement: *A potential improvement that could have been done to the circuit development process is to ensure beforehand what were the available components at the institution were in order for us to utilize the same ones during the*

simulation process, which would have clearly identified if the reason was due to the components or a simulator-related issue. Other than that, there are no other major improvements that could have been made to the development process other than potentially testing the circuit with the use of different capacitors and resistors in as a way of acquiring further data for analysis and seeing the effects of said components on the amplified output of the circuit.

Non-inverting op-amp circuit



Circuit analysis: *The following circuit represents an operational amplifier which outputting a non-inverted signal, which can be proved by seeing that the pin two (the inverting pin) is the one that has been gotten grounded, rather than pin three (the non-inverting pin), which is connected to the function generator which is the pin's main power source, additionally, it should also be noted that the second pin is connected to two resistor, with one leading the terminal to ground, while the other is going to the output terminal, causing the feedback loop mentioned within the knowledge gained section. The power supply causing the IC to function can be seen being given from terminals 7 and 4, with 7 being the terminal utilizes for the positive Vcc while 4 for negative Vcc as the operational amplifier shown is working with an Alternating Current. Finally, the output of the operational amplifier is connected to an oscilloscope for the sake of testing the circuit and measuring values in order to utilize them in calculating the gain.*

Circuit development:

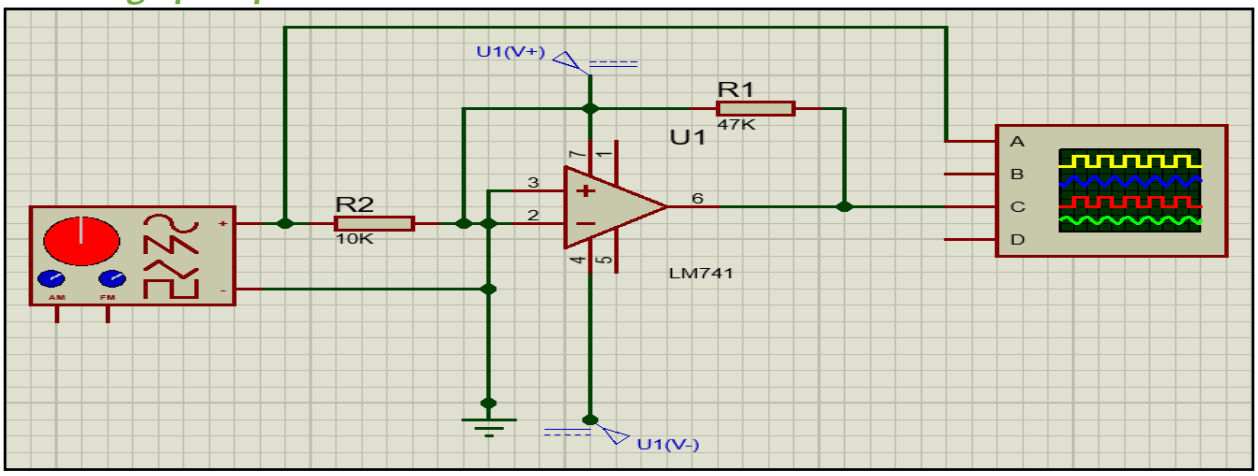
Simulation: *The simulation process for the inverting op-amp circuit was done using Proteus, due to us being familiar with the User-Interface of the program at this point, the simulation process was done relatively quickly without any issues. With the way that the diagram was drawn being by placing the op-amp in the middle and selecting each pin and connecting it to wherever it was required.*

Construction: *Constructing the op-amp was our first time utilizing an IC, and it was rather different in comparison to simply drawing the diagram from the circuit due to the availability of additional pins that are not available in the simulator. However, the supervisor showed us how the connections were meant to be made on a breadboard, and as such, utilizing the IC practically was a relatively simple task. Just like with the simulation, constructing the circuit was done by initially placing the IC in the middle of the breadboard and then branching out to the required components of the circuit. No major issues were run into during the construction process, however, it should also be noted that the construction process was done as groups rather than each person working on their own circuit.*

Testing and comparison to simulation: *The testing process for the non-inverting op-amp circuit that was developed was done by connecting the oscilloscope terminals to two Male-Male wires placed on the breadboard, with one of them being placed right after the power supply in order to show the initial value before amplification, with the other being placed at the op-amp's output terminal to show the outputted/amplified value. From there, the calculations that were made revolved around trying to get the gain using the formula* $\frac{V_{out}}{V_{in}} + 1$*, with Vout being gotten using the amplitude formula that was stated earlier. Compared to the simulation, the results that were gotten were slightly off, which was the case since it was realized during the construction process that the resistor available had a slightly off resistance than the one used in the simulation for both the 47k Ohms and 100k Ohms circuit, otherwise, the results were relatively similar.*

Development improvement: *Although there we no issues in terms of simulation process itself, the type ore resistors available at the institution should have been checked prior to simulating and drawing the circuit, as this would have provided more accurate results when it comes to testing the constructed circuit. Additionally, another improvement that could have been made during the construction process is to have everyone work on their individual circuits, as this way, each person would be able to work more easily and clearly. Finally, during the testing process, an improvement that could have been made was to calculate other parameters such as the frequency or time period as a way of having additional data for further analysis.*

Inverting op-amp circuit



Circuit analysis: *Unlike the non-inverting op-amp circuit, it can be noticed within this one that pin three (non-inverting pin) is the one that has been grounded, and from which it can be deduced that the circuit is going to output an inverted signal, with pin two (inverting pin) being initially connected to a resistor leading to the function generator which is acting as the pin's power source, additionally, the signal from the function generator is taken to output through an additional resistor, creating the aforementioned feedback loop. Just like with the previously shown circuit, pins four and seven are also connected to a positive and negative Vcc, which is utilized in order to run the operational amplifier. Finally, the output pin is connected to an oscilloscope for the purpose of testing the circuit and measuring values in order to calculate the op-amp's gain properties during inverting amplification.*

Circuit development:

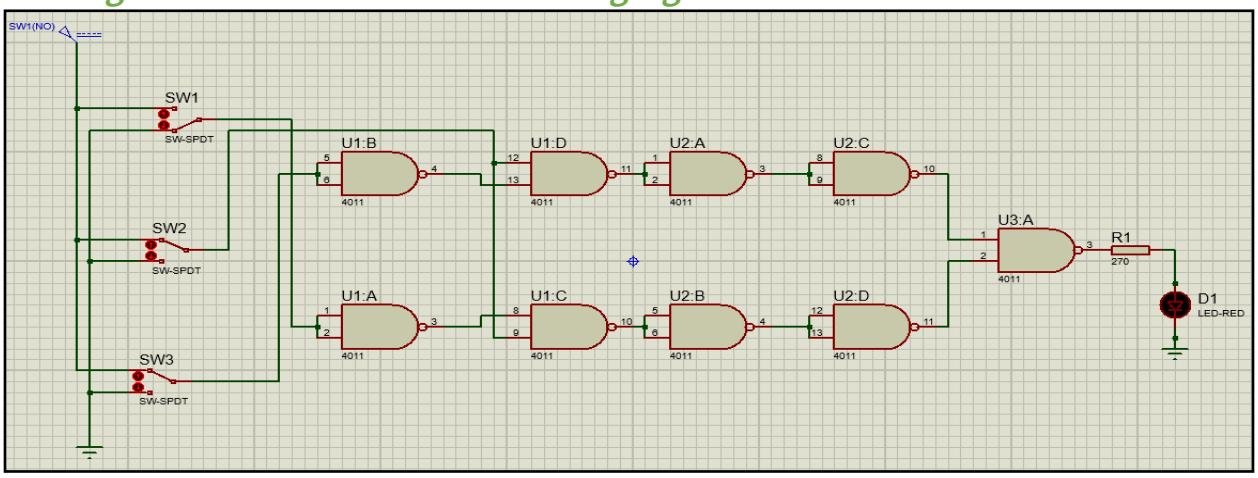
Simulation: *The simulation aspect of the inverting op-amp circuit was done relatively quickly and within the same session that was used for the inverting op-amp, which was the case due to the major similarity seen between the two circuits, meaning only slight changes had to made in order to convert the circuit from non-inverting to inverting, with said changes involving changing the grounded pin from pin two to pin three and changing the position of the resistors.*

Construction: *Just like with the simulation process, construction for the inverting circuit was done during the same session as the non-inverting one as the changes that had to be made to the circuit were relatively insignificant in terms of time consumption and effort as only 3 wires' location had to be changed and the resistor on the circuit had to be moved. This also means that constructing the circuit was done as a team rather than each person working for their own.*

Testing and comparison to simulation: *In order to avoid repetition, the testing process would not be explained again as it was the same as the one previously mentioned for the non-inverting circuit. However, it should be noted that this time around, the calculations revolved around working out the amplitude of the Vout in order to utilize it in the following calculation:* $-1\left(\frac{V_{out}}{V_{in}}\right)$. *Overall, just like with the other circuit, the values that were gotten from the measurements and calculations were slightly off in comparison to that of the ones deduced from the simulation due to the unavailability of the required resistors.*

Development improvement: *Since the non-inverting and inverting circuits had almost the same development processes, the potential improvements to the process for the inverting circuit is the same as the ones stated earlier within the non-inverting section. As such, in order to avoid repetition, the improvements would not be mentioned again.*

NAND gate converted combinational logic gate circuit



Circuit analysis: *The initial circuit that was simplified with the use of the Karnaugh map constituted of three switches that control the input values, with switch one going into a NOT gate that controls one terminal from the second AND gate, the second switch goes into one terminal in both AND gates, and switch three going into a NOT gate that controls one terminal from the first AND gate, from there, the output of said AND gates goes into a single OR gate. When considering the conversion process for each of the stated logic gates into NAND gates, the shown circuit is gotten. In that the NOT gates are replaced with a single NAND gate with a single signal controlling both pins of the NAND gate. From there, the AND gates following the two NOTs are replaced with two NAND gates for each AND, with the NAND gates being placed subsequent to each other, with the first having two INPUTS placed in the same way as it was stated earlier for the AND gates in the initial circuit, with the second NAND gate's terminals being both connected to the previous NAND gate's output. After that, in order to create the NAND gate equivalent of an OR gate, two NAND gates are placed with their input terminals being both connected to the output of the previous NAND gate (the NAND equivalent of the AND gate) and their output being connected to another NAND gate's terminals, with said NAND gate's output being the final one which is connected to an LED.*

Circuit development:

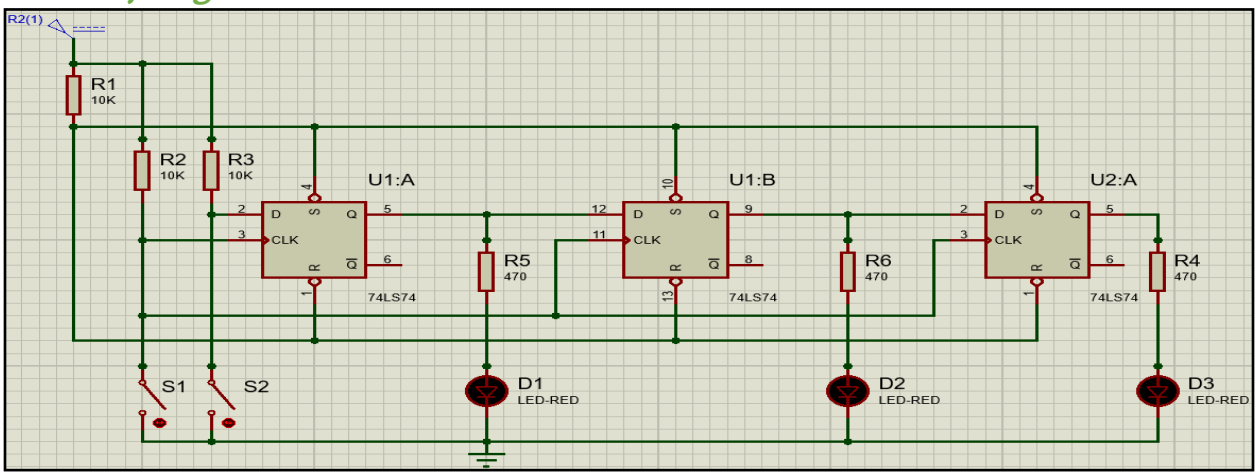
Simulation: *The simulation process of the logic gate initially went through three different phases. The first was when the circuit utilized the simplified Boolean expression (*$Y = \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot C + A \cdot B \cdot \overline{C}$*), meaning the simulation included a logic gate for each of the of the shown functions in order to achieve the required values from the truth table. From there, a Karnaugh Map was used in order to minimize the circuit, and due to the HIGH values being 010, 110, and 011, the Karnaugh Map's layout resulted in the values being next to each other both horizontally for 010 and 110 as well vertically for 010 and 011, which led to the Boolean expression being simplified to (*$Y = B \cdot \overline{C} + \overline{A} \cdot B$*), which was then simulated and also provided the required results. From there, the circuit was once again converted so that it contains NAND gates only using the methodology stated in the circuit analysis, from there, the circuit was simulated once again. Overall, the simulation process was quite lengthy, however, some aspects of the initially simulated circuit such as the LED and the switches remained the same throughout all simulated circuits, which helped in decreasing the time consumption for the simulations.*

Construction: *Although three different circuits were simulated, only the final one required being actually constructed (The NAND equivalent of the simplified circuit). Due to the number of terminals seen within the NAND equivalent circuit being bigger than what would be capable of being constructed using one IC which was available at the institution, 2 different ICs had to be utilized. The way the circuit was constructed was that the ICs were initially placed onto the breadboard, and from there the wiring branched out onto the other section of the circuit, which was done in order to try and make the circuit tidy and ensure that all wires were connected successfully. Most of the construction process went smoothly, however, an issue that was faced was that some people misplaced certain wires by placing input signals into output terminals and vice versa.*

Testing and comparison to simulation: *The testing process for the circuit did not involve anything as intensive as what was seen from the previous circuits, in that testing the circuit simply involved checking if the combinational logic circuit was able to output the same values as the ones seen from the truth table. Overall, the outputted values from the simulation compared to the practical testing were the same without any deviations from the truth table being noticed.*

Development improvement: *There are no major improvements that could be made to the development process for the NAND gate equivalent combinational logic gate due to most of the development process going smoothly, however, a single improvement that could have been made to make working with the IC less confusing would have been to print a guide image that shows the input and output terminals within the IC, which would have assisted in making sure that people constructing the circuit do not misplace wires.*

3-bit shift register



Circuit analysis: *Overall, the 3-bit shift register circuit constitutes of three different D-Type flip flops. Initially, the circuit constitutes of a 5 volt power supply that is connected to three 10k ohm resistors, with said resistors going to the first flip flop's Data and a wire the transmits a signal to each flip flop's Clock pin, with the Clock pin's ground being blocked off using a switch, meaning current would not circulate unless the switch is closed. From there, the first flip flop's output powers an LED as well as the subsequent flip flop's Data pin, with the same configuration for the output being seen for the second and third flip flops. In terms of the function of the circuit, it should initially be noted that the first flip flop already possesses a HIGH signal within its Data terminal due to the signal being provided from the initial 5 volt power supply, however, its clock has not went to its rising edge yet since it is blocked off with the switch, therefore the output for the first flip flop is LOW. What this means is that when the switch is closed, the clock pin would go to its rising edge, and send a signal to every flip flop's Clock pin, however, only the first flip flop would transmit a HIGH output since it is the only one with a HIGH Data pin, and therefore the initial LED would turn on, and the Data pin for the second flip flop would receive a HIGH signal since it is connected to the first flip flop's output pin. This means that the second time the switch is closed, a signal would once again be sent to each Clock pin, however, this time, the second flip flop's Data would have been HIGH due to the first flip flop's HIGH output, consequently causing the same operation that occurred with the first flip flop to happen again but with the second flip flop, in that the second LED would turn on, and the third flip flop's Data pin would be HIGH. Thus, the third time the switch is closed, the third LED would turn on since the third flip flop's Data pin is currently HIGH.*

Circuit development:

Simulation: *Simulating the 3-bit shift register was a rather long process due to the size of the circuit being relatively bigger in comparison to what was previously drawn, and the wiring looked somewhat confusing from a drawing perspective, which at certain points led to time issues that some had to face. However, other than that, the simulation process went smoothly without any significant issues.*

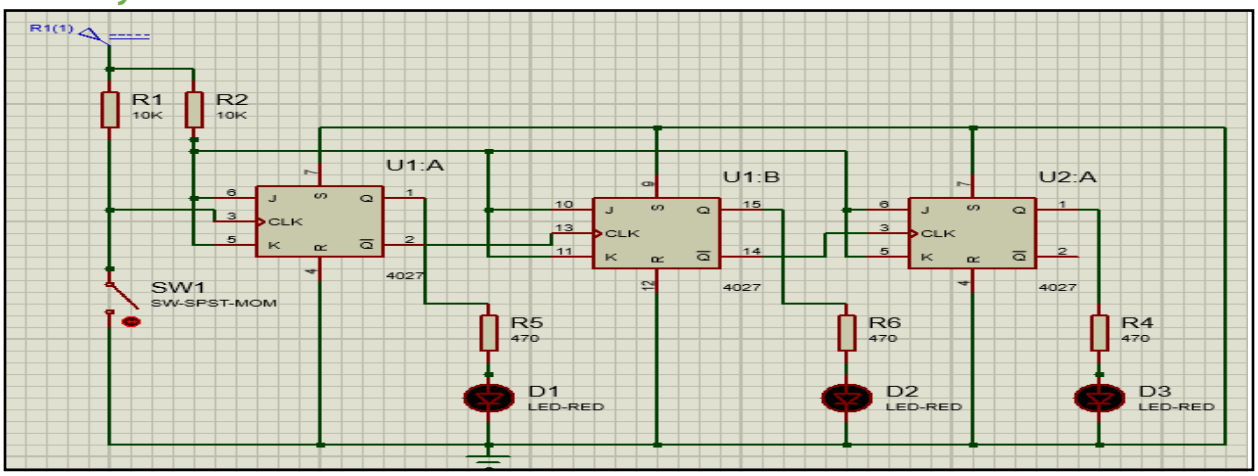
Construction: *The construction process of the 3-bit shift register was somewhat cluttered and unorganized due to the fact that the available breadboards at the institution were mini breadboards for the exception of two or three normal sized breadboards that were available but certainly not sufficient compared to the quantity that was required. This was a major issue as the circuit required the use of 2 different 14 pin ICs as the specific flip flop that was used was the 74HC74 dual D-Type flip flop with positive edge triggers, which was a lot to be placed on a mini breadboard, which led to the overall circuit being unorganized and somewhat cluttered. In addition to that, not all the wires which were available were jumper wires, which led to further issues in terms of placing wires onto the breadboard as normal wires can easily fall out of breadboard pins especially when considering the huge quantity of wires that have to be used for the 3-bit shift register circuit. As such, the way that the circuit was placed was that the ICs were initially placed onto the breadboard, and from there, all the required resistors and LEDs were placed so that the final step of connecting the components together using wires would be easier to do since only the breadboard would be relatively tidy. In addition to what was mentioned, at the time of construction, switches were not available, therefore pushbuttons were used instead.*

Testing and comparison to simulation: *Just like with the NAND gate equivalent combinational logic gate, the 3-bit shift register's testing process simply involved checking if the circuit is able to provide the required outputs from the truth table, which is the case due to the circuit's purpose not having any involvement with electronic parameters such as the voltage, current, or resistance, but rather it is used for transmitting binary data from one flip flop to another, which is what the testing procedure showcases. However, it should be*

noted that one issue that was encountered during the testing process that was due to the utilization of a pushbutton instead of switch, in certain circumstances, the pushbutton would transmit two signals at a time due to the person using it pressing it for a relatively long duration on accident, and although it was not a major issue, it was inconvenient at times.

Development improvement: *Both the testing and simulation processes went smoothly and as expected, as such, neither of them require any improvements. However, the construction process on the other hand had major organizational issues due to the small space available to work on in comparison to the circuit's relatively big size. As such, an improvement that could have been made was to provide longer breadboards as it would have made the construction process much more organized, and thus much easier. Additionally, more jumper wires should be provided especially when the quantity of wires required is huge as they assist in ensuring wires stay in place and cannot easily fall out. Additionally, a potential addition to the to the construction of the circuit itself is inclusion of use of a secondary switch – the one seem in the circuit diagram itself – for resetting the circuit, since with the current circuit configuration, the switch does not have any particular use, as such, by connecting the switch to the wire going to every flip flop's reset pin, closing it would cause a rising signal to be sent to the reset pins, and therefore resetting the flip flops, which could be a useful functionality for the circuit that would provide it with greater functionality and flexibility.*

3-bit asynchronous counter



Circuit analysis: *The 3-bit asynchronous counter circuit mainly constitutes of three JK flip flops. The initial part of the circuits involves a 5 volt power supply connected to two 10k ohm resistors, with the first going to the clock pin of the first flip flop only unlike the 3-bit shift register which had the clock pin going to every flip flop's clock pin, however, the clock pin's ground is blocked using a switch, meaning in order to send a rising edge signal to the clock pin, the switch would have to be closed. While the second resistor is connected to both the J and K pins of all flip flops, thus causing a toggle procedure to the output of the flip flop whenever the clock pin reaches its rising edge. From there, each flip flop's Q pin goes to an LED that is connected to a 470-ohm resistor, while their QB pin goes to the subsequent flip flop's clock pin. Meaning that whenever a flip flop's QB pin reaches its rising edge, the following flip flop's Q pin will become HIGH and the following LED will turns on. If the first three iterations of the circuit were to be taken as an example, what would occur is that when the switch is closed, the first flip flop's Q pin will become HIGH, and its QB pin will become LOW, meaning only the first LED would turn on. From there, if the switch were to be closed a second time, the first flip flop's Q pin will toggle back to LOW, turning off the first LED, while its QB pin will become HIGH, consequently, the second flip flop's clock pin will reach its rising edge, therefore the second flip flop's Q pin will become HIGH turning on the second LED. After which, if the switch were to be closed for a third time, the first flip flop's' Q pin will become HIGH, which will turn on the first LED, and the QB pin will become LOW, however, the second flip flop will not be affected since its clock pin went to LOW due to the first flip flop's QB also becoming LOW, however, a flip flop is only affected when the clock pin reaches its rising edge, not when it toggles between HIGH and LOW. Overall, the stated operation will repeat for four more iterations, which would overall result in a special LED configuration each time, after which, when the switch is closed for the eighth time, the cycle will repeat and go back to the initial iteration of the circuit.*

Circuit development:

Simulation: *Due to the resembles seen between the 3-bit shit register's and 3-bit asynchronous counter's circuitry, in order to save time, what was done is that the same file utilized for the 3-bit shift register's simulation was utilized, with the major changes that were made being the flip flop that was utilized, the exclusion of one additional resistor that is found in the 3-bit shift register's circuit, and the addition of some wires that*

were utilized for the J and K pins. After doing so, the simulation nonetheless showed the expected results, which were the ones from the truth table.

Construction: *Just like with the 3-bit shift register, two different ICs had to be used and a bigger breadboard was unavailable, forcing us to use mini breadboards for a circuit that is relatively big for such a small board. While the issue being even bigger here due to the addition of two extra pins that are seen with the JK flip flops, with the one that was specifically utilized being the 4027B dual JK flip flop with positive edge trigger. As such, the same issue that was encountered during the construction process of the 3-bit shit register was also encountered here, except for the fact that more jumper wires were available as well as switches this time.*

Testing and comparison to simulation: *Just like with the previous two circuits, the testing process simply involved checking if the final output for the circuit followed the same outputs as the truth table, which was the case for this circuit, in that the LED configuration for each iteration of the counting process was the same configuration as the one seen from the truth table. As stated, switches were available during the construction process of this circuit, therefore no issues were encountered where two signals were being sent at a time.*

Development improvement: *Due to the similarities found within the development processes of both 3-bit shift register as well as the 3-bit asynchronous counter circuits, the improvements that were stated for the 3-bit shift register can be utilized for the 3-bit asynchronous counter. Therefore, for the sake of avoiding repetition, the potential improvements to the development process would not be stated once again here.*

Conclusion

What went well?

Although negative statements were made about the time management, communication between supervisor, and the development processes for the circuits that were constructed, the majority of the assessment period for the initial and second assignments has nonetheless rather went well, with most sections going as planned and as a whole out having learnt a lot from the assessments.

Overall, the sections or aspects that went without hinderances were most of the theoretical and knowledge-based aspects of the assessments such semiconductors and device's theory due to the guidebooks that were utilized and research that was done on was really helpful in learning them. Additionally, most of the practical sessions went well in both health and safety and utilizing said sessions in order to do actual work, in that all health and safety precautions were followed, and no major issues were run into due to faulty equipment, components such as the devices themselves, or the computers and laptops that were being utilized in simulating the circuits.

Finally, personal communication skills and their development went extremely well, as working in a team in order to assist and get assisted by peers was a major aspect of the assessments. In terms of the development processes however, only developing the power supply and NAND gate equivalent circuits were the ones that went well without any major obstructions.

What could have been better and its potential improvements

There are three major areas in which they could have gone better or have been handled more appropriately, with them being the time management, communication with the supervisor, and the availability of the required components.

In terms of time management, it did not go well due to the inefficient way that time was distributed between different sections, with the research section having significantly less time than some of the construction or simulation sections, which did not necessarily require the amount of time they were given. A potential method of improving such issue is to either increase the overall time given or change the distribution appropriately and accordingly relative to the sections that necessitate the most amount of research and time.

With regards to the communication with the supervisor, as stated earlier, the main issues with it was the lack of theoretical explanation as well the minimal time available in it was possible to communicate with the supervisor. Ways to improve this issue for the following projects or assessments is to organize beforehand times in which we could communicate with our supervisor with the use of online communication platforms such as WhatsApp or Discord. Additionally, extra sessions could be made purely for theoretical explanation, although this could potentially lead issues related to time distribution, what could done is replacing some of the practical sessions for the stated theory explanation of the circuits and devices, since – as stated earlier – the time given for practical sessions was more than necessary.

Finally, the last major issue concerns the unavailability of the required components, specifically the current resistors and capacitors, which hindered the testing process as it led to making many assumption when comparing the simulation and measured results. Resolving this issue is rather simple, as it could be done by checking before starting the simulation process whether or not the required components are available, and if not, then a simple change in the resistor and capacitor value within the simulator would resolve the issue.

“*Nothing is too wonderful to be true if it be consistent with the laws of nature*.”

-Michael Faraday

Inventor of the first electrical motor