LVDS (Tx/Rx) Design
With 5V Devices in Sky130nm Process
Simulation Methodology

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Revision 0.0

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1. Versioning Information

1.1 Tool version:

SkyWater 130 nm PDK version 1.0.437-2-g8a7d53a

Xschem V3.4.2

NGSpice ngspice-41

2. Design parameters

LVDS Transceiver

Frequency: 1 GHz

Following are the PVT corners for which the design was simulated:

Process corners: TT, SS, FF, SF, FS

Voltage variations by 10 percent: 4.5V, 5.5V

Temperature extremes: -40C. 125C

	Models	Vcc	Junction Temp(C)
1	TT	5	25
2	TT	5	-40
3	TT	5	125
4	TT	4.5	25
5	TT	4.5	-40
6	TT	4.5	125
7	TT	5.5	25
8	TT	5.5	-40
9	TT	5.5	125
10	SS	5	25
11	SS	5	-40
12	SS	5	125
13	SS	4.5	25
14	SS	4.5	-40
15	SS	4.5	125
16	SS	5.5	25
17	SS	5.5	-40
18	SS	5.5	125
19	FF	5	25
20	FF	5	-40
21	FF	5	125
22	FF	4.5	25

23	FF	4.5	-40
24	FF	4.5	125
25	FF	5.5	25
26	FF	5.5	-40
27	FF	5.5	125
28	SF	5	25
29	SF	5	-40
30	SF	5	125
31	SF	4.5	25
32	SF	4.5	-40
33	SF	4.5	125
34	SF	5.5	25
35	SF	5.5	-40
36	SF	5.5	125
37	FS	5	25
38	FS	5	-40
39	FS	5	125
40	FS	4.5	25
41	FS	4.5	-40
42	FS	4.5	125
43	FS	5.5	25
44	FS	5.5	-40
45	FS	5.5	125

3. Steps to Simulate

Steps for running simulation:

1. Draw the Schematic
2. Include the libraries, the process and temperature for the simulation

   For eg.

```
.lib
/usr/local/share/pdk/sky130A/libs.tech/ngspice/sky130.lib.spice
tt

.include
/usr/local/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky1
30_fd_sc_hd.spice

.option TEMP=-40C
```

   for TT models and simulation temperature of –40C.

3. Extract the Netlist
4. For DC Simulation, include the following code for the swept voltage source, in the netlist:

```
.dc srcnam vstart vstop vincr
```

   For eg.

```
.dc V2 0 5V 1m
```

   to sweep V2 from 0 to 5V in steps of 1 mV

5. For Transient Simulation, include the following code in the netlist:

```
.tran tstep tstop tstart
```

   For eg.

```
.tran 0.2n 15n 5n
```

   for transient analyses in steps of 0.2 ns, from 0 to 15 ns, outputs getting stored from 5 ns

   Note: The simulation always starts at 0, tstart is the time when outputs start getting stored

   A. For simulation with regular voltages pulses, the above step is sufficient
   B. For simulation using PWL (Piece-wise linear) sources,

```
V6 INP Vss PWL(0 3.5 10n 3.5 10.3n 3.3 10.5n 3.3 10.8n
 3.5 11n 3.5)
```

```
+ r=10n
```

Here, V6 is a PWL source connected between nodes INP and Vss. It starts at 3.5V, stays 3.5V till 10ns, transitions to 3.3V by 10.3 ns, stays at 3.3V till 10.5 ns, transitions to 3.5V by 10.8 ns and stays at 3.5V till 11 ns.

r=10n implies that once the first pulse ends (here, at 11ns), the cycle is repeated from 10ns, periodically

6. Run the Simulation and plot the desired waveform using the ngspice terminal

   For eg.

   ```
   plot Vout
   ```

   to plot signal Vout