Oct 2020
B.Tech. (CE/CE(H)/IT) (IV Semester)
Computer organization and architecture (PCC-CS-402)

Time: 3 hours **Max. Marks: 75**

PART A (1.5 marks each)

Q1 (a) Define Memory Address Register.

(b) What do you understand by bus arbitration?

(c) Perform $(12)_{10}$ - $(14)_{10}$ using 2's complement notation.

(d) What is the difference between a subroutine and an Interrupt Service Routine (ISR) ?

(e) Under what situations the microprogram counter is not incremented after a new instruction is fetched from microprogram memory?

(f) Determine the four pages that are resident in the memory after each page reference change, if the replacement algorithm used is FIFO page if the following references to pages are made: 4 2 0 1 2 6 1 4 0 1 0 2 3 5 7.

(g) Differentiate between SRAM and DRAM.

(h) How many memory chips are needed to construct a 2M x 16 memory system using 512k x 8 memory chips?

(i) What are the major characteristics of a Pipeline?

(j) Draw a space time diagram for a 4-segment pipeline showing the time to process six tasks.

PART B

Q2 (a) What are addressing modes? An instruction is stored at location 860 with address field at location 801. The address field has the value 960. A process or register Rx contains the number 800. Evaluate the effective address if the addressing mode of instruction is (i) direct (ii) immediate (iii) relative (iv) register indirect (4)

(b) What are different types of instruction in a basic CPU? Name a few of each type. (4)

(c) Design a 4-bit carry look-ahead adder. (4)

(d) What is RTL? Write RTL representation and interpretation for loading a register. (3)

Q3 (a) Represent 52.21875 in 32-bit binary floating point format. (3)

(b) Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 4-bit registers for holding signed numbers: (i) (+5) x (+3) (ii) (-5) x (-3) (2)

(c) Show the contents of registers E, A, Q and SC during the process of division of (i) 10110011 by 1001 (ii) 11110000 by 0011. [use a dividend of 8 bits.] (5)

(d) Starting from an initial value of R=11110110, determine the sequence of binary values of R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. (5)

Q4 (a) What is meant by Micro programmed Control? Draw and explain the design of such a control unit. (10)

(b) What are static and dynamic memories? Explain. (5) (5)

Q5 (a) With the help of a diagram, describe USB architecture. (5)

(b) Explain DMA. Discuss DMA controller using block diagrams. (5)

(c) Explain program controlled and interrupt initiated data transfer. (5)

Q6 (a) Draw and explain the flowchart for the interrupt cycle. (5)

(b) Explain set associative cache organization with a suitable example. (5)

(c) Explain the different write policies. (5)

(d) What is meant by memory interleaving? Explain. (5)

Q7 Write short notes on:

(i) Pipelining and its hazards. (8)

(ii) Booth's multiplication. (7)

PYQFORT

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