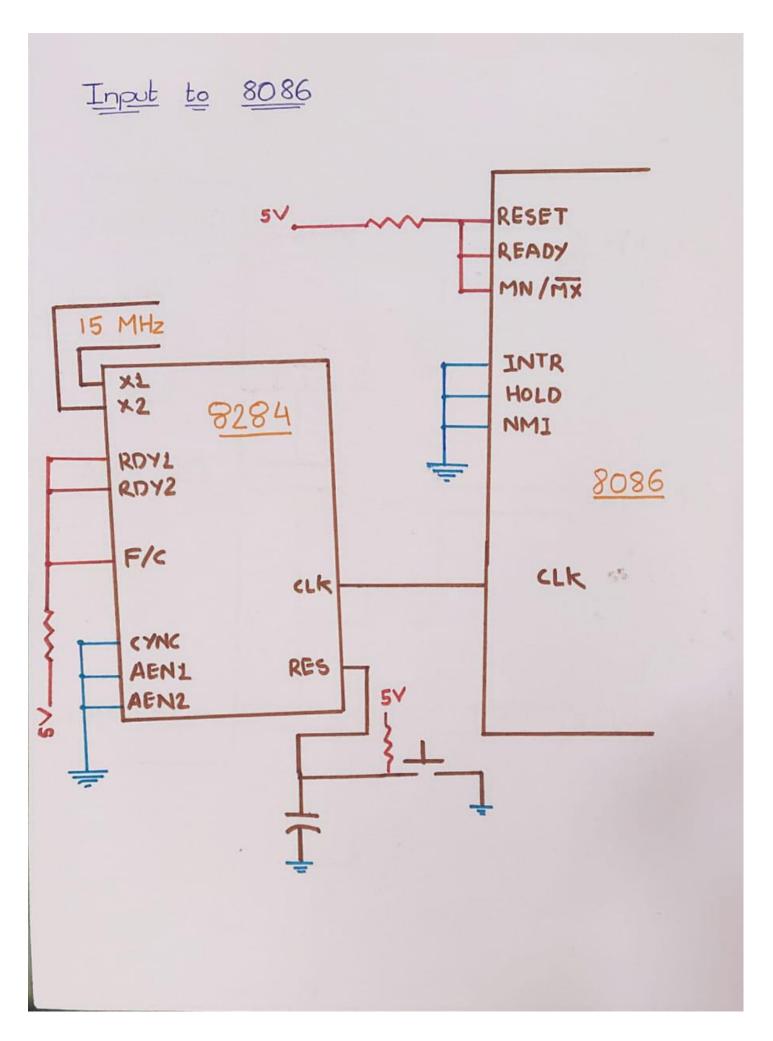
# **Smart Garage System**

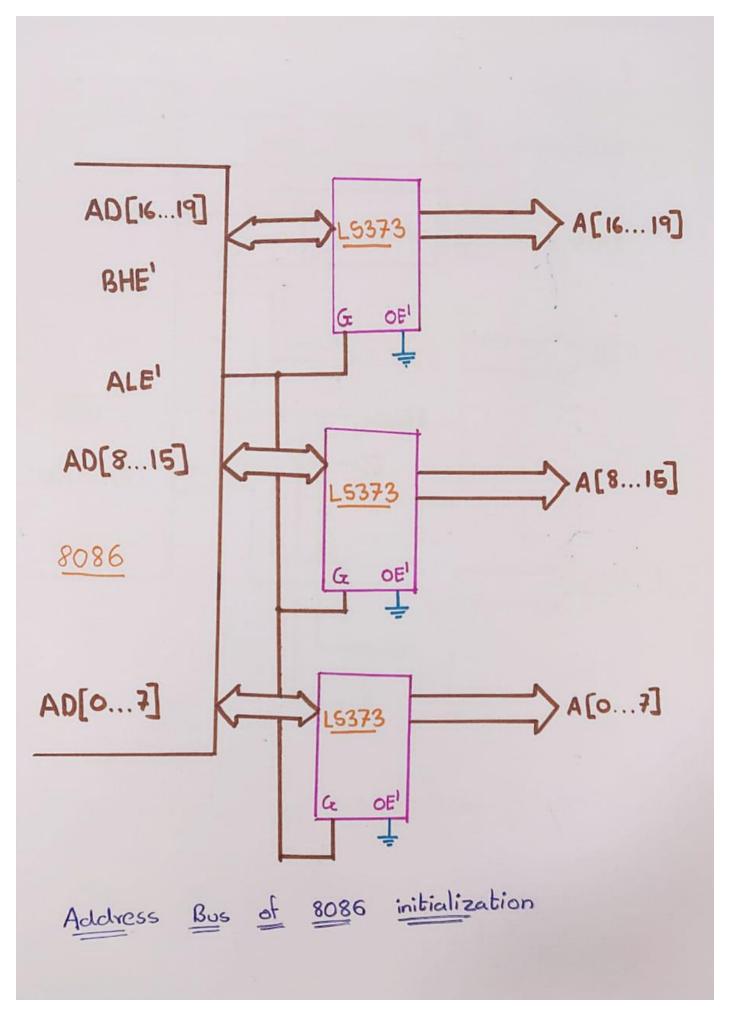
MuP design problem No. 19

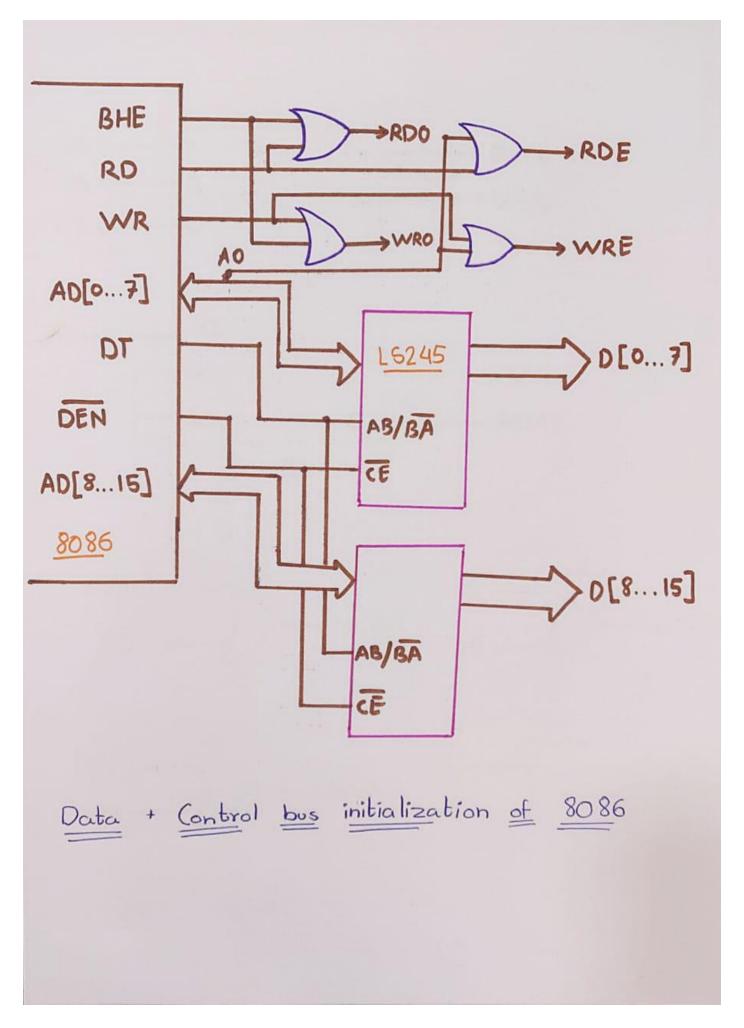
#### **On Paper Design**

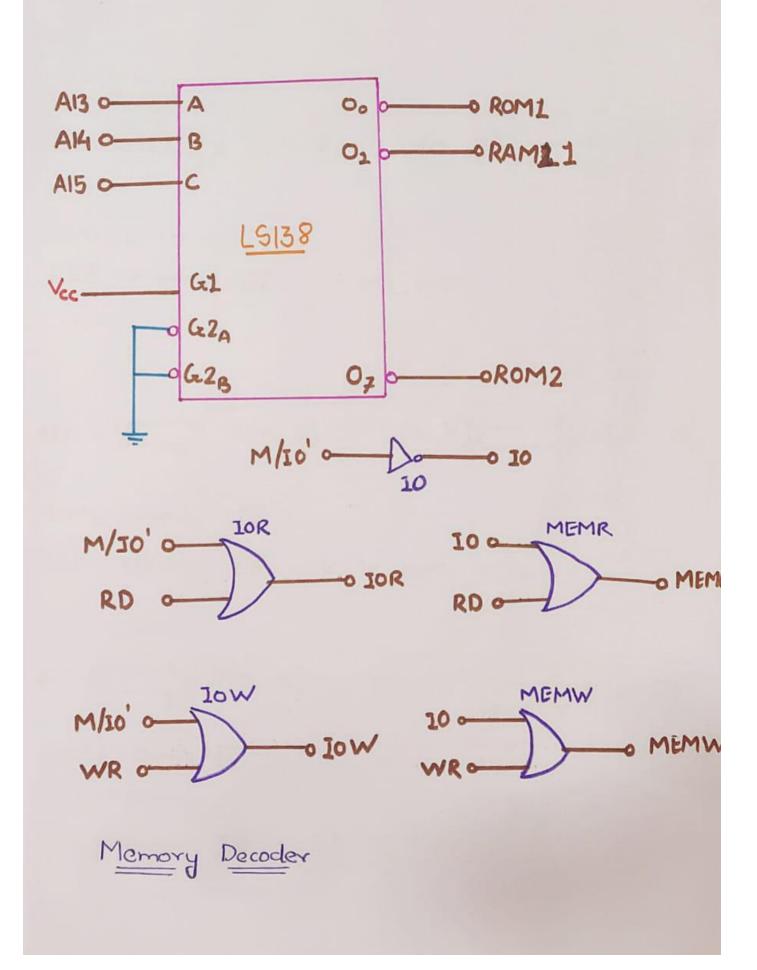
#### Group 93:

- 1. Sidhartha Jain (2018AAPS0335G)
- 2. Rishabh Vaidya (2018AAPS0328G)
- 3. Saumya Bhatt (2018A3PS0303G)
- 4. Samesh Lakhotia (2018AAPS0553G)
- 5. Ritick Srivastava (2018AAPS0366G)





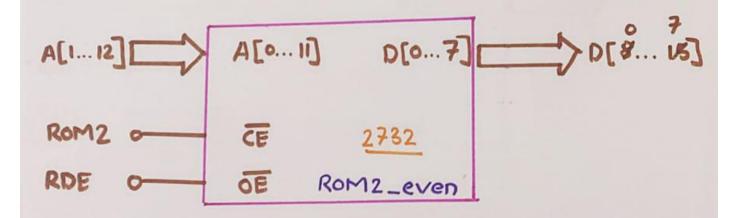


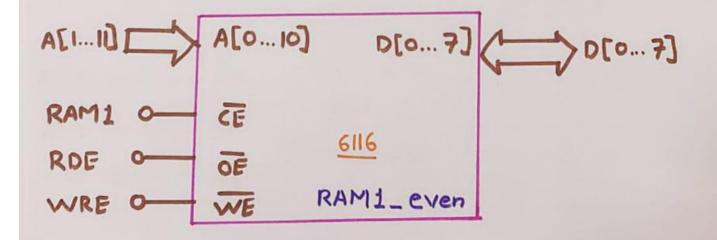


A[I... 12] 
$$A[O...11]$$
  $D[O...7]$   $D[O...7]$ 

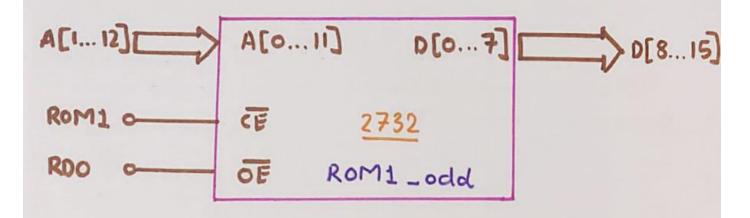
ROM1  $O$   $CE$   $R$   $2732$ 

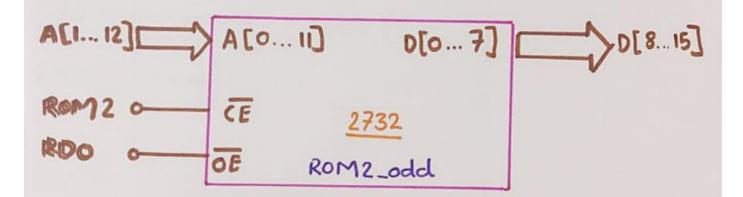
RDE  $O$   $OE$   $ROM1_even$ 

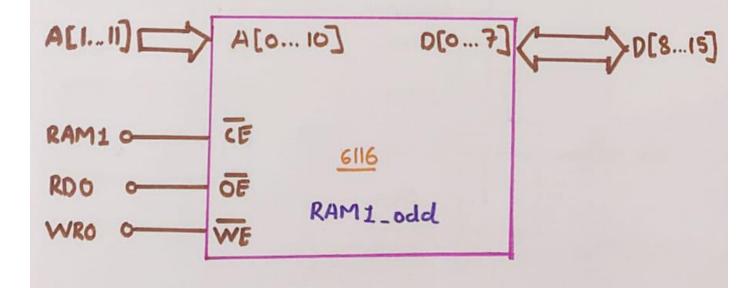




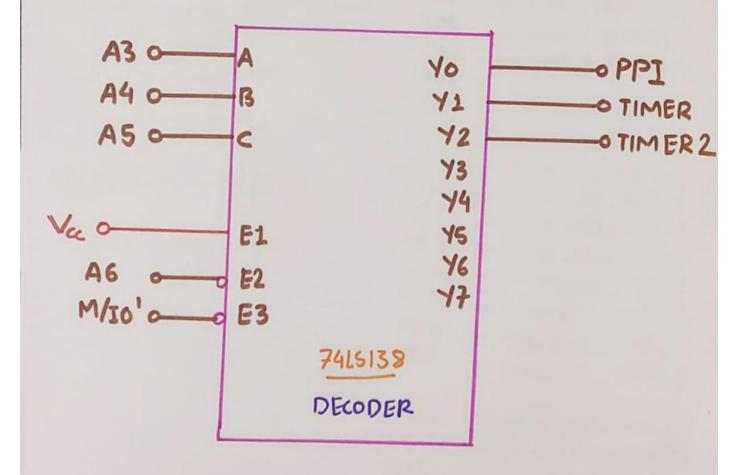
## ROM(1+2) + RAM1 Odd Banks



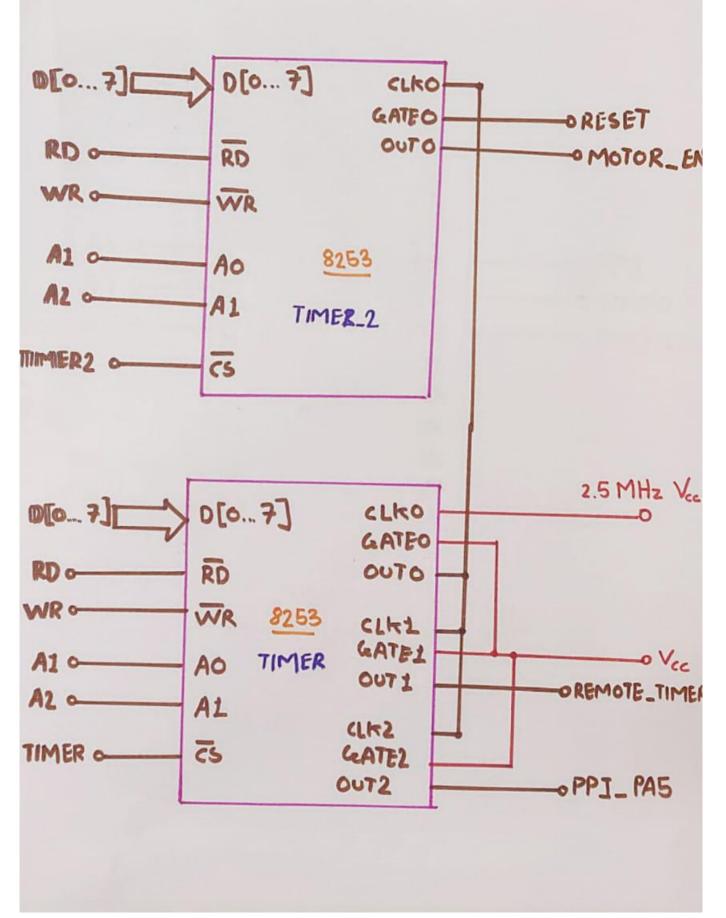




#### Address lines to PPI decoder

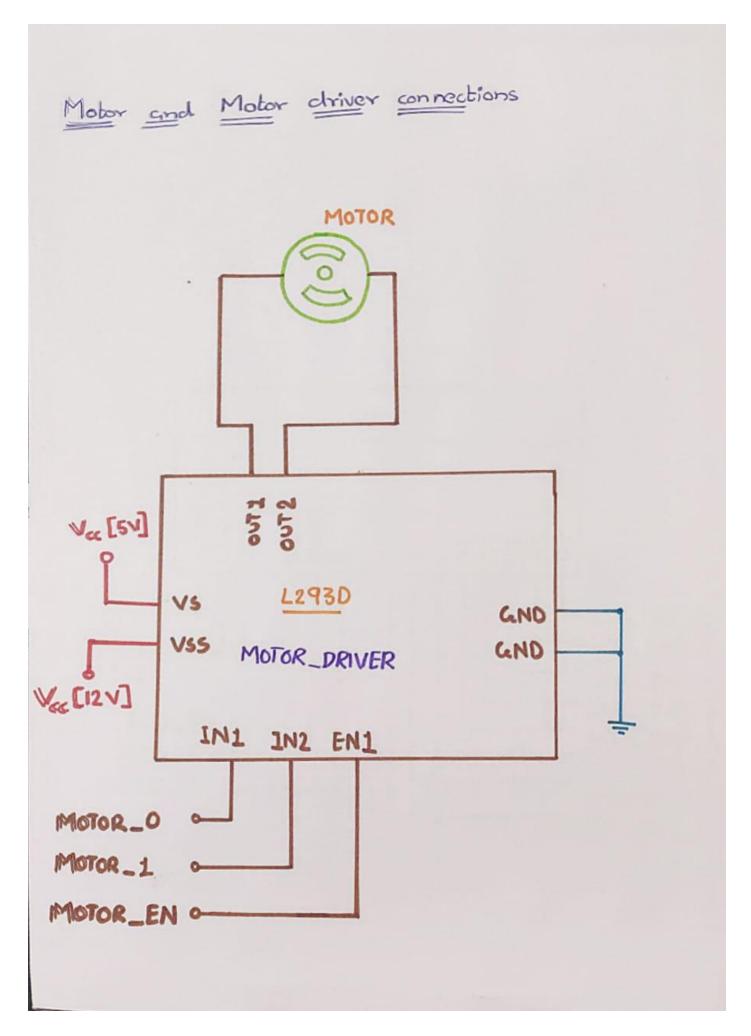


# Timer (1+2) connections



### PPI connections

IOR 0— IOW 0— A1 0— A2 0—	D[07]  RD  WR  AO  A1	PAO PAI PA2 PA3 PA4 PA5 PA6 PA7	OREMOTE OUTER_IR OTRANSDUCER OINNER_IR OREMOTE_TIME OPI_PA5
RESET O	RESET  CS  8255	PBO PBI PB2 PB3 PB4 PB5 PB6 PB7	OLCO_DAT_1 OLCO_DAT_2 OLCO_DAT_3 OLCO_DAT_4 OLCO_DAT_5 OLCO_DAT_6 OLCO_DAT_7 OLCO_DAT_7
	PPI	PCO PCI PC2 PC3 PC4 PC5 PC6 PC7	O LCD_RWS  O LCD_E  O MOTOR_O  O MOTOR_1



# LCD connections

