PAPER ID-311725

Subject Code: BCS302

Roll No: | | | | | | | | | | | | | |

BTECH

(SEM III) THEORY EXAMINATION 2023-24

COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 3HRS **M.MARKS: 70**

Note: 1. Attempt all sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief.

Q no.	Question	Marks
a.	What are the different types of Buses used in computer architecture?	2
b.	Name the different types of multipliers.	2
c.	What are the different phases of an instruction cycle?	2
d.	How does control unit of a computer works?	2
e.	Write a short not on locality of reference.	2
f.	Define 2 ½ D memory organization.	2
g.	In what way synchronous and asynchronous serial modes of data transfer differ?	2

SECTION B

2. Attempt any *three* of the following:

a.	What is meant by the term BUS arbitration? Why is it needed? How can bus arbitration be implemented in Daisy changing scheme?	7
b.	Show the multiplication process using Booth's algorithm when the following numbers are multiplied: - (-12) *(-18).	7
c.	What is pipelining? What are the different stages of pipelining? Explain in detail.	7
d.	Give classification of memory based on the method of access. Also discuss construction and working of magnetic disk and various components of disk access time.	7
e.	What are the basic differences between interrupt initiated I/O and programmed I/O? Explain in detail.	7

SECTION C

3. Attempt any *one* part of the following:

a.	What do you mean by processor organization? Explain various types of processor organization with suitable example.	7
b.	Differentiate between Memory stack and register stack.	7

4. Attempt any *one* part of the following:

a.	Explain in detail the principle of carry looks ahead adder and design 4-bit CLA adder.	7
b.	Represent the following decimal number in IEEE standard floating-point format in a single precision method (32 bit) representation method. (i) $(85.125)_{10}$ (ii) $(-307.1875)_{10}$	7

5. Attempt any *one* part of the following:

a.	Explain the different cycles of an instruction execution.	7
b.	Differentiate between hardwired and micro programmed control unit. Explain each component of hardwired control unit organization.	7

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TIME: 3HRS **M.MARKS: 70**

6. Attempt any *one* part of the following:

a.	Consider a cache (M1) and memory (M2) hierarchy with following characteristics: - M1 : 16K word, 50 ns Access time M2 : 1M word, 400 ns Access time Assume 8-word cache blocks and set size 256 words with set associative mapping. (i) Show and explain the mapping between M2 and M1. (ii) Calculate the effective memory access time with cache hit ratio=0.95.	7
b.	Explain the direct mapping technique. Consider a digital computer has a memory unit of 64k*16 and cache memory of 1k words. The cache uses direct mapping with 4 block size of four words. (i) How many bits are there in the tag, block and word fields of the address format? (ii) How many blocks can the cache accommodate?	7

7. Attempt any *one* part of the following: **7 x 1 = 7**

a.	What do you mean by asynchronous data transfer? Explain strobe control and handshaking mechanism.	7
b.	Explain the various modes of data transfer and discuss direct memory access mode in detail. Also explain how DMA is superior to other modes.	7

Printed Pages:02 **Sub Code: KCS-302**

Paper Id: 233647 **Roll No.** | | | | | | | | | | |

B. TECH.
(SEM III) THEORY EXAMINATION 2022-23
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

(a) List the steps involved in an instruction cycle.
(b) How memory read and write operations are performed in computer system?
(c) Define bus and memory transfer?
(d) Define HIT and MISS ratio in memory with an example.
(e) Define instruction cycle.
(f) Differentiate between RISC and CISC.
(g) List the difference between static RAM and dynamic RAM.
(h) Define Virtual memory.
(i) List down the functions performed by an Input/Output unit.
(j) Why does the DMA get priority over CPU when both request memory transfer?

SECTION B

2. Attempt any *three* of the following: **10x3=30**

(a) Explain functional units of computer system in detail.
(b) Explain IEEE-754 standard for floating point representation. Express $(314.175)_{10}$ in all the IEEE-754 models.
(c) Explain the concept of pipelining and also explain types of pipelining.
(d) Consider a cache consisting of 256 blocks of 16 words each for a total of 4096 words and assume that the main memory is addressable by a 16 bits address and it consists of 4K blocks. How many bits are there in each of TAG, SET, WORD field for 2-way set associative technique?
(e) Define interrupt. Also discuss different types of interrupt.

SECTION C

3. Attempt any *one* part of the following: **10x1=10**

(a) Explain about stack organization used in processors. What do you understand by register stack?
(b) What is an effective address? How it is calculated in different types of addressing modes? Explain.

4. Attempt any *one* part of the following: 10x1=10

(a) Describe the derivation procedure of look ahead carry adder by an example with the help of block diagram.
(b) Show the systematic multiplication process of (-15) × (-16) using Booth's Algorithm.

5. Attempt any *one* part of the following: 10x1=10

(a) Write a program to evaluate the arithmetic statement.
$P = ((X - Y + Z) * (A \wedge B))/(C \wedge D * E)$
By using (i) Two address instructions (ii) One address instructions (iii) Zero address instructions
(b) What are the differences between hardwired and micro-programmed control unit?

6. Attempt any *one* part of the following: 10x1=10

(a) Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost.
(b) Write a short notes on magnetic disk, magnetic tape and optical disk.

7. Attempt any *one* part of the following: 10x1=10

(a) With a neat schematic diagram, explain about DMA controller and its mode of data transfer.
(b) Discuss the design of a typical input or output interface.

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BTECH
(SEM III) THEORY EXAMINATION 2021-22
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If you require any missing data, then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2x10 = 20

Qno	Questions	CO
(a)	List and briefly define the main structural components of a computer.	CO1
(b)	Differentiate between horizontal and vertical microprogramming.	CO3
(c)	Represent the following conditional control statements by two register transfer statements with control functions. If(P=1) then (R1 ←R2) else if (Q=1) then (R1←R3)	CO1
(d)	Design a 4-bit combinational incremental circuit using four full adder circuits.	CO2
(e)	Differentiate between Daisy chaining and centralized parallel arbitration.	CO5
(f)	What is the transfer rate of an eight-track magnetic tape whose speed is 120 inches per second and whose density is 1600 bits per inch?	CO5
(g)	Register A holds the binary values 10011101.What is the register value after arithmetic shift right? Starting from the initial number 10011101, determine the register value after arithmetic shift left, and state whether there is an overflow.	CO2
(h)	What is an Associative memory? What are its advantages and disadvantages?	CO4
(i)	Differentiate between static RAM and Dynamic RAM.	CO4
(j)	What are the different types of instruction formats?	CO3

SECTION B

2. Attempt any *three* of the following: 10x3 = 30

Qno	Questions	CO
(a)	A digital computer has a common bus system for 8 registers of 16 bit each. The bus is constructed using multiplexers. I. How many select input are there in each multiplexer? II. What is the size of multiplexers needed? III. How many multiplexers are there in the bus?	CO1
(b)	Explain destination-initiated transfer using handshaking method.	CO5
(c)	Explain 2-bit by 2-bit Array multiplier. Draw the flowchart for divide operation of two numbers in signed magnitude form.	CO2
(d)	A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. I. How many bits are there in the tag, index, block, and word fields of the address format? II. How many bits are there in each word of cache, and how they are divided into functions? Include a valid bit. III. How many blocks can the cache accommodate?	CO4
(e)	Explain with neat diagram, the address selection for control memory.	CO3

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(SEM III) THEORY EXAMINATION 2021-22
COMPUTER ORGANIZATION AND ARCHITECTURE

SECTION C

3. Attempt any *one* part of the following: 10x1 = 10

Qno	Questions	CO
(a)	A binary floating-point number has seven bits for a biased exponent. The constant used for the bias is 64. I. List the biased representation of all exponents from -64 to +63. II. Show that after addition of two biased exponents, it is necessary to subtract 64 in order to have a biased exponent's sum. III. Show that after subtraction of two biased exponents, it is necessary to add 64 in order to have a biased exponent's difference.	CO2
(b)	Show the multiplication process using Booth algorithm, when the following binary numbers, (+13) x (-15) are multiplied.	CO2

4. Attempt any *one* part of the following: 10x1 = 10

Qno	Questions	CO
(a)	Draw a diagram of a Bus system in which it uses 3 state buffers and a decoder instead of the multiplexers.	CO1
(b)	Explain in detail multiple bus organization with the help of a diagram.	CO1

5. Attempt any *one* part of the following: 10x1 = 10

Qno	Questions	CO
(a)	The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words each. Physical memory consists of 4K blocks of 4K words each. Formulate the logical and physical address formats.	CO4
(b)	How is the Virtual address mapped into physical address? What are the different methods of writing into cache?	CO4

6. Attempt any *one* part of the following: 10x1 = 10

Qno	Questions	CO
(a)	Explain how the computer buses can be used to communicate with memory and I/O. Also draw the block diagram for CPU-IOP communication.	CO5
(b)	What are the different methods of asynchronous data transfer? Explain in detail.	CO5

7. Attempt any *one* part of the following: 10x1 = 10

Qno	Questions	CO
(a)	Write a program to evaluate arithmetic expression using stack organized computer with 0-address instructions. X = (A-B) * (((C - D * E) / F) / G)	CO3
(b)	List the differences between hardwired and micro programmed control in tabular format. Write the sequence of control steps for the following instruction for single bus architecture. R1 ← R2 * (R3)	CO3

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B TECH
(SEM-III) THEORY EXAMINATION 2020-21
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Q no.	Question	Marks	CO
a.	Define the term Computer architecture and Computer organization.	2	1
b.	What is mean by bus arbitration? List different types of bus arbitration.	2	1
c.	Discuss biasing with reference to floating point representation.	2	2
d.	What is restoring method in division algorithm?	2	2
e.	Define micro operation and micro code.	2	3
f.	Write short note on RISC.	2	3
g.	Define hit ratio.	2	4
h.	What do you mean by page fault?	2	4
i.	Explain the term cycle stealing.	2	5
j.	What do you mean by vector interrupt? Explain.	2	5

SECTION B

2. Attempt any *three* of the following: **3 x 10 = 30**

Q no.	Question	Marks	CO
a.	i. Draw a diagram of bus system using MUX which has four registers of size 4 bits each. ii. Evaluate the arithmetic statement. X = A + B * [C * D + E * (F + G)] using a stack organized computer with zero address operation instructions.	10	1
b.	Explain in detail the principle of carry look ahead adder and design 4-bit CLA adder.	10	2
c.	Draw the flowchart for instruction cycle with neat diagram and explain.	10	3
d.	Discuss 2 D RAM and 2.5D RAM with suitable diagram.	10	4
e.	Draw and explain the block diagram of typical DMA controller.	10	5

SECTION C

3. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	An instruction is stored at location 400 with its address field at location 401.The address field has the value 500.A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) immediate (iii) relative (iv) register indirect (v) index with R1 as index register	10	1
b.	What do you mean by processor organization? Explain various types of processor organization.	10	1

4. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	Show the systemic multiplication process of (20) X (-19) using Booth's algorithm	10	2
b.	Explain IEEE standard for floating point representation. Represent the number $(-1460.125)_{10}$ in single precision and double precision format.	10	2

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5. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	What is a micro program sequencer? With block diagram, explain the working of micro program sequencer.	10	3
b.	Differentiate between hardwired and micro programmed control unit. Explain each component of hardwired control unit organization.	10	3

6. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	Calculate the page fault for a given string with the help of LRU & FIFO page replacement algorithm, Size of frames = 4 and string 1 2 3 4 2 1 5 6 2 1 2 3 7 6 3 2 1 2 3 6	10	4
b.	A computer uses RAM chips of 1024*1 capacity. i) How many chips are needed & how should their address lines be connected to provide a memory capacity of 1024*8? ii) How many chips are needed to provide a memory capacity of 16 KB?	10	4

7. Attempt any *one* part of the following:

Q no.	Question	Marks	CO
a.	What do you mean by asynchronous data transfer? Explain strobe control and hand shaking mechanism.	10	5
b.	Discuss the different modes of data transfer.	10	5

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B. TECH.
(SEM-III) THEORY EXAMINATION 2019-20
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours *Total Marks: 100*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Qno.	Question	Marks	CO
a.	Define the term Computer Architecture.	2	1
b.	Draw the basic functional units of a computer.	2	1
c.	Perform the 2's complement subtraction of smaller number (101011) from larger number (111001).	2	2
d.	What is the role of Multiplexer and Decoder?	2	2
e.	Write the differences between RISC and CISC.	2	3
f.	What are the types of microinstructions available?	2	3
g.	What is SRAM and DRAM?	2	4
h.	What is the difference between 2D and $2^{1/2}$ D memory organization?	2	4
i.	What is I/O control method?	2	5
j.	What is bus arbitration?	2	5

SECTION B

2. Attempt any *three* of the following:

Qno.	Question	Marks	CO
a.	Convert the following arithmetic expressions from infix to reverse polish notation: i. A*B+C*D+E*F ii. A*[B+C*CD+E]/F*(G+H)	5+5	1
b.	Design a 4-bit Carry-Look ahead Adder and explain its operation with an example.	10	2
c.	i. Draw the timing diagram for a instruction cycle and explain. ii. Give a note on subroutine.	5+5	3
d.	What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory.	10	4
e.	What is DMA? Describe how DMA is used to transfer data from peripherals.	10	5

SECTION C

3. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Describe in detail the different kinds of addressing modes with an example.	10	1
b.	Discuss stack Organization. Explain the following in details- (i) Register stack (ii) Memory stack	10	1

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Paper Id: 110322 Roll No: | | | | | | | | | | | | | |

4. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Represent the following decimal number in IEEE standard floating-point format in a single precision method (32-bit) representation method. i. $(65.175)_{10}$ ii. $(-307.1875)_{10}$	5+5	2
b.	Using Booth algorithm perform the multiplication on the following 6-bit unsigned integer 10110011 * 11010101	10	2

5. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	What is parallelism and pipelining in computer Architecture?	10	3
b.	Explain the organization of Microprogrammed control unit in detail.	10	3

6. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Discuss the different mapping techniques used in cache memories and their relative merits and demerits.	10	4
b.	RAM chip 4096 × 8 bits has two enable lines. How many pins are needed for the integrated circuits package? Draw a block diagram and label all input and outputs of the RAM. What is main feature of random-access memory?	5+5	4

7. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Write down the difference between isolated I/O and memory mapped I/O. Also discuss advantages and disadvantages of isolated I/O and memory mapped I/O.	10	5
b.	i. Discuss the design of a typical input or output interface. ii. What are interrupts? How are they handled?	10	5