



Electronics Notes 1 Year

B.tech (Dr. A.P.J. Abdul Kalam Technical University)

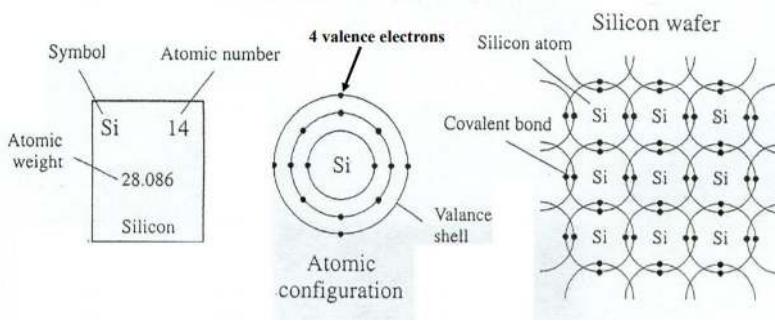


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UNIT 1

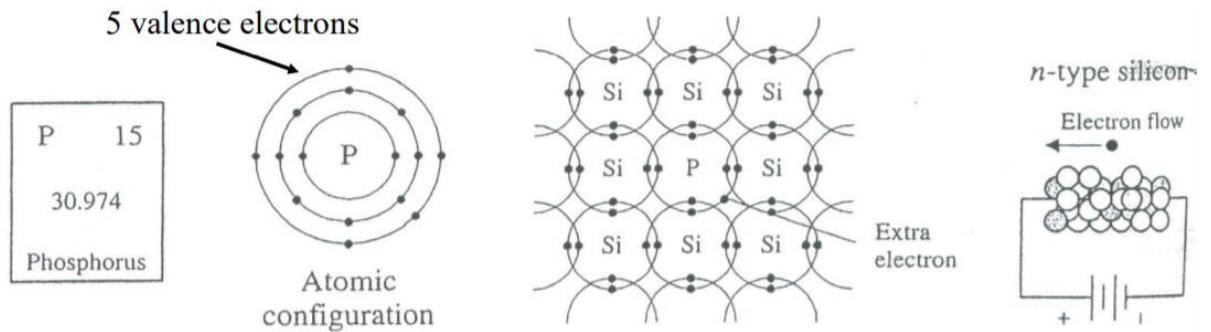
Semiconductors

- Materials that permit flow of electrons are called conductors (e.g., gold, silver, copper, etc.).
- Materials that block flow of electrons are called insulators (e.g., rubber, glass, Teflon, mica, etc.).
- Materials whose conductivity falls between those of conductors and insulators are called semiconductors.
- Semiconductors are “part-time” conductors whose conductivity can be controlled.
- There are two types of semiconductors (i) Elemental Semiconductors and (ii) Compound semiconductors.
- Elemental semiconductors are usually Group IV elements of Periodic Table.
- Silicon and Germanium are two very popular elemental semiconductors. Their atomic numbers are 14 and 32 respectively.
- They are tetravalent elements i.e having 4 valence electrons.
- Atoms in a pure silicon wafer contains four electrons in outer orbit (called valence electrons). – Germanium is another semiconductor material with four valence electrons.
- In the crystalline lattice structure of Si, the valence electrons of every Si atom are locked up in covalent bonds with the valence electrons of four neighbouring Si atoms. In pure form, Si wafer does not contain any free charge carriers.
- An applied voltage across pure Si wafer does not yield electron flow through the wafer. A pure Si wafer is said to act as an insulator.
- Silicon is the most common material used to build semiconductor devices.
- Si is the main ingredient of sand and it is estimated that a cubic mile of seawater contains 15,000 tons of Si.



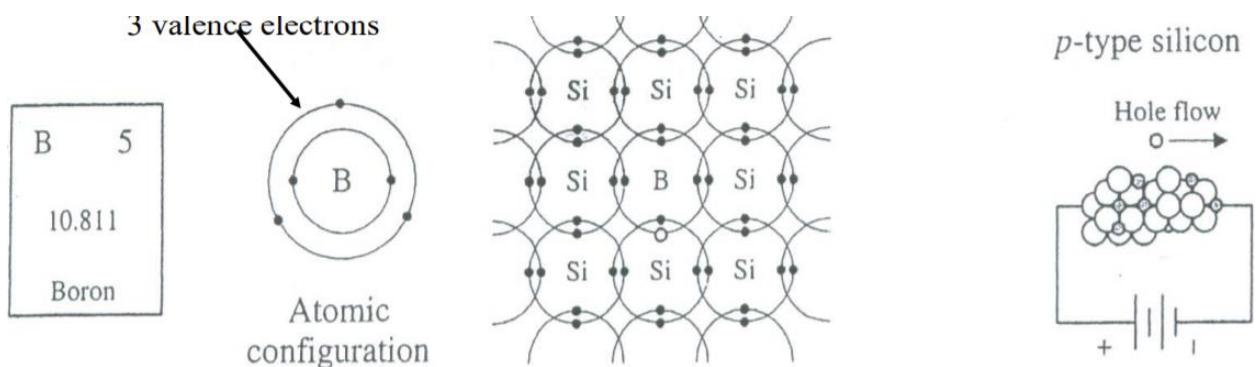
N-Type Semiconductor

- Pentavalent impurities such as phosphorus, arsenic, antimony, and bismuth have 5 valence electrons.
- When phosphorus impurity is added to Si, every phosphorus atom's four valence electrons are locked up in covalent bond with valence electrons of four neighbouring Si atoms. However, the 5th valence electron of phosphorus atom does not find a binding electron and thus remains free to float.
- When a voltage is applied across the silicon-phosphorus mixture, free electrons migrate toward the positive voltage end.
- When phosphorus is added to Si to yield the above effect, we say that Si is doped with phosphorus. The resulting mixture is called N-type silicon (N: negative charge carrier silicon).
- The pentavalent impurities are referred to as donor impurities.
- In an n-type material, the electron is called the majority carrier and the hole the minority carrier.



P-Type Semiconductor

- Trivalent impurities e.g., boron, aluminium, indium, and gallium have 3 valence electrons.
- When boron is added to Si, every boron atom's three valence electrons are locked up in covalent bond with valence electrons of three neighbouring Si atoms. However, a vacant spot "hole" is created within the covalent bond between one boron atom and a neighbouring Si atom.
- The holes are considered to be positive charge carriers. When a voltage is applied across the silicon-boron mixture, a hole moves toward the negative voltage end while a neighbouring electron fills in its place.
- When boron is added to Si to yield the above effect, we say that Si is doped with boron. The resulting mixture is called P-type silicon (P: positive charge carrier silicon).
- The trivalent impurities are referred to as acceptor impurities.



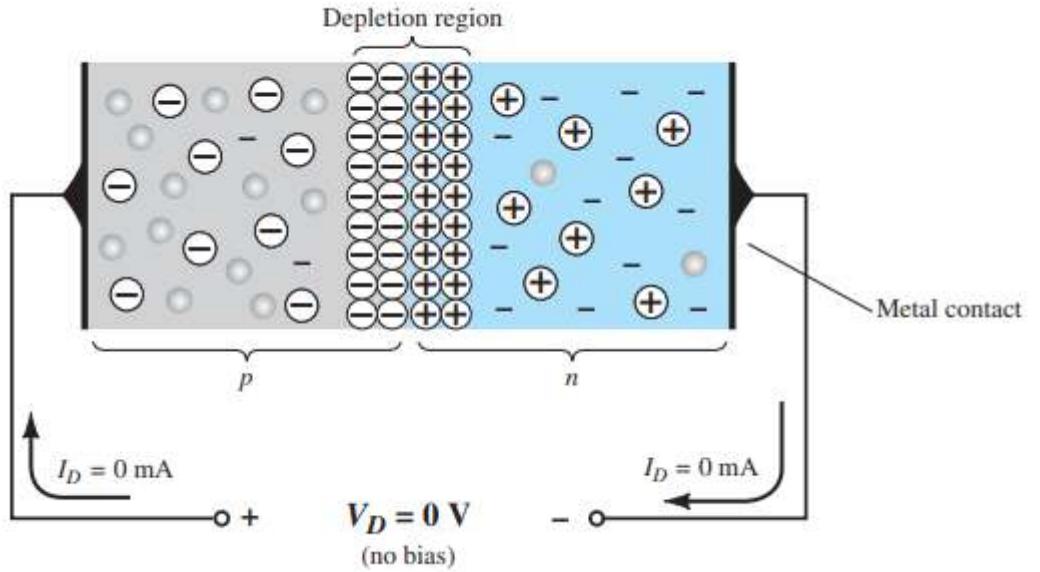
- The hole of boron atom points towards the negative terminal.
- The electron of neighbouring silicon atom points toward positive terminal.
- The electron from neighbouring silicon atom falls into the boron atom filling the hole in boron atom and creating a "new" hole in the silicon atom.
- It appears as though a hole moves toward the negative terminal.
- In a p-type material the hole is the majority carrier and the electron is the minority carrier.

PN Junction Diode

- Now that both n - and p -type materials are available, we can construct our first solid-state electronic device: The PN Junction diode.

No Applied Bias ($V_D = 0 \text{ V}$)

- At the instant the two materials are “joined” the electrons and the holes in the region of the junction will combine, resulting in a lack of free carriers in the region near the junction.
- This region of uncovered positive and negative ions is called the depletion region due to the “depletion” of free carriers in the region.

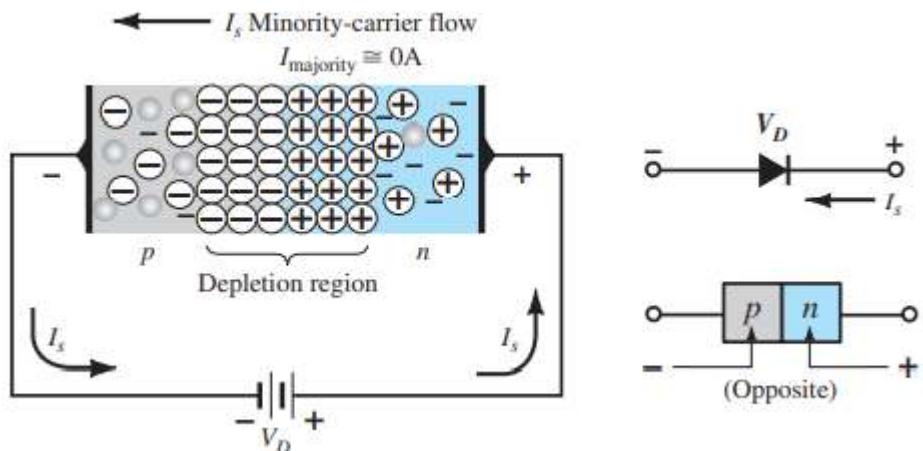


- The term bias refers to the application of an external voltage across the two terminals of the device to extract a response.
- It is clear that the applied voltage is 0 V (no bias) and the resulting current is 0 A, much like an isolated resistor.

- Under no-bias conditions, any minority carriers (holes) in the n -type material that find themselves within the depletion region for any reason whatsoever will pass quickly into the p -type material and vice versa.
- The majority carriers (electrons) of the n -type material must overcome the attractive forces of the layer of positive ions in the n -type material and the shield of negative ions in the p -type material to migrate into the area beyond the depletion region of the p -type material.
- In the absence of an applied bias across a semiconductor diode, the net flow of charge in one direction is zero.

Reverse-Bias Condition ($V_D = 0 \text{ V}$)

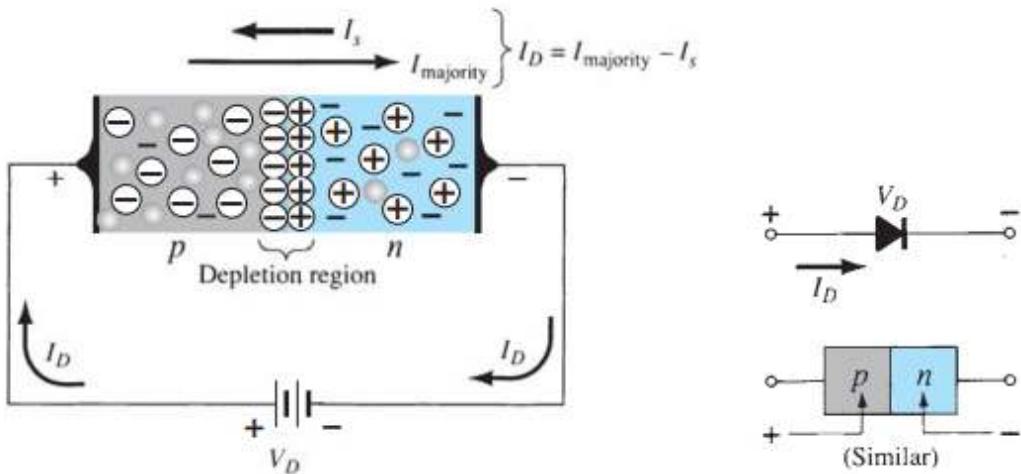
- If an external potential of V volts is applied across the p – n junction such that the positive terminal is connected to the n -type material and the negative terminal is connected to the p -type material.
- The number of uncovered positive ions in the depletion region of the n -type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the p -type material.
- The net effect is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero.



- Number of minority carriers, however, entering the depletion region will not change, resulting in minority-carrier flow.
- The current that exists under reverse-bias conditions is called the reverse saturation current.

Forward-Bias Condition ($V_D \geq 0$ V)

- A forward-bias or “on” condition is established by applying the positive potential to the p -type material and the negative potential to the n -type material.
- The application of a forward-bias potential V_D will “pressure” electrons in the n -type material and holes in the p -type material to recombine with the ions near the boundary and reduce the width of the depletion region.
- The reduction in the width of the depletion region has resulted in a heavy majority flow across the junction. An electron of the n -type material now “sees” a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the p -type material.



- As the applied bias increases in magnitude, the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current.
- It can be demonstrated through the use of solid-state physics that the general characteristics of a semiconductor diode can be defined by the following equation, referred to as Shockley’s equation, for the forward- and reverse-bias regions:

$$I_D = I_s(e^{V_D/nV_T} - 1)$$

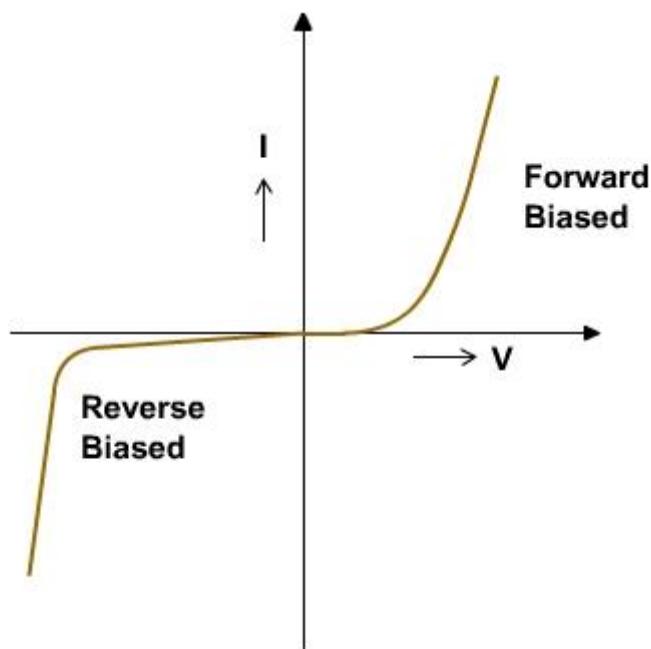
where I_s is the reverse saturation current V_D is the applied forward-bias voltage across the diode n is an ideality factor, which is a function of the operating conditions and physical construction; it has a range between 1 and 2 depending on a wide variety of factors.

- The voltage V_T in is called the thermal voltage and is determined by

$$V_T = \frac{kT_K}{q}$$

where k is Boltzmann's constant 1.38×10^{-23} J/K,
 T_K is the absolute temperature in kelvins
q is the magnitude of electronic charge 1.6×10^{-19} C

V-I Characteristics



Breakdown Region (Avalanche & Zener Breakdown)

- In tens of volts in the negative region, there is a point where the application of too negative a voltage with the reverse polarity will result in a sharp change in the characteristics, as shown in above Fig.
- The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the breakdown potential.
- As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation

current I_s will also increase. Eventually, their velocity and associated kinetic energy will be sufficient to release additional carriers through collisions with otherwise stable atomic structures.

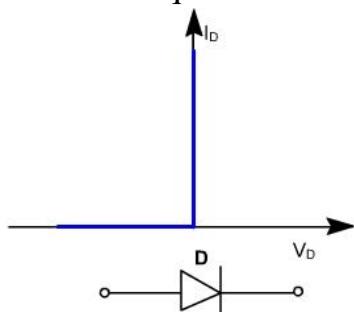
- That is, an ionization process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high avalanche current is established and the avalanche breakdown region determined.
- The avalanche region can be brought closer to the vertical axis by increasing the doping levels in the p - and n -type materials. However, as breakdown voltage decreases to very low levels, such as - 5 V, another mechanism, called Zener breakdown , will contribute to the sharp change in the characteristic.
- It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and “generate” carriers.
- The maximum reverse-bias potential that can be applied before entering the breakdown region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted the PRV rating).

Diode Equivalent Circuits

Ideal Diode:

- When diode is forward biased, resistance offered is zero,
- When it is reverse biased resistance offered is infinity. It acts as a perfect switch.

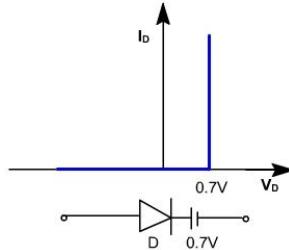
The characteristic and the equivalent circuit of the diode



Second Approximation:

- When forward voltage is more than 0.7 V, for Si diode then it conducts and offers zero resistance. The drop across the diode is 0.7V.
- When reverse biased it offers infinite resistance.

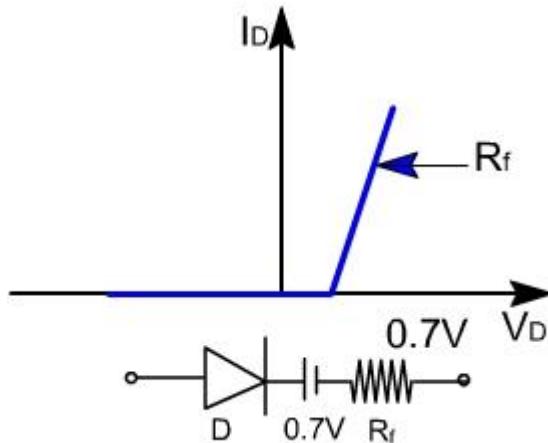
The characteristic and the equivalent circuit is shown



3rd Approximation:

- When forward voltage is more than 0.7 V, then the diode conducts and the voltage drop across the diode becomes 0.7 V and it offers resistance R_f (slope of the current).

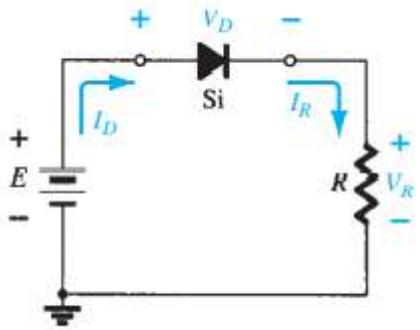
The output characteristic and the equivalent circuit is shown



Diode Applications

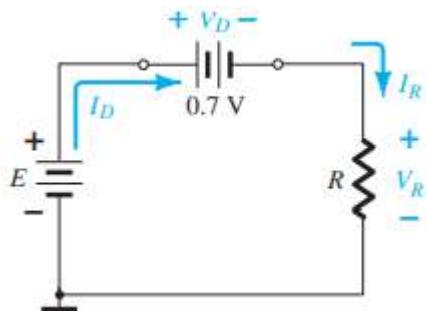
SERIES DIODE CONFIGURATIONS

- The primary purpose of this text is to develop a general knowledge of the behaviour, capabilities, and possible areas of application of a device in a manner that will minimize the need for extensive mathematical developments.
- For all the analysis to follow in this chapter it is assumed that The forward resistance of the diode is usually so small compared to the other series elements of the network that it can be ignored.
- In general, a diode is in the “on” state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D = 0.7 \text{ V}$ for silicon, $V_D = 0.3 \text{ V}$ for germanium.



Series Diode Configuration

- If a diode is in the “on” state, one can place a 0.7-V drop across the element. ($E > 0.7\text{V}$)

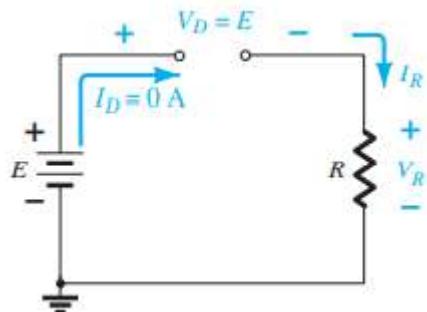


- By applying KVL in above circuit

$$V_R = E - 0.7V$$

$$I_R = I_D = V_R/R$$

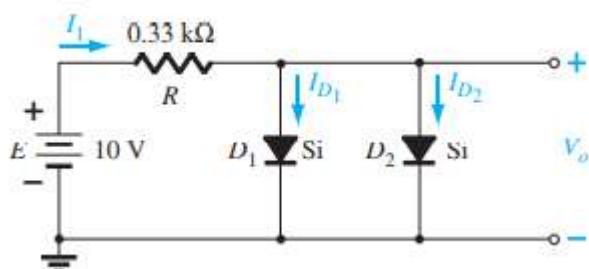
- If a diode is in the “off” state, one can place open circuit across the element. ($E < 0.7V$)



- $I_R = I_D = 0 \text{ & } V_R = 0V$

PARALLEL CONFIGURATION

The methods applied in above Section can be extended to the analysis of parallel configurations.



- through each diode in the same direction as shown in above Fig. Since For the applied voltage the “pressure” of the source acts to establish a current the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes

are in the “on” state. The voltage across parallel elements is always the same and

$$V_O = 0.7 \text{ V}$$

$$I_1 = (E - V_O)/R = (10 - 0.7)/0.33 = 28.18 \text{ mA}$$

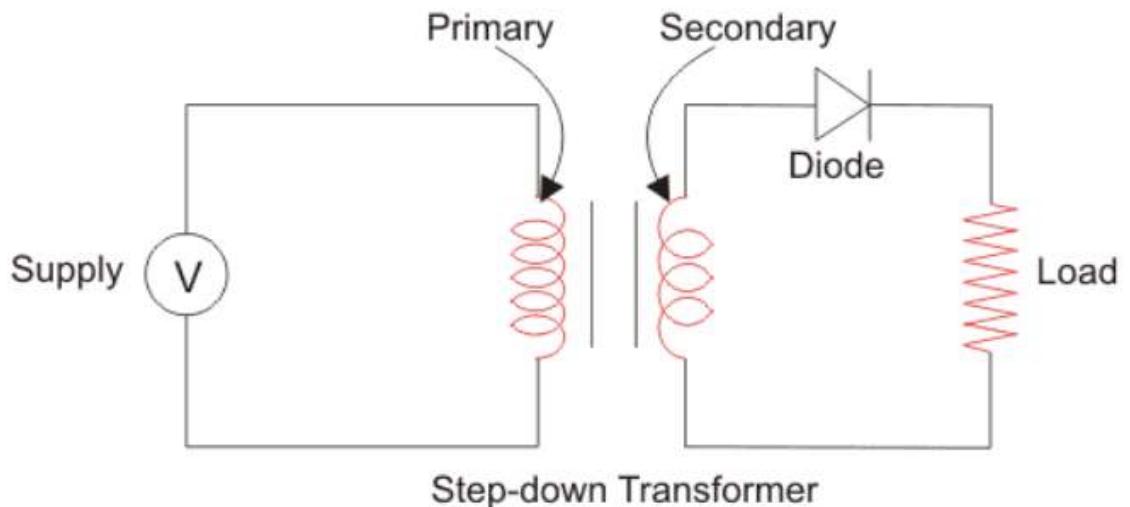
$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18 \text{ mA}}{2} = 14.09 \text{ mA}$$

This example demonstrates one reason for placing diodes in parallel. If the current rating of the diodes of Fig. is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. By placing two in parallel, we limit the current to a safe value of 14.09 mA with the same terminal voltage.

RECTIFIERS

- A Rectifier is an electrical device that is made of one or more than one diodes that converts the **alternating current (AC)** into **direct current (DC)**. It is used for rectification where the process below shows that how it convert AC into DC.
- Rectification is the **process** of conversion of the alternating current (which periodically changes direction) into direct current (flow in a single direction).
- The rectifiers are classified into two categories.
Half wave rectifier
Full wave rectifier

Half wave rectifier



$$V_i = V_m \sin \omega t$$



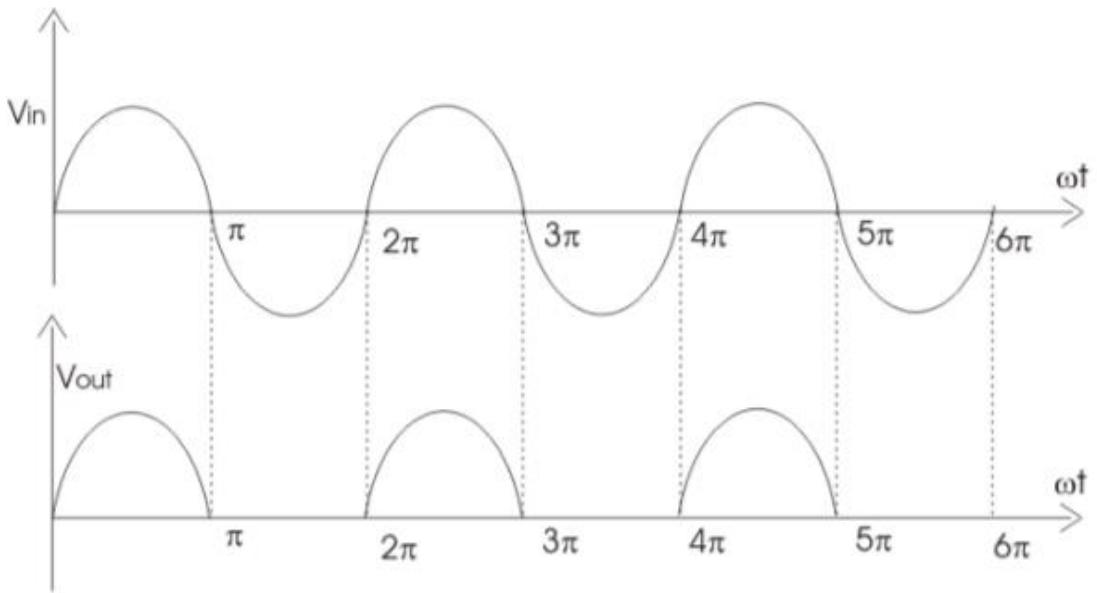
- During positive half cycle, Diode is ON and output voltage i.e. voltage across load is same as input voltage

$$V_o = V_i = V_m \sin \omega t$$



- During negative half cycle, Diode is OFF and output voltage

$$V_o = 0$$



Output of Halfwave Rectifier

- Different parameters for half wave rectifier is given below The average of load current (I_{DC}) : Let, the load current be $I_L = I_m \sin \omega t$

$$I_{dc} = \frac{1}{2\pi} \int_0^{\pi} I_m \sin \omega t dt = \frac{I_m}{\pi}$$

- The rms value of the load current (I_{rms})

$$I_{rms} = \frac{I_m}{4}$$

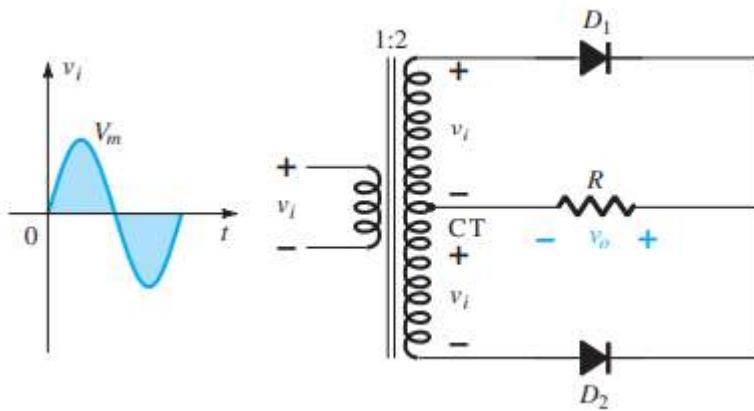
- Ripple factor of half wave rectifier

$$\text{Ripple factor}(r) = \frac{(I_{rms}^2 - I_{dc}^2)}{I_{dc}} = 1.21$$

FULL WAVE DIODE RECTIFIER

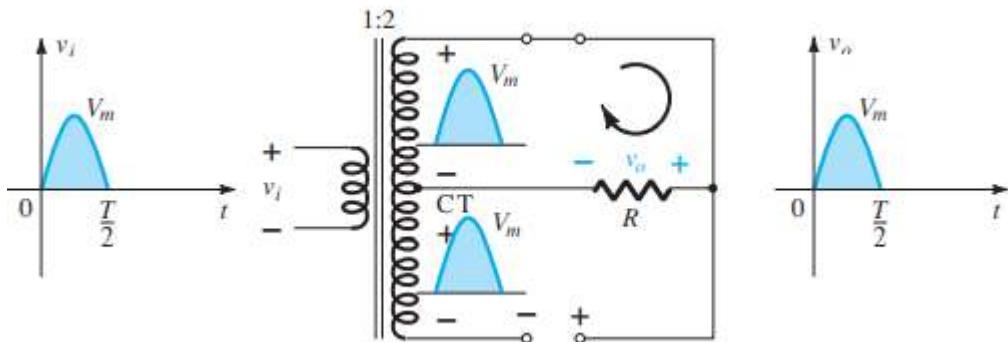
- The diode works only when it is in forward bias, only the current flows through p-n junction diode and output current across the load is found.
- If two diodes are connected in such a way that one diode conducts during one half of the input voltage and the other one conducts during the next half of the cycle, in a unidirectional can flow through the load during the full cycle of the impact voltage. This is known as full wave rectifier.

Center-Tapped Full Wave Rectifier



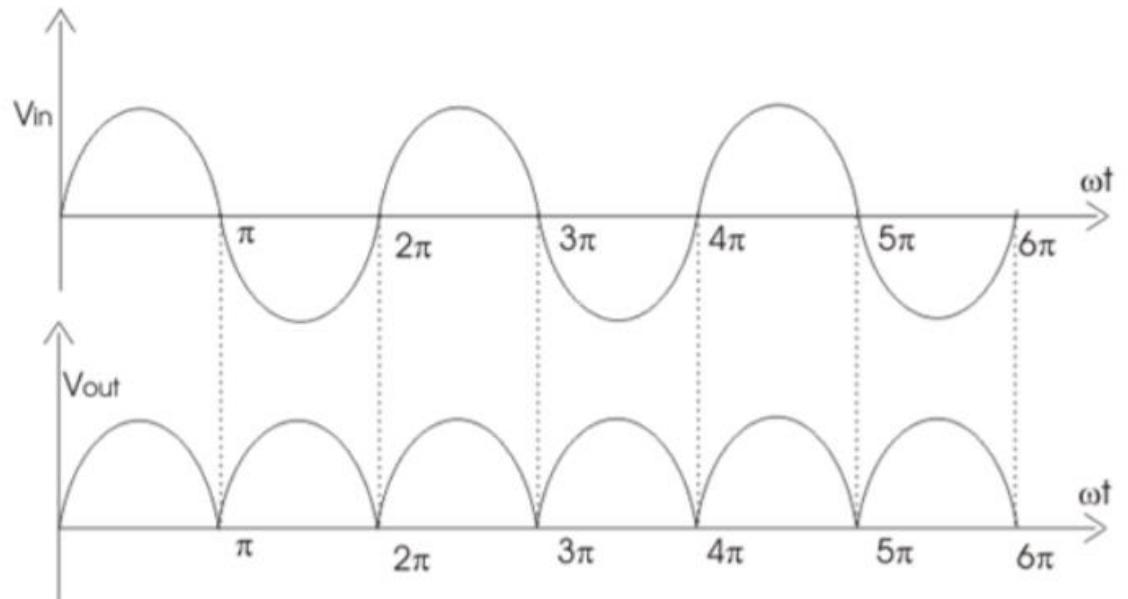
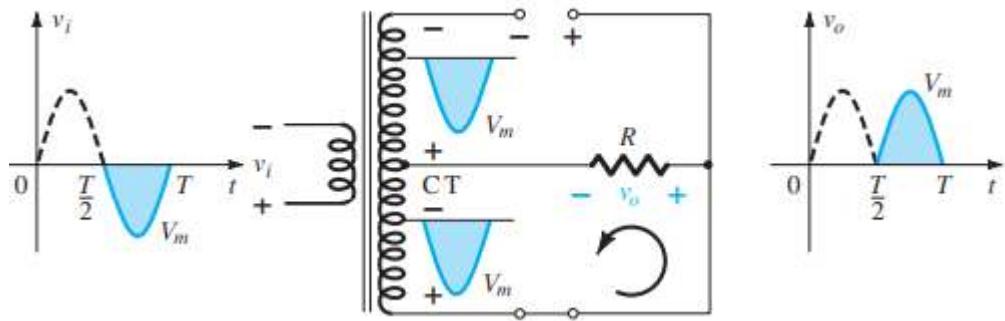
- During the positive cycle of V_i applied to the primary of the transformer, D_1 is ON so it replaced by short circuit equivalent and D_2 is OFF so it is replaced by open-circuit equivalent.

$$V_o = V_i$$



- During the negative cycle of V_i applied to the primary of the transformer, D_2 is ON so it replaced by short circuit equivalent and D_1 is OFF so it is replaced by open-circuit equivalent.

$$V_o = -V_i$$



Input- Output Waveforms

Different parameters for Full wave rectifier is given below. The average of load current (I_{dc}) : Let, the load current be $I_L = I_m \sin \omega t$

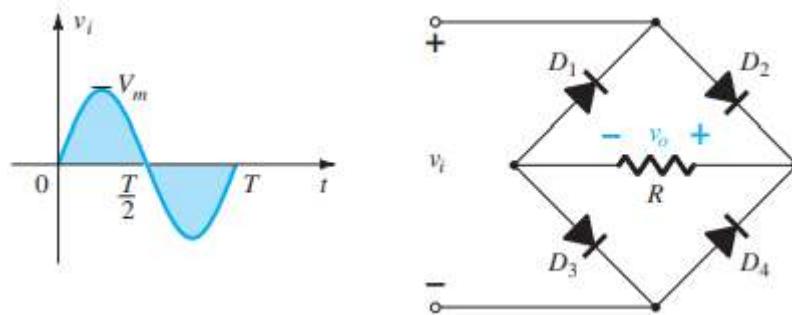
$$I_{dc} = \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t = \frac{2I_m}{\pi}$$

Ripple factor of half wave rectifier,

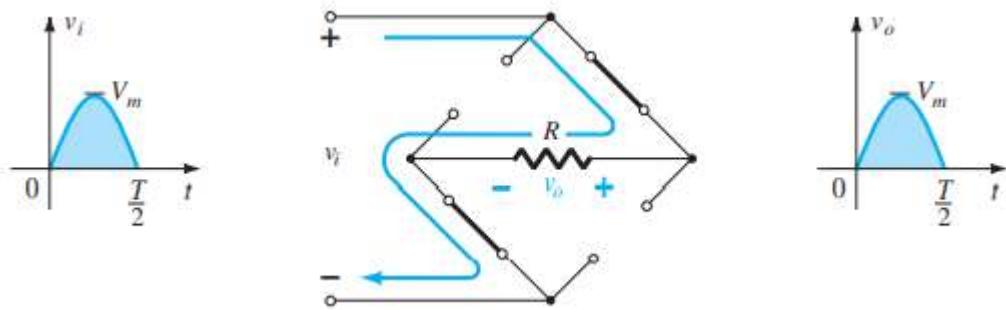
$$\text{Ripple factor}(r) = \frac{(I_{rms}^2 - I_{dc}^2)^{\frac{1}{2}}}{I_{dc}} = 0.482$$

$$\text{Here, } I_{rms} = \frac{I_m}{\sqrt{2}}$$

Bridge Rectifier



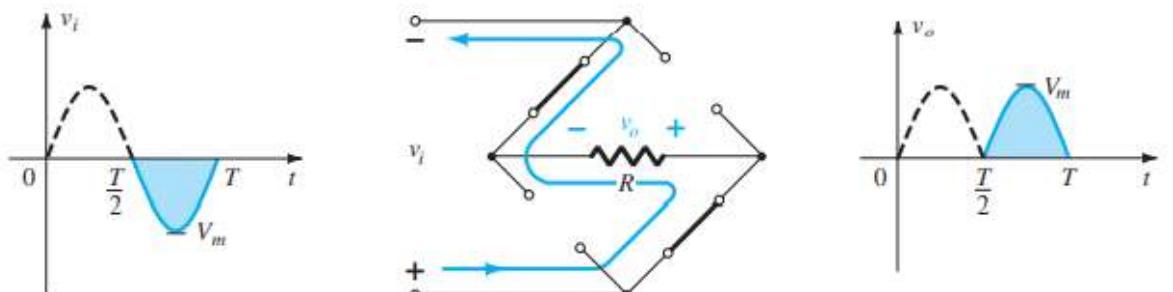
During positive half of input V_i , D_2 & D_3 are On and D_1 & D_4 are Off



then

$$V_o = V_i$$

During negative half of input V_i , D_2 & D_3 are Off and D_1 & D_4 are On



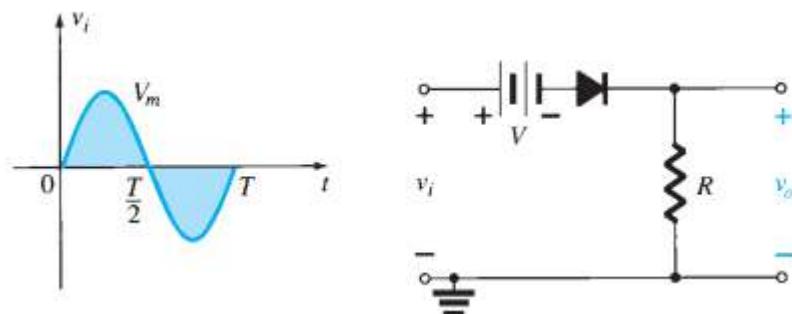
Then

$$V_o = -V_i$$

CLIPPERS

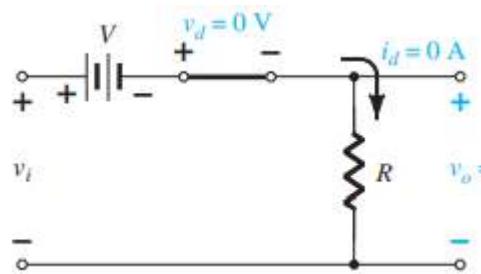
- Clippers are networks that employ diodes to “clip” away a portion of an input signal without distorting the remaining part of the applied waveform.
- The half-wave rectifier of discussed above is an example of the simplest form of diode clipper consisting of one resistor and a diode. Depending on the orientation of the diode, the positive or negative region of the applied signal is “clipped” off.
- There are two general categories of clippers: series and parallel.
- The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

Series Clipper



Input is in series with diode so it is called series clipper.

When $V_i > V$, diode is ON. Replace diode with short circuit equivalent and apply KVL

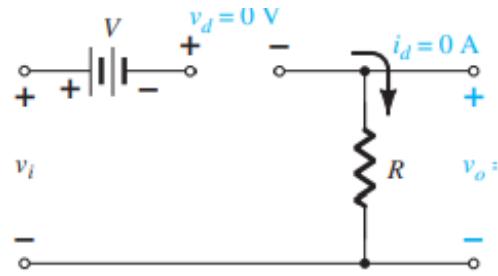


KVL in above loop

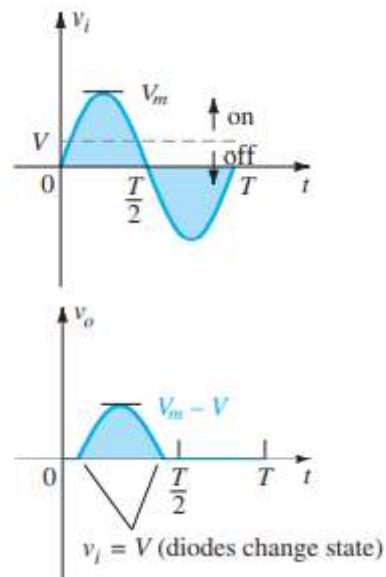
$$V_i - V - V_o = 0$$

$$\text{So } V_o = (V_i - V)$$

When $V_i < V$, diode is OFF. Replace diode with open circuit equivalent and apply KVL

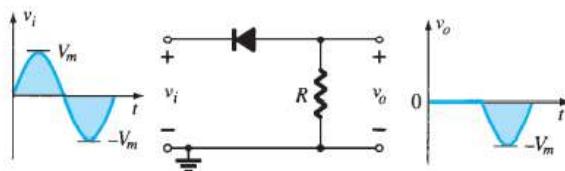


Current is zero so $V_o = 0$

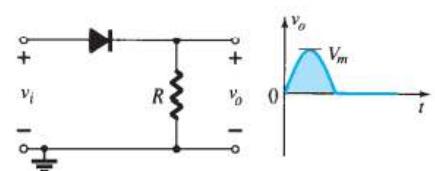


- Certain portion of input is clipped by this circuit.

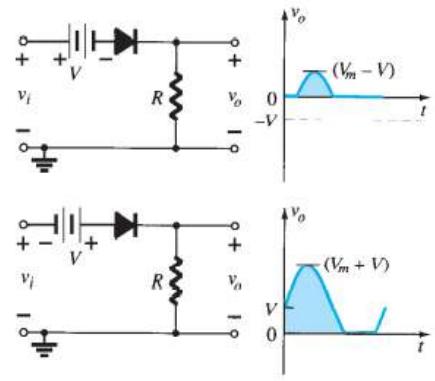
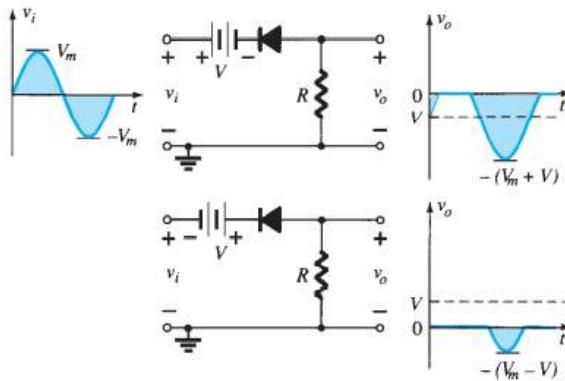
POSITIVE



NEGATIVE

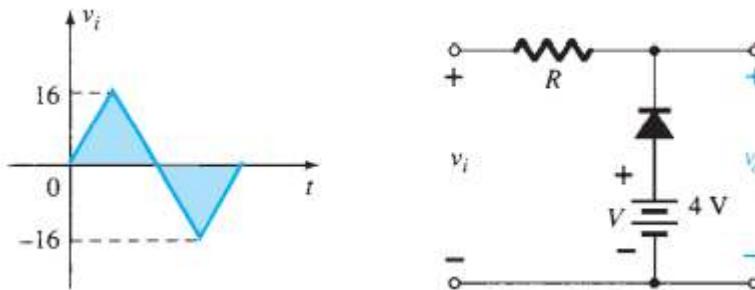


Biased Series Clippers (Ideal Diodes)



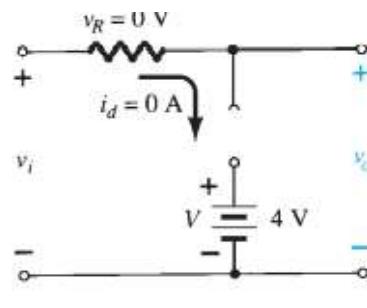
Parallel Clipper

Input is in parallel with diode so these types of clipper are called parallel clipper or shunt clipper.



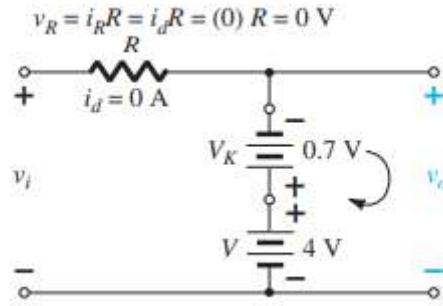
We will assume our diode to be an ideal diode.

When $V_i > 4V$, diode is OFF and is replaced by open circuit equivalent



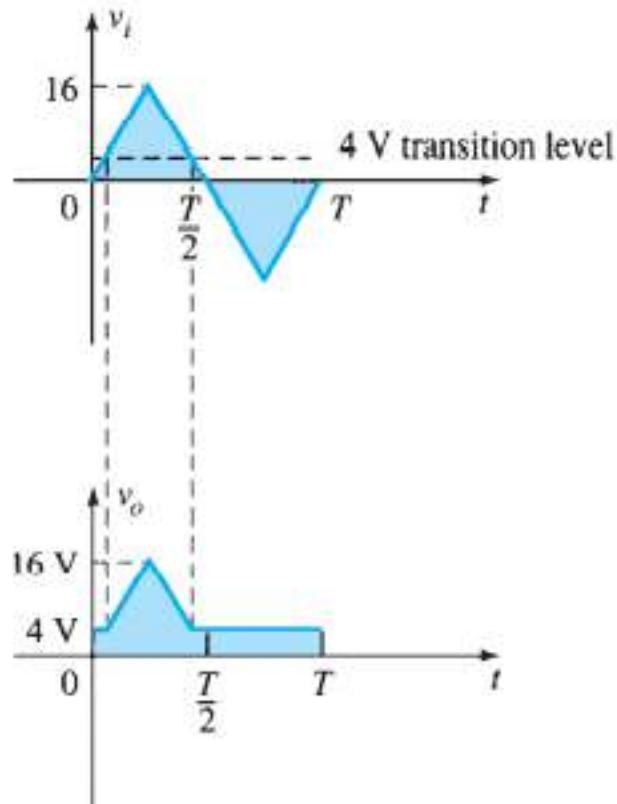
$$V_o = 0 \text{ V}$$

When $V_i < 4V$, diode is OFF and is replaced by short circuit equivalent



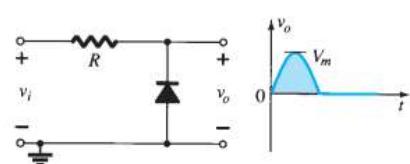
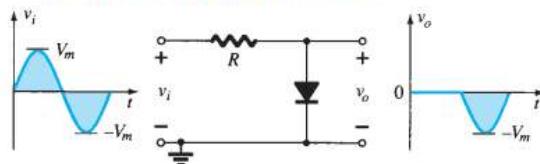
Apply KVL in the above circuit and ignore V_k (0.7V)

$$V_o = 4V$$

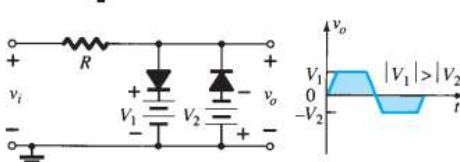
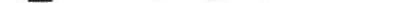
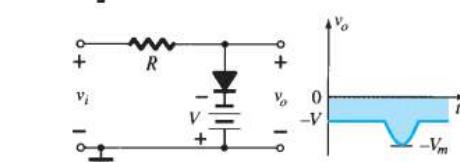
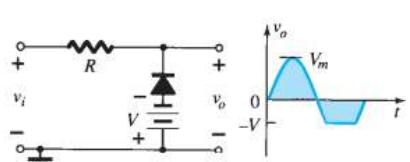
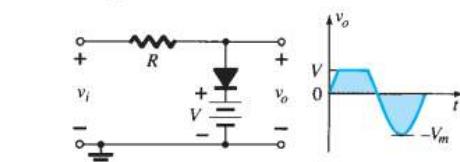


That part of V_i less than 4V is clipped by this clipper.

Simple Parallel Clippers (Ideal Diodes)

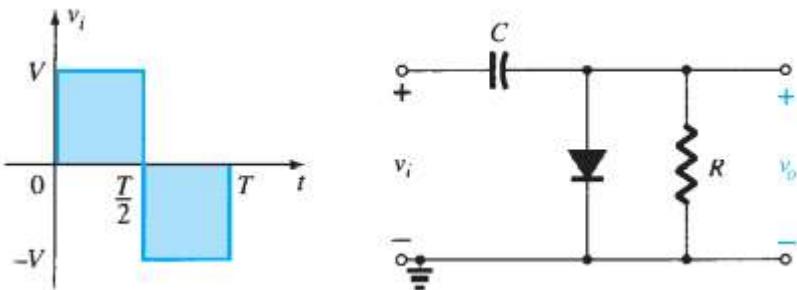


Biased Parallel Clippers (Ideal Diodes)



CLAMPERS

- A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.
- Additional shifts can also be obtained by introducing a dc supply to the basic structure.
- The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $t \text{ RC}$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting.
- Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.
- Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal.
- The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.



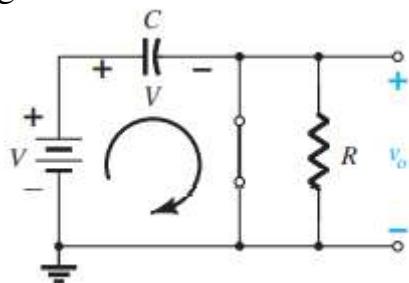
Clamper

Analysis

There is a sequence of steps that can be applied to help make the analysis straightforward

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the “on” state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.



During positive half cycle Diode is On, so we start analysis with positive cycle. Replace Diode with short circuit equivalent and apply KVL to find V_c (voltage across capacitor) & V_o (Output Voltage)

$$V - V_c = 0 \text{ volt}$$

$$V_c = V$$

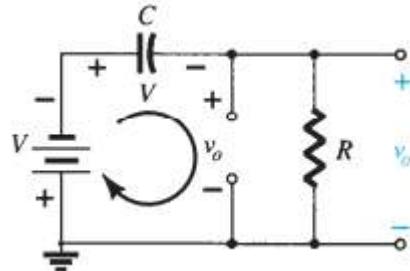
KVL in other loop

$$V_o = 0 \text{ Volt}$$

Step 3: Assume that during the period when the diode is in the “off” state the capacitor holds on to its established voltage level.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

During negative half cycle Diode is off, diode is replaced with open circuit equivalent. Change the polarity of input V but don't change polarity as well as magnitude of V_c (Voltage across capacitor).



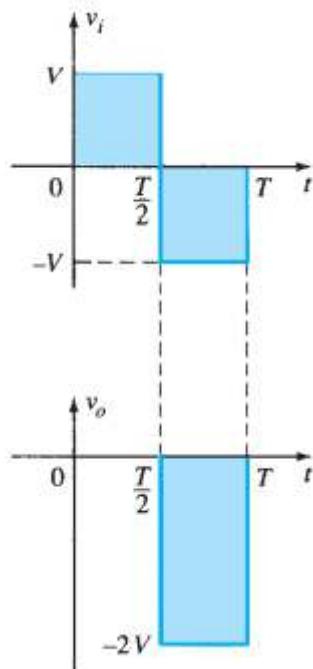
Apply KVL in outermost loop and find V_o

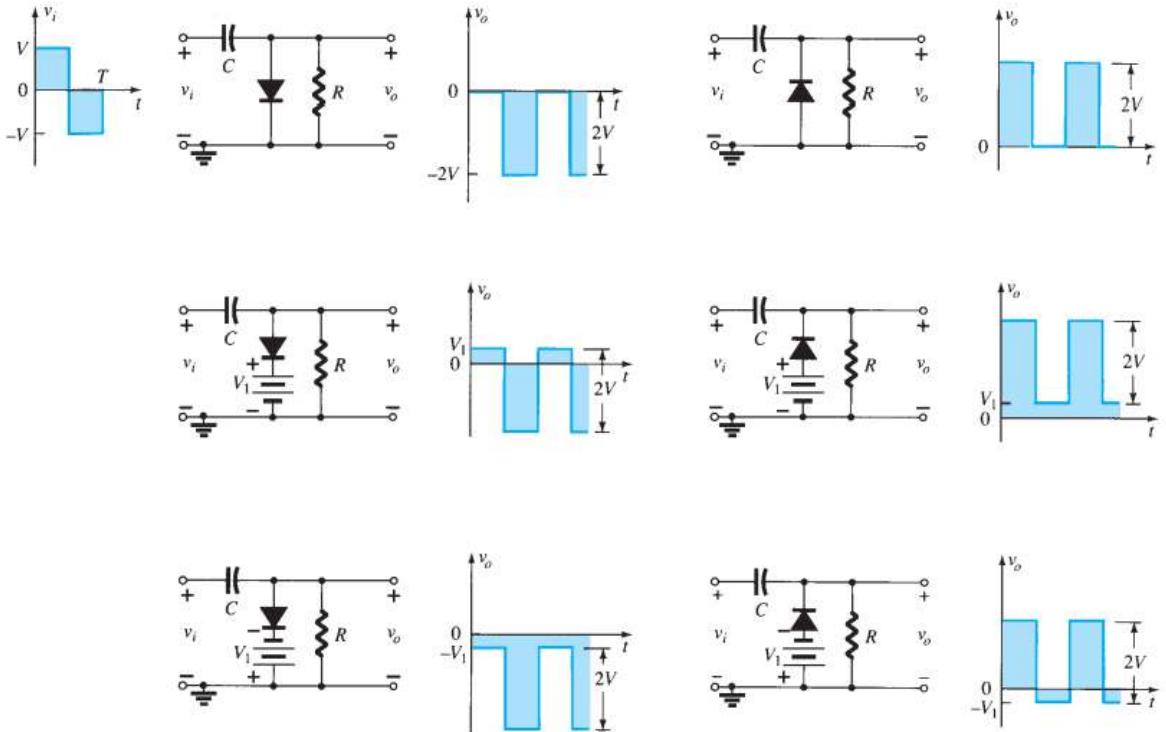
$$-V - V_c - V_o = 0$$

$$V_o = -V_c - V \quad (V_c = V)$$

$$V_o = -2V$$

Step 5: Check that the total swing of the output matches that of the input. This is a property that applies for all clamping networks, giving an excellent check on the results obtained.





Different combinations of Clampers with their outputs

VOLTAGE-MULTIPLIER CIRCUITS

Voltage Doubler

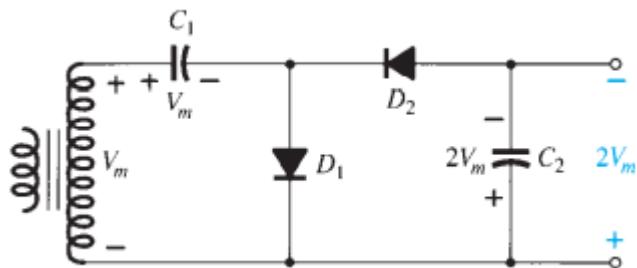
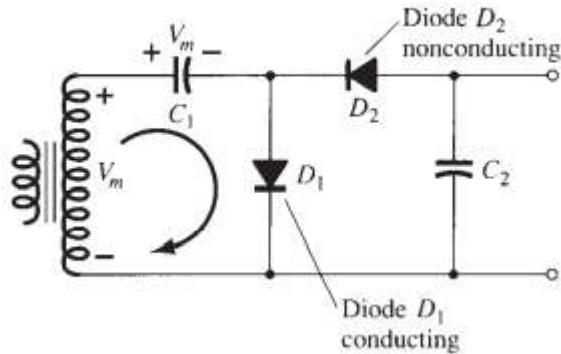
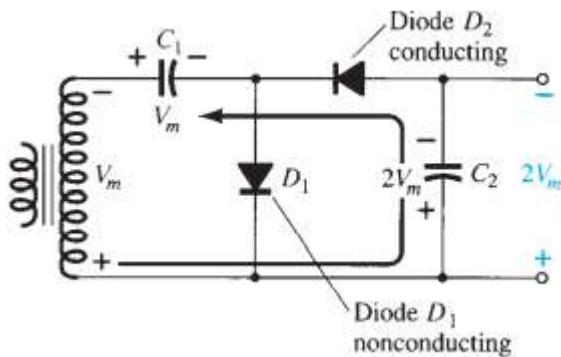


Fig. is a half-wave voltage doubler

- During the positive voltage half cycle across the transformer, secondary diode D1 conducts (and diode D2 is cut off), charging capacitor C1 up to the peak rectified voltage (V_m).
- Diode D1 is ideally a short during this half-cycle, and the input voltage charges capacitor C1 to V_m with the polarity shown in Fig below.



- During the negative half-cycle of the secondary voltage, diode D1 is cut off and diode D2 conducts charging capacitor C2 .
- Since diode D2 acts as a short during the negative half-cycle (and diode D1 is open), we can sum the voltages around the outside loop.



- On the next positive half-cycle, diode D2 is nonconducting and capacitor C2 will discharge through the load.
- If no load is connected across capacitor C2 , both capacitors stay charged— C1 to V m and C2 to 2 V m .
- If there is a load connected to the output of the voltage doubler, the voltage across capacitor C2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to 2 V m during the negative half cycle.

Light Emitting Diode (LED)

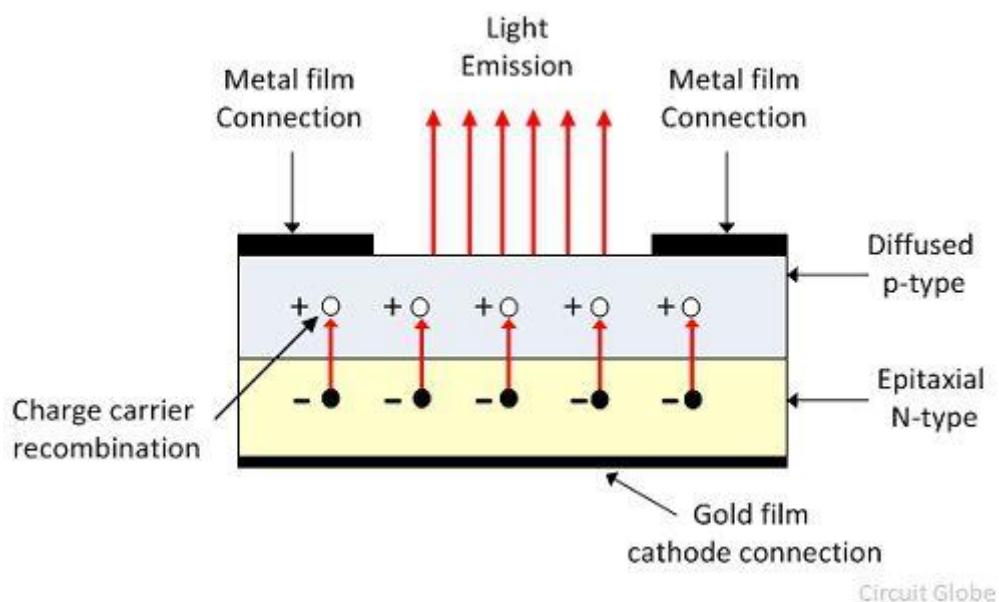
Definition:

The LED is a PN-junction diode which emits light when an electric current passes through it in the forward direction. In the LED, the recombination of the charge carrier takes place. The electron from the N-side and the hole from the P-side are combined and gives the energy in the form of heat and light. The LED is made of semiconductor material which is colourless, and the light is radiated through the junction of the diode.

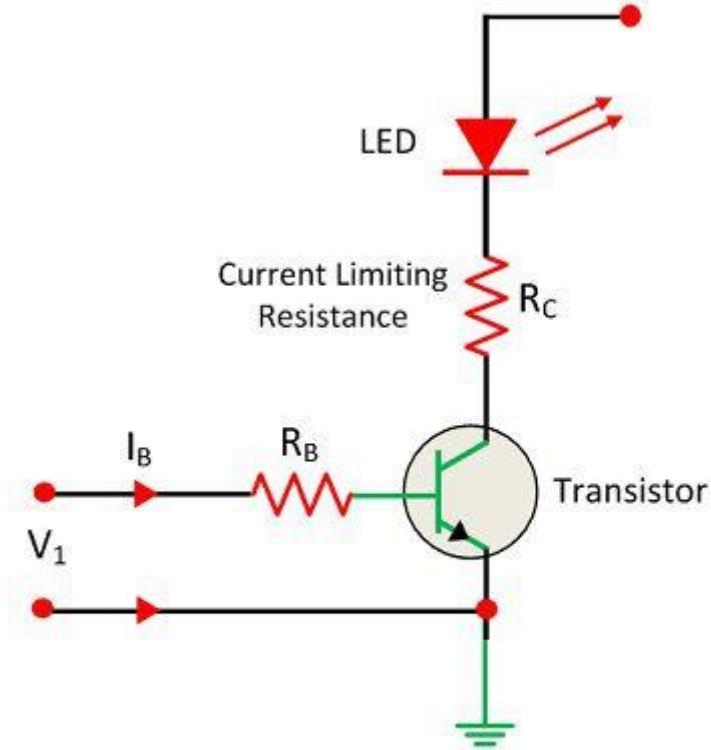
The LEDs are extensively used in segmental and dot matrix displays of numeric and alphanumeric characters. The several LEDs are used for making the single line segment while for making the decimal point single LED is used.

Construction of LED

The recombination of the charge carrier occurs in the P-type material, and hence P-material is the surface of the LED. For the maximum emission of light, the anode is deposited at the edge of the P-type material. The cathode is made of gold film, and it is usually placed at the bottom of the N-region. This gold layer of cathode helps in reflecting the light to the surface.



The gallium arsenide phosphide is used for the manufacturing of LED which emits red or yellow light for emission. The LED are also available in green, yellow amber and red in colour.



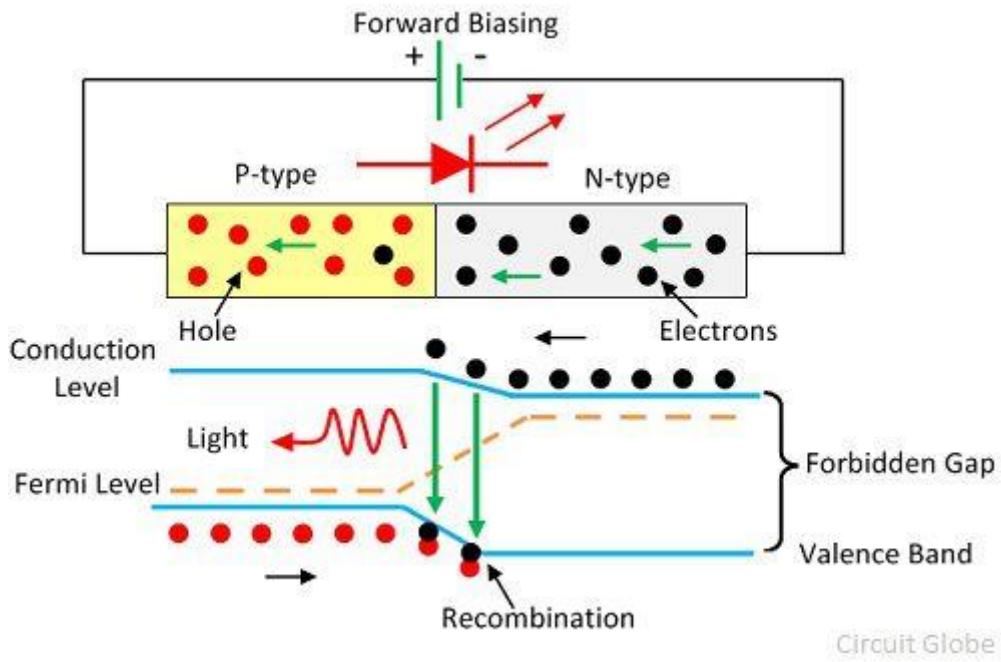
LED controlled by a Transistor switch

Circuit Globe

The simple transistor can be used for off/on of a LED as shown in the figure above. The base current I_B conducts the transistor, and the transistor conducts heavily. The resistance R_C limits the current of the LED.

Working of LED

The working of the LED depends on the quantum theory. The quantum theory states that when the energy of electrons decreases from the higher level to lower level, it emits energy in the form of photons. The energy of the photons is equal to the gap between the higher and lower level



The LED is connected in the forward biased, which allows the current to flow in the forward direction. The flow of current is because of the movement of electrons in the opposite direction. The recombination shows that the electrons move from the conduction band to valence band and they emit electromagnetic energy in the form of photons. The energy of photons is equal to the gap between the valence and the conduction band.

Advantages of LED in electronic displays

The following are the major advantages of the LED in an electronics display.

1. The LEDs are smaller in size, and they can be stacked together to form numeric and alphanumeric displays in the high-density matrix.
2. The intensity of the light output of the LED depends on the current flowing through it. The intensity of their light can be controlled smoothly.
3. The LEDs are available which emit light in the different colours like red, yellow, green and amber.
4. The on and off time or switching time of the LED is less than 1 nanoseconds. Because of this, the LEDs are used for the dynamic operation.
5. The LEDs are very economical and give the high degree of reliability because they are manufactured with the same technology as that of the transistor.

6. The LEDs are operated over a wide range of temperature say $0^\circ - 70^\circ$. Also, it is very durable and can withstand shock and variation.
7. The LEDs have a high efficiency, but they require moderate power for operation. Typically, the voltage of 1.2V and the current of 20mA is required for full brightness. Therefore, it is used in a place where less power is available.

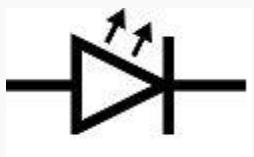
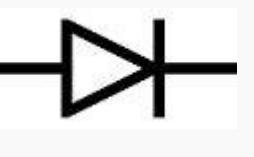
Disadvantages of LED

The LED consumes more power as compared to LCD, and their cost is high. Also, it is not used for making the large display.

Home Work:

1. Difference Between LED & Diode
2. Difference Between LED & LCD

Comparison Chart of LED & Diode

Basis for Comparison	LED	Diode
Definition	The type of diode which when placed in an electric field emits light.	It is a semiconductor diode which conducts only in one direction.
Symbol		

Material	GaAs (Gallium Arsenide) and GaP (Gallium Phosphide)	Silicon and Germanium
Principle	Converts energy into light.	Converts energy into heat.
Reverse Breakdown Voltage value	Low	High
On-state voltage range	1.2v – 2.0v	0.7v for silicon and 0.3v for germanium.
Application	Rectification i.e., converts the ac to dc.	Emits light
Uses	Indicators in seven segment displays, use as light source.	Rectifiers, voltage multipliers, clamping, etc.

Comparison Chart of LED & Lcd

Basis For Comparison	LED	LCD
Definition	PN-Junction device which discharge visible lights when an electrical charge passes through it.	It is an optical device used for displaying the information in the form of text and images.
Stand For	Light Emitting Diode	Liquid Crystal Display
Backlight	No backlight	Cold cathode fluorescent lamp provides backlight.

Resolution	High	Low
Power Requirement	More	Less
Display Area	Small	Large
Cost	High	Low
Material	Gallium arsenide phosphide.	Liquid crystals and glass electrodes.
Switching Time	Fast	Slow
Direct Current	Do not effects.	Reduces Life Span
Contrast Ratio	Low	High
Mercury	Not used	Used

Photodiode

Definition: A special type of PN junction device that generates current when exposed to light is known as Photodiode. It is also known as a photodetector or photosensor. It operates in reverse biased mode and **converts light energy into electrical energy**.

The figure below shows the symbolic representation of a photodiode:



Symbolic representation of Photodiode

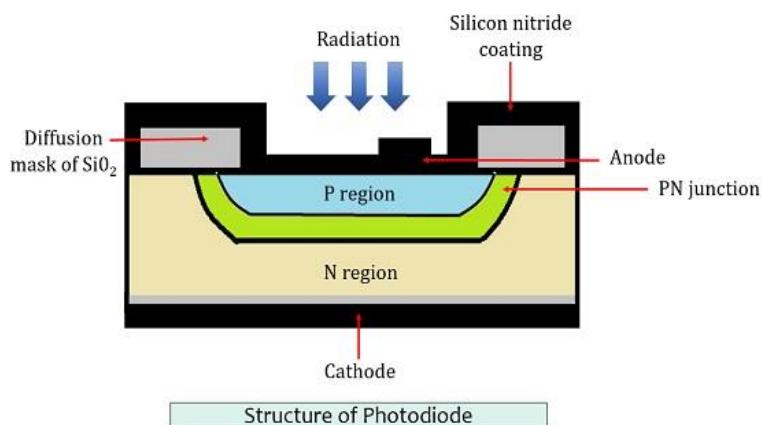
Principle of Photodiode

It works on the principle of **Photoelectric effect**.

The operating principle of the photodiode is such that when the junction of this two-terminal semiconductor device is illuminated then the electric current starts flowing through it. Only minority current flows through the device when the certain reverse potential is applied to it.

Construction of Photodiode

The figure below shows the constructional detail of a photodiode:



The PN junction of the device is placed inside a glass material. This is done in order to allow the light energy to pass through it. As only the junction is exposed to radiation, thus, the other portion of the glass material is painted black or is metallised.

The overall unit is of very small dimension, nearly about **2.5 mm**.

It is noteworthy that the current flowing through the device is in **micro-ampere** and is measured through an ammeter.

Operational Modes of Photodiode

Photodiode basically operates in two modes:

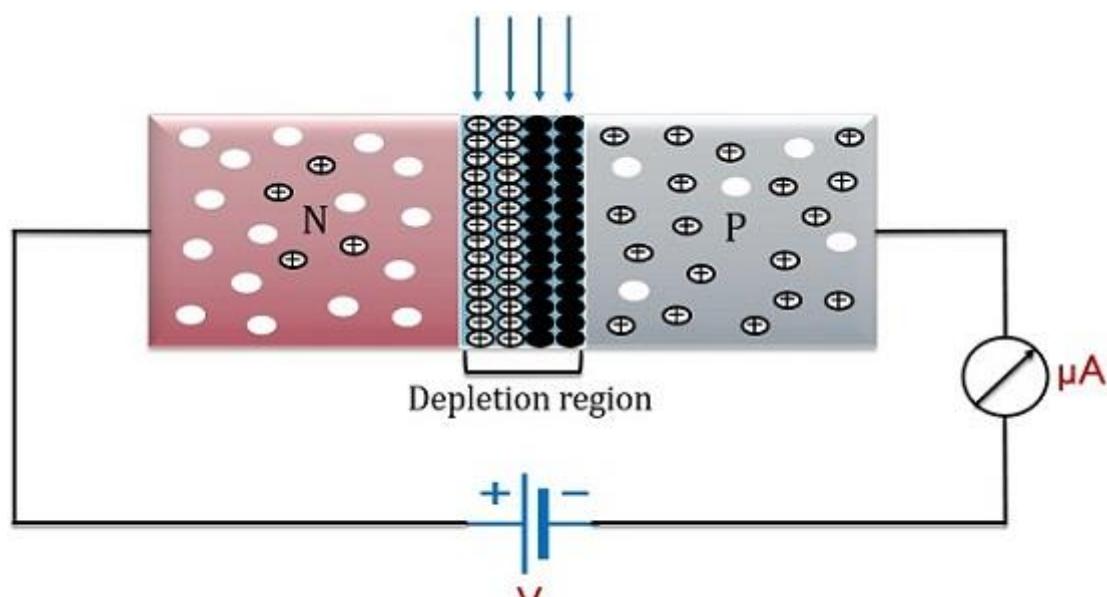
- **Photovoltaic mode:** It is also known as zero-bias mode because no external reverse potential is provided to the device. However, the flow of minority carriers will take place when the device is exposed to light.

- **Photoconductive mode:** When a certain reverse potential is applied to the device then it behaves as a photoconductive device. Here, an increase in depletion width is seen with the corresponding change in reverse voltage.

Let us now understand the detailed circuit arrangement and working of the photodiode.

Working of Photodiode

In the photodiode, a very small reverse current flows through the device that is termed as **dark current**. It is called so because this current is totally the result of the flow of minority carriers and is thus flows when the device is not exposed to radiation



Structure and biasing arrangement of Photodiode

The electrons present in the p side and holes present in n side are the minority carriers. When a certain reverse-biased voltage is applied then minority carrier, holes from n-side experiences repulsive force from the positive potential of the battery.

Similarly, the electrons present in the p side experience repulsion from the negative potential of the battery. Due to this movement electrons and holes recombine at the junction resultantly in a depletion region at the junction.

Due to this movement, a very small reverse current flows through the device known as dark current.

The combination of electron and hole at the junction generates a neutral atom at the depletion. Due to which any further flow of current is restricted.

Now, the junction of the device is illuminated with light. As the light falls on the surface of the junction, then the temperature of the junction gets increased. This causes the electron and hole to get separated from each other.

At the two gets separated then electrons from n side gets attracted towards the positive potential of the battery. Similarly, holes present in the p side get attracted to the negative potential of the battery.

This movement then generates high reverse current through the device.

With the rise in the light intensity, more charge carriers are generated and flow through the device. Thereby, producing a large electric current through the device.

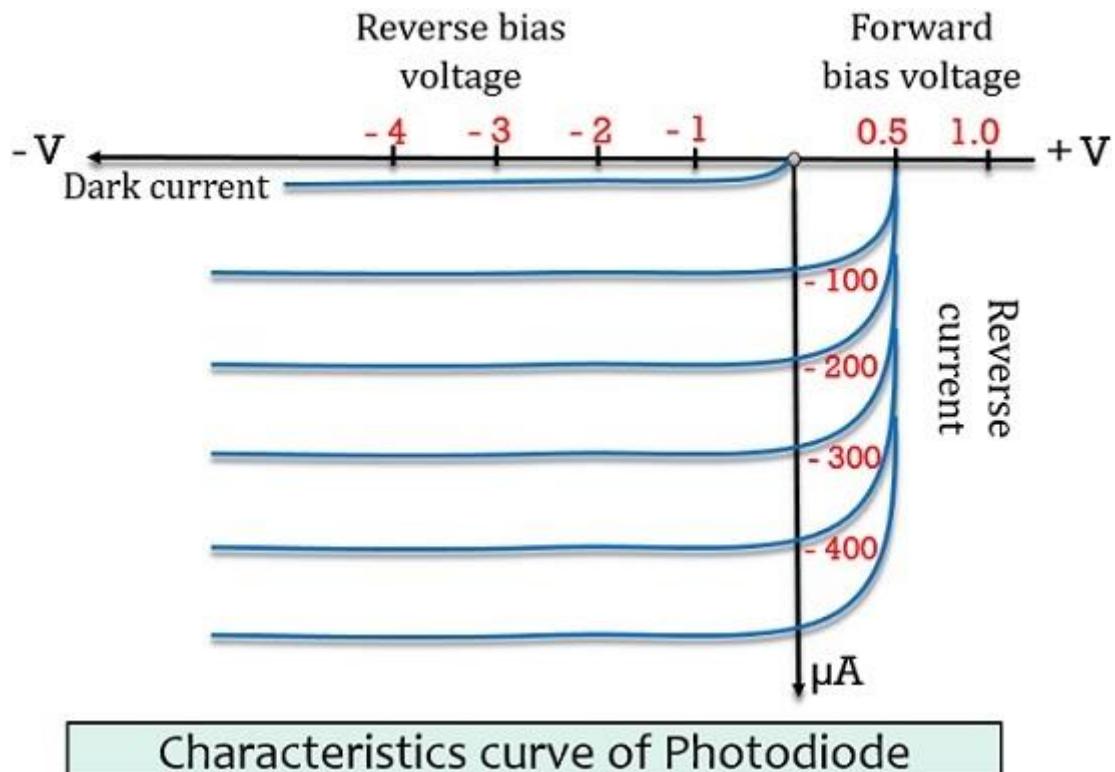
This current is then used to drive other circuits of the system.

So, we can say the intensity of light energy is directly proportional to the current through the device.

Only positive biased potential can put the device in no current condition in case of the photodiode.

CHARACTERISTICS OF PHOTODIODE

The figure below shows the VI characteristic curve of a photodiode:



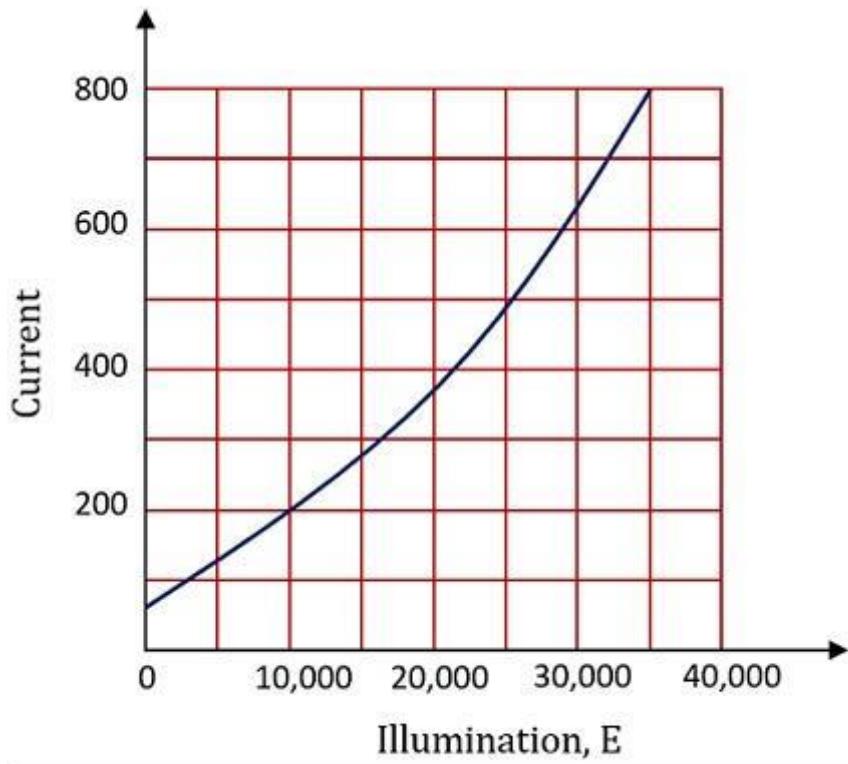
Characteristics curve of Photodiode

Here, the vertical line represents the reverse current flowing through the device and the horizontal line represents the reverse-biased potential.

The first curve represents the dark current that generates due to minority carriers in the absence of light.

As we can see in the above figure that all the curves show almost equal spacing in between them. This is so because current proportionally increases with the luminous flux.

The figure below shows the curve for current versus illumination:



Illumination versus current curve

It is noteworthy here that the reverse current does not show a significant increase with the increase in the reverse potential.

Advantages of Photodiode

- It shows a quick response when exposed to light.
- Photodiode offers high operational speed.
- It provides a linear response.
- It is a low-cost device.

Disadvantages of Photodiode

- It is a temperature-dependent device. And shows poor temperature stability.
- When low illumination is provided, then amplification is necessary.

Applications of Photodiode

1. Photodiodes majorly find its use in counters and switching circuits.
2. Photodiodes are extensively used in an optical communication system.
3. Logic circuits and encoders also make use of photodiodes.
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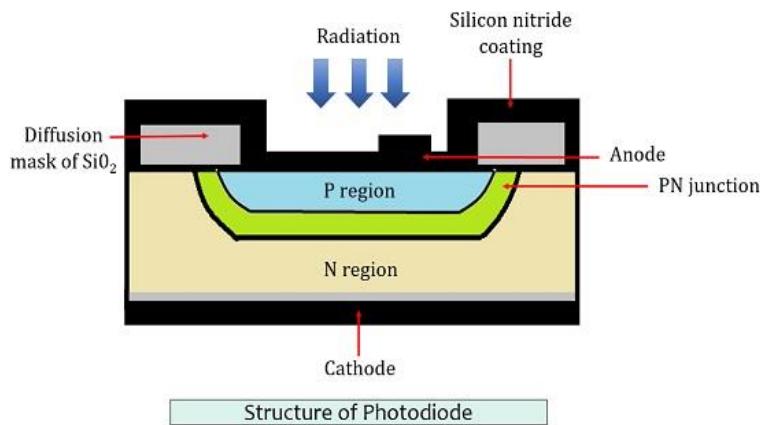
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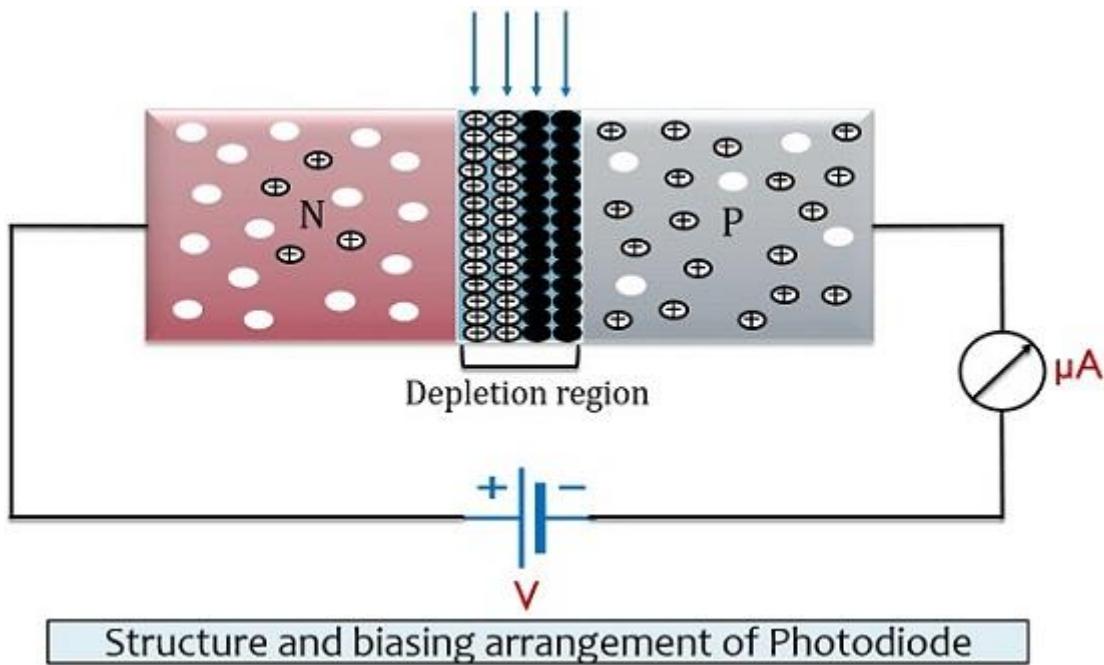
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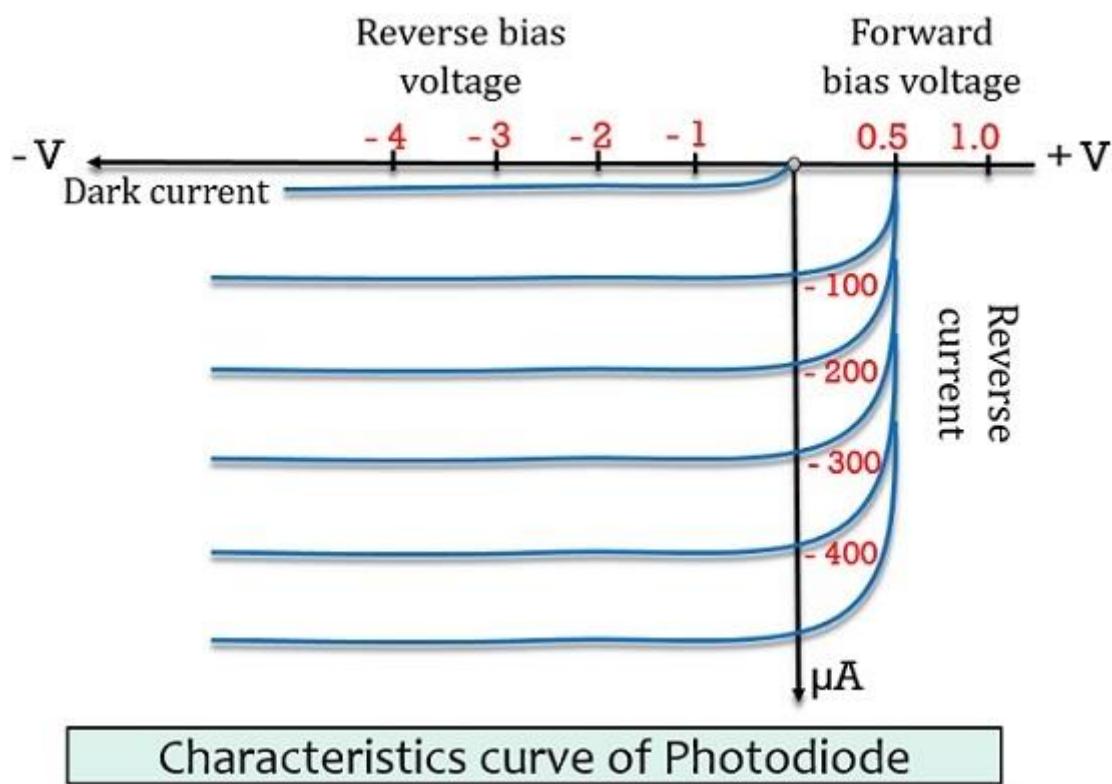
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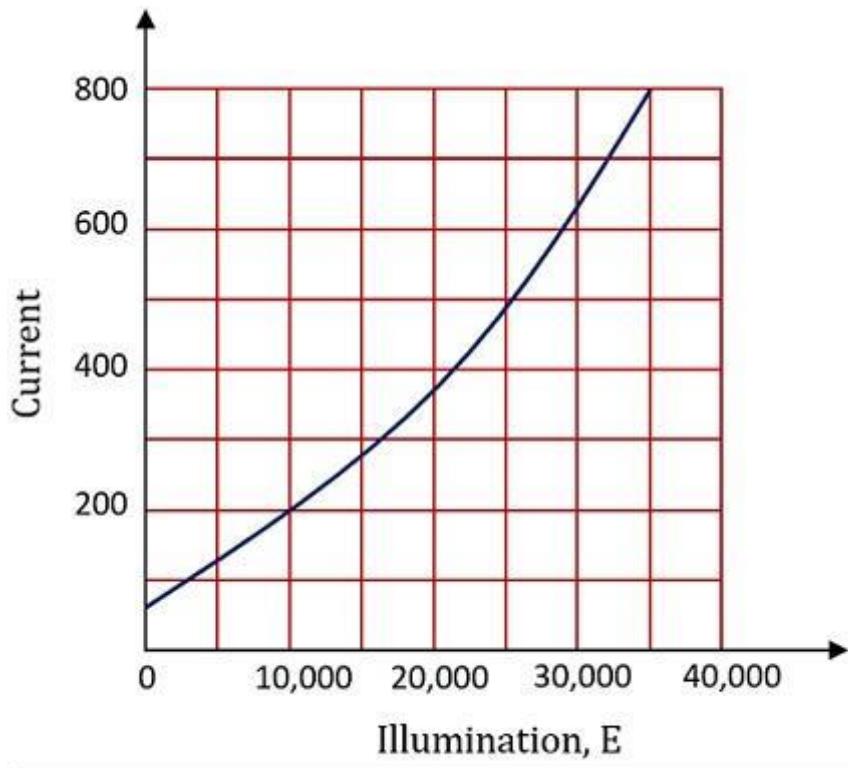


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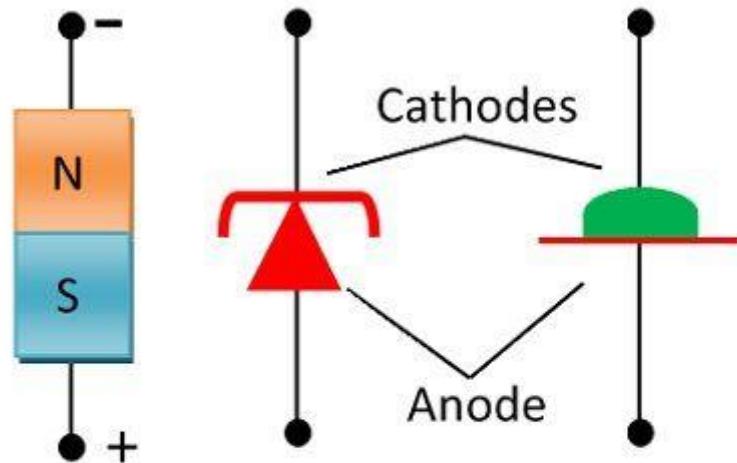
Tunnel Diode

Definition: The tunnel diode is a highly conductive, heavily doped PN-junction diode in which the current induces because of the tunnelling. The tunnelling is the phenomenon of conduction in the semiconductor material in which the charge carrier punches the barrier instead of climbing through it.

The tunnel diode is a heavily doped PN-junction diode. The concentration of impurity in the normal PN-junction diode is about 1 part in 10⁸. And in the tunnel diode, the concentration of the impurity is about 1 part in 10³. Because of the heavy doping, the diode conducts current both in the forward as well as in the reverse direction. It is a fast switching device; thereby it is used in high-frequency oscillators, computers and amplifiers.

Symbol of Tunnel Diode

The symbol of the tunnel diode is shown in the figure below. The cathode and anode are the two terminals of semiconductor material. The p-type material attracts the electrons and hence it is called anode while the n-type material emits the electrons and it is named as the cathode.

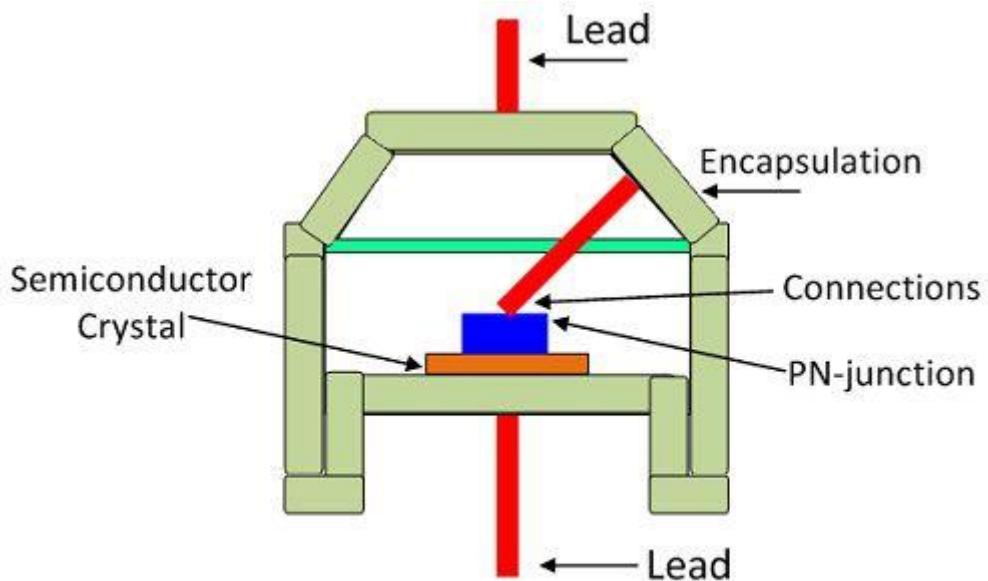


Tunnel Diode Symbols

Circuit Globe

Construction of Tunnel Diode

The device is constructed by using the two terminals namely anode and cathode. The p-type semiconductor acts as an anode, and the n-type semiconductor material acts as a cathode. The gallium arsenide, germanium and gallium antimonide are used for manufacturing the tunnel diode.



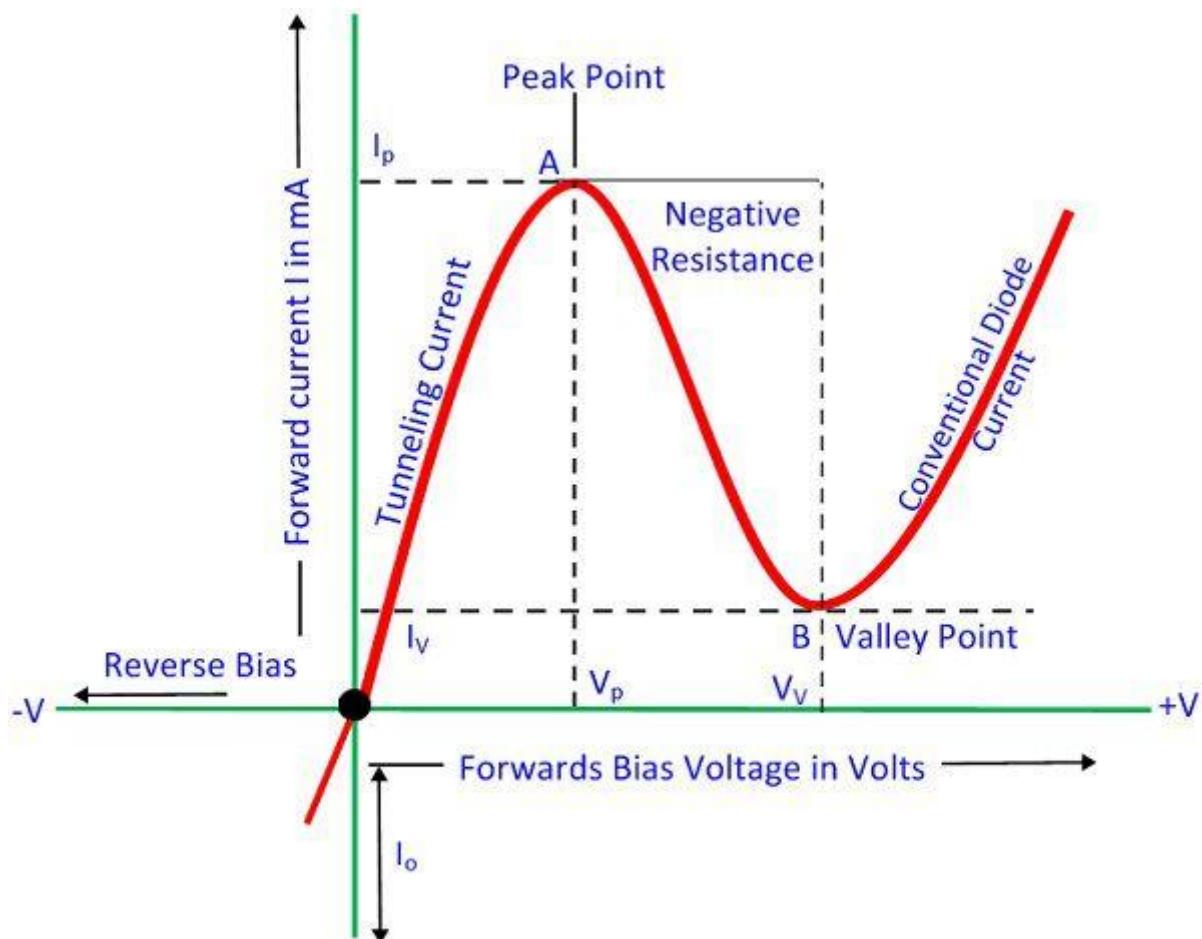
Pellet Tunnel Diode

Circuit Globe

The ratio of the peak value of the forward current to the value of the valley current is maximum in case of germanium and less in silicon. Hence silicon is not used for fabricating the tunnel diode. The doping density of the tunnel diode is 1000 times higher than that of the ordinary diode.

Volt-Amp Characteristic

In forward biasing, the immediate conduction occurs in the diode because of their heavy doping. The current in a diode reached their maximum value I_p when the V_p voltage applied across it. When further the voltage increases, the current across the terminal decreases. And it decreases until it reaches their minimum value. This minimum value of current is called the valley current I_v .



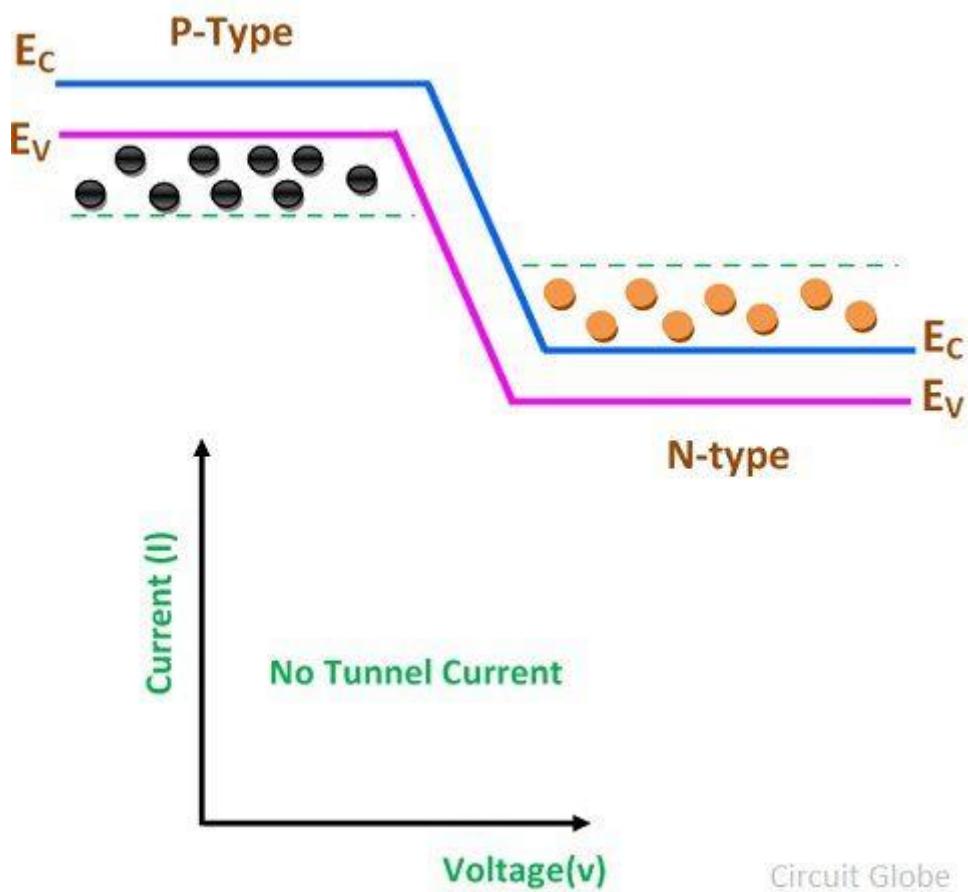
The graph above shows that from point A to point B the value of current decreases with the increase of voltage. So, from A to B, the graph shows the

negative resistance region of the tunnel diode. This region shows the most important property of the diode. Here in this region, the tunnel diode produces the power instead of absorbing it.

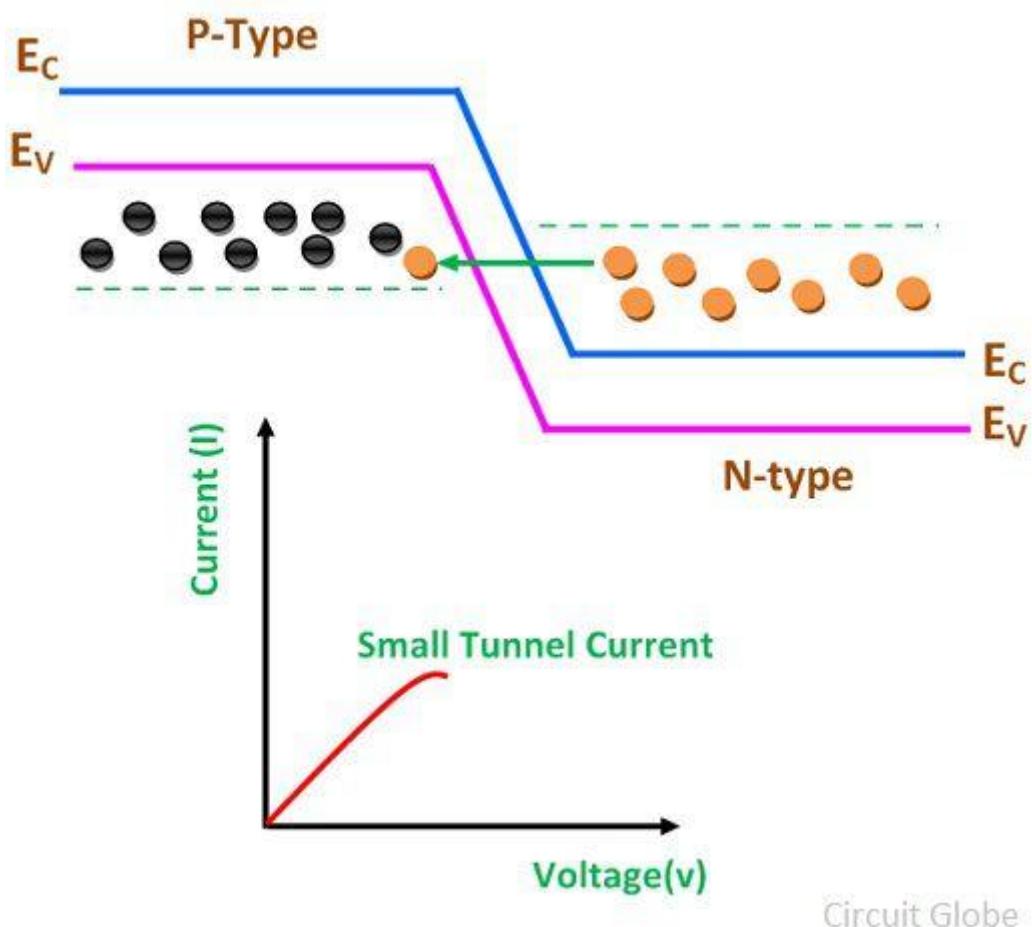
Tunnel Diode Working

When the tunnel diode is unbiased, or we can say when no voltage is applied across the diode in that case the conduction band of the n-type semiconductor material overlaps with the valence band of the p-type material. This happens because of the heavy doping. The energy levels of the hole and the electron in the p and n-side respectively remain the same.

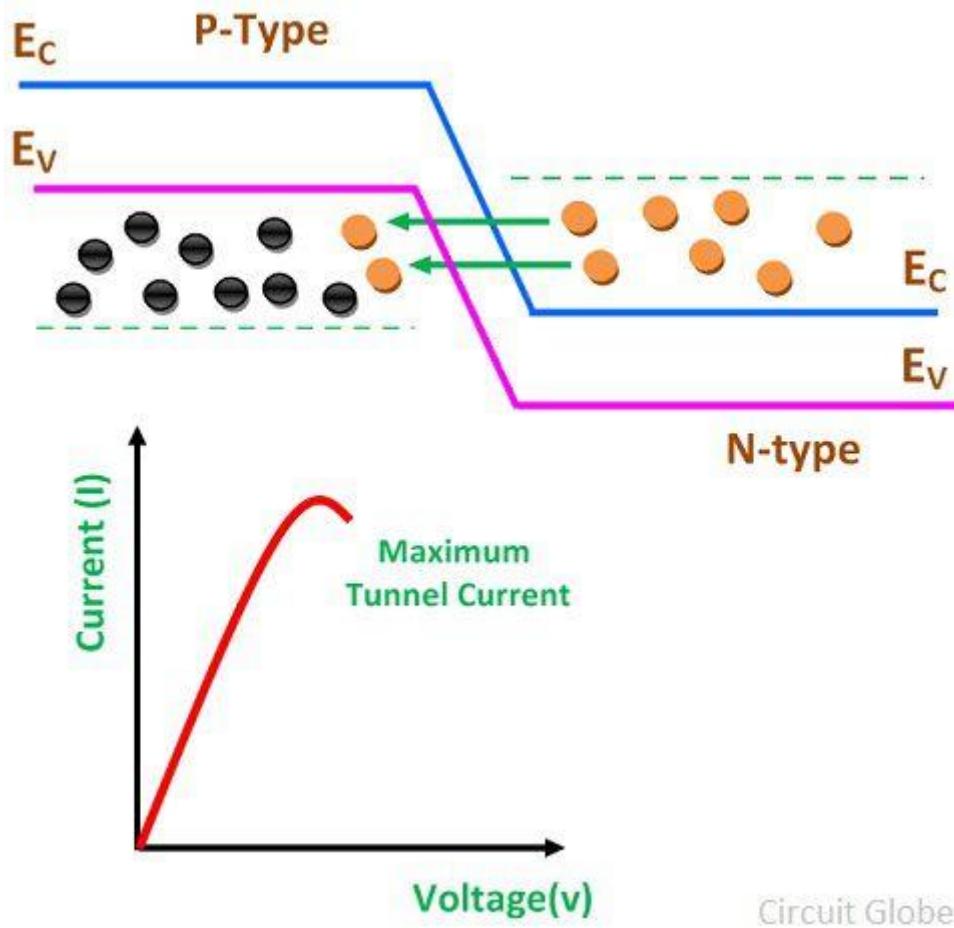
When the temperature rises, the electrons tunnel from the conduction band of the n-region to the valence band of the p-region. Similarly, the hole, tunnel from the valence band of the p-region to the conduction band of n-region. The zero current flows through the diode in the unbiased condition.



When the small voltage is applied across the tunnel diode whose magnitude is less than built-in-depletion region voltage, then no electrons cross the depletion region and zero current flows through the diode. The few electrons from n-region of the conduction band are tunnelled into the p-region of the valence band. Because of the tunnelling of electrons, the small forward current flows through the depletion region.

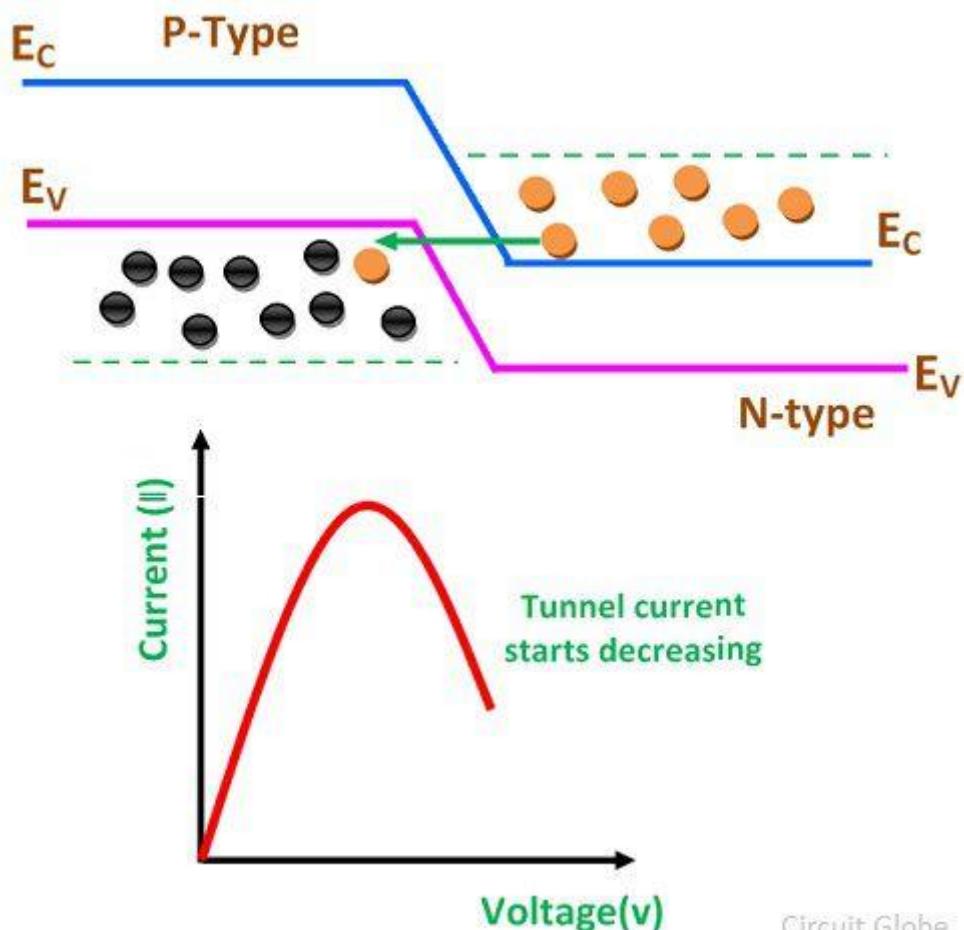


When the heavy voltage applied across the tunnel diode, the number of electrons and holes are generated. The increase in voltage increases the overlapping of conduction and valence band. The energy levels of the n-side valence band and the p-side conduction band is equal. Thus, the maximum current flows through the tunnel.



Circuit Globe

When the applied voltage is further increased then the valence and conduction band of the diode is slightly misaligned. But the conduction band of the n-type region and the valence band of the p-type region still overlap. The small current flows through the diode, and thus the tunnel current starts decreasing.



Circuit Globe

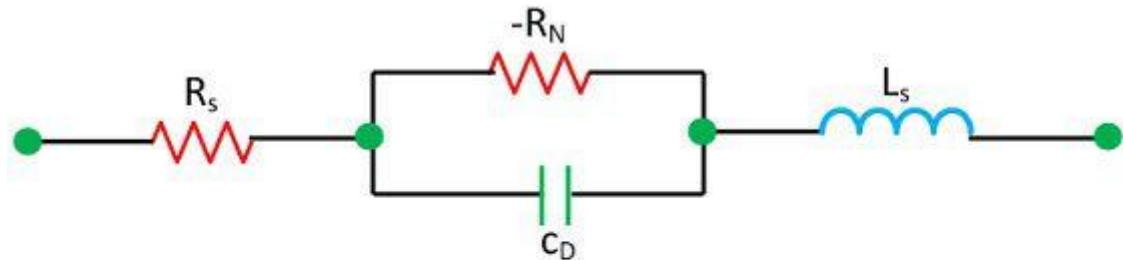
If the voltage across the conductor is heavily increasing, the tunnel current drops down to zero. In this condition, the conduction band of the n-side and valence band of P-side are not overlapping each other, and the diode behaves like an ordinary PN-junction diode. If the magnitude of the voltage is larger than the built-in voltage, the forward current flows through the diode.

What is negative Resistance in Tunnel Diode?

It is shown above in the graph that between the point I_v and I_p the current starts decreasing when the voltage is applied to it. This region of the graph is known as the negative resistance region. It is the most important characteristic of the tunnel diode. In this region, the tunnel diode generates the power instead of absorbing it.

The equivalent circuit of the tunnel diode is expressed in the figure below. The R_s represents the resistance of the connecting leads of the diode and the semiconductor material. It is approximately equal to the 5Ω . The L_s is the

inductance of the connecting leads, and it is nearly equal to the 0.5nH. The Cd is the junction diffusion capacitance, and their magnitude lies between 5 to 100pF.



Equivalent Circuit for a Tunnel Diode

Circuit Globe

Advantages & Disadvantages of Tunnel Diode

The tunnel diode has low cost. It produces low noise, and their fabrication is also very simple. The diode gives a fast response, and it is moderate in operation. The tunnel diode works on low power.

The disadvantage of the tunnel diode is that the output voltage of the diode swings. It is a two terminal device, but their input and output circuits are not isolated from each other.

Applications of Tunnel Diode

The tunnel diode can be used as an amplifier and as an oscillator for detecting small high-frequency or as a switch. It is a high-frequency component because it gives the very fast responses to the inputs.

The tunnel diode is not widely used because it is a low current device.

Liquid Crystal Diode (LCD)

Definition:

The LCD is defined as the diode that uses small cells and the ionised gases for the production of images. The LCD works on the modulating property of light. The light modulation is the technique of sending and receiving the signal through the light. The liquid crystal consumes a small amount of energy because they are the reflector and the transmitter of light. It is normally used for seven segmental display.

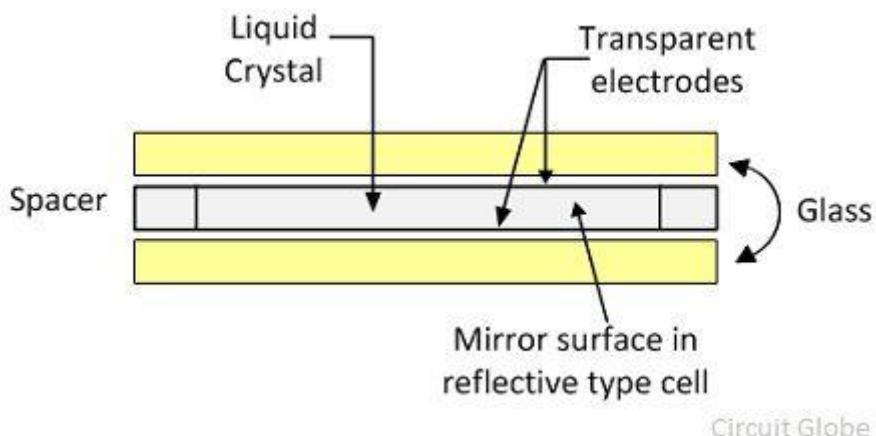
Construction of LCD

The liquid crystals are the organic compound which is in liquid form and shows the property of optical crystals. The layer of liquid crystals is deposited on the inner surface of glass electrodes for the scattering of light. The liquid crystal cell is of two types; they are Transmittive Type and the Reflective Type.

Transmittive Type – In transmitter cell both the glass sheets are transparent so that the light is scattered in the forward direction when the cell becomes active.

Reflective Type – The reflective type cell consists the reflecting surface of the glass sheet on one end. The light incident on the front surface of the cell is scattered by the activated cell.

Both the reflective and transmittive type cells appear brights, even under small ambient light conditions.



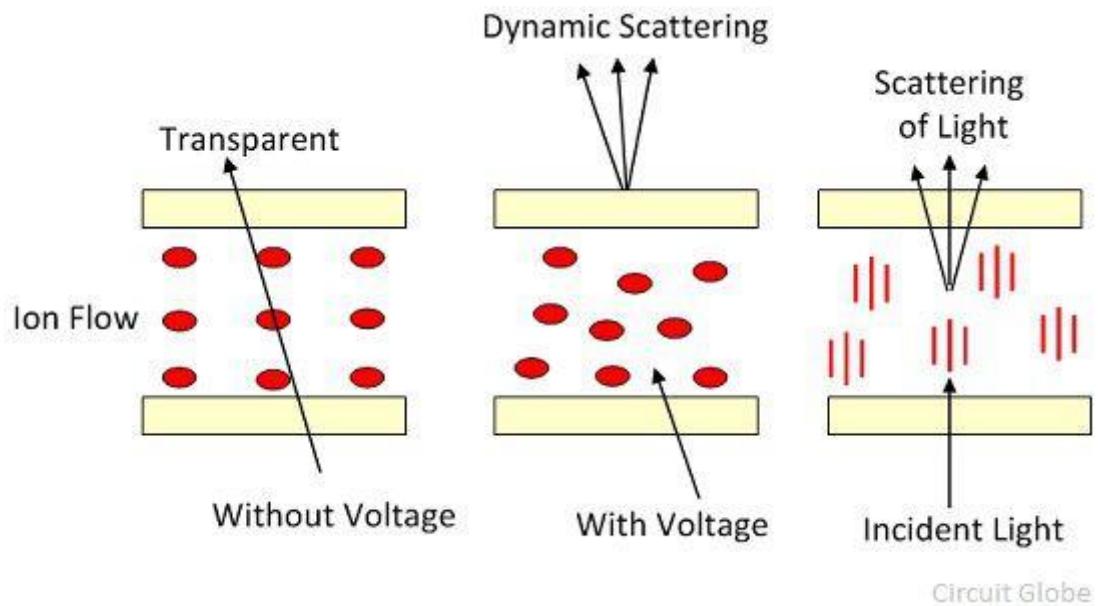
Circuit Globe

Working Principle of LCD

The working principle of the LCD is of two types. They are the dynamic scattering type and the field effects type. Their details explanation is shown below.

Dynamic Scattering

When the potential carrier flows through the light, the molecular alignment of the liquid crystal disrupts, and they produce disturbances. The liquid becomes transparent when they are not active. But when they are active their molecules turbulence causes scattered of light in all directions, and their cell appears bright. This type of scattering is known as the dynamic scattering. The construction of the dynamic scattering of the liquid crystal cell is shown in the figure



Field Effect Type

The construction of liquid crystals is similar to that of the dynamic scattering types the only difference is that in field effect type LCD the two thin polarising optical fibres are placed inside the each glass sheet. The liquid crystals used in field effect LCDs are of different scattering types that operated in the dynamic scattering cell.

The field affects type LCD uses the nematic material which twists the unenergised light passing through the cell. The nematic type material means the liquid crystals in which the molecules are arranged in parallel but not in a well-defined plane. The light after passing through the nematic material passing through the optical filters and appears bright. When the cell has energised no twisting of light occurs, and the cell appears dull.

Advantages of LCD

The following are the advantages of LCD.

The power consumption of LCD is low. The seven segmental display of LCD requires about $140\mu\text{W}$ which is the major advantages over LED which uses approximately 40mW per numeral.

The cost of the LCD is low.

Disadvantages of LCD

The following are the disadvantages of LCD.

The LCD is a slow device because their turning on and off times are quite large. The turn-on time of the LCD is millisecond while there turn off time is ten milliseconds.

The LCD requires the large area.

The direct current reduces the lifespan of LCD. Therefore, the LCD uses with AC supply, having the frequency less than 500Hz.

The LCD requires AC voltage for working.

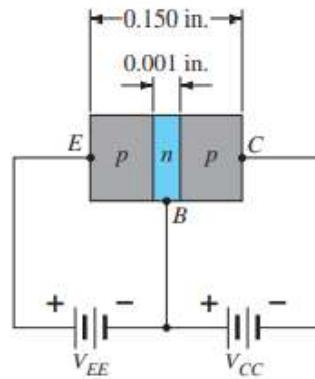
UNIT 2

Bipolar Junction Transistor

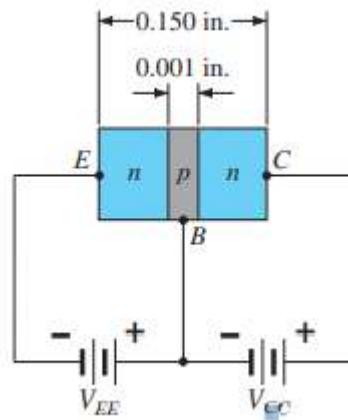
Transistor Construction

The transistor is a three-layer semiconductor device consisting of either two n - and one p -type layers of material or two p - and one n -type

layers of material. The former is called an npn transistor , and the latter is called a pnp transistor.



pnp Transistor

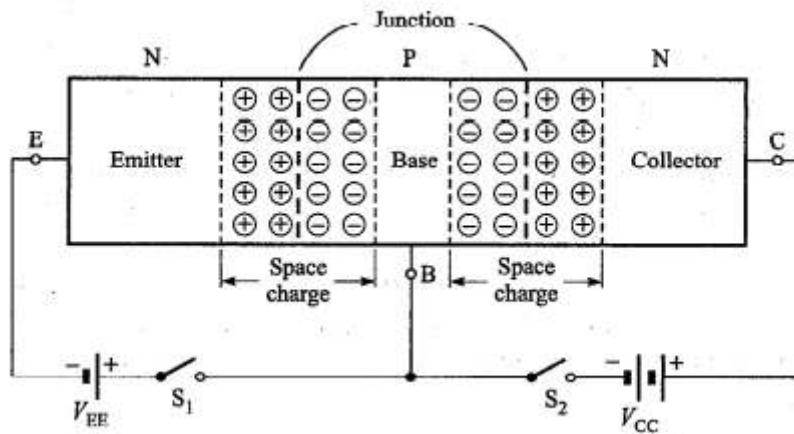


npn Transistor

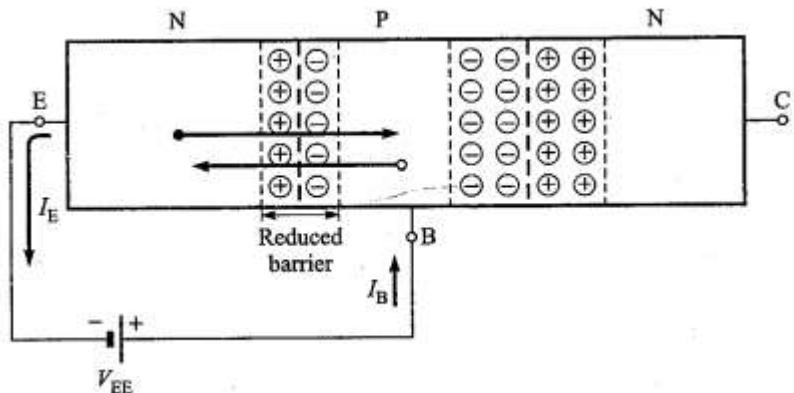
- The emitter layer is heavily doped, with the base and collector only lightly doped.
- The outer layers have widths much greater than the sandwiched p - or n - type material. For the transistors shown in Fig. the ratio of the total width to that of the center layer is 0.150/0.001 = 150:1.
- The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 1:10 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of “free” carriers.
- The terminals have been indicated by the capital letters E for emitter , C for collector and B for base.
- The abbreviation BJT, from bipolar junction transistor, is often applied to this three-terminal device.
- The term bipolar reflects the fact that holes and electrons participate in the injection process.

TRANSISTOR OPERATION

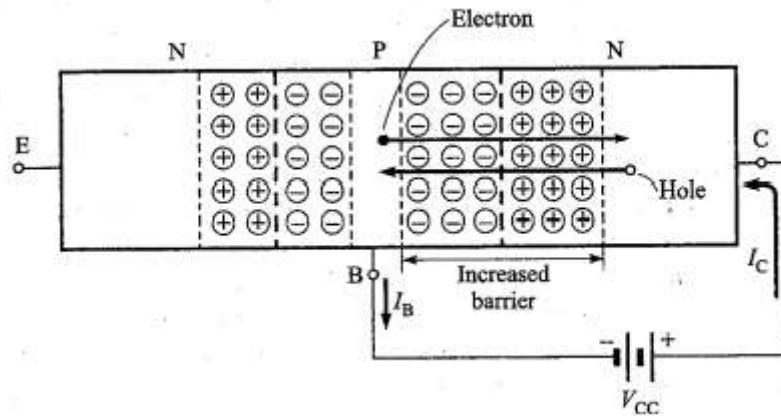
A transistor has two junctions-emitter junction and a collection junction.



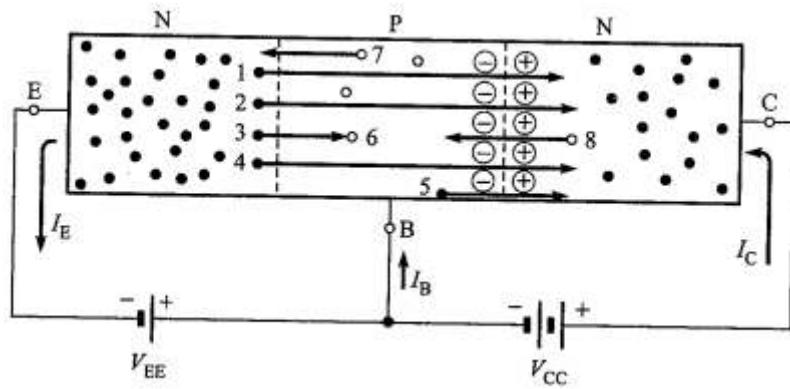
- For the sake of clarity, the base region has been shown very wide. (Remember, the base is actually made very narrow.)
- The battery V_{EE} acts to forward bias the emitter junction, and the battery V_{CC} acts to reverse bias the collector junction.
- Switches S_1 and S_2 have been provided in the emitter and collector circuits. When the two switches are open, the two junctions are unbiased. We thus have depletion or space-charge regions at the two junctions.



- If we close the switch S_1 and keep the switch S_2 open, the emitter junction will be forward biased as shown in Fig.
- The barrier at the emitter junction is reduced. Since the emitter and base regions are just like those in a PN diode, we can expect a large current due to forward biasing. This current consists of majority carriers diffusing across the junction
- The total current flowing across the junction is the sum of the electron diffusion current and the hole diffusion current



- Next, we close switch S2 and keep the switch S1 open in above Fig. The collector junction is reverse biased. Very small current flows across this reverse-biased junction. The reverse leakage current is due to the movement of minority carriers. These carriers are accelerated by the potential barrier. This leakage current is very much temperature dependent.
- The current flows into the collector lead and out of the base lead. There is no emitter current ($I_E = 0$). The small collector current is called the collector leakage current.

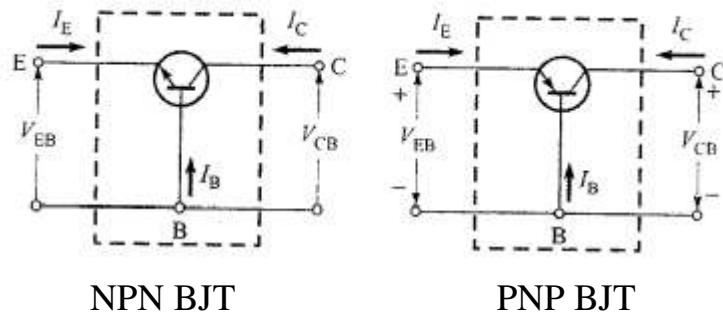


- The emitter junction is forward biased (may be, by a few tenths of a volt). The barrier potential is reduced. As such, majority charge carriers diffuse across the junction.
- The resulting current consists of electrons travelling from the emitter to the base and holes passing from the base to the emitter.
- As will soon be evident, only the electron current is useful in the action of the transistor. Therefore, the electron current is made much larger than the hole current. This is done by doping the base region more lightly than the emitter region.
- In above Fig., we have shown electrons 1, 2, 3 and 4 crossing from the emitter to the base, and hole 7 from the base to the emitter. The total sum

of these charge-carrier movements constitutes the emitter current I_E . Only a portion of this current is due to the movement of electrons 1, 2, 3 and 4. These are the electrons injected by the emitter into the base.

- The ratio of the electron current to the total emitter current is known as emitter injection ratio, or the emitter efficiency. This ratio is denoted by symbol γ (Greek letter gamma). Typically, γ is equal to 0.995.
- Once the electrons are injected by the emitter into the base, they become minority carriers (in the base region).
- The central idea in transistor action is that the base is made very narrow (about 25 μm) and is very lightly doped. Because of this, most of the minority carriers (electrons) travelling from the emitter end of the base region to its collector end do not recombine with holes in this journey.
- Only a few electrons (like 3) may recombine with holes (like 6). The ratio of the number of electrons arriving at collector to the number of emitted electrons is known as the base transportation factor. It is designated by symbol β .
- The collector current is less than the emitter current. There are two reasons for this. First, a part of the emitter current consists of holes that do not contribute to the collector current. Secondly, not all the electrons injected into the base are successful in reaching the collector.

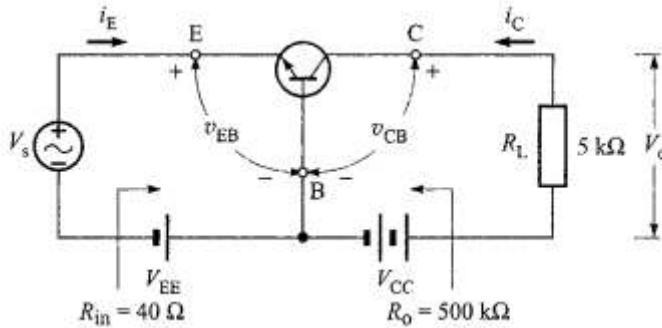
Sign Conventions



TRANSISTOR AMPLIFYING ACTION

- Though a transistor can perform a number of other functions, its main use lies in amplifying electrical signals. Figure just below shows a basic transistor amplifier.

- Here, the transistor (NPN) is connected in common-base configuration. The emitter is the input terminal and the collector is the output terminal. The transistor is biased to operate in the active region.

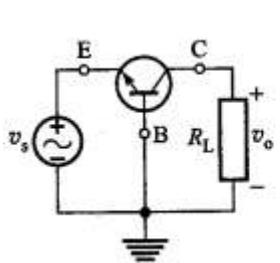


- When the signal V_s is superimposed on the dc voltage V_{EE} , the emitter voltage V_{EB} varies with time. As a result, the emitter current I_E also varies with time.
- Since the collector current is a function of the emitter current, a similar variation occurs in the collector current I_C . This varying current passes through the load resistor R_L and a varying voltage is developed across it. This varying voltage is the output voltage V_o . The output signal V_o is many times greater than the input signal voltage V_s .
- The transistor's amplifying action is basically due to its capability of transferring its signal current from a low resistance circuit to high resistance circuit. Contracting the two terms transfer and resistor results in the name transistor; that is

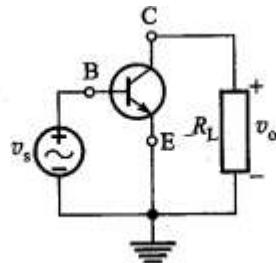
transfer + resistor → transistor

TRANSISTOR CONFIGURATION

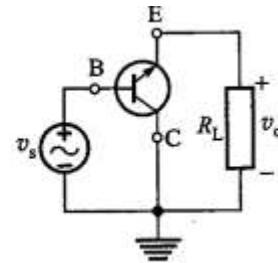
Any of its three terminals can be made common to input and output. (This common terminal is usually grounded or connected to the chassis.) The connection is then described in terms of the common terminal.



Common Base



Common Emitter



Common Collector

- First figure is the base terminal has been made common to both input and output. This connection is called common-base connection.
- The input signal is fed between the emitter and the base. The output signal is developed between the collector and the base.
- By making the emitter or the collector common, we can have what are known as common-emitter (CE) or common-collector (CC) configurations, respectively.
- In all the configurations, the emitter-base junction is always forward-biased and the collector-base junction is always reverse-biased, to keep it in the active region.
- In common-emitter configuration (second fig) the base is the input terminal and the collector is the output terminal. The input signal is connected between the base and the emitter and the load resistor is connected between the collector and the emitter. The output appears across this load resistor.
- Third figure shows common-collector (CC) configuration. Here, the input signal is connected between the base and the collector. The output appears between the emitter and the collector.
- This circuit is popularly known as emitter follower. The voltage gain of this amplifier is poor (it never exceeds unity). But it has got an important characteristic of having very high input resistance and very low output resistance. This property of the emitter follower makes it very useful in certain applications.

Field Effect Transistor: Construction and Characteristic of JFETs. Transfer Characteristic. MOSFET (MOS) (Depletion and Enhancement) Type, Transfer Characteristic.

Introduction of Field Effect Transistor

The concept of the field effect transistor is based around the concept that charge on a nearby object can attract charges within a semiconductor channel. It essentially operates using an electric field effect - hence the name.

The FET transistors are voltage controlled devices, whereas the BJT transistors are current controlled devices. The FET transistors have basically three terminals, such as Drain (D), Source (S) and Gate (G) which are equivalent to the collector, emitter and base terminals in the corresponding BJT transistor.

In BJT transistors the output current is controlled by the input current which is applied to the base, but in the FET transistors the output current is controlled by the input voltage applied to the gate terminal.

In the FET transistors the output current passes between the drain and source terminals and this path is called channel and this channel may be made of either P-type or N-type semiconductor materials. In BJT transistor a small input current operates the large load, but in FET a small input voltage operates the large load at the output.

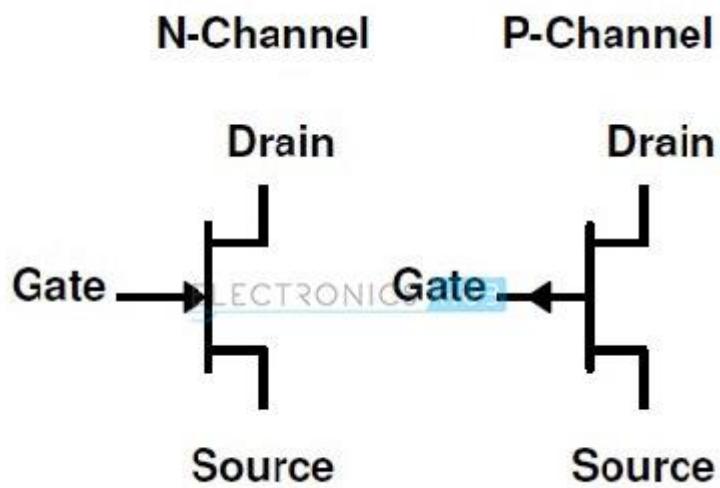
The BJT transistors are ‘bipolar’ devices because they operate with both types of charge carriers, such as electrons and holes but the FET transistors are ‘unipolar’ devices because they operate with the charge carriers of either electrons (for N-channel) or holes (for P-channel).

The FET transistors can be made smaller in size compared to BJT transistor and also they have less power dissipation. Due to this high efficiency the FET transistors are used in many electronic circuit applications by replacing the corresponding BJT transistors. These FET transistors are very useful in the chip designing due to their low power consumption behavior. Like BJT the FET transistors are also available in both P-channel and N-channel.

The FET transistors have high input impedance where as BJT has relatively low. Due to this high impedance values the FET transistors are very sensitive to small input voltages.

Classification of Field Effect Transistor:-

The FET transistors are mainly classified into two types; they are Junction Field Effect Transistor (JFET) and Insulated Gate FET (IG-FET) or Metal Oxide Semiconductor FET (MOSFET).



Construction of JFET:

A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e. electrons or holes.

The current conduction is controlled by means of an electric field between the gate and the conducting channel of the device.

The JFET has high input impedance and low noise level.

Construction Details:

A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides as shown in fig.1.

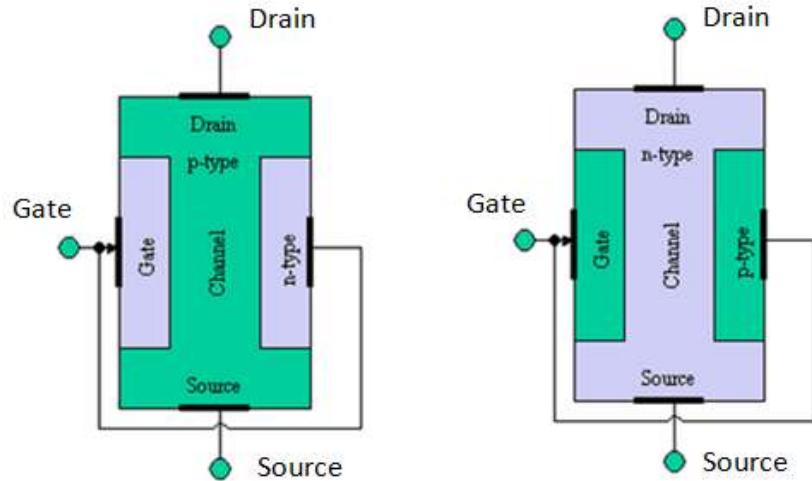


Fig 1.(i)

Fig 1.(ii)

The bar forms the conducting channel for the charge carriers.

If the bar is of p-type, it is called p-channel JFET as shown in fig.1(i) and if the bar is of n-type, it is called n-channel JFET as shown in fig.1(ii).

The two PN junctions forming diodes are connected internally and a common terminal called gate is taken out.

Other terminals are source and drain taken out from the bar as shown in fig.1.

Thus a JFET has three terminals such as , gate (G), source (S) and drain (D).

JFET Polarities

Fig.2 (i) shows the n-channel JFET polarities and fig.2 (ii) shows the p-channel JFET polarities.

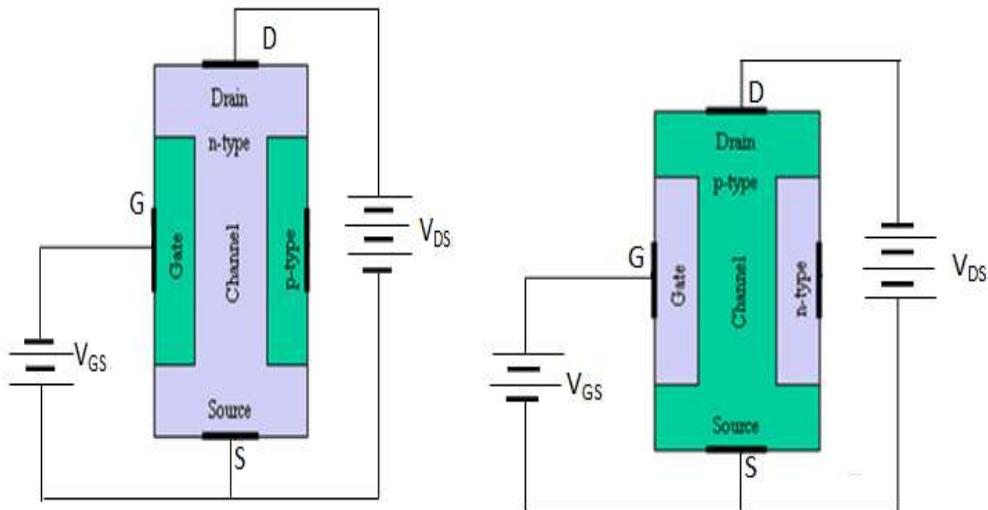


Fig.2 (i)

Fig.2 (ii)

In each case, the voltage between the gate and source is such that the gate is reverse biased.

The source and the drain terminals are interchangeable.

The following points may be noted:

1. The input circuit (i.e. gate to source) of a JFET is reverse biased. This means that the device has high input impedance.
2. The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.
3. In all JFETs, source current I_S is equal to the drain current i.e $I_S = I_D$.

Principle and Working of JFET

Principle of JEFT

Fig.3 shows the circuit of n-channel JFET with normal polarities.

The two pn junctions at the sides form two depletion layers.

The current conduction by charge carriers (i.e. electrons) is through the channel between the two depletion layers and out of the drain.

The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS} .

The greater the reverse voltage V_{GS} , the wider will be the depletion layer and narrower will be the conducting channel.

The narrower channel means greater resistance and hence source to drain current decreases.

Reverse will happen when V_{GS} decreases.

Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS} .

In other word, the magnitude of drain current I_D can be changed by altering V_{GS} .

Working of JEFT

The working of JFET can be explained as follows:

Case-i:

When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero as shown in fig.3(i), the two pn junctions at the sides of the bar establish depletion layers.

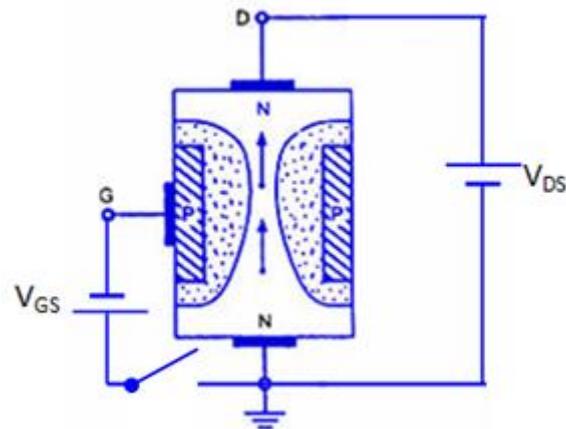


Fig.3 (i)

The electrons will flow from source to drain through a channel between the depletion layers.

The size of the depletion layers determines the width of the channel and hence current conduction through the bar.

Case-ii:

When a reverse voltage V_{GS} is applied between gate and source terminals, as shown in fig.3(ii), the width of depletion layer is increased.

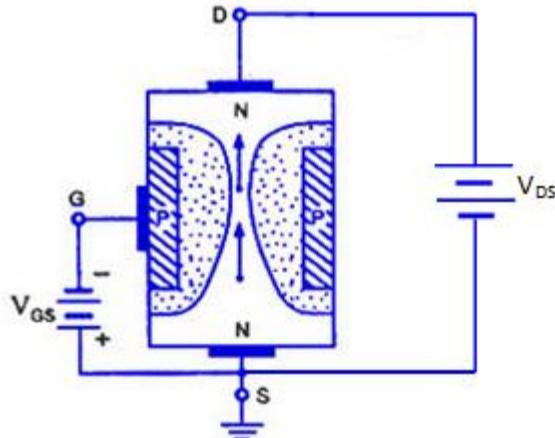


fig.3(ii),

This reduces the width of conducting channel, thereby increasing the resistance of n-type bar.

Consequently, the current from source to drain is decreased.

On the other hand, when the reverse bias on the gate is decreased, the width of the depletion layer also decreases.

This increases the width of the conducting channel and hence source to drain current.

A p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and polarities of V_{GS} and V_{DS} are reversed.

Schematic Symbol of JFET

Fig.4 shows the schematic symbol of JFET.

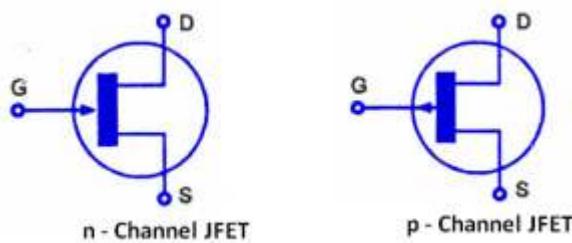


Fig.4

Difference Between JFET and BJT

The JFET differs from an ordinary BJT in the following ways:

1. In a JFET, there is only one type of carrier, i.e. holes in p-type channel and electrons in n-type channel. For this reason it is also called unipolar transistor. However, in

an ordinary BJT, both electrons and holes play role in conduction. Therefore, it is called as bipolar transistor.

2. As the input circuit of a JFET is reverse biased, therefore, it has a high input impedance. However, the input circuit of a BJT is forward biased and hence has low input impedance.
3. The primary functional difference between the JFET and BJT is that no current enters the gate of JFET. However, in typical BJT base current might be a few μA .
4. A BJT uses the current into its base to control a large current between collector and emitter. Whereas a JFET uses voltage on the gate terminal to control the current between drain and source.
5. In JFET, there is no junction. Therefore, noise level in JFET is very small.

Advantages of JFET

A JFET is a voltage controlled, constant current device in which variation in input voltage control the output current. Some of the advantages of JFET are:

1. It has a very high input impedance. This permits high degree of isolation between the input and output circuits.
2. The operation of a JFET depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes and those of transistors are not present in a JFET.
3. A JFET has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.
4. A JFET has a very high-power gain. This eliminates the necessity of using driver stages.
5. A JFET has a smaller size, longer life and high efficiency

Output Characteristics and transfer characteristics of JFET

Output Characteristics of JFET

The curve between drain current, I_D and drain-source voltage, V_{DS} of a JFET at constant gate-source voltage, V_{GS} is known as output characteristics of JFET.

1. Drain Characteristic With Shorted-Gate

Fig.1 (i) shows the circuit diagram for determining the drain characteristic with shorted-gate for an n-channel JFET. Fig.1(ii) shows the drain characteristic with shorted-gate.

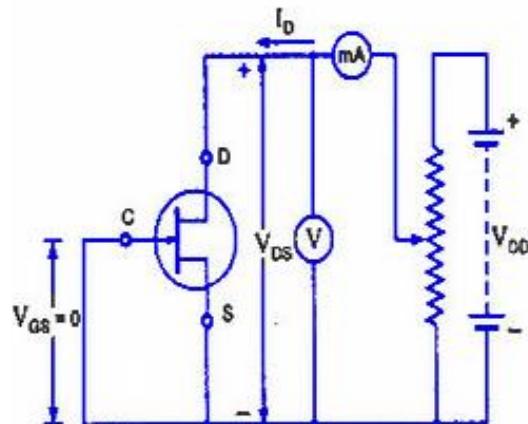


Fig.1(i)

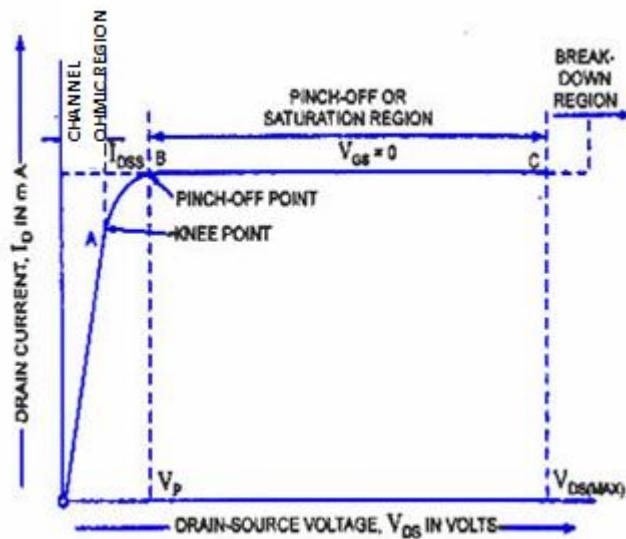


Fig.1 (ii)

when drain-source voltage V_{DS} is zero, there is no attracting potential at the drain, so no current flows inspite of the fact that the channel is fully open. So, drain current $I_D = 0$.

For small applied voltage V_{DS} , the n-type bar acts as a simple semiconductor resistor, and the drain current increases linearly with the increase in V_{DS} , upto the knee point.

This region, to the left of the knee point of the curve is called the channel ohmic *region*, as in this region the JFET behaves like an ordinary resistor.

With the increase in drain current I_D , the ohmic voltage drop between the source and channel region reverse-biases the gate junction.

The reverse-biasing of the gate junction is not uniform throughout. The reverse bias is more at the drain end than at the source end of the channel.

So with the increase in V_{DS} , the conducting portion of the channel begins to constrict more at the drain end. Eventually a voltage V_{DS} is reached at which the channel is pinched off.

The drain current I_D no longer increases with the increase in V_{DS} . It approaches a constant saturation value.

The value of voltage V_{DS} at which the channel is pinched off i.e. all the free charges from the channel get removed, and the drain current I_D attains a constant value, is called the *pinch-off voltage* V_p .

From point A (knee point) to the point B (pinch-off point) the drain current I_D increases with the increase In voltage V_{DS} following a reverse square law.

The region of the characteristic in which drain current I_D remains fairly constant is called the *pinch-off region*. It is also sometimes called the *saturation region* or *amplifier region*.

In this region the JFET operates as a *constant current device* since drain current (or output current) remains almost constant. It is the normal operating region of the JFET where it is used as an amplifier.

The drain current in the pinch-off region with $V_{GS} = 0$ is referred to the *drain-source saturation current*, I_{DSS}).

Drain current in the pinch-of region is given by Shockley's equation:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$$

Where I_D = Drain current at given V_{GS}

I_{DSS} = Shorted – gate drain current

V_{GS} = gate-source Voltage

$V_{GS(off)}$ = gate-source cut off voltage

If drain-source voltage, V_{DS} is continuously increased, a stage comes when the gate-channel junction breaks down. At this point current increases very rapidly. and the JFET may be destroyed. This happens because the charge carriers making up the saturation current at the gate channel junction accelerate to a high velocity and produce an *avalanche effect*.

2. Drain Characteristics With External Bias

The circuit diagram for determining the drain characteristics with different values of external bias is shown in Fig.2(i). and a family of drain characteristics for different values of gate-source voltage V_{GS} is shown in Fig.2(ii).

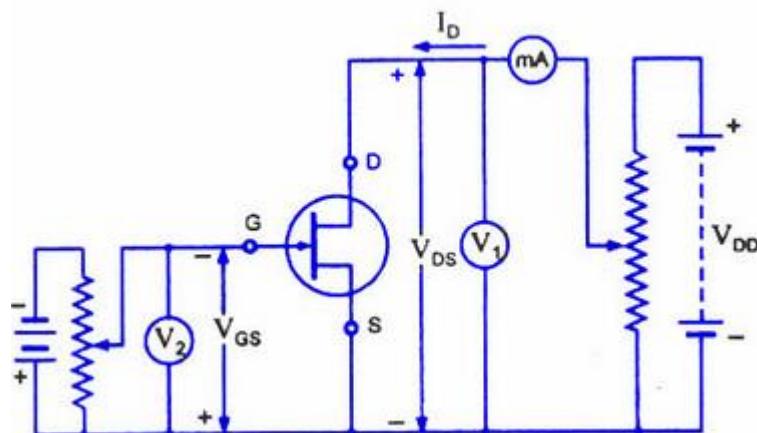


Fig.2 (i)

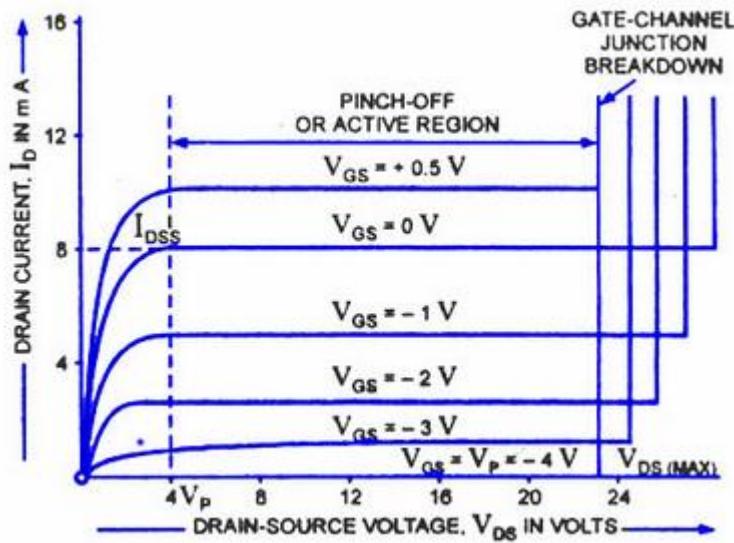


Fig.2 (ii)

It is observed that as the negative gate bias voltage V_{GS} is increased;

(1) The maximum saturation drain current becomes smaller because the conducting channel now becomes narrower.

(2) Pinch-off voltage is reached at a lower value of drain current I_D than when $V_{GS} = 0$.

When an external bias of, say -1 V is applied between the gate and the source, the gate-channel junctions are reverse-biased even when drain current, I_D is zero. Hence the depletion regions are already penetrating the channel to a certain extent when drain-source voltage, V_{DS} is zero. Due to this reason, a smaller voltage drop along the channel (i.e. smaller than that for $V_{GS} = 0$) will increase the depletion regions to the point where they pinch-off the current. Consequently, the pinch-off voltage V_P is reached at a lower drain current, I_D .

(3) Value of drain-source voltage V_{DS} for the avalanche breakdown of the gate junction is reduced.

It is simply due to the fact that gate-source voltage, V_{GS} keeps adding to the reverse bias at the junction produced by current flow.

Transfer Characteristic of JFET

The transfer characteristic for a JFET can be determined experimentally, keeping drain-source voltage, V_{DS} constant and determining drain current, I_D for various values of gate-source voltage, V_{GS} .

The circuit diagram is shown in fig.3 (i).

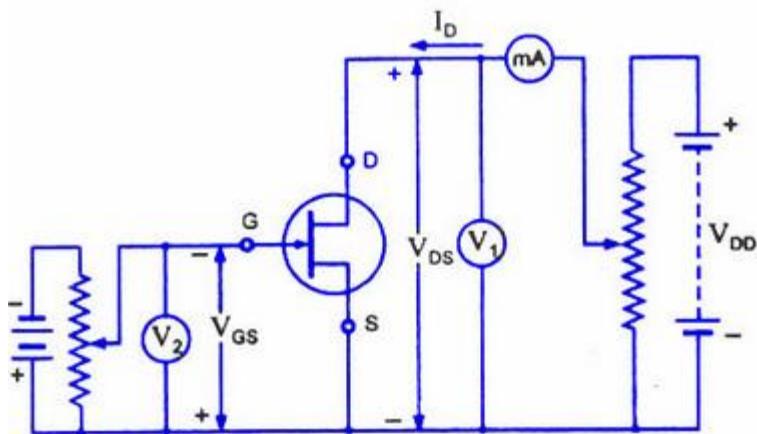


fig.3 (i)

The curve is plotted between gate-source voltage, V_{GS} and drain current, I_D , as shown in fig. 3 (ii).

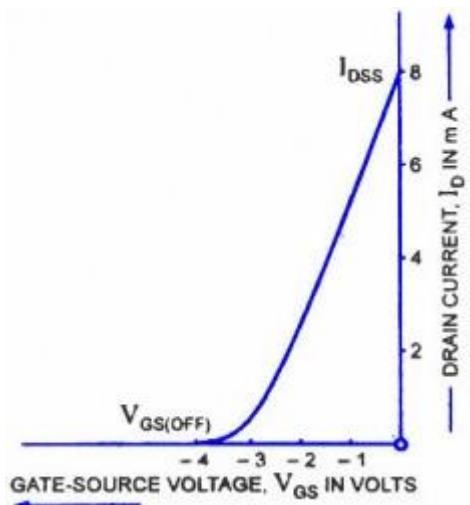


Fig.3 (ii)

It can be observed that:

- (i) Drain current decreases with the increase in negative gate-source bias
- (ii) Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$
- (iii) Drain current, $I_D = 0$ when $V_{GS} = V_D$

The transfer characteristic can also be derived from the drain characteristic by noting values of drain current, I_D corresponding to various values of gate-source voltage, V_{GS} for a constant drain-source voltage and plotting them.

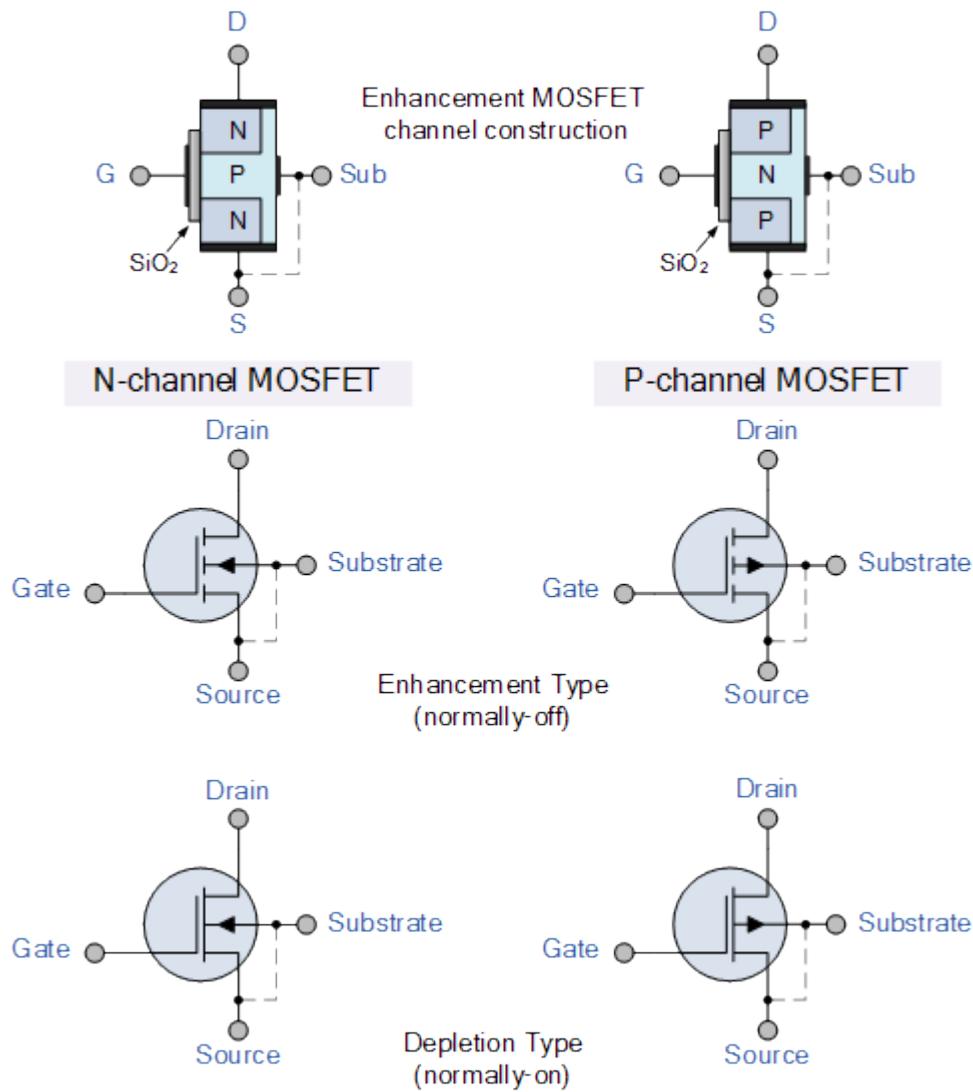
It may be noted that a P-channel JFET operates in the same way and have the similar characteristics as an N-channel JFET except that channel carriers are holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

- As well as the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel and is therefore called an **Insulated Gate Field Effect Transistor**.
- The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.
- The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.
- This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high way up in the Mega-ohms ($M\Omega$) region thereby making it almost infinite.
- As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, “**NO current flows into the gate**” and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the **MOSFET** becoming easily damaged unless carefully handled or protected.
- Like the previous JFET tutorial, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:
 - Depletion Type – the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.

- Enhancement Type – the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “Normally Open” switch.

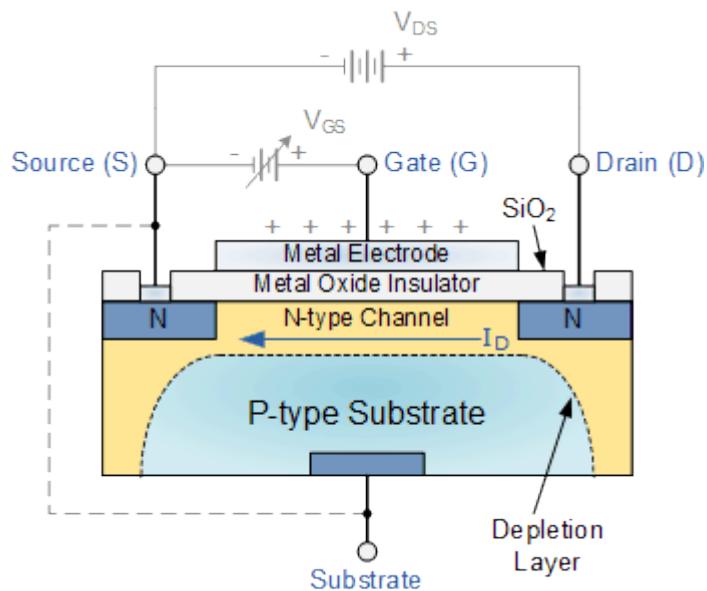
The symbols and basic construction for both configurations of MOSFETs are shown below.



- The four MOSFET symbols above show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semiconductive channel through a diode junction to the body or metal tab of the MOSFET.
- Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal. When this is the case, as in enhancement types it is omitted from the symbol for clarification.

- The line in the MOSFET symbol between the drain (D) and source (S) connections represents the transistors semiconductive channel. If this channel line is a solid unbroken line then it represents a “Depletion” (normally-ON) type MOSFET as drain current can flow with zero gate biasing potential.
- If the channel line is shown as a dotted or broken line, then it represents an “Enhancement” (normally-OFF) type MOSFET as zero drain current flows with zero gate potential. The direction of the arrow pointing to this channel line indicates whether the conductive channel is a P-type or an N-type semiconductor device.

Basic MOSFET Structure and Symbol



- The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes.
- We saw in the previous tutorial, that the gate of a junction field effect transistor, JFET must be biased in such a way as to reverse-bias the pn-junction. With a insulated gate

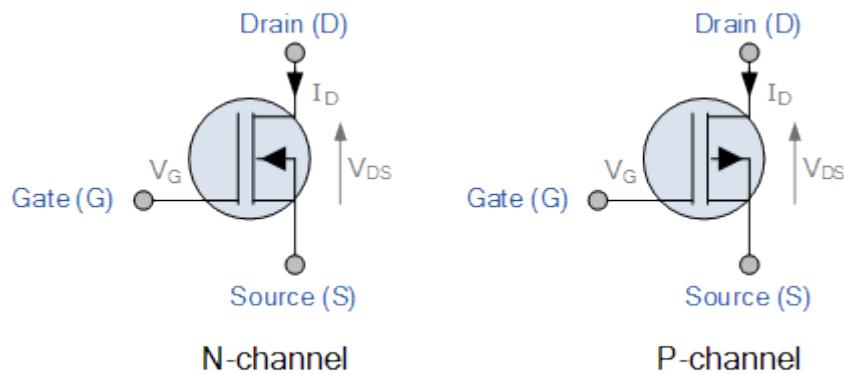
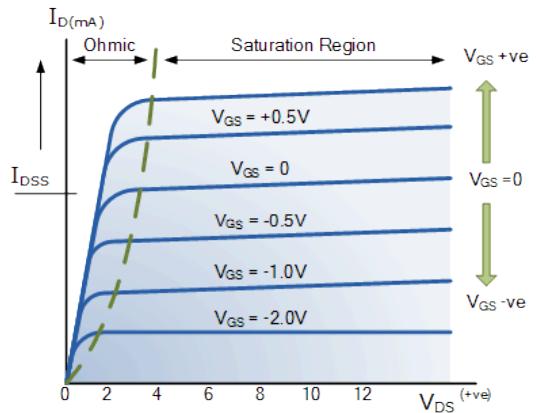
MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve).

- This makes the MOSFET device especially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the **Enhancement** type and the **Depletion** type.

Depletion-mode MOSFET

- The **Depletion-mode MOSFET**, which is less common than the enhancement mode types is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when $V_{GS} = 0$ making it a “normally-closed” device. The circuit symbol shown above for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.
- For the n-channel depletion MOS transistor, a negative gate-source voltage, $-V_{GS}$ will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, $+V_{GS}$ will deplete the channel of its free holes turning it “OFF”.
- In other words, for an n-channel depletion mode MOSFET: $+V_{GS}$ means more electrons and more current. While a $-V_{GS}$ means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

Depletion-mode N-Channel MOSFET and circuit Symbols



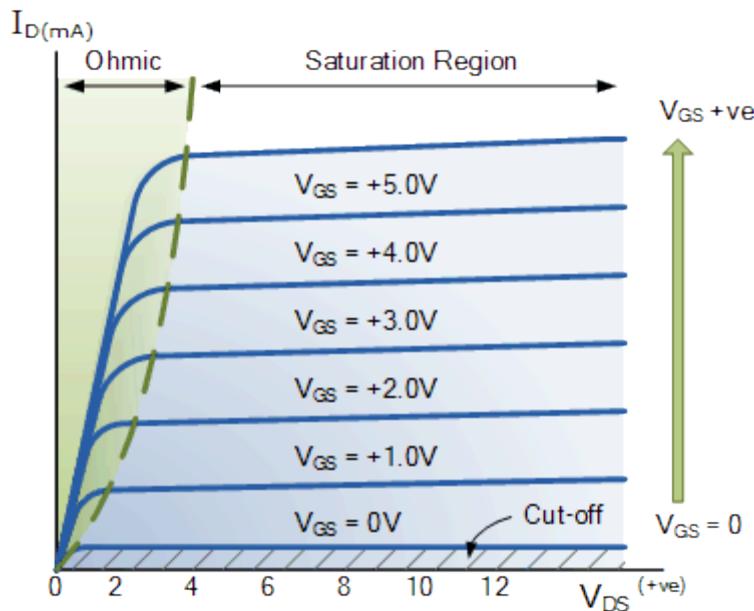
- The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts where the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain and Source with zero Gate bias.

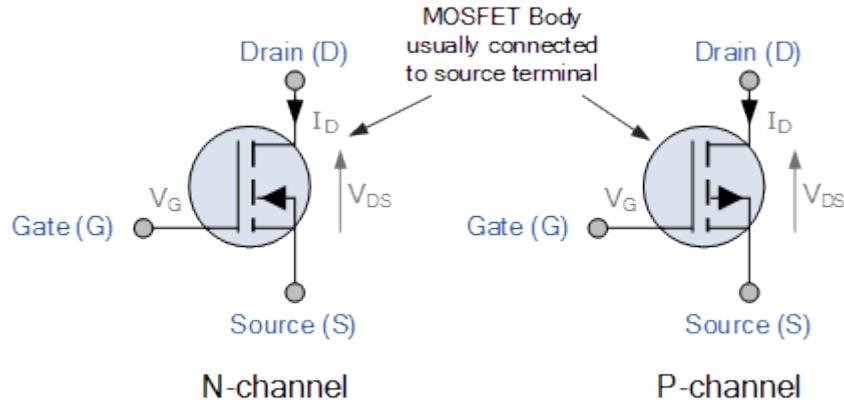
ENHANCEMENT-MODE MOSFET

- The more common **Enhancement-mode MOSFET** or E-MOSFET, is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally “OFF” (non-conducting) when the gate bias voltage, V_{GS} is equal to zero. The circuit symbol shown above for an enhancement MOS transistor uses a broken channel line to signify a normally open non-conducting channel.

- For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage (V_{GS}) is applied to the gate terminal greater than the threshold voltage (V_{TH}) level in which conductance takes place making it a transconductance device.
- The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.
- Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, I_D through the channel. In other words, for an n-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor “ON”, while a zero or $-V_{GS}$ turns the transistor “OFF”. Thus the enhancement-mode MOSFET is equivalent to a “normally-open” switch.
- The reverse is true for the p-channel enhancement MOS transistor. When $V_{GS} = 0$ the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor “OFF”, while $-V_{GS}$ turns the transistor “ON”.

ENHANCEMENT-MODE N-CHANNEL MOSFET AND CIRCUIT SYMBOLS





- Enhancement-mode MOSFETs make excellent electronics switches due to their low “ON” resistance and extremely high “OFF” resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for *Complementary MOS* meaning that the logic device has both PMOS and NMOS within its design.

UNIT 3

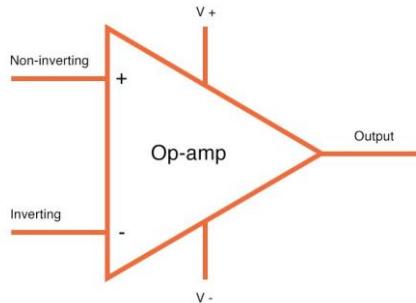
Introduction

- An **Operational Amplifier** is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals.
- These feedback components determine the resulting function or “operation” of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of “Operational Amplifier”.

Op-Amp Basic:

- An *Operational Amplifier* is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the Inverting Input, marked with a

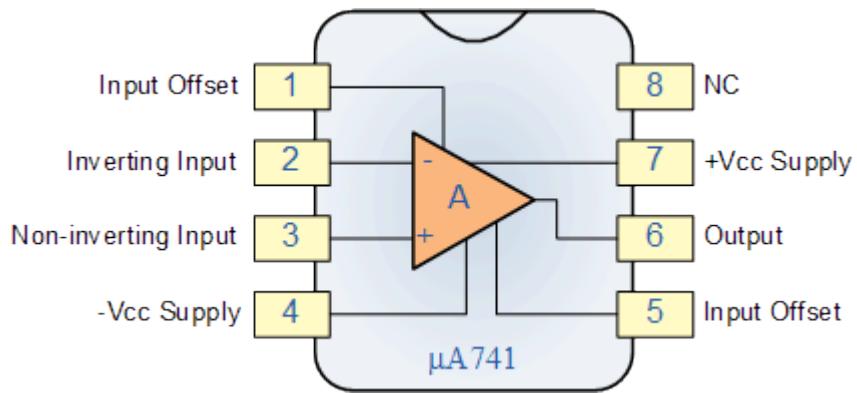
negative or “minus” sign, (-). The other input is called the Non-inverting Input, marked with a positive or “plus” sign (+).



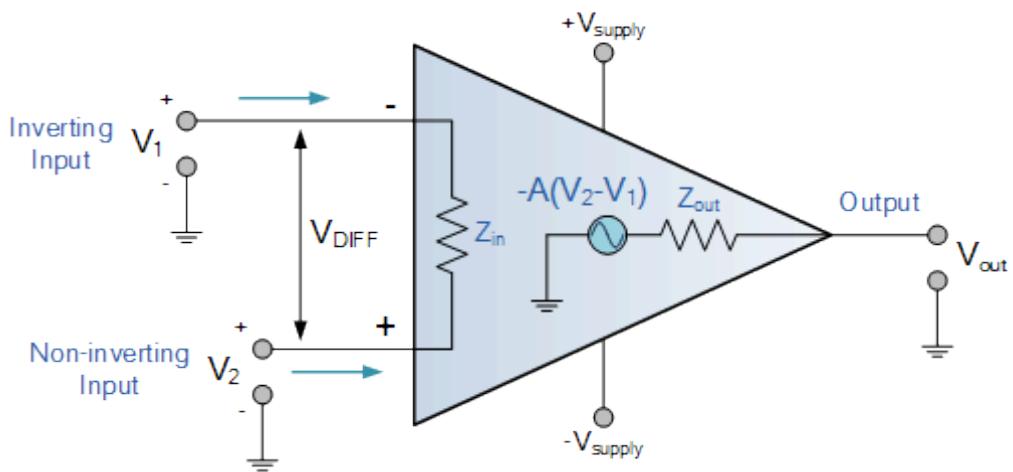
- A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.
 - Voltage – Voltage “in” and Voltage “out”
 - Current – Current “in” and Current “out”
 - Transconductance – Voltage “in” and Current “out”
 - Transresistance – Current “in” and Voltage “out”

Since most of the circuits dealing with operational amplifiers are voltage amplifiers, we will limit the tutorials in this section to voltage amplifiers only, (V_{in} and V_{out}).

- The output voltage signal from an Operational Amplifier is the difference between the signals being applied to its two individual inputs. In other words, an op-amps output signal is the difference between the two input signals as the input stage of an Operational Amplifier is in fact a differential amplifier.
- **Pin diagram of OPAMP(741).**



Equivalent Circuit of an Ideal Operational Amplifier



Ideal and Practical Characteristic of OPAMP

1. Open Loop Gain, (A_{VO}): Infinite and typical real values range from about 20,000 to 200,000.
2. Input impedance, (Z_{IN}): Infinite and typical real values range of 1×10^6 ohms.
3. Output impedance, (Z_{OUT}): Zero and Real op-amps have output impedances in the 75Ω range.

4. Bandwidth, (BW) : Infinite and With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity. 1MHZ
5. Offset Voltage, (V_{IO}) : Zero and mv
6. Slew Rate : Infinite and real value is 0.5 V/uS.
7. Common Mode rejection Ratio (CMRR): Infinite and real value is 90dB.

Concept of Virtual Short and Virtual Ground

- Assume ideal OP-Amp. The input impedance (R_i) of an OP-AMP is ideally Infinite. Hence current “I” flowing from one input terminal to other will be zero . Thus Voltage drop across $R_i=0$ Both the i/p terminals will be at the same potential. → i.e. virtually shorted

$$\text{i.e. } V_0 = A_v \times V_d$$

$$V_0 = \text{o/p Voltage}$$

$$V_d = \text{Differential Input voltage}$$

$$A_v = \text{open loop gain}$$

$$\therefore V_d = V_0 / A_v$$

But $A_v=\infty$ for an ideal op-amp and $A_v=2\times 10^5$ for IC 741

- For ideal, $V_d = 0$, Thus potential difference between input terminals = 0
- When we short circuit two point , they will have same potential. Due to this reason, the two OP-AMP terminals which are almost equipotential are to be virtually (not actually) short circuited.

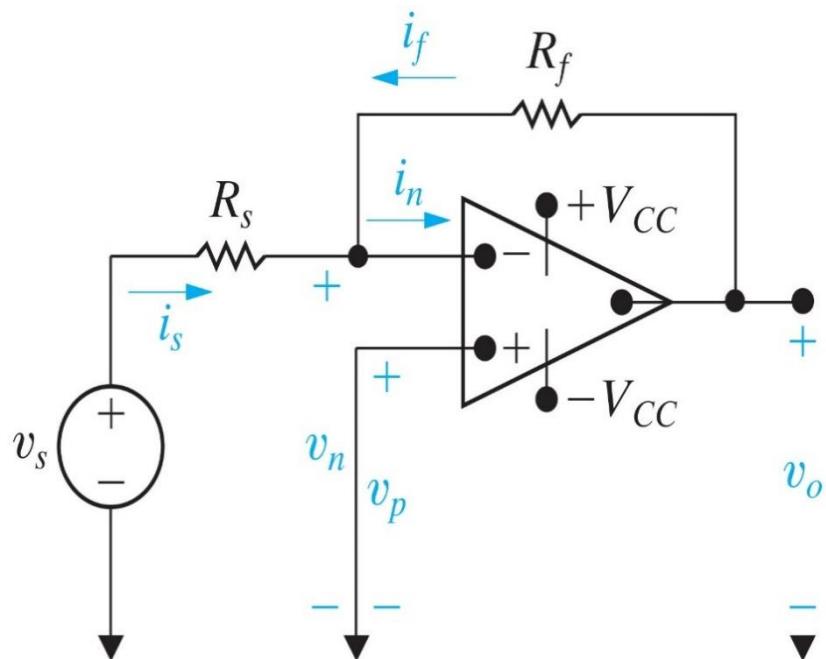
Virtual Ground :

- If (+) terminal is connected to ground, they due to “virtual short”, (-) terminal will also be grid potential. Hence it is “virtual ground”

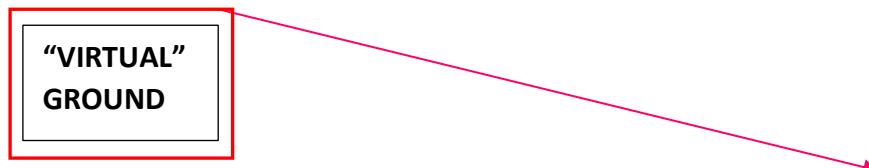
- Similarly, if (-) terminal is connected to ground then (+) terminal will be at “virtual ground” potential. The concept of virtual ground has been used extensively in analysing various closed loop configuration, especially we use this concept in the inverting amplifier analysis.

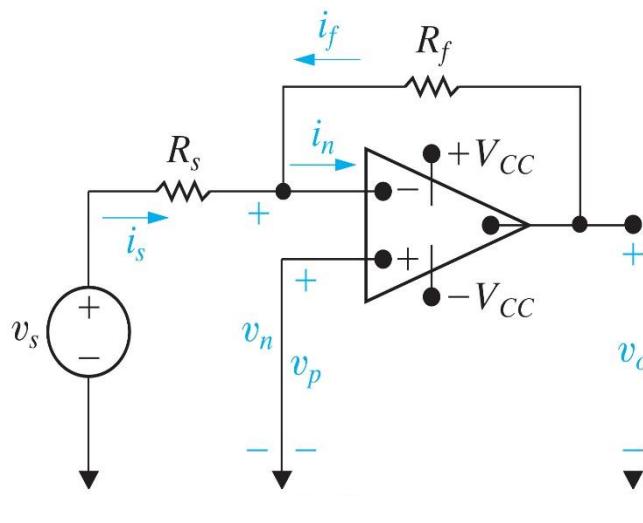
Practical Op-Amp Circuits

1. Inverting Amplifier:



Analysis Using the Ideal OP AMP



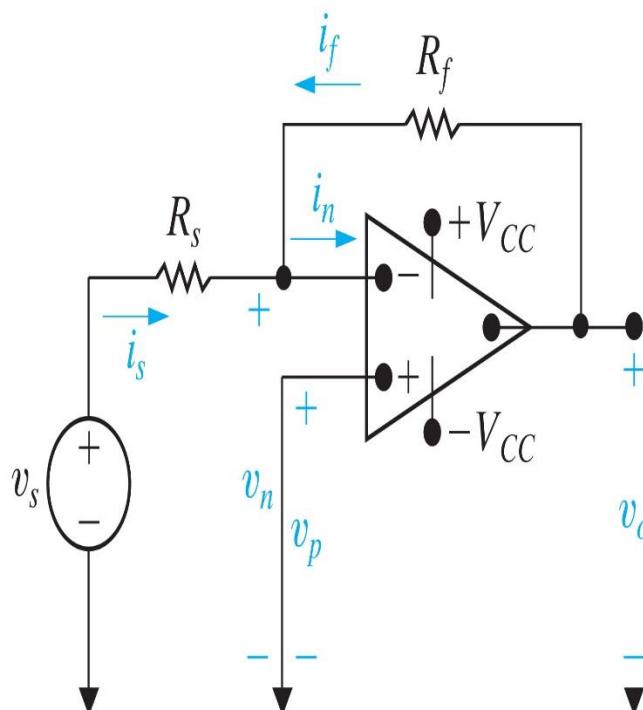


$$i_s + i_f = i_n$$

$$v_n = v_p = 0$$

$$i_s = \frac{v_s}{R_s}$$

$$i_f = \frac{v_o}{R_f}$$



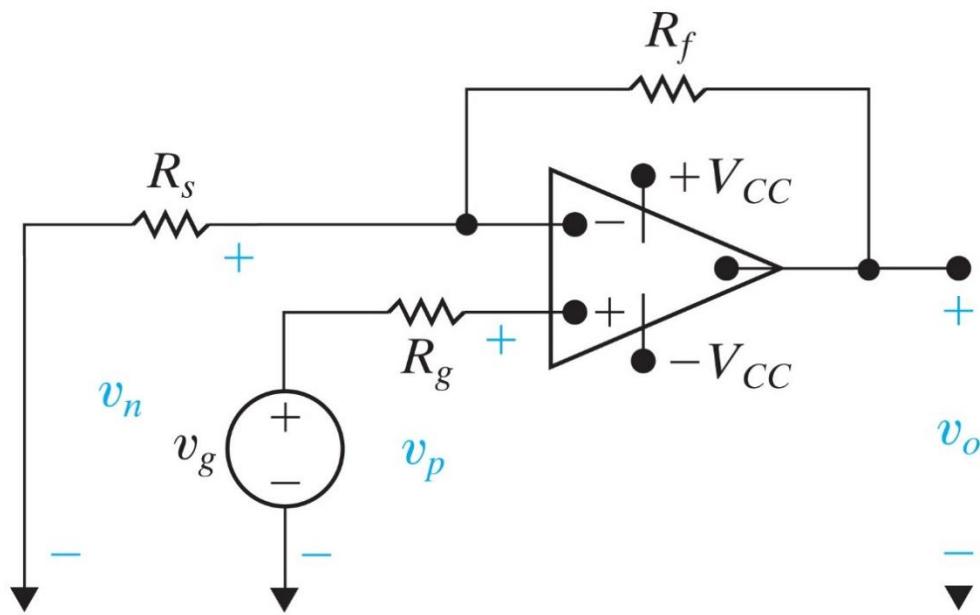
$$i_n = 0$$

$$i_f = -i_s$$

$$\frac{v_o}{R_f} = -\frac{v_s}{R_s}$$

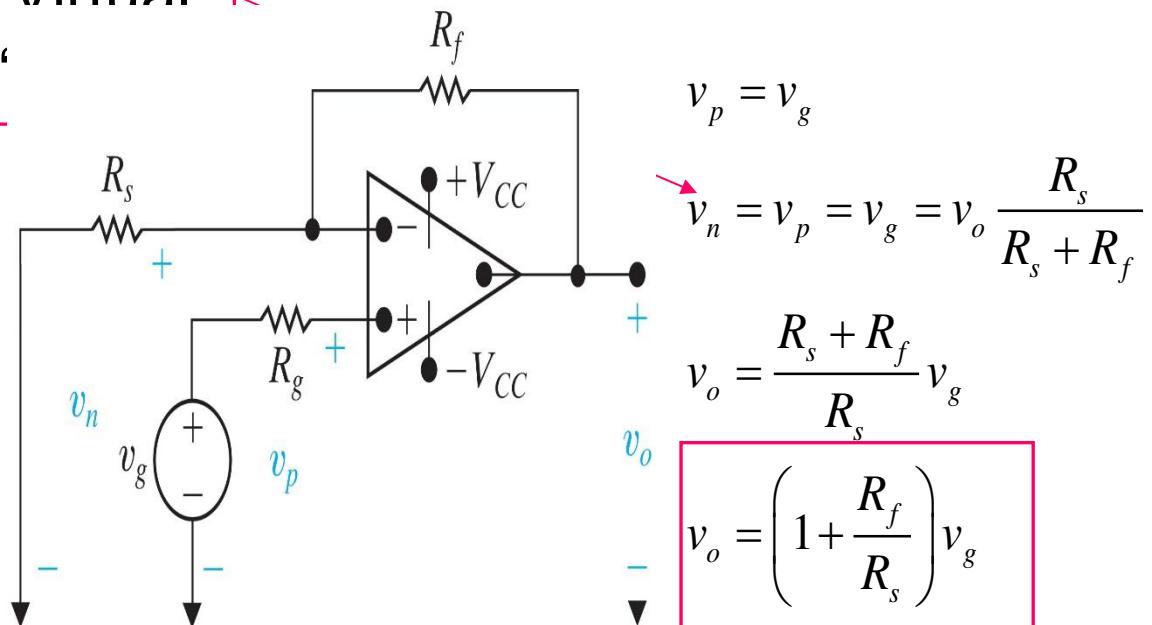
$$v_o = -\frac{R_f}{R_s} v_s$$

2. Non Inverting amplifier:



Analysis Using the Ideal OP AMP

“Virtual



3. Voltage follower:

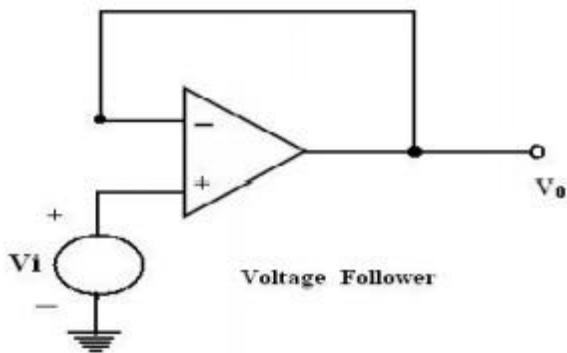
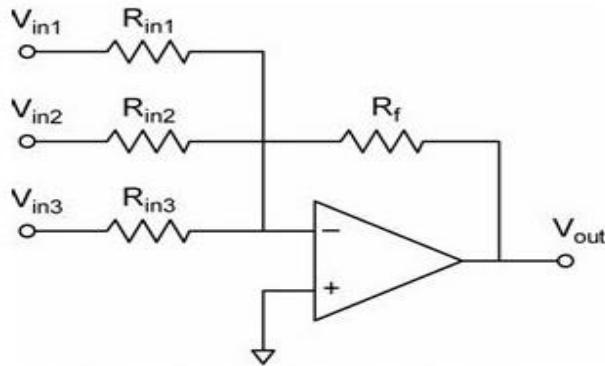


Fig 2.6 Voltage follower

- If $R_1 = \infty$ and $R_f = 0$ in the non inverting amplifier configuration. The amplifier act as a unity-gain amplifier or voltage follower.
- The circuit consists of an op -amp and a wire connecting the output voltage to the input, i.e. the output voltage V_o is equal to the input voltage, both in magnitude and phase. $V_o = V_i$. Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of $M\Omega$ and very low output impedance.
- Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

4. Summing Amplifier

- Many applications in electronic circuits require two or more analog signals to be added or combined into a single output. The summing amplifier does the exact same thing.
- For this reason, summing amplifier is also called as Voltage adder since its output is the addition of voltages present at its input terminal.
- The summing amplifier uses an inverting amplifier configuration, i.e. the input is applied to the inverting input terminal of the op-amp, while the non-inverting input terminal is connected to ground. Due to this configuration, the output of voltage adder is out of phase with respect to the input by 180°



The Summing Amplifier Circuit Diagram

For an inverting amplifier, the output voltage is given as,

$$V_{\text{OUT}} = - (R_f/R_{\text{IN}}) V_{\text{IN}}$$

So for the summing amplifier shown above, the output equation would be,

$$V_{\text{OUT}} = - \{(R_f/R_{\text{IN}1}) V_{\text{IN}1} + (R_f/R_{\text{IN}2}) V_{\text{IN}2} + (R_f/R_{\text{IN}3}) V_{\text{IN}3}\}$$

If all the input resistances are chosen to be of equal magnitude (R_{IN}), then the output equation of the summing amplifier can be rewritten as,

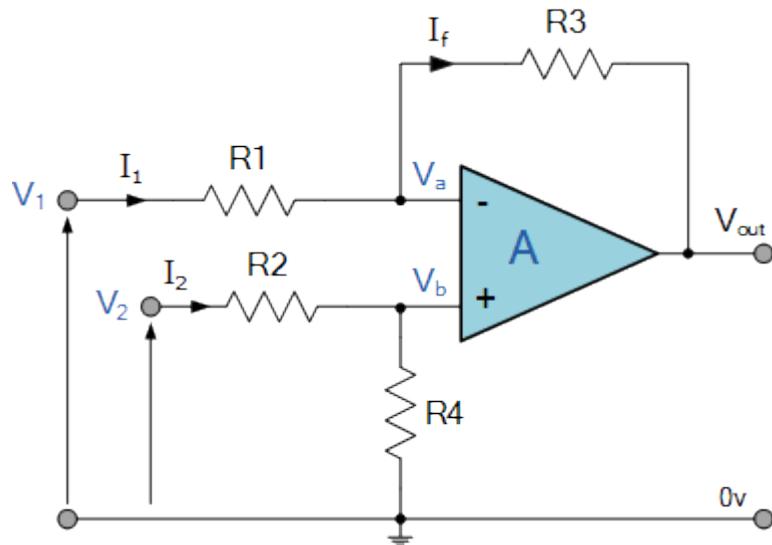
$$V_{\text{OUT}} = - \{(R_f/R_{\text{IN}}) \{V_{\text{IN}1} + V_{\text{IN}2} + V_{\text{IN}3}\}\}$$

In general, a summing amplifier output equation is given as,

$$V_{\text{OUT}} = - \{(R_f/R_{\text{IN}}) \{V_1 + V_2 + V_3 + \dots + V_N\}\}$$

Sometimes, it is necessary to just add the input voltages without amplifying them. In such situations, the value of input resistance $R_{\text{IN}1}$, $R_{\text{IN}2}$, $R_{\text{IN}3}$, etc. must be chosen equal to that of the feedback resistor R_f . Then, the gain of the amplifier will be unity. Hence the output voltage will be an addition of the input voltages.

5. Differential Amplifier (Subtractor)



- By connecting each input in turn to 0v ground we can use superposition to solve for the output voltage V_{out} . Then the transfer function for a **Differential Amplifier** circuit is given as:

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - (V_{out})}{R_3}$$

Summing point $V_a = V_b$

$$\text{and } V_b = V_2 \left(\frac{R_4}{R_2 + R_4} \right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(a)} = -V_1 \left(\frac{R_3}{R_1} \right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(b)} = V_2 \left(\frac{R_4}{R_2 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1 \left(\frac{R_3}{R_1} \right) + V_2 \left(\frac{R_4}{R_2 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

- When resistors, $R_1 = R_2$ and $R_3 = R_4$ the above transfer function for the differential amplifier can be simplified to the following expression:

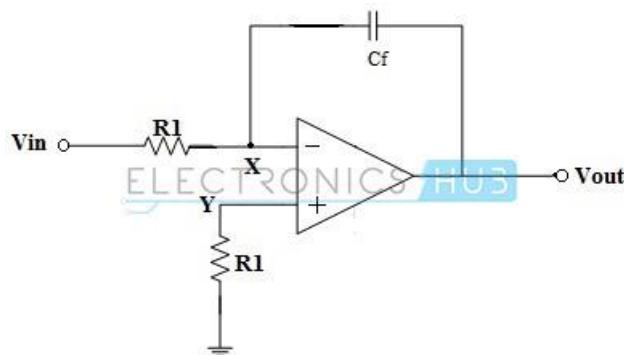
Differential Amplifier Equation

$$V_{\text{OUT}} = \frac{R_3}{R_1} (V_2 - V_1)$$

- If all the resistors are all of the same ohmic value, that is: $R_1 = R_2 = R_3 = R_4$ then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be $V_{\text{out}} = V_2 - V_1$.

6. Op-amp Integrator Circuit

- Operational amplifier can be configured to perform calculus operations such as differentiation and integration. In an integrating circuit, the output is the integration of the input voltage with respect to time. A passive integrator is a circuit which does not use any active devices like op-amps or transistors.
- An integrator circuit which consists of active devices is called an Active integrator. An active integrator provides a much lower output resistance and higher output voltage than is possible with a simple RC circuit.
- Op-amp differentiating and integrating circuits are inverting amplifiers, with appropriately placed capacitors. Integrator circuits are usually designed to produce a triangular wave output from a square wave input.
- Integrating circuits have frequency limitations while operating on sine wave input signals.



An Ideal Op-amp Integrator

- From the circuit, it is seen that node Y is grounded through a compensating resistor R1. Node X will also be at ground potential, due to the virtual ground.

$$V_X = V_Y = 0$$

- Since the input current to an op-amp is ideally zero, the current flowing through the input resistor, due to V_{in} , also flows through the capacitor C_f .
- From the input side, the current I is given as,

$$I = (V_{in} - V_X) / R_1 = V_{in} / R_1$$

- From the output side, the current I is given as,

$$I = C_f [d(V_X - V_{out})/dt] = -C_f [d(V_{out})/dt]$$

- Equating the above two equations of I, we get,

$$[V_{in} / R_1] = -C_f [d(V_{out})/dt]$$

- Integrating both the sides of the above equation,

$$\int_0^t \frac{V_{in}}{R_1} dt = -C_f \int_0^t d \frac{V_{out}}{dt} dt$$

$$\int_0^t \frac{V_{in}}{R_1} dt = -C_f V_{out}$$

$$\text{Therefore, } V_{out} = -\frac{1}{R_1 C_f} \int_0^t V_{in} dt$$

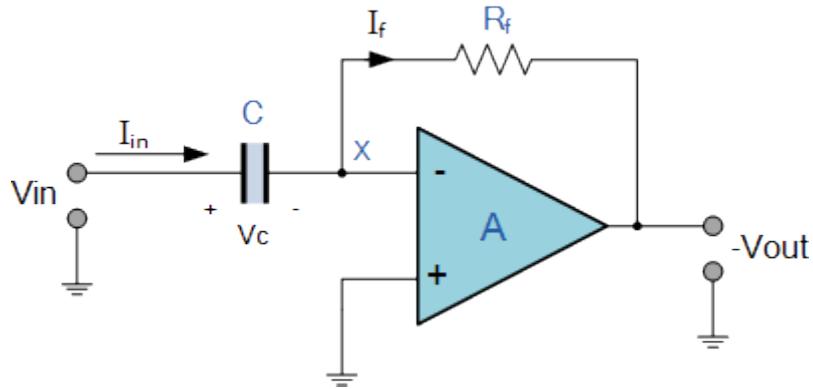
- The negative sign indicates that there is a phase shift of 180° between input and output, because the input is provided to the inverting input terminal of the op-amp.

7. OPAMP Differentiator Circuit

A differentiator circuit is one in which the voltage output is directly proportional to the rate of change of the input voltage with respect to time.

- This means that a fast change to the input voltage signal, the greater the output voltage change in response.

- As a differentiator circuit has an output that is proportional to the input change, some of the standard waveforms such as sine waves, square waves and triangular waves give very different waveforms at the output of the differentiator circuit.



$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

- Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C \frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current, i

$$I_{IN} = C \frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C \frac{dV_{IN}}{dt}$$

- from which we have an ideal voltage output for the op-amp differentiator is given as:

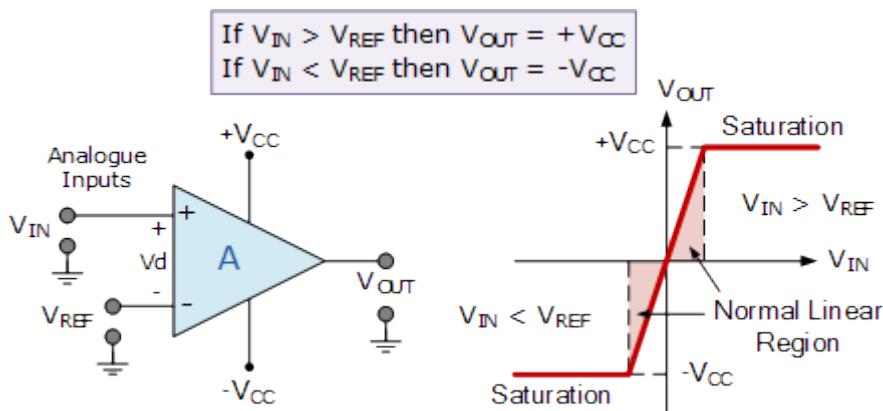
$$V_{OUT} = -R_F C \frac{dV_{IN}}{dt}$$

- Therefore, the output voltage V_{OUT} is a constant $-R_F C$ times the derivative of the input voltage V_{IN} with respect to time. The minus sign (-) indicates a 180° phase shift

because the input signal is connected to the inverting input terminal of the operational amplifier.

Op-Amp Comparator:

- The **Op-amp comparator** compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison.



- lets first assume that V_{IN} is less than the DC voltage level at V_{REF} , ($V_{IN} < V_{REF}$). As the non-inverting (positive) input of the comparator is less than the inverting (negative) input, the output will be LOW and at the negative supply voltage, $-V_{CC}$ resulting in a negative saturation of the output.
- input voltage, V_{IN} so that its value is greater than the reference voltage V_{REF} on the inverting input, the output voltage rapidly switches HIGH towards the positive supply voltage, $+V_{CC}$ resulting in a positive saturation of the output.
- we can see that the op-amp voltage comparator is a device whose output is dependant on the value of the input voltage, V_{IN} with respect to some DC voltage level as the output is HIGH when the voltage on the non-inverting input is greater than the voltage on the inverting input, and LOW when the non-inverting input is less than the inverting input voltage.

- op-amps high open-loop gain the magnitude of its output voltage could be infinite in both directions, ($\pm\infty$). However practically, and for obvious reasons it is limited by the op-amps supply rails giving $V_{OUT} = +V_{CC}$ or $V_{OUT} = -V_{CC}$.

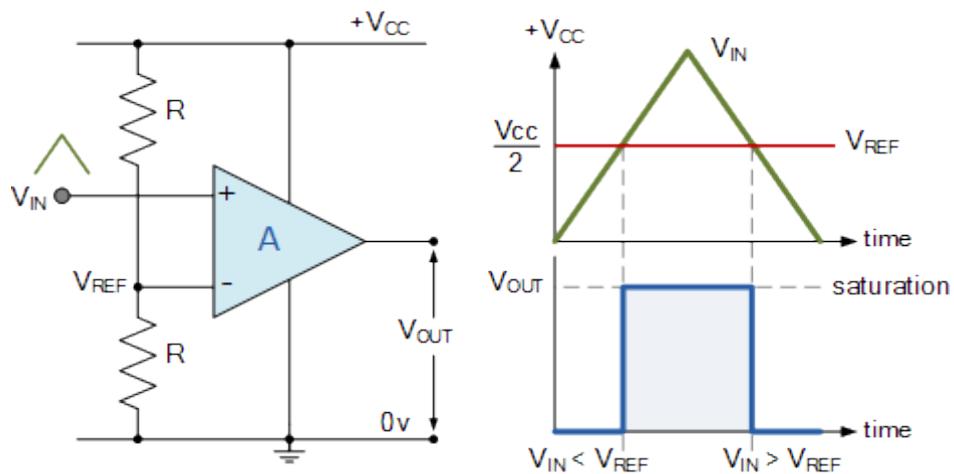
Positive and Negative Voltage Comparators

- A basic op-amp comparator circuit can be used to detect either a positive or a negative going input voltage depending upon which input of the operational amplifier we connect the fixed reference voltage source and the input voltage too.

Positive Voltage Comparator

- The basic configuration for the positive voltage comparator, also known as a non-inverting comparator circuit detects when the input signal, V_{IN} is ABOVE or more positive than the reference voltage, V_{REF} producing an output at V_{OUT} which is HIGH as shown.

Non-inverting Comparator Circuit



- In this non-inverting configuration, the reference voltage is connected to the inverting input of the operational amplifier with the input signal connected to

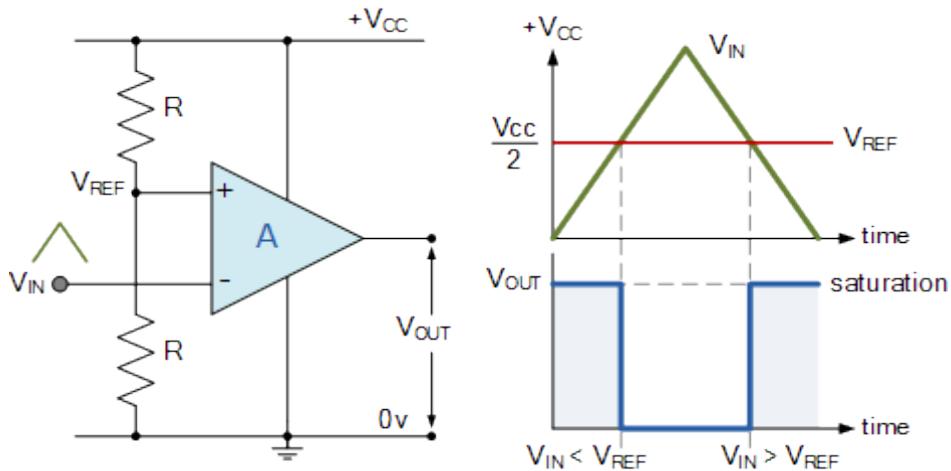
the non-inverting input. To keep things simple, we have assumed that the two resistors forming the potential divider network are equal and: $R_1 = R_2 = R$. This will produce a fixed reference voltage which is one half that of the supply voltage, that is $V_{cc}/2$, while the input voltage is variable from zero to the supply voltage.

- When V_{IN} is greater than V_{REF} , the op-amp comparators output will saturate towards the positive supply rail, V_{cc} . When V_{IN} is less than V_{REF} the op-amp comparators output will change state and saturate at the negative supply rail, $0v$ as shown.

• Negative Voltage Comparator

- The basic configuration for the negative voltage comparator, also known as an inverting comparator circuit detects when the input signal, V_{IN} is BELOW or more negative than the reference voltage, V_{REF} producing an output at V_{OUT} which is HIGH as shown.

Inverting Comparator Circuit



- In the inverting configuration, which is the opposite of the positive configuration above, the reference voltage is connected to the non-inverting input of the operational amplifier while the input signal is connected to the inverting input. Then when V_{IN} is less than V_{REF} the op-amp comparators output will saturate towards the positive supply rail, V_{cc} .

- Likewise the reverse is true, when V_{IN} is greater than V_{REF} , the op-amp comparators output will change state and saturate towards the negative supply rail, 0v.
- Then depending upon which op-amp inputs we use for the signal and the reference voltage, we can produce an inverting or non-inverting output. We can take this idea of detecting either a negative or positive going signal one step further by combining the two op-amp comparator circuits above to produce a window comparator circuit.

Differential and Common-Mode Operation

common Mode operation

- In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig.
- In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across R E, which add together. Hence R E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

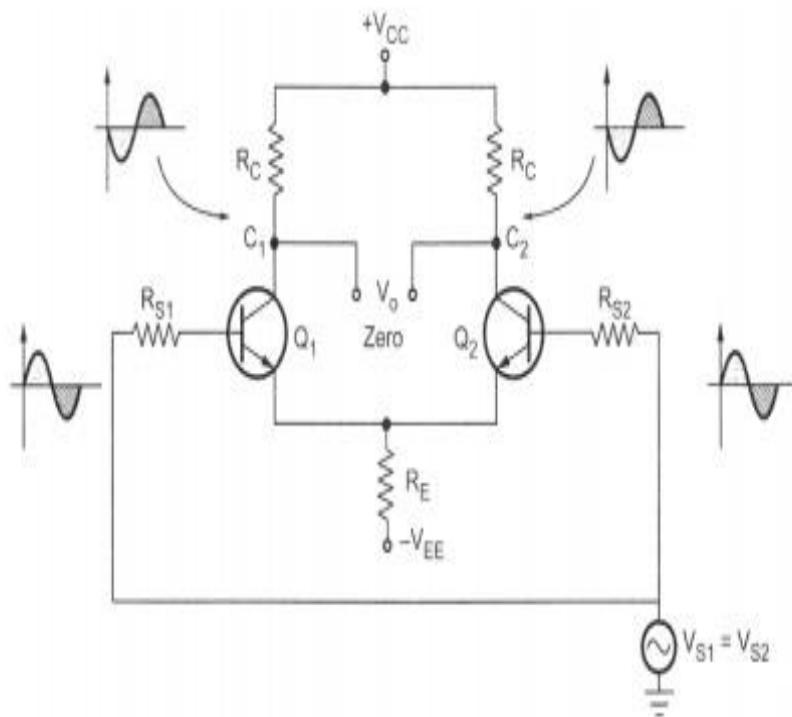


Fig. Common mode operation

- While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase,

Eg. $(20) - (20) = 0$. Thus the difference output V_o is almost zero, negligibly small. ideally it should be zero.

Differential Mode Operation

- In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180° out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig..

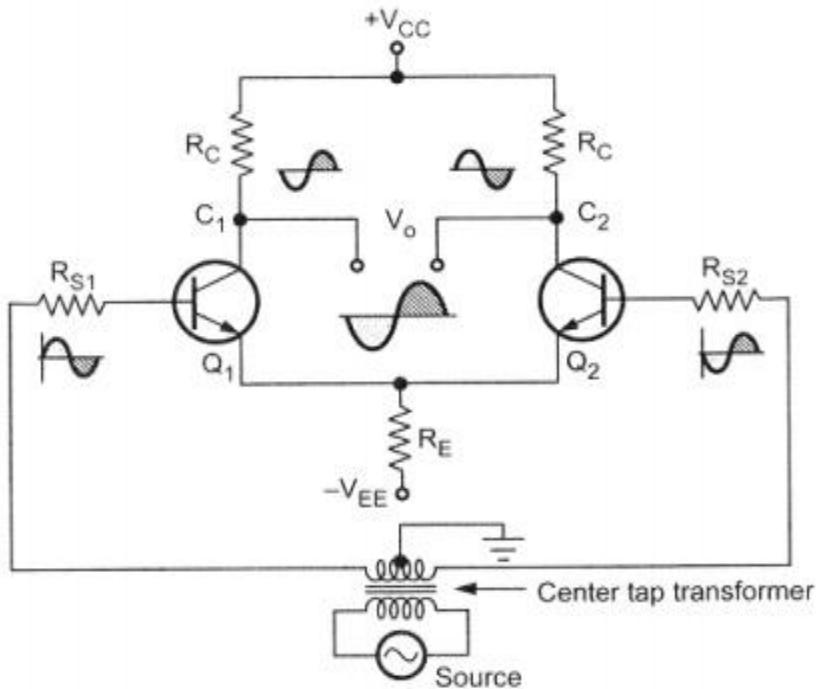


Fig Differential mode operation

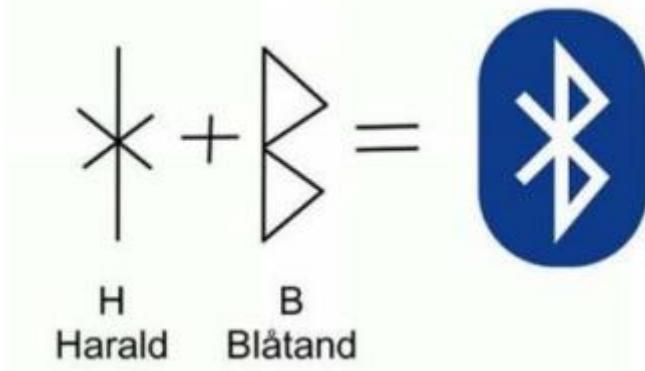
- Assume that the sine wave on the base of Q_1 is positive going while on the base of Q_2 is negative going. With a positive going signal on the base of Q_1 , an amplified negative going signal develops on the collector of Q_1 .
- Due to positive going signal, current through R_E also increases and hence a positive going wave is developed across R_E .
- Due to negative going signal on the base of Q_2 , an amplified positive going signal develops on the collector of Q_2 . And a negative going signal develops across R_E , because of emitter follower action of Q_2 .
- So signal voltages across R_E , due to the effect of Q_1 and Q_2 are equal in magnitude and 180° out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance.
- Hence R_E in this case does not introduce negative feedback. While V_o is the output taken across collector of Q_1 and collector of Q_2 . The two outputs on collector 1 and 2 are equal in magnitude but opposite in polarity. And V_o is the difference between these two signals, e.g. $+10 - (-10) = +20$.
- Hence the difference output V_o is twice as large as the signal voltage from either collector to ground.

Bluetooth

Definition:

Bluetooth wireless technology is a short-range radio technology, which is developed for Personal Area Network (PAN).

- The Bluetooth wireless specification design was named after the king in 1997, based on an analogy that the technology would unite devices the way Harald Bluetooth united the tribes of Denmark into a single kingdom. The Bluetooth logo consists of a Younger futhark bindrune for his initials, H (ᚼ) and B (ᛒ).



- Bluetooth invented in 1994, first time by Ericsson
- It is a wireless alternative to RS-232 cable.
- In 1997 -98 Ericsson, Nokia, Toshiba, IBM, Intel proposed Ver 0.7, 0.8
- Known as IEEE 802.15.1, now maintained by SIG (Special Interest Group).
- Bluetooth wireless technology makes it possible to transmit signals over short distances between telephones, computers and other devices and thereby simplify communication and synchronization between devices.
- Bluetooth is a dynamic standard where devices can automatically find each other, establish connections, and discover what they can do for each other on an ad hoc basis.

Global standard

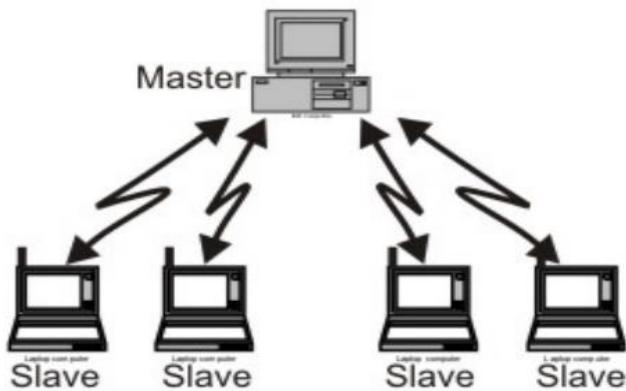
- Eliminates wires and cables between both stationary and mobile devices

- Facilitates both data and voice communication
- Offers the possibility of ad hoc networks and delivers the ultimate synchronicity between all your personal devices

Topology There are two types of topology for Bluetooth –

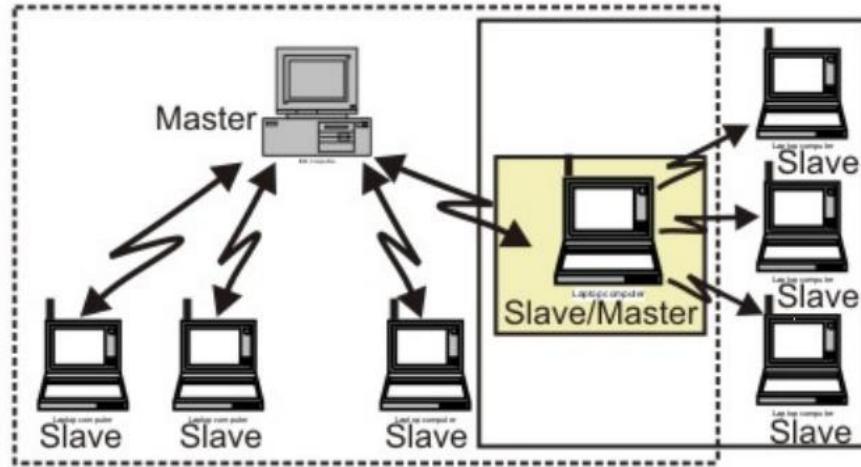
1. **Piconet**
2. **Scatternet**

Piconet Piconet is a small ad hoc network of devices (normally 8 stations) as shown in Fig.1 it has the following features:



- One is called Master and the others are called Slaves
- All slave stations synchronize their clocks with the master
- Possible communication - One-to-one or one-to-many
- There may be one station in parked state
- Each piconet has a unique hopping pattern/ID
- Each master can connect to 7 simultaneous or 200+ inactive (parked) slaves per piconet

Scatternet By making one slave as master of another Piconet, Scatternet is formed by combining several Piconets as shown in Fig. 2 Key features of the scatternet topology are mentioned below:



- A Scatternet is the linking of multiple co-located piconets through the sharing of common master or slave devices.
- A device can be both a master and a slave.
- Radios are symmetric (same radio can be master or slave).
- High capacity system, each piconet has maximum capacity (720 Kbps)

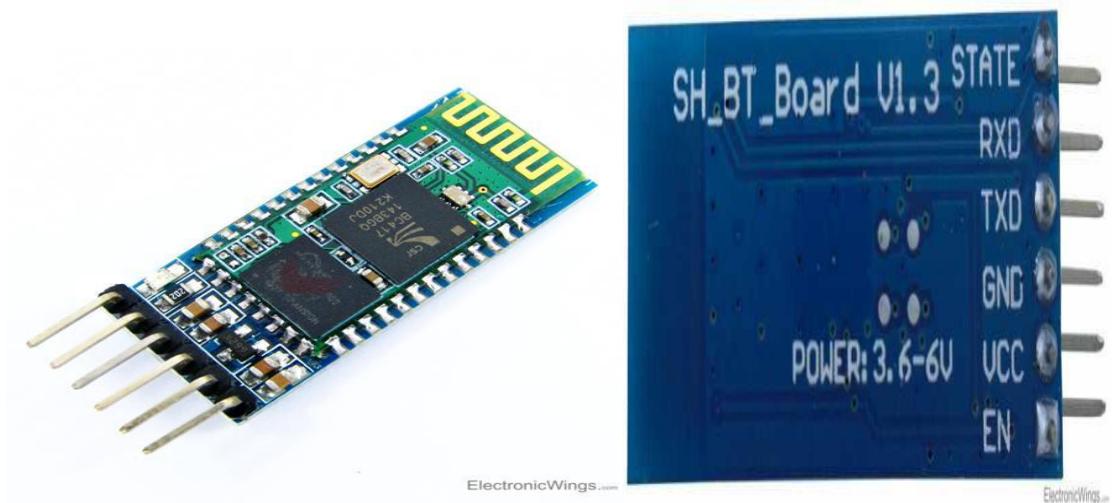
Description of Bluetooth Module HC-05

Introduction

- It is used for many applications like wireless headset, game controllers, wireless mouse, wireless keyboard and many more consumer applications.
- It has range up to <100m which depends upon transmitter and receiver, atmosphere, geographic & urban conditions.
- It is IEEE 802.15.1 standardized protocol, through which one can build wireless Personal Area Network (PAN). It uses frequency-hopping spread spectrum (FHSS) radio technology to send data over air.
- It uses serial communication to communicate with devices. It communicates with a microcontroller using serial port (USART).

HC-05 Bluetooth Module

HC-05 is a Bluetooth module which is designed for wireless communication. This module can be used in a master or slave configuration.



Pin Description It has 6 pins,

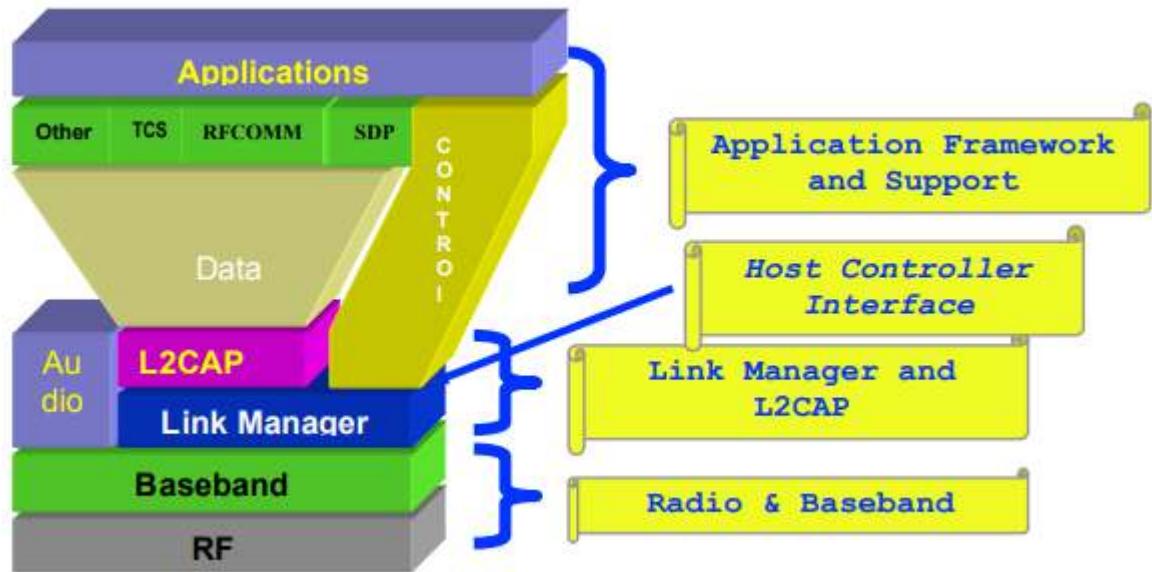
1. STATE 2.RXD 3.TXD 4.GNC 5.VCC 6.EN

1. Key/EN: It is used to bring Bluetooth modules in AT commands mode. If Key/EN pin is set to high, then this module will work in command mode. Otherwise by default it is in data mode.

HC-05 module has two modes

1. Data mode: Exchange of data between devices.
2. Command mode: It uses AT commands which are used to change the setting of HC-05. To send these commands to the module serial (USART) port is used.
2. **VCC:** Connect 5 V or 3.3 V to this Pin.
3. **GND:** Ground Pin of module

Bluetooth Architecture



- **Radio:** The Radio layer defines the requirements for a Bluetooth transceiver operating in the 2.4 GHz ISM band.
- **Baseband:** The Baseband layer describes the specification of the Bluetooth Link Controller (LC), which carries out the baseband protocols and other low-level link routines. It specifies Piconet/Channel definition, “Low-level” packet definition, Channel sharing
- **LMP:** The Link Manager Protocol (LMP) is used by the Link Managers (on either side) for link set-up and control.
- **HCI:** The Host Controller Interface (HCI) provides a command interface to the Baseband Link Controller and Link Manager, and access to hardware status and control registers.
- **L2CAP:** Logical Link Control and Adaptation Protocol (L2CAP) supports higher level protocol multiplexing, packet segmentation and reassembly, and the conveying of quality of service information.
- **RFCOMM:** The RFCOMM protocol provides emulation of serial ports over the L2CAP protocol. The protocol is based on the ETSI standard TS 07.10.
- **SDP:** The Service Discovery Protocol (SDP) provides a means for applications to discover, which services are provided by or available through a Bluetooth device. It also allows applications to determine the characteristics of those available services.

Advantages of Bluetooth

- It avoids **interference** from other wireless devices.
- It has **lower power** consumption.
- It is **easily** upgradeable.
- It has a **better range** than Infrared communication.
- The Bluetooth is used for **voice and data** transfer.
- Bluetooth devices are available at very **cheap cost**.
- No line of sight hence can connect through any obstacles.
- **Free to use** if the device is installed with Bluetooth.
- The technology is **adopted** in many products such as headset, in car system, printer, web cam, GPS system, keyboard and mouse.

Disadvantages of Bluetooth

- It can **lose connection** in certain conditions.
- It has **low bandwidth** as compared to Wi-Fi.
- It allows only **short range** communication between devices.
- **Security** is a very key aspect as it can be hacked.

UNIT 4

Introduction to digital electronics

When we type some letters or words, the computer translates them in numbers as computers can understand only numbers. A computer can understand the positional number system where there are only a few symbols called digits and these symbols represent different values depending on the position they occupy in the number.

The value of each digit in a number can be determined using –

- The digit
- The position of the digit in the number
- The base of the number system (where the base is defined as the total number of digits available in the number system)

Number System

Decimal Number System

The number system that we use in our day-to-day life is the decimal number system. Decimal number system has base 10 as it uses 10 digits from 0 to 9. In decimal number system, the successive positions to the left of the decimal point represent units, tens, hundreds, thousands, and so on.

Each position represents a specific power of the base (10). For example, the decimal number 1234 consists of the digit 4 in the units position, 3 in the tens position, 2 in the hundreds position, and 1 in the thousands position. Its value can be written as

$$(1 \times 1000) + (2 \times 100) + (3 \times 10) + (4 \times 1)$$

$$(1 \times 10^3) + (2 \times 10^2) + (3 \times 10^1) + (4 \times 10^0)$$

$$1000 + 200 + 30 + 4$$

$$1234$$

As a computer programmer or an IT professional, you should understand the following number systems which are frequently used in computers.

S.No.	Number System and Description
1	Binary Number System Base 2. Digits used : 0, 1
2	Octal Number System Base 8. Digits used : 0 to 7
3	Hexa Decimal Number System Base 16. Digits used: 0 to 9, Letters used : A- F

Binary Number System

Characteristics of the binary number system are as follows –

- Uses two digits, 0 and 1
- Also called as base 2 number system
- Each position in a binary number represents a 0 power of the base (2). Example 2^0
- Last position in a binary number represents a x power of the base (2). Example 2^x where x represents the last position - 1.

Example

Binary Number: 10101₂

Calculating Decimal Equivalent –

Step	Binary Number	Decimal Number

Step 1	10101_2	$((1 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0))_{10}$
Step 2	10101_2	$(16 + 0 + 4 + 0 + 1)_{10}$
Step 3	10101_2	21_{10}

Note – 10101_2 is normally written as 10101.

Octal Number System

Characteristics of the octal number system are as follows –

- Uses eight digits, 0,1,2,3,4,5,6,7
- Also called as base 8 number system
- Each position in an octal number represents a **0** power of the base (8). Example 8^0
- Last position in an octal number represents a **x** power of the base (8). Example 8^x where **x** represents the last position - 1

Example

Octal Number: 12570_8

Calculating Decimal Equivalent –

Step	Octal Number	Decimal Number
Step 1	12570_8	$((1 \times 8^4) + (2 \times 8^3) + (5 \times 8^2) + (7 \times 8^1) + (0 \times 8^0))_{10}$
Step 2	12570_8	$(4096 + 1024 + 320 + 56 + 0)_{10}$
Step 3	12570_8	5496_{10}

Note – 12570_8 is normally written as 12570.

Hexadecimal Number System

Characteristics of hexadecimal number system are as follows –

- Uses 10 digits and 6 letters, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F
- Letters represent the numbers starting from 10. A = 10, B = 11, C = 12, D = 13, E = 14, F = 15
- Also called as base 16 number system
- Each position in a hexadecimal number represents a **0** power of the base (16). Example, 16^0

- Last position in a hexadecimal number represents a x power of the base (16). Example 16^x where x represents the last position - 1

Example

Hexadecimal Number: $19FDE_{16}$

Calculating Decimal Equivalent –

Step	Binary Number	Decimal Number
Step 1	$19FDE_{16}$	$((1 \times 16^4) + (9 \times 16^3) + (F \times 16^2) + (D \times 16^1) + (E \times 16^0))_{10}$
Step 2	$19FDE_{16}$	$((1 \times 16^4) + (9 \times 16^3) + (15 \times 16^2) + (13 \times 16^1) + (14 \times 16^0))_{10}$
Step 3	$19FDE_{16}$	$(65536 + 36864 + 3840 + 208 + 14)_{10}$
Step 4	$19FDE_{16}$	106462_{10}

Note – $19FDE_{16}$ is normally written as $19FDE$.

There are many methods or techniques which can be used to convert numbers from one base to another. In this chapter, we'll demonstrate the following –

- Decimal to Other Base System
- Other Base System to Decimal
- Other Base System to Non-Decimal
- Shortcut method - Binary to Octal
- Shortcut method - Octal to Binary
- Shortcut method - Binary to Hexadecimal
- Shortcut method - Hexadecimal to Binary

Decimal to Other Base System

Step 1 – Divide the decimal number to be converted by the value of the new base.

Step 2 – Get the remainder from Step 1 as the rightmost digit (least significant digit) of the new base number.

Step 3 – Divide the quotient of the previous divide by the new base.

Step 4 – Record the remainder from Step 3 as the next digit (to the left) of the new base number.

Repeat Steps 3 and 4, getting remainders from right to left, until the quotient becomes zero in Step 3.

The last remainder thus obtained will be the Most Significant Digit (MSD) of the new base number.

Example

Decimal Number: 29_{10}

Calculating Binary Equivalent –

Step	Operation	Result
Step 1	$29 / 2$	14
Step 2	$14 / 2$	7
Step 3	$7 / 2$	3
Step 4	$3 / 2$	1
Step 5	$1 / 2$	0

As mentioned in Steps 2 and 4, the remainders have to be arranged in the reverse order so that the first remainder becomes the Least Significant Digit (LSD) and the last remainder becomes the Most Significant Digit (MSD).

Decimal Number : 29_{10} = Binary Number : 11101_2

Other Base System to Decimal System

Step 1 – Determine the column (positional) value of each digit (this depends on the position of the digit and the base of the number system).

Step 2 – Multiply the obtained column values (in Step 1) by the digits in the corresponding columns.

Step 3 – Sum the products calculated in Step 2. The total is the equivalent value in decimal.

Example

Binary Number: 11101_2

Calculating Decimal Equivalent –

Step	Binary Number	Decimal Number
Step 1	11101_2	$((1 \times 2^4) + (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0))_{10}$
Step 2	11101_2	$(16 + 8 + 4 + 0 + 1)_{10}$
Step 3	11101_2	29_{10}

Binary Number : 11101_2 = Decimal Number : 29_{10}

Other Base System to Non-Decimal System

Step 1 – Convert the original number to a decimal number (base 10).

Step 2 – Convert the decimal number so obtained to the new base number.

Example

Octal Number : 25_8

Calculating Binary Equivalent –

Step 1 - Convert to Decimal

Step	Octal Number	Decimal Number
Step 1	25_8	$((2 \times 8^1) + (5 \times 8^0))$
Step 2	25_8	$(16 + 5)_{10}$
Step 3	25_8	21_{10}

Octal Number : 25_8 = Decimal Number : 21_{10}

Step 2 - Convert Decimal to Binary

Step	Operation	Result	Remainder
Step 1	$21 / 2$	10	1
Step 2	$10 / 2$	5	0
Step 3	$5 / 2$	2	1
Step 4	$2 / 2$	1	0
Step 5	$1 / 2$	0	1

Decimal Number : 21_{10} = Binary Number : 10101_2

Octal Number : 25_8 = Binary Number : 10101_2

Shortcut Method – Binary to Octal

Step 1 – Divide the binary digits into groups of three (starting from the right).

Step 2 – Convert each group of three binary digits to one octal digit.

Example

Binary Number : 10101_2

Calculating Octal Equivalent –

Step	Binary Number	Octal Number
Step 1	10101_2	$010\ 101$
Step 2	10101_2	$2_8\ 5_8$
Step 3	10101_2	25_8

Binary Number : 10101_2 = Octal Number : 25_8

Shortcut Method — Octal to Binary

Step 1 – Convert each octal digit to a 3-digit binary number (the octal digits may be treated as decimal for this conversion).

Step 2 – Combine all the resulting binary groups (of 3 digits each) into a single binary number.

Example

Octal Number : 25_8

Calculating Binary Equivalent –

Step	Octal Number	Binary Number
Step 1	25_8	$2_{10}\ 5_{10}$
Step 2	25_8	$010_2\ 101_2$
Step 3	25_8	010101_2

Octal Number : 25_8 = Binary Number : 10101_2

Shortcut Method — Binary to Hexadecimal

Step 1 – Divide the binary digits into groups of four (starting from the right).

Step 2 – Convert each group of four binary digits to one hexadecimal symbol.

Example

Binary Number : 10101_2

Calculating hexadecimal Equivalent –

Step	Binary Number	Hexadecimal Number

Step 1	10101_2	$0001\ 0101$
Step 2	10101_2	$1_{10}\ 5_{10}$
Step 3	10101_2	15_{16}

Binary Number : 10101_2 = Hexadecimal Number : 15_{16}

Shortcut Method - Hexadecimal to Binary

Step 1 – Convert each hexadecimal digit to a 4-digit binary number (the hexadecimal digits may be treated as decimal for this conversion).

Step 2 – Combine all the resulting binary groups (of 4 digits each) into a single binary number.

Example

Hexadecimal Number : 15_{16}

Calculating Binary Equivalent –

Step	Hexadecimal Number	Binary Number
Step 1	15_{16}	$1_{10}\ 5_{10}$
Step 2	15_{16}	$0001_2\ 0101_2$
Step 3	15_{16}	00010101_2

Hexadecimal Number : 15_{16} = Binary Number : 10101_2

Implementation of Boolean Logic by Digital Circuits

We now consider the use of electronic circuits to implement Boolean functions
and arithmetic functions that can be derived from these Boolean functions.

Digital circuits are built from standard analog components, such as transistors.

It is the manner in which these transistors are used that causes them to display
the properties required for a digital circuit.

Early digital circuits were based on electromechanical relays, automatic switches that were either “on” or “off”.



Relay On Relay Off

In 1937, George Stibitz of Bell Labs developed what he called the “Model K”.

It was a binary full adder based on relays implementing Boolean logic. He developed the device at home in his kitchen; hence the name.

In 1938, Konrad Zuse developed a relay-based digital computer, the Z-1, in his parents’ apartment in Berlin. It was lost to bombing during the war.

Digital Technologies

There are quite a few ways to build digital circuits. The choice of which to use

in any given device is based on a tradeoff of cost, speed, and power usage.

This course is based on an older technology that is a bit simpler to understand.

This technology is still seen in digital labs used for teaching.

The technology is called TTL (Transistor–Transistor Logic). It is based on the

use of transistors in a mode in which they act as switches, much like relays.

Logically, each TTL device is a Boolean device. All inputs to this device and

outputs from this device are either logic 0 or logic 1.

Electrically, these TTL devices are built to a standard that determines how voltages into the device will be interpreted and what voltage is output.

Here are the voltage standards for active high TTL, the variety we study.

<u>Input to Device</u>	<u>Output by Device</u>
------------------------	-------------------------

Logic 1	2.0 to 5.0 volts	2.4 to 5.0 volts
---------	------------------	------------------

Logic 0	0.0 to 0.8 volts	0.0 to 0.4 volts
---------	------------------	------------------

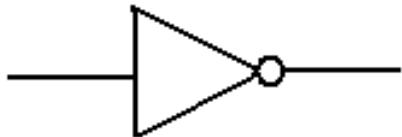
Note the greater latitude on input specifications to allow for voltage degradation.

Basic Digital Circuit Elements

We have already discussed these gates, but present them again.

NOT This function takes one input and produces one output. The gate is shown

below. The circle at the right end of the triangle is important.



Algebraically, this function is denoted $f(X) = X'$ or $f(X) = \overline{X}$

The evaluation of the function is simple: $\bar{0} = 1$ and $\bar{1} = 0$.

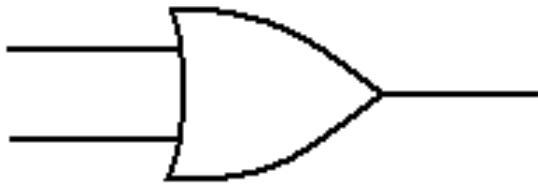
Here is the truth table for the NOT operator.

X	\overline{X}
0	1
1	0

Basic Boolean Operators (Part 2)

Logic OR

This is a function of two Boolean variables. We denote the logical OR of two Boolean variables X and Y by “X + Y”. Some logic books will use “X \vee Y”.



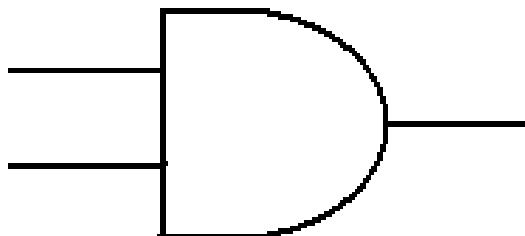
The evaluation of the logical OR function is shown by a truth table

X	Y	X + Y
0	0	0
0	1	1
1	0	1
1	1	1

Basic Boolean Operators (Part 3)

Logic AND

This is a function of two Boolean variables. We denote the logical AND of two Boolean variables X and Y by " $X \bullet Y$ ". Some logic books will use " $X \wedge Y$ ".



The evaluation of the logical AND function is shown by a truth table

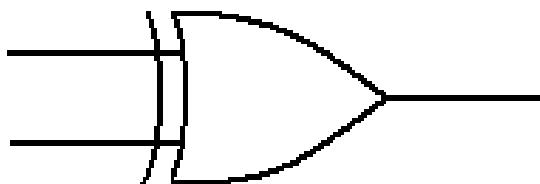
X	Y	$X \bullet Y$
0	0	0
0	1	0
1	0	0
1	1	1

Another Boolean Operator

While not a basic Boolean operator, the exclusive OR is very handy.

Logic XOR

This is a function of two Boolean variables. We denote the logical XOR of two Boolean variables X and Y by “ $X \oplus Y$ ”. Most logic books seem to ignore this function.



The evaluation of the logical XOR function is shown by a truth table

X	Y	$X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

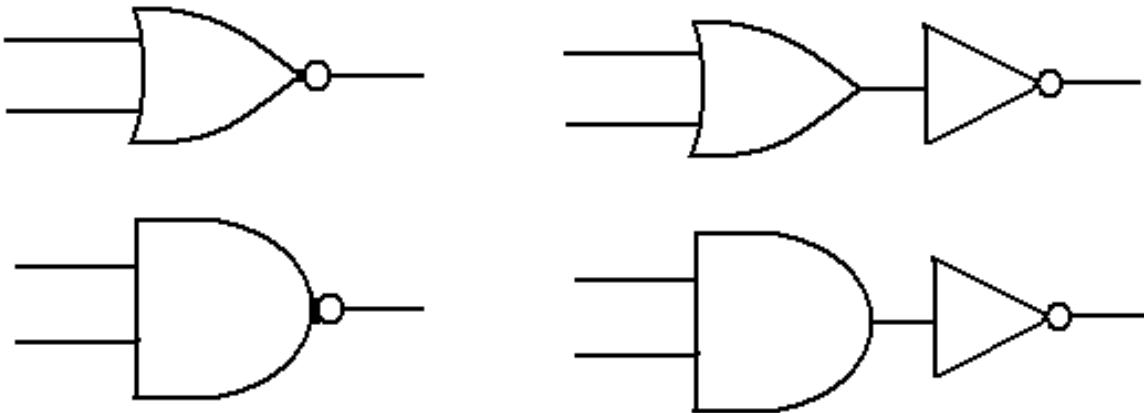
From this last table, we see immediately that

$$X \oplus 0 = X \text{ and } X \oplus 1 = \overline{X}$$

Other Logic Gates

The top gate shows the NOR gate and its logical equivalent.

The bottom line shows the NAND gate and its logical equivalent.



In my notes, I call these “derived gates” as they are composites of Boolean gates

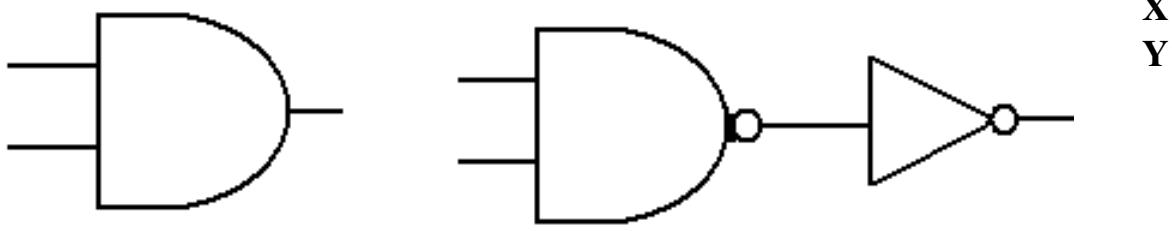
that are more basic from the purely theoretical approach.

X	Y	OR	NOR	X	Y	AND	NAND
0	0	0	1	0	0	0	1
0	1	1	0	0	1	0	1
1	0	1	0	1	0	0	1
1	1	1	0	1	1	1	0

AND Gates and OR Gates: The Real Way

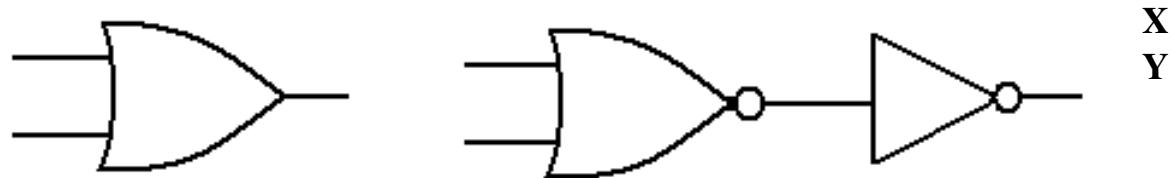
In actual fact, the NAND and NOR gates are more primitive than the AND, OR, and NOT gates in that they are easier to build from transistors.

AND is NOT (NAND)



NAND	AND
0 0	1 0
0 1	1 0
1 0	1 0
1 1	0 1

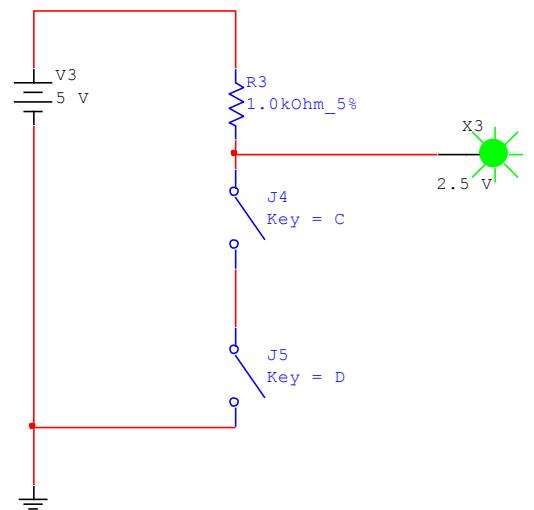
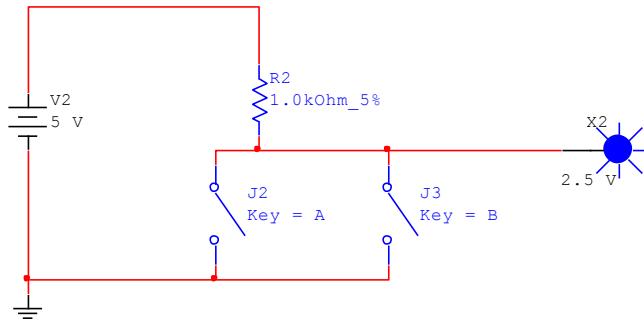
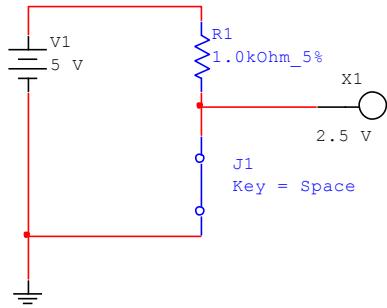
OR is NOT (NOR)



NOR OR	AND
0 0	1 0
0 1	0 1
1 0	0 1
1 1	0 1

Implementation of Basic Circuits

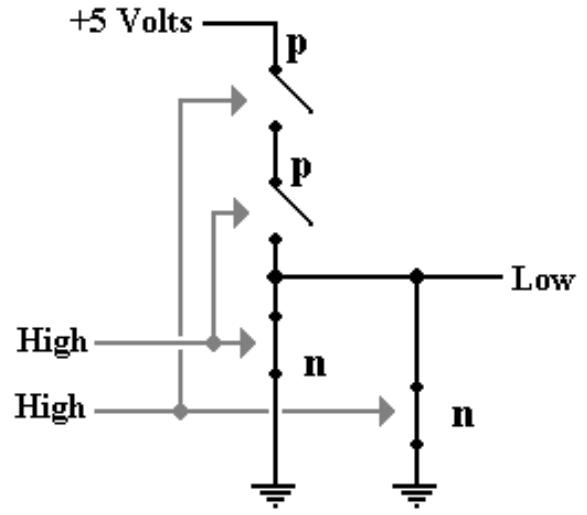
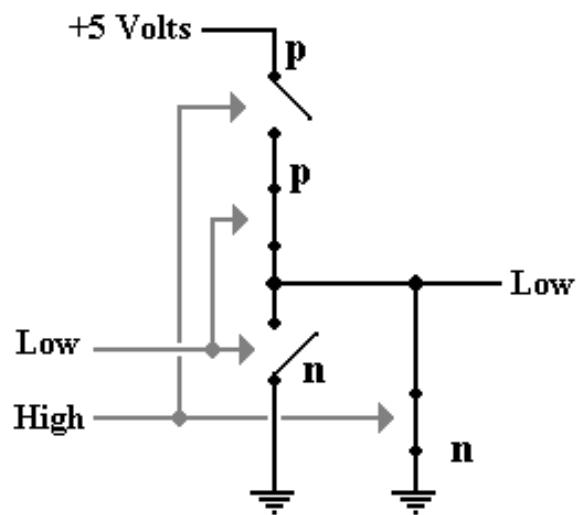
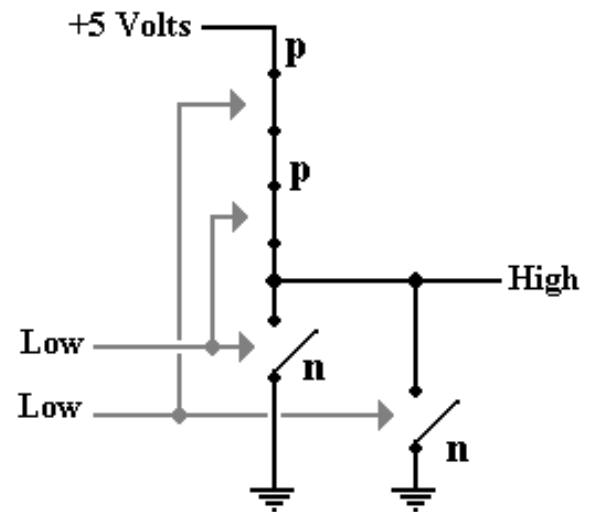
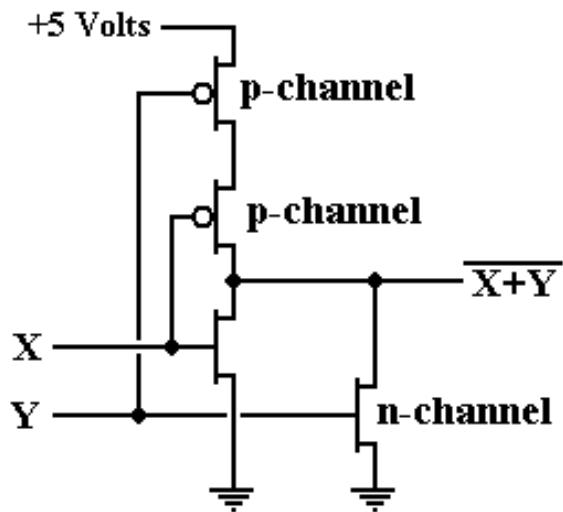
These circuits use simple switches to implement NOT, NOR, and NAND gates.



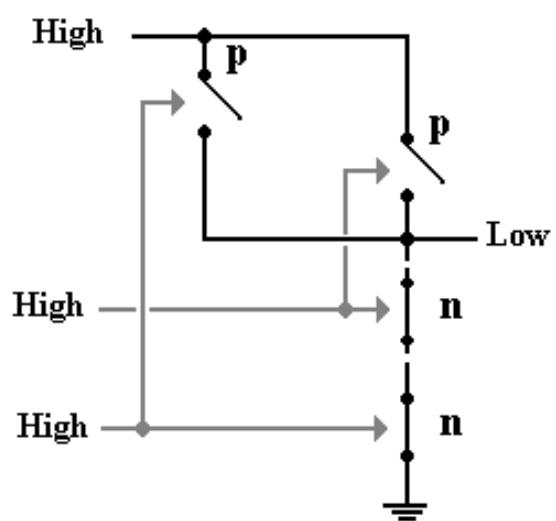
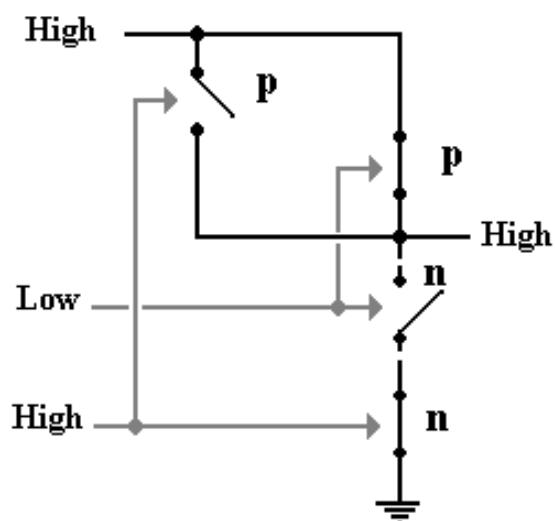
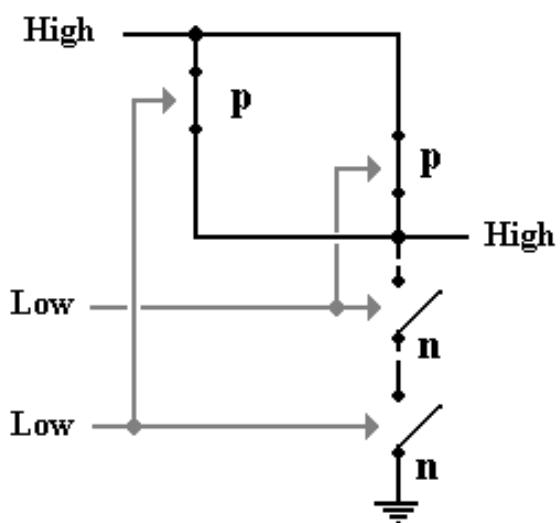
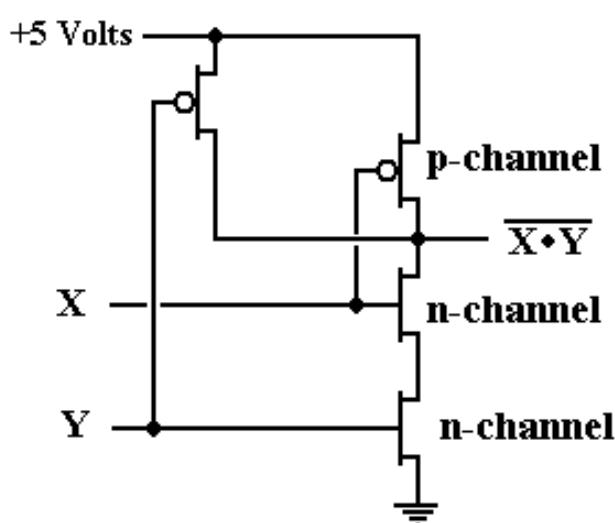
In the circuit at right, if both switches are closed, (logic 1), the output is 0 volts.

If neither or only one is closed, the output is 5 volts. This is a NAND gate.

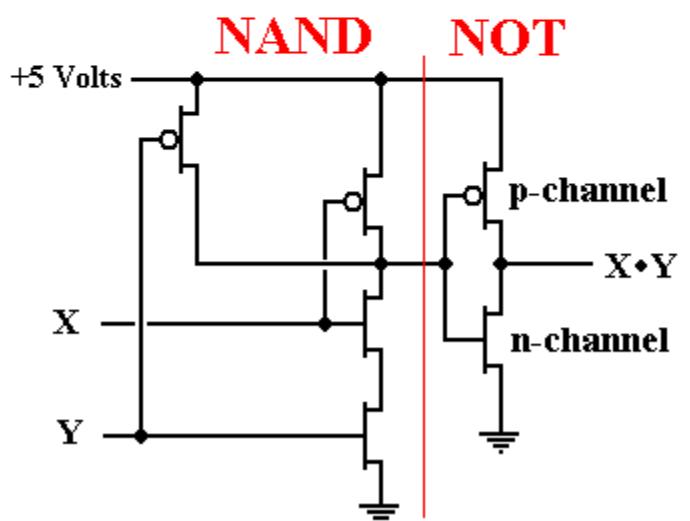
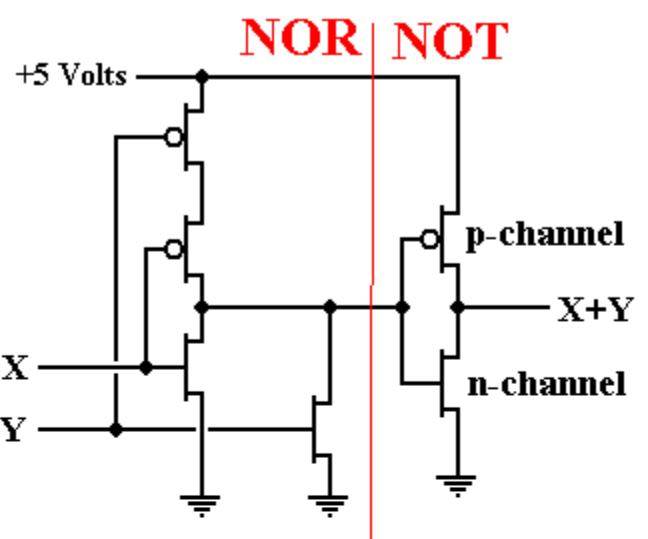
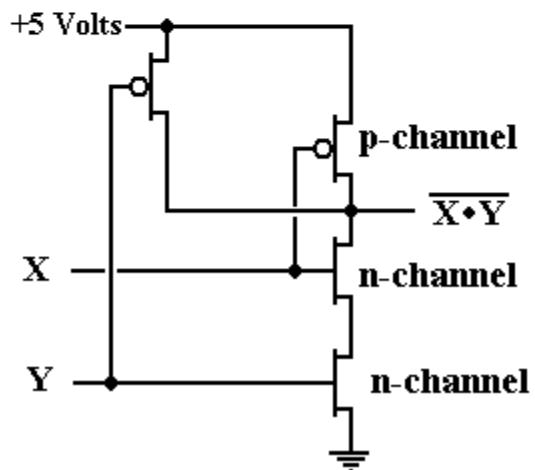
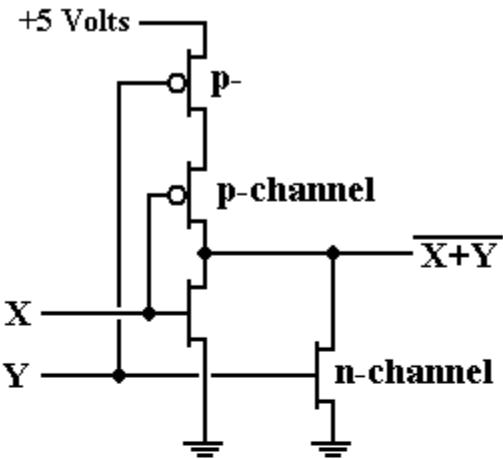
The NOR Gate Implemented in CMOS



The NAND Gate Implemented in CMOS



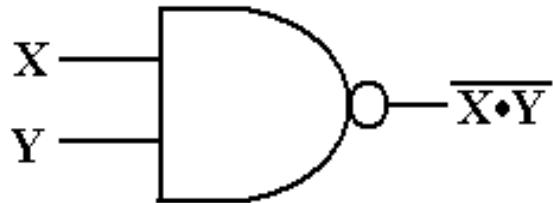
The OR Gate and the AND Gate



The NAND Gate as a Universal Gate

We show how to use a NAND gate to implement the three basic gates of Boolean logic: AND, OR, and NOT.

We begin with a simple NAND gate and its truth table.



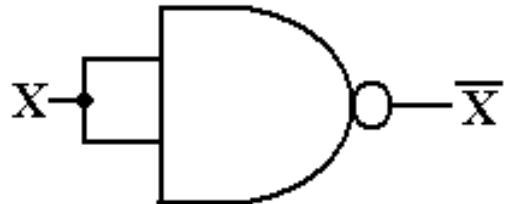
X	Y	$X \bullet Y$	$(X \bullet Y)$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

We now use the NAND gate to implement the basic Boolean devices.

The NAND Gate as a NOT Gate or an AND Gate

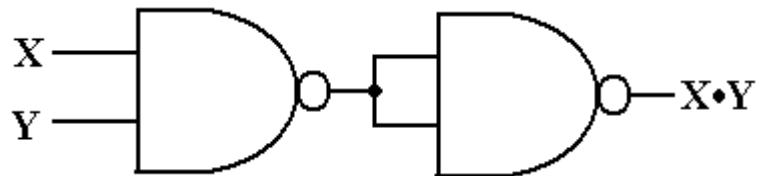
Note in the above truth table, that if $Y = X$, then $\overline{(X \bullet Y)} = \overline{(X \bullet X)} = \overline{X}$.

Here is the NAND implementation of the NOT gate.



Since the NAND gate is logically equivalent to NOT (AND), we may use “double negation” to say that the AND gate is equivalent to NOT (NAND).

Here is the AND gate as implemented from two NAND gates.



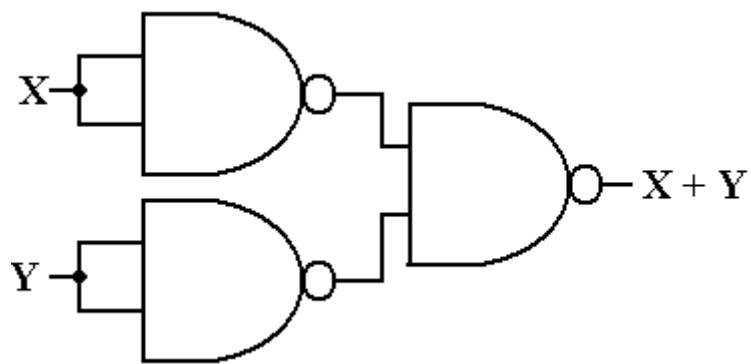
The NAND Gate as an OR Gate

In order to fabricate an OR gate from NAND gates, we must recall DeMorgan's laws.

One of DeMorgan's laws is usually stated as $(\overline{X} \bullet \overline{Y}) = \overline{X + Y}$.

This can be changed to the form $(\overline{X} \bullet \overline{Y}) = \overline{\overline{X}} + \overline{\overline{Y}} = X + Y$.

Here is the circuit.



Multiple–Input Gates

The standard definitions of the AND and OR gates call for two inputs.

3–input and 4–input varieties of these gates are quite common.

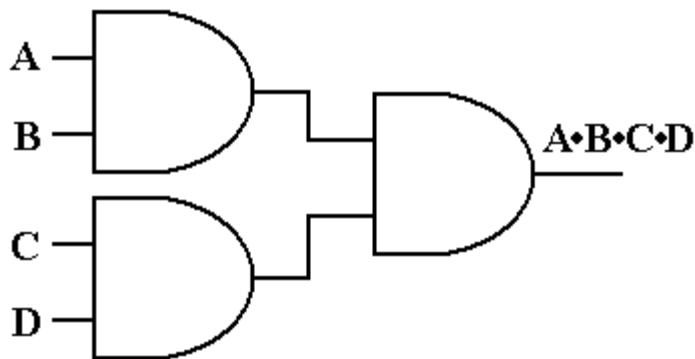
Here we give informal, but precise, definitions.

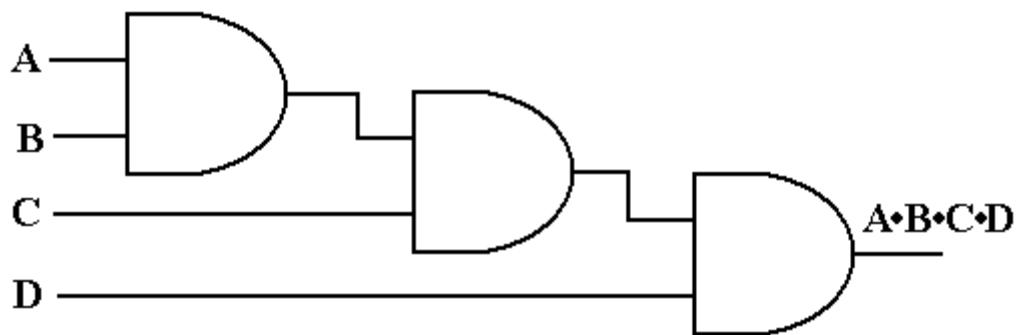
Gate	Number of Inputs	Output
NOT	Exactly 1	0 if input is 1, 1 if input is 0
AND	2 or more	0 if any input is 0 1 if and only if all inputs are 1.
OR	2 or more	1 if any input is 1 0 if and only if all inputs are 0.
NAND	2 or more	1 if any input is 0 0 if and only if all inputs are 1
NOR	2 or more	0 if any input is 1 1 if and only if all inputs are 0.

Example: “Changing the Number of Inputs”

Some lab experiments call for gates with input counts other than what we have.

We begin with two ways to fabricate a 4–input AND gate from 2–input ANDs.



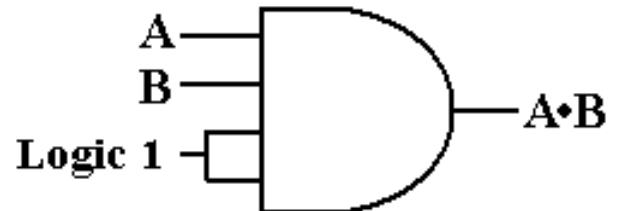
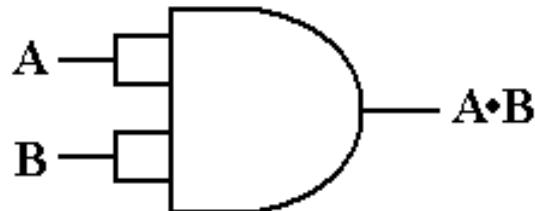


Another Example

We now consider how to take a 4–input AND gate and make it act as if it were a 2–input AND gate.

There are always multiple solutions. Here are two solutions.

There are many others.

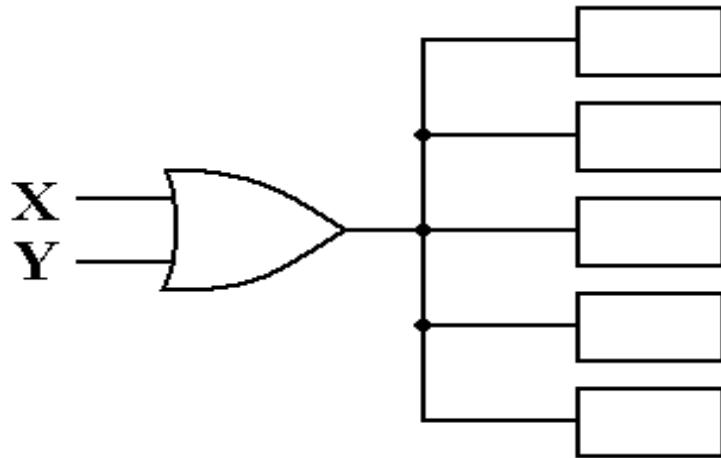


Fan-Out

By definition, the fan-out of a logic gate is the number of other logic gates receiving input from it.

Considerations based on electrical engineering limit the fan-out of any gate.

Here is an OR gate with a fan-out of 5. It drives five other gates of some kind.



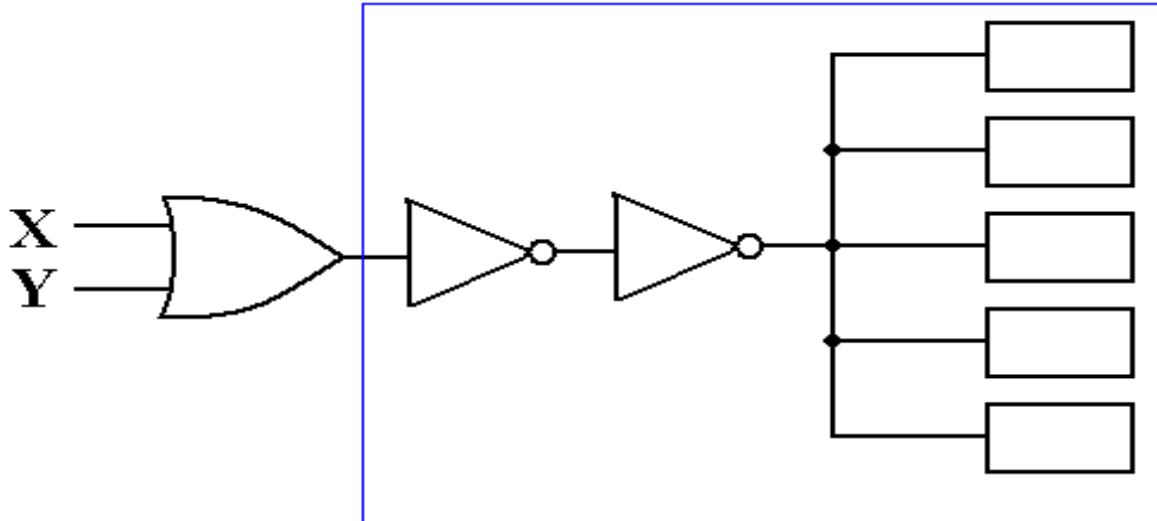
When the fan-out of a circuit element gets too large, there is a voltage sag.

This is similar to what can happen in a building when a large motor or large electric heater turns on.

Controlling Fan-Out

Upon occasion, a given large circuit element will have a number of smaller circuit elements fed from the same input.

There is a standard design trick to cause that big circuit to present only one input to the “outside world”. Here is that trick.



Larger Circuit Element

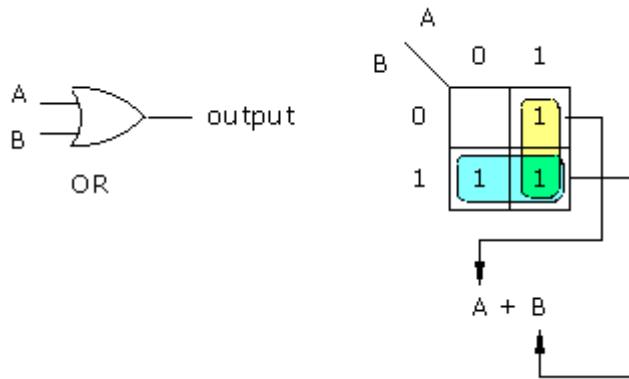
Here the fan-out issue is transferred to the second NOT gate, which is internal to the larger circuit element.

Karnaugh maps (K-Map)

Karnaugh maps provide an alternative way of simplifying logic circuits. Instead of using Boolean algebra simplification techniques, you can transfer logic values from a Boolean statement or a truth table into a Karnaugh map. The arrangement of 0's and 1's within the map helps you to visualize the logic relationships between the variables and leads directly to a simplified Boolean statement.

Karnaugh maps, or K-maps, are often used to simplify logic problems with 2, 3 or 4 variables.

2-variable Karnaugh maps are trivial but can be used to introduce the methods you need to learn. The map for a 2-input OR gate looks like this:



The values of one variable appear across the top of the map, defining the column values, while the values of the other variable appear at the side, defining the values of the variable in each row.

The Karnaugh map for the OR gate is completed by entering a '1' in each of the appropriate cells. Usually, you don't write in the '0's'. Within the map, adjacent cells containing 1's are grouped together in twos, fours, or eights. In this case, there is one horizontal and one vertical group of two. You indicate these groupings by drawing a circle round each one.

The horizontal group corresponds to a B value of 1. In the left hand cell, A=0 and in the right hand cell, A=1. In other words, the value of A does not affect the outcome of the Boolean expression for these cells. Before grouping, you might have written the Boolean expression for these two cells as:

$$\bar{A}.B + A.B$$

After grouping, this reduces to:

$$B$$

In a similar way, the vertical group could have been written as:

$$A.\bar{B} + A.B$$

From the map, you can see that the value of B does not affect the value written in the cells for this group. In other words, the vertical group reduces to:

$$A$$

In this way, the Karnaugh map leads to the overall expression $A + B$.

This is not very exciting but if you apply the same methods to a more complex logic problem, you will begin to understand how Karnaugh maps lead to simpler Boolean statements.

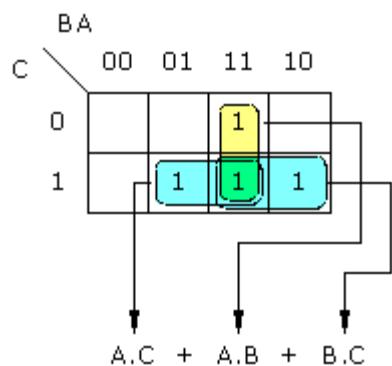
• **3-variable Karnaugh maps**

Here is the truth table for a 3-person majority voting system:

<i>input C</i>	<i>input B</i>	<i>input A</i>	<i>output</i>
0	0	0	0

0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

This is converted into a Karnaugh map, as follows:



Look carefully at the variables at the top of the Karnaugh map. These are *not* written in binary order 00, 01, 10, 11 etc. Instead, each column differs from the previous one by just one bit. This is called Grey code and it is essential for your Karnaugh map to work that you enter the column values in this order. (You will find out more about Grey code later.)

Within the K-map, you can identify three groups of two, as indicated. The left hand horizontal group combines the cells $A\bar{B}C$ and $A.B.C$. Within this group, the value of B does not affect the cell values. This means that B can be eliminated from the expression, leaving $A.C$.

Work through the other groups to confirm that you understand how the remaining terms in the Boolean expression were derived.

With a little practice, this method is going to be quicker than the alternative, simplifying the Boolean expression derived from the truth table:

$$A.B.\bar{C} + A.\bar{B}.C + \bar{A}.B.C + A.B.C$$

3-variable examples

1. Simplify the following expression using a Karnaugh map:

$$A\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + \bar{A}B{C}$$

You may be able to tell what is going to happen by completing the truth table for this expression.

2. Simplify the following expression using a Karnaugh map:

$$\bar{A}(\bar{B}C + \bar{B}\bar{C}) + \bar{A}B\bar{C}$$

From this expression, you can't complete the truth table or Karnaugh map directly. First, you need to convert the statement into **sum of products**, or **SOP** form:

$$A\bar{B}C + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$$

Continue from this point and check your answer by clicking the link

3. Here is another expression to simplify:

$$\bar{A}B + \bar{A}\bar{B}\bar{C} + A.B\bar{C} + A.\bar{B}\bar{C}$$

Note that $\bar{A}.B$ has no C variable and fills two cells in the map. This condition is satisfied when C=0 and also when C=1.

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4-variable maps

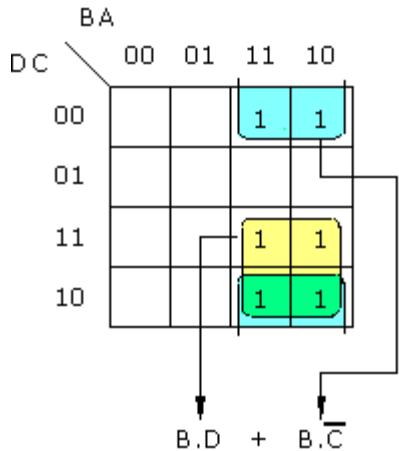
A 4-variable map will contain $2^4 = 16$ cells. It is important to write the variable values along the columns and rows in Grey code:

		B	A		
		00	01	11	10
D	C	00			
		01			
D	C	11			
		10			

To simplify the equation:

$$x = B.\bar{C}.\bar{D} + \bar{A}.B.\bar{C}.D + A.B.\bar{C}.D + \bar{A}.B.C.D + A.B.C.D$$

The Karnaugh map becomes:



To give the simplest Boolean statement, you should put a circle round the maximum number of terms.

In this case, you can make two groups of four, one of which wraps around from top to bottom. You identify the two variables which remain constant in each group and eliminate the other two:

$$x = BD + BC$$

Introduction to IC Technology

The growth of electronics started with invention of vacuum tubes and associated electronic circuits. This activity termed as vacuum tube electronics, subsequently the evolution of solid state devices and consequent development of integrated circuits are responsible for the present status of communication, computing and instrumentation.

Due to its small dimension, low cost, and very high reliability even the common man is familiar with its applications like smart phones and laptops.

The IC's also found its way in military applications, state of the art communication systems, and industrial applications due to its high reliability and compact size. basically these terminologies like SSI,MSI,LSI and VLSI are emerged from the complexity of IC(Integrated circuit).i.e the number of transistors of are fabricated on chip(usually single substrate).

first IC was invented around 1959 by Jack Kilby.

The first integrated circuits contained only a few transistors and so were called "Small-Scale Integration (**SSI**)". They used circuits containing transistors numbering in the tens. They were very crucial in development of early computers. SSI was followed by introduction of the devices which contained hundreds of transistors on each chip, and so were called "Medium-Scale Integration (**MSI**)".

MSI were attractive economically because which they cost little more systems to be produced using smaller circuit boards, less assembly work, and a number of other advantages. Next development was of Large Scale Integration (**LSI**). The development of LSI was driven by economic factors and each chip comprised tens of thousands of transistors. It was in 1970s, when LSI started getting manufactured in huge quantities.

LSI was followed by Very Large Scale Integration (**VLSI**) where hundreds of thousands of transistors were used and still being developed. It was for the first time that a CPU was fabricated on a single

integrated circuit, to create a microprocessor. In 1986, with the introduction of first one megabit RAM chips, more than one million transistors were integrated.

Microprocessor chips produced in 1994 contained more than three million transistors. ULSI refer to “Ultra-Large Scale Integration” and correspond to more than 1 million of transistors. However there is no qualitative leap between VLSI and ULSI, hence normally in technical texts the “VLSI” term cover ULSI.

Summary

1. **SSI** - Small Scale integration

less than 100 components (about 10 gates)

2. **MSI** - Medium Scale integration

less than 500 components (more than 10 but less than 100 gates)

3. **LSI** - Large Scale integration

components b/w 500 and 300000 (more than 100 gates)

4. **VLSI** - Very Large Scale integration

it contains more than 300000 components per chip

Nowadays, an IC that has the size of a fingernail consists of more than a million transistors and other discrete components embedded into it.

Thus an integrated circuit can also be called a microchip and is basically a collection of some discrete circuits on a small chip that is made of a semiconductor material like silicon.

Integrated circuit

It is a circuit where all discrete components such as passive as well as active elements are fabricated on a single crystal chip

- The first semiconductor chip held two transistors each.
- The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors, and capacitors, making it possible to fabricate one or more logic gates on a single device.

As on increasing the number of components(or transistors) per integrated circuit the technology was developed as:

Small scale integration(SSI)

The technology was developed by integrating the number of transistors of 1-100 on a single chip.

Ex: Gates, flip-flops, op-amps.

Medium scale integration(MSI)

The technology was developed by integrating the number of transistors of 100-1000 on a single chip.

Ex: Counters, MUX, adders, 4-bit microprocessors.

Large scale integration(LSI)

The technology was developed by integrating the number of transistors of 1000-10000 on a single chip.

Ex:8-bit microprocessors,ROM,RAM.

Very large scale integration(VLSI)

The technology was developed by integrating the number of transistors of 10000-1Million on a single chip.

Ex:16-32 bit microprocessors,peripherals,complimentary high MOS.

Ultra large scale integration(ULSI)

The technology was developed by integrating the number of transistors of 1Million-10 Millions on a single chip.

Ex: special purpose processors.

Giant scale integration(GSI)

The technology was developed by integrating the number of transistors of above 10 Millions on a single chip.

Ex:Embedded system, system on chip.

Advantages of Integrated Circuits

Integrated circuits possess the following advantages over discrete circuits:

- Increased reliability due to lesser number of connections.
- Extremely small size due to the fabrication of various circuit elements in a single chip of semiconductor material.
- Lesser weight and space requirement due to miniaturized circuit.
- Low power requirements.
- Greater ability to operate at extreme values of temperature.
- Low cost because of simultaneous production of hundreds of alike circuits on a small semiconductor wafer.
- The circuit layout is greatly simplified because integrated circuits are constrained to use minimum number of external connections.

Disadvantages of Integrated Circuits

- If any component in an IC goes out of order, the whole IC has to be replaced by the new one.
- In an IC, it is neither convenient nor economical to fabricate capacitance exceeding 30 pF. Therefore, for high value of capacitance, discrete components exterior to IC chip are connected.

- It is not possible to fabricate inductors and transformers on the surface of semiconductor chip. Therefore, these components are connected exterior to the semiconductor chip.
- It is not possible to produce high power ICs greater than 10 W.
- There is a lack of flexibility in an IC i.e. it is generally not possible to modify the parameters within which an integrated circuit will operate.

Types of ICs

Metal-can IC Ceramic flat pack IC 14-Pin Dual In-line Package(DIP) 8-Pin Dual In-line Package(DIP)Plastic

On the basis of applications ICs are of two types namely: **Linear Integrated Circuits** and **Digital Integrated Circuits**.

Linear IC's are used in cases when the relationship between the input and output of a circuit is linear. An important application of linear IC is the operational amplifier commonly referred to as op-amp.

When the circuit is either in on-state or off-state and not in between the two, the circuit is called a digital circuit. IC's used in such circuits are called **digital IC's**. They find wide applications in computers and logic circuits.

Here are some further classification of integrated circuits based on the fabrication techniques used.

1. Mono-lithic
2. Thin-film
3. Thick-film
4. Hybrid

UNIT 5

Evolution of mobile Radio Communication

Over the most recent couple of decades, there has been a huge progression in mobile wireless communications.

Mobile Communication systems have encountered an astounding change. It started with 1G technology of which in a very short amount of time got superseded by 2G, 3G, 4G, & now even 5G.

Mobile telecommunications has turned out to be more mainstream in the most recent couple of years because of a quick change from 1G to 5G in portable innovation and how we use technology today. This change is because of the necessity of perfect transmission innovation and high increment in telecoms clients for everyday uses including businesses, the education sector, and just about every other industry.

The different types of Mobile Telephony (Cellular) Systems

1G:

As a matter of first importance when we discuss 1G etc what does this G stand for? Well, it stands for Generation, so 1G is the first generation of mobile communication systems.

In the 1970's privately owned businesses began building up their own particular correspondence frameworks to advance existing frameworks further. Those private frameworks were

Analogue mobile phone systems (AMPS) utilized in parts of America and the United Kingdom. Total Access Communications Systems (TACS) and Nordic Mobile Telephone (NMT) were also used in parts of Europe. These created frameworks are now what is known as the first Generation of mobile communication frameworks.

2G:

2G alludes to the second era in light of GSM and was developed in the late 1980s. It utilises computerised signals for voice transmission. The principal focal point of this innovation was on advanced flags and gives individuals the ability to convey content and picture messages at low speed.

The GSM innovation was ceaselessly enhanced to give better administrations which prompted improvement of cutting-edge Technology in the vicinity of 2g and 3g mobile networks.

3G:

Third Generation (3G) is likewise in light of GSM and was propelled in the year 2000. The point of this innovation was to offer rapid information across the world. The first innovation was enhanced to permit information up to 14 Mbps and all the more utilising bundle exchanging. It utilises Wide Band Wireless Networks with which clearness is expanded. It likewise offers information administrations, access to TV/Video, Data, Text, etc. as well as new administrations like

Global Roaming is now possible. It works at a scope of 2100MHz and has a data transmission of 15-20MHz utilised for High-speed network access and video visiting.

The 3G mobile framework was called a UMTS (Universal Mobile Telecommunication System) in Europe, while CDMA2000 is the name of American 3G variation.

4G:

4G offers a much improved downloading rate of up to 100Mbps. 4G gives the same element advantages as 3G but also includes extra administrations like Multi-Media Newspapers, watching TV programs online using services such as Netflix with a lot more clarity due to the send/receive speeds of Data now being significantly quicker than past ages. It introduced us to the Mobile Social Media and Mobile App world used how it is today. LTE (Long Term Evolution) is considered a 4G innovation.

5G is next

5G refers to Fifth Generation of which initial trials began from the late 2010's but hasn't rolled out in most countries as of yet.

All investigations of the release date of when 5G will be available points to the year 2020. In spite of the fact that the system will start to be deployed in 2018 and the lion's share

of administrators, administrative bodies and producers are as of now occupied with converses orchestrating a standard, as it occurred before the deployment of the 4G innovation. Truth be told, Qualcomm has effectively built up the initial 5G modem, particularly made to help this sort of system, along these lines making ready for the new age of mobile phones. On its part, the European Union looks to finish the 5G scope by 2025. At this quick rate of advancement, that date is now around the bend.

5G innovation has remarkable information capacities and has the capacity to integrate unhindered call volumes and unbounded information communicates inside the most recent portable working framework. 5G innovation has a splendid future since it can deal with best advances and offer invaluable handsets to their clients. Maybe in the coming days, 5G innovation assumes control over the world market. 5G Technologies have an unprecedented capacity to help Software and Consultancy. The Router and switch innovation utilised as a part of 5G deployment gives an extremely powerful high-speed network.

What is GPRS? - packet switching

The key element of GPRS technology was that it uses packet switched data rather than circuit switched data, and this technique made much more efficient use of the available capacity. This is because most data transfer occurs in what is often termed a "bursty" fashion. The transfer occurs in short peaks, followed by breaks when there is little or no activity.

GPRS - General Packet Radio Service was the evolution of 2G GSM to provide packet switched data at rates up to a maximum of 172 kbps.

GPRS was something of a revolution because all previous mobile phone systems had used circuit switched channels. Also previous cell phone systems including GSM had focussed in voice communications, but the need for mobile data was starting to come about and GPRS was one of the first to address this in a real way.

Although 2G GSM could provide some data capability it was far too slow to be used for any real applications. As a result, GPRS was developed to enable data to be handled and it also provided a stepping stone on the path to 3G.

GPRS technology offered some significant benefits when it was launched:

- **Speed:** One of the headline benefits of GPRS technology is that it offers a much higher data rate than was possible with GSM. Rates up to 172 kbps are possible, although the maximum data rates realistically achievable under most conditions will be in the range 15 - 40 kbps.
- **Packet switched operation:** Unlike GSM which was used circuit switched techniques, GPRS technology uses packet switching in line with the Internet. This makes far more efficient use of the available capacity, and it allows greater commonality with Internet techniques.
- **Always on connectivity:** A further advantage of GPRS is that it offers an "Always On" capability. When using circuit switched techniques, charges are based on the time a circuit is used, i.e. how long the call is. For packet switched technology charges are for the amount of data carried as this is what uses the services provider's capacity. Accordingly, always on connectivity is possible.
- **More applications:** The packet switched technology including the always on connectivity combined with the higher data rates opens up many more possibilities for new applications. One of the chief growth areas that arose from GPRS was the Blackberry form of mobile or PDA. This provided for remote email applications along with web browsing, etc.

Global System for Mobile Communications (GSM)

The **Global System for Mobile Communications (GSM)** is a standard developed by the [European Telecommunications Standards Institute](#) (ETSI) to describe the protocols for second-generation (2G) digital [cellular networks](#) used by mobile devices such as mobile phones and tablets. It was first deployed in [Finland](#) in December 1991. By the mid-2010s, it became a global standard for mobile communications achieving over 90% market share, and operating in over 193 countries and territories.¹

GSM utilizes a [cellular network](#), meaning that [cell phones](#) connect to it by searching for cells in the immediate vicinity.

- GSM is a circuit-switched system that divides each 200 kHz channel into eight 25 kHz time-slots. GSM operates on the mobile communication bands 900 MHz and 1800 MHz in most parts of the world. In the US, GSM operates in the bands 850 MHz and 1900 MHz.
- GSM owns a market share of more than 70 percent of the world's digital cellular subscribers.
- GSM makes use of narrowband Time Division Multiple Access (TDMA) technique for transmitting signals.
- GSM was developed using digital technology. It has an ability to carry 64 kbps to 120 Mbps of data rates.
- Presently GSM supports more than one billion mobile subscribers in more than 210 countries throughout the world.
- GSM provides basic to advanced voice and data services including roaming service. Roaming is the ability to use your GSM phone number in another GSM network.

Listed below are the features of GSM that account for its popularity and wide acceptance.

- Improved spectrum efficiency
- International roaming
- Low-cost mobile sets and base stations (BSs)
- High-quality speech
- Compatibility with Integrated Services Digital Network (ISDN) and other telephone company services
- Support for new services

CDMA

CDMA: Code Division Multiple Access

Code Division Multiple Access is a *channel access method used by several radio communication technologies*. It is a digital cellular technology and an example of multiple access. It is generally used for mobile communication.

Multiple access means that several transmitters can send information simultaneously over a single communication channel. In this system, different CDMA codes are assigned to different users and the user can access the whole bandwidth for the entire duration. It optimizes the use of available bandwidth as it transmits over the entire frequency range and does not limit the user's frequency range.

Thus, CDMA allows several users to share a band of frequencies without undue interference between the users. It is used as a access method in many mobile phone standards.

Usage

- It is used in the Global Positioning System (GPS).
- It is used by several mobile phone companies (e.g. Qualcomm standard IS-2000 also known as CDMA2000)
- W-CDMA is used in UTMS 3G mobile phone standard.
- CDMA has been used in OmniTRACS satellite system for transportation.

Categories of CDMA

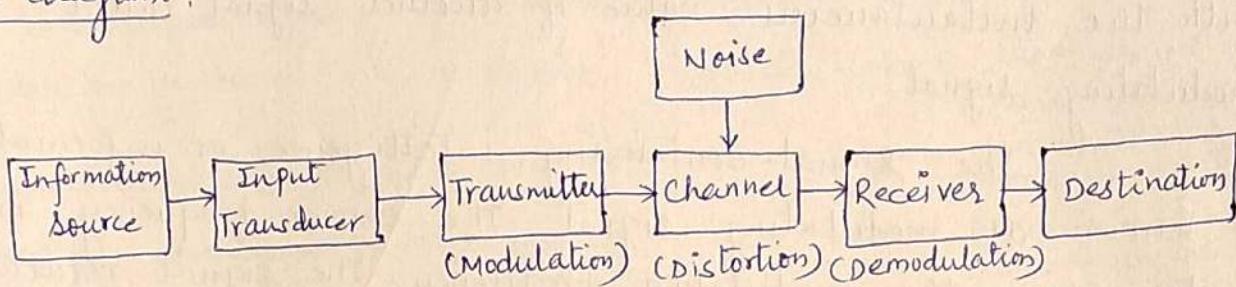
- Synchronous CDMA (orthogonal codes)
- Asynchronous CDMA (pseudorandom codes)

Difference between CDMA and GSM

Criteria	CDMA	GSM
Technology	CDMA is based on spread-spectrum technology which makes the optimum use of available bandwidth.	GSM operates on the wedge spectrum. it uses both time division multiple access (TDMA) and frequency division multiple access (fdma). TDMA provide multi-user access by cutting up the channel into different time slice and fdma provides the multi-user access by separating the used frequency.
Security	CDMA is more secure than GSM.	GSM is less secure than CDMA.
Global reach	CDMA is used in usa and some part of canada and japan. CDMA is used only by 24% of the users worldwide.	GSM is used over 80% of the world network in over 210 countries. GSM is used 76% of the users worldwide.
Data Transfer Rate	CDMA has faster data transfer as compared to GSM.	GSM has slower data transfer as compared to CDMA.

Introduction: - In communication system, we sending, receiving and processing of information.

Block diagram:-



- i) Information source:- The message or information which we have to communicate comes from the information source.
- ii) Input Transducer:- The message obtained from the information source may or may not be electrical in nature. If the message is not electrical in nature, then an input transducer is used to convert into a time varying electrical signal.
- iii) Transmitter:- The function of the transmitter is to process the electrical signal from different aspects.
- iv) Communication channel and noise:- The main function of channel is to provide a physical connection between the transmitter and receiver. The transmission from the transmitter in between a certain frequency range called the channel. Noise may be defined as an unwanted signal present in a communication system due to variety of causes.
- v) Receiver:- The function of a receiver is to receive the message signal and perform a process which is reverse to what was done at transmitter stage. This process is known as demodulation.
- vi) Destination:- It is used to convert an electrical message signal into its original message which transmit from information source.

Modulation:- Modulation is the process by which audio frequency waves are superimposed on radio frequencies.

Modulation may be defined as the process by which some characteristics of a signal called carrier is varied in accordance with the instantaneous value of another signal called modulating signal.

The signal containing intelligence or information are known as modulating signal. The carrier frequency is greater than the modulating frequency. The signal resulting from the process of modulation is known as modulated signal.

Need of modulation:-

i) Practical Antenna Length

The signals are transmitted and received with the help of antennas. For better radiation and reception, the transmitting and receiving antennas must have length to quarter wavelength of the frequency used. $l = \frac{\lambda}{4} = \frac{1}{4} \left(\frac{c}{f} \right)$ meters

l = length of antenna, λ = wavelength of the signal

c = speed of light = 3×10^8 m/sec., f = frequency of signal

$$\text{for a signal } 20\text{ Hz to } 20\text{ KHz}, \quad l = \frac{1}{4} \times \frac{3 \times 10^8}{20 \times 10^3} = 3750 \text{ metres}$$

$$l = \frac{1}{4} \times \frac{3 \times 10^8}{10^2} = \frac{3 \times 10^6}{4} = 750 \text{ m.}$$

ii) Noise Reduction! - Noise is the main disadvantage of any communication. Although, noise can not be eliminated completely, but with the help of modulation, the effect of noise can be reduced.

iii) Remove interference! - Different messages having different frequency level can be transmitted simultaneously without any interference.

(Multiplexing)

iv) Increases the range of communication \rightarrow at long distance the baseband signal is suppressed (attenuated).

3 baseband signals.

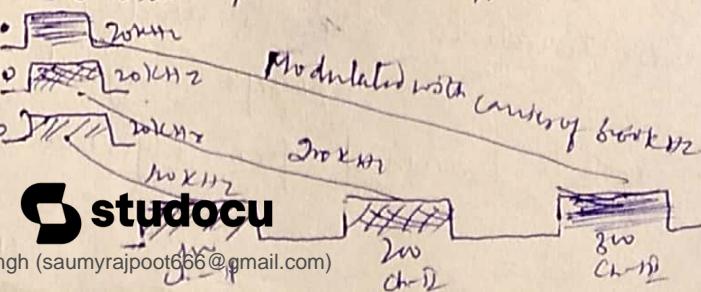
v) Avoids mixing of signals

Multiplexing is a process by which two or more signals can be transmitted over the same communication channel simultaneously.

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Electro magnetic spectrum :- The frequency of EM signal can be very low or it can be extremely high. This entire range of frequencies of EM waves is called as electro magnetic spectrum.

<u>St. No.</u>	<u>Band</u>	<u>Frequency</u>	<u>Wavelength</u>	<u>Applications</u>
1.	Extremely Low Frequency (ELF)	30 - 300 Hz	10000 km - 1000 km	Power Transmission
2.	Voice frequencies (VF)	300 - 3000 Hz	1000 km - 100 km	Audio Applications
3.	Very low frequencies (VLF)	3 - 30 KHz	100 Km - 10 km	Long range navigation and marine radio
4.	Low Frequencies (LF)	30 - 300 KHz	10 Km - 1 Km (long waves)	Aeronautical and marine navigation
5.	Medium Frequencies (MF)	300 - 3000 KHz	1 Km - 100 m (Medium waves)	AM radio and radio telecommunication
6.	High Frequencies (HF)	3 - 30 MHz	100 m - 10 m (Short waves)	BBC broadcast -
7.	Very high frequencies (VHF)	30 - 300 MHz	10 m - 1 m	FM radio broadcasting
8.	Ultra high frequencies (UHF)	300 MHz - 3 GHz	1 m - 10 cm	Cellular phones
9.	Microwave and Super High Frequencies (SHF)	3 - 30 GHz	10 cm - 1 cm	Radar, Microwave ovens
10.	Extremely high frequencies (EHF)	30 - 300 GHz	1 cm - 1 mm	Satellite communication
11.	Infrared	300 GHz - 430 THz	.7 to 10 mm	

Terminologies in communication system :-

i) Transducer ii) signal iii) Transmitter iv) Noise v) Receiver

vi) Attenuation:- the loss of strength of a signal while propagating through a medium is known as attenuation.

vii) Range:- the largest distance between a source and destination upto which the signal is received with sufficient strength.

viii) BW:- basics of signals representation and analysis:-

'A function of one or more independent variables which contains some information is called a signal.'

Signals may be classified as :

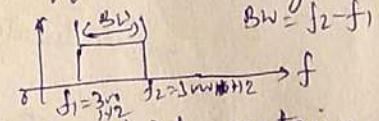
i) continuous time signals and discrete time signals

ii) Periodic signals and Non-periodic signals

iii) Even and odd signals iv) Energy signal and power signal

v) Real and complex signal

Multiplexing allows the same channel to be used by many signals.



Amplitude Modulation :- Amplitude modulation is defined as a type of modulation in which the amplitude of the carrier is made proportional to the instantaneous value of the modulating or base band signal. In amplitude modulation, the amplitude of a carrier signal is varied by the modulating voltage.

Let us consider carrier and modulating voltage, v_c and v_m .

$$v_c = V_c \sin \omega_c t \quad \text{--- (1)}$$

$$v_m = V_m \sin \omega_m t \quad \text{--- (2)}$$

V_c - max. amplitude of carrier signal

V_m - " " " modulating "

ω_c - carrier frequency = $2\pi f_c$

ω_m - modulating frequency = $2\pi f_m$

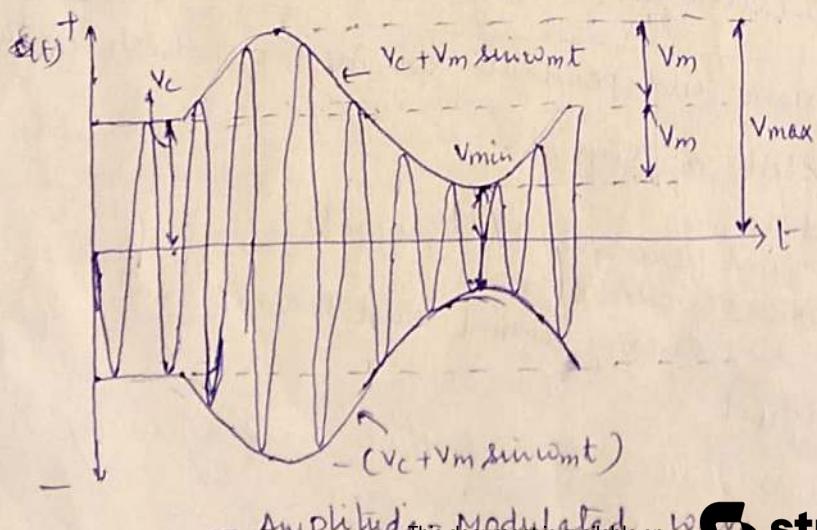
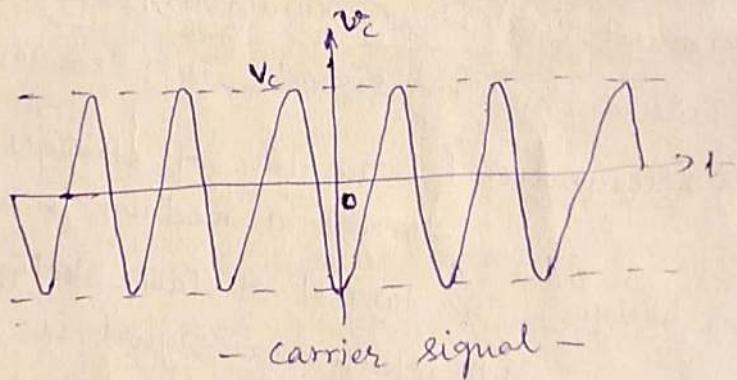
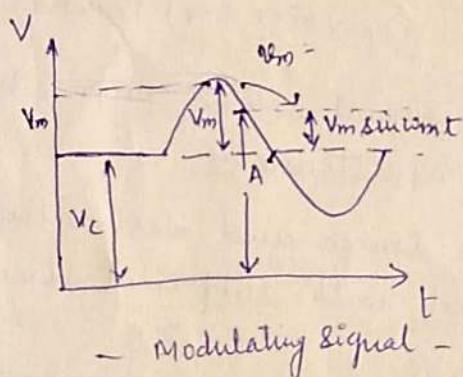
According to AM, the max. amplitude V_c of the carrier wave will have to be made proportional to the instantaneous amplitude of the modulating signal.

The amplitude of the AM wave is given by

$$(V_{AM}) A = V_c + V_m \sin \omega_m t \quad \text{--- (3)} \quad (\because A = V_c + v_m)$$

$$\boxed{\text{Modulation index } m = \frac{V_m}{V_c} \Rightarrow V_m = m V_c}$$

$$\text{The instantaneous value of the amplitude modulated wave } v_t = A \sin \omega_c t = (V_c + V_m \sin \omega_m t) \sin \omega_c t \quad \text{--- (4)}$$



$$\text{Modulation Index} : - (m) = \frac{V_m}{V_c} = \frac{\text{max. amplitude of modulating signal}}{\text{max. amplitude of carrier signal}}$$

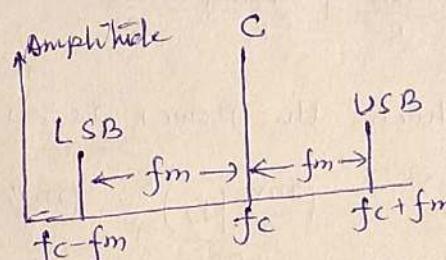
The modulation index is also known as depth of modulation, modulation factor or degree of modulation.

The absolute value of m multiplied by 100 is called as percentage modulation.

The modulation index is a number lying between 0 & 1.

Frequency Spectrum of AM:

AM is shown simply as consisting of three discrete frequencies.



LSB - Lower Side Band
USB - Upper Side Band

The central frequency i.e. the carrier has the highest amplitude & other two are having amplitudes which are equal to each other, but which can never exceed half the carrier amplitude.

$$V_m = m V_c$$

$$2V_m = V_{\max} - V_{\min}$$

$$\therefore V_m = \frac{V_{\max} - V_{\min}}{2}$$

$$V_c = \frac{V_{\max} - V_m}{2}$$

$$= V_{\max} - \frac{V_{\max} - V_{\min}}{2}$$

$$V_c = \frac{V_{\max} + V_{\min}}{2}$$

$$m = \frac{V_m}{V_c} = \frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}}$$

$$V_m = m V_c \sin \omega_m t$$

$$A = V_c + V_m$$

$$= V_c (1 + m \sin \omega_m t)$$

Instantaneous voltage of resulting AM wave is

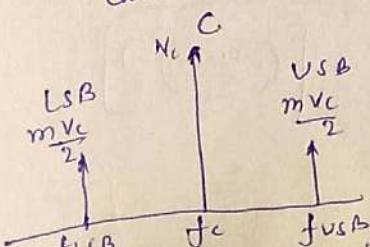
$$V = V_c \sin \omega_c t + m V_c (\sin \omega_m t \cdot \sin \omega_c t)$$

$$V = V_c \sin \omega_c t + \frac{m V_c}{2} \cos(\omega_c - \omega_m)t - \frac{m V_c}{2} \cos(\omega_c + \omega_m)t$$

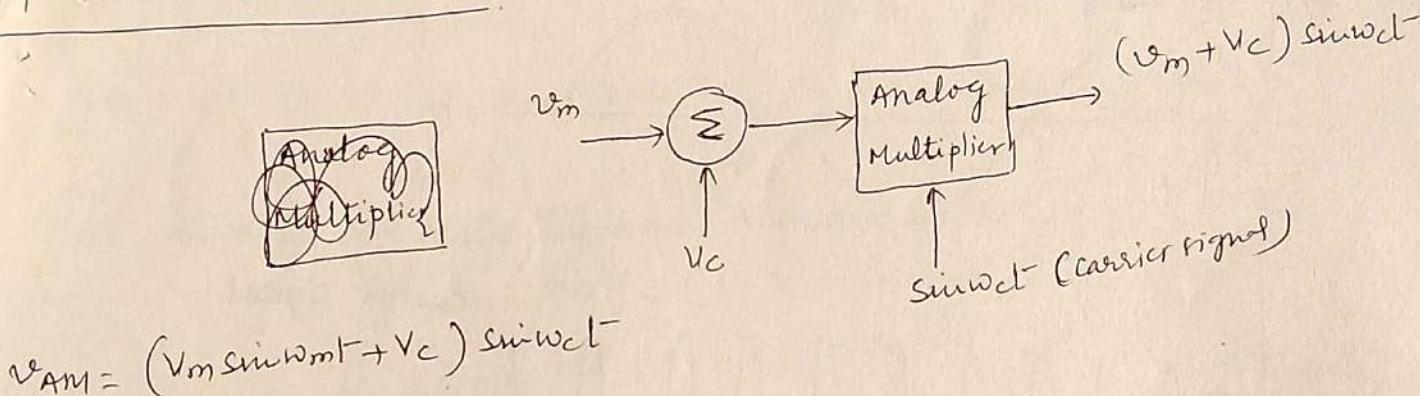
Carrier Lower Side Band Upper Side Band

$$\begin{aligned} BW &= f_{USB} - f_{LSB} \\ &= f_{c+fm} - f_{c-fm} \\ &= 2fm \end{aligned}$$

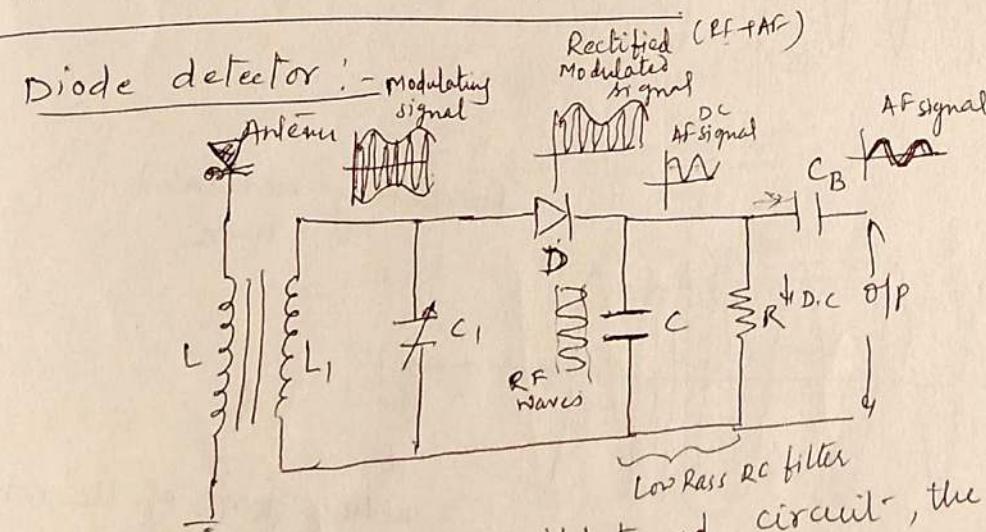
BW required for AM is twice the frequency of



AM Modulation Technique:-



AM Demodulation Technique:-



With the help of this parallel tuned circuit, the modulated wave of desired frequency may be selected.

Frequency Modulation:-

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