



PAPER ID-311295

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Subject Code: BOE310

Roll No:

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BTECH
(SEM III) THEORY EXAMINATION 2023-24
DIGITAL ELECTRONICS

TIME: 3HRS

M.MARKS: 70

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt all questions in brief.

Q no.	Question	2 x 7 = 14	Marks	CO
a.	What is the difference between binary, decimal, and hexadecimal number systems?	2	1	
b.	What is a don't-care condition in Karnaugh maps?	2	1	
c.	Explain the function of a magnitude comparator.	2	2	
d.	Differentiate between synchronous and asynchronous counters.	2	3	
e.	Explain the concept of a ring counter.	2	3	
f.	What are the advantages of synchronous counters over asynchronous counters?	2	4	
g.	Differentiate between RAM and ROM.	2	5	

SECTION B

2. Attempt any three of the following:

Q no.	Question	7 x 3 = 21	Marks	CO
a.	Explain the SOP and POS forms in Boolean algebra. How are they derived?	7	1	
b.	Describe the operation of half and full adders. Provide truth tables and circuit diagrams.	7	2	
c.	Define storage elements and discuss the characteristics of latches and flip-flops.	7	3	
d.	Explain the concept of hazards in digital circuits and methods to eliminate them.	7	4	
e.	Compare and contrast different digital logic families such as DTL, DCTL, TTL, ECL, and CMOS in terms of their characteristics.	7	5	

SECTION C

3. Attempt any one part of the following:

Q no.	Question	7 x 1 = 7	Marks	CO
a.	Minimize the Boolean function $F(A, B, C, D) = \Sigma(0, 1, 2, 4, 6, 7, 9, 12, 14)$ using the Karnaugh map method.	7	1	
b.	Implement the Boolean function $F = AB + AC + BC$ using only NAND gates.	7	1	

4. Attempt any one part of the following:

Q no.	Question	7 x 1 = 7	Marks	CO
a.	Discuss the operation of BCD adders and their significance.	7	2	
b.	Implement a 4-to-1 multiplexer using basic logic gates.	7	2	

5. Attempt any one part of the following:

Q no.	Question	7 x 1 = 7	Marks	CO
a.	Explain the concept of ripple counters and synchronous counters.	7	3	
b.	Convert a JK flip-flop to a T flip-flop and demonstrate its operation with characteristic equations.	7	3	



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TIME: 3HRS**M.MARKS: 70****6. Attempt any one part of the following:****7 x 1 = 7**

a.	Describe the process of state reduction and assignments in sequential circuit design.	7	4
b.	Discuss the concept of race-free state assignment and how it is achieved.	7	4

7. Attempt any one part of the following:**7 x 1 = 7**

a.	Describe the working principles of PLA and PAL and their applications.	7	5
b.	Explain the concepts of fan-out, fan-in, and noise margin in digital circuits.	7	5