```
-- megafunction wizard: %RAM: 1-PORT%
-- GENERATION: STANDARD
-- VERSION: WM1.0
-- MODULE: altsyncram

-- ============================================================
-- File Name: ram.vhd
-- Megafunction Name(s):
--          altsyncram
--
-- Simulation Library Files(s):
--          altera_mf
-- ============================================================
-- ************************************************************
-- THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
--
-- 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
-- ************************************************************


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--applicable agreement for further details.


LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY altera_mf;
USE altera_mf.all;

ENTITY ram_n IS
   PORT
   (
      address     : IN STD_LOGIC_VECTOR (8 DOWNTO 0);
      clock    : IN STD_LOGIC  := '1';
      data     : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
      rden     : IN STD_LOGIC  := '1';
      wren     : IN STD_LOGIC ;
      q     : OUT STD_LOGIC_VECTOR (31 DOWNTO 0)
   );
END ram_n;


ARCHITECTURE SYN OF ram_n IS

   SIGNAL sub_wire0  : STD_LOGIC_VECTOR (31 DOWNTO 0);



   COMPONENT altsyncram
   GENERIC (
      clock_enable_input_a    : STRING;
      clock_enable_output_a      : STRING;
      intended_device_family     : STRING;
      lpm_hint    : STRING;
      lpm_type    : STRING;
      numwords_a     : NATURAL;
      operation_mode    : STRING;
      outdata_aclr_a    : STRING;
      outdata_reg_a     : STRING;
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72          power up uninitialized     : STRING;
73          read_during_write_mode_port_a    : STRING;
74          widthad a       : NATURAL;
75          width_a     : NATURAL;
76          width byteena a      : NATURAL
77       );
78       PORT (
79             address_a    : IN STD_LOGIC_VECTOR (8 DOWNTO 0);
80             clock0    : IN STD_LOGIC ;
81             data_a    : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
82             wren_a    : IN STD_LOGIC ;
83             q_a    : OUT STD_LOGIC_VECTOR (31 DOWNTO 0);
84             rden_a    : IN STD_LOGIC
85       );
86       END COMPONENT;
87
88    BEGIN
89       q    <= sub_wire0(31 DOWNTO 0);
90
91       altsyncram_component : altsyncram
92       GENERIC MAP (
93          clock_enable_input_a => "BYPASS",
94          clock_enable_output_a => "BYPASS",
95          intended_device_family => "Cyclone III",
96          lpm_hint => "ENABLE_RUNTIME_MOD=NO",
97          lpm_type => "altsyncram",
98          numwords_a => 512,
99          operation_mode => "SINGLE_PORT",
100         outdata_aclr_a => "NONE",
101         outdata_reg_a => "CLOCK0",
102         power_up_uninitialized => "FALSE",
103         read_during_write_mode_port_a => "NEW_DATA_NO_NBE_READ",
104         widthad_a => 9,
105         width_a => 32,
106         width_byteena_a => 1
107      )
108      PORT MAP (
109         address_a => address,
110         clock0 => clock,
111         data_a => data,
112         wren_a => wren,
113         rden_a => rden,
114         q_a => sub_wire0
115      );
116
117
118
119   END SYN;
120
121   -- ============================================================
122   -- CNX file retrieval info
123   -- ============================================================
124   -- Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
125   -- Retrieval info: PRIVATE: AclrAddr NUMERIC "0"
126   -- Retrieval info: PRIVATE: AclrByte NUMERIC "0"
127   -- Retrieval info: PRIVATE: AclrData NUMERIC "0"
128   -- Retrieval info: PRIVATE: AclrOutput NUMERIC "0"
129   -- Retrieval info: PRIVATE: BYTE_ENABLE NUMERIC "0"
130   -- Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
131   -- Retrieval info: PRIVATE: BlankMemory NUMERIC "1"
132   -- Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
133   -- Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "0"
134   -- Retrieval info: PRIVATE: Clken NUMERIC "0"
135   -- Retrieval info: PRIVATE: DataBusSeparated NUMERIC "1"
136   -- Retrieval info: PRIVATE: IMPLEMENT_IN_LES NUMERIC "0"
137   -- Retrieval info: PRIVATE: INIT_FILE_LAYOUT STRING "PORT_A"
138   -- Retrieval info: PRIVATE: INIT_TO_SIM_X NUMERIC "0"
139   -- Retrieval info: PRIVATE: INTENDED_DEVICE_FAMILY STRING "Cyclone III"
140   -- Retrieval info: PRIVATE: JTAG_ENABLED NUMERIC "0"
141   -- Retrieval info: PRIVATE: JTAG_ID STRING "NONE"
142   -- Retrieval info: PRIVATE: MAXIMUM_DEPTH NUMERIC "0"
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143   -- Retrieval info: PRIVATE: MIFfilename STRING ""
144   -- Retrieval info: PRIVATE: NUMWORDS_A NUMERIC "512"
145   -- Retrieval info: PRIVATE: RAM BLOCK TYPE NUMERIC "0"
146   -- Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_PORT_A NUMERIC "3"
147   -- Retrieval info: PRIVATE: RegAddr NUMERIC "1"
148   -- Retrieval info: PRIVATE: RegData NUMERIC "1"
149   -- Retrieval info: PRIVATE: RegOutput NUMERIC "1"
150   -- Retrieval info: PRIVATE: SYNTH_WRAPPER_GEN_POSTFIX STRING "0"
151   -- Retrieval info: PRIVATE: SingleClock NUMERIC "1"
152   -- Retrieval info: PRIVATE: UseDQRAM NUMERIC "1"
153   -- Retrieval info: PRIVATE: WRCONTROL_ACLR_A NUMERIC "0"
154   -- Retrieval info: PRIVATE: WidthAddr NUMERIC "9"
155   -- Retrieval info: PRIVATE: WidthData NUMERIC "32"
156   -- Retrieval info: PRIVATE: rden NUMERIC "1"
157   -- Retrieval info: LIBRARY: altera_mf altera_mf.altera_mf_components.all
158   -- Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_A STRING "BYPASS"
159   -- Retrieval info: CONSTANT: CLOCK_ENABLE_OUTPUT_A STRING "BYPASS"
160   -- Retrieval info: CONSTANT: INTENDED_DEVICE_FAMILY STRING "Cyclone III"
161   -- Retrieval info: CONSTANT: LPM_HINT STRING "ENABLE_RUNTIME_MOD=NO"
162   -- Retrieval info: CONSTANT: LPM_TYPE STRING "altsyncram"
163   -- Retrieval info: CONSTANT: NUMWORDS_A NUMERIC "512"
164   -- Retrieval info: CONSTANT: OPERATION_MODE STRING "SINGLE_PORT"
165   -- Retrieval info: CONSTANT: OUTDATA_ACLR_A STRING "NONE"
166   -- Retrieval info: CONSTANT: OUTDATA_REG_A STRING "CLOCK0"
167   -- Retrieval info: CONSTANT: POWER_UP_UNINITIALIZED STRING "FALSE"
168   -- Retrieval info: CONSTANT: READ_DURING_WRITE_MODE_PORT_A STRING "NEW_DATA_NO_NBE_READ"
169   -- Retrieval info: CONSTANT: WIDTHAD_A NUMERIC "9"
170   -- Retrieval info: CONSTANT: WIDTH_A NUMERIC "32"
171   -- Retrieval info: CONSTANT: WIDTH_BYTEENA_A NUMERIC "1"
172   -- Retrieval info: USED_PORT: address 0 0 9 0 INPUT NODEFVAL "address[8..0]"
173   -- Retrieval info: USED_PORT: clock 0 0 0 0 INPUT VCC "clock"
174   -- Retrieval info: USED_PORT: data 0 0 32 0 INPUT NODEFVAL "data[31..0]"
175   -- Retrieval info: USED_PORT: q 0 0 32 0 OUTPUT NODEFVAL "q[31..0]"
176   -- Retrieval info: USED_PORT: rden 0 0 0 0 INPUT VCC "rden"
177   -- Retrieval info: USED_PORT: wren 0 0 0 0 INPUT NODEFVAL "wren"
178   -- Retrieval info: CONNECT: @address_a 0 0 9 0 address 0 0 9 0
179   -- Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0
180   -- Retrieval info: CONNECT: @data_a 0 0 32 0 data 0 0 32 0
181   -- Retrieval info: CONNECT: @rden_a 0 0 0 0 rden 0 0 0 0
182   -- Retrieval info: CONNECT: @wren_a 0 0 0 0 wren 0 0 0 0
183   -- Retrieval info: CONNECT: q 0 0 32 0 @q_a 0 0 32 0
184   -- Retrieval info: GEN_FILE: TYPE_NORMAL ram.vhd TRUE
185   -- Retrieval info: GEN_FILE: TYPE_NORMAL ram.inc FALSE
186   -- Retrieval info: GEN_FILE: TYPE_NORMAL ram.cmp TRUE
187   -- Retrieval info: GEN_FILE: TYPE_NORMAL ram.bsf FALSE
188   -- Retrieval info: GEN_FILE: TYPE_NORMAL ram_inst.vhd FALSE
189   -- Retrieval info: LIB_FILE: altera_mf
190
```