```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   library work;
5
6   entity reg_IR_tb is
7   end;
8
9   architecture behaviour of reg IR tb is
10
11  signal clk tb, clr tb, Rin tb    : std logic;
12  signal BusMuxIn_tb, BusMuxOut_tb : std_logic_vector(31 downto 0);
13
14  component reg_IR IS
15     PORT(
16        clk, clr, Rin : IN STD_LOGIC;
17        BusMuxOut : IN STD LOGIC VECTOR(31 DOWNTO 0);
18        BusMuxIn : OUT STD_LOGIC_VECTOR(31 DOWNTO 0)
19        );
20  END component reg_IR;
21
22
23  begin
24     DUT1 : reg_IR port map(
25        clk   => clk tb,
26        clr   => clr_tb,
27        Rin   => Rin tb,
28        BusMuxOut => BusMuxOut_tb,
29        BusMuxIn => BusMuxIn tb
30     );
31
32     sim_process: process
33     begin
34
35        wait for 1 ns;
36        clk_tb      <= '1';
37        clr tb      <= '0';
38        Rin_tb      <= '1';
39        BusMuxOut tb<= x"07ff0000";
40        clr_tb      <= '1';
41        wait for 9 ns;
42        clk_tb      <= '0';
43        wait for 10 ns;
44        clk_tb      <= '1';
45        BusMuxOut tb<= x"07fff000";
46        wait for 10 ns;
47        wait;
48     end process sim_process;
49  end behaviour;
```