```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3
 4  entity conFF is
 5     port(
 6        clk                              : in std_logic;
 7        IRout                            : in std_logic_vector(31 downto 0);
 8        BusMuxOut                        : in std_logic_vector(31 downto 0);
 9        CONout                           : out std_logic
10     );
11  end entity;
12
13  architecture behaviour of conFF is
14
15  component decoder4bits is
16     port (
17        input  : IN STD_LOGIC_VECTOR (1 DOWNTO 0);
18        output : OUT STD_LOGIC_VECTOR(3 downto 0)
19     );
20  end component;
21
22  component conFFSubComponent1 is
23     port(
24        decoderOutput                    : in std_logic_vector(3 downto 0);
25        BusMuxOut                        : in std_logic_vector(31 downto 0);
26        conFFOutput                      : out std_logic;
27        busOrOut                         : inout std_logic
28     );
29  end component;
30
31  component flipFlop is
32     port(
33        clk         : in std_logic;
34        D           : in std_logic;
35        Q           : out std_logic
36     );
37  end component;
38
39  signal decoderInput  : std_logic_vector(1 downto 0);
40  signal decoderOutput : std_logic_vector(3 downto 0);
41  signal orGateToFlipFlop, conFFOutput, busOrOutInternal   : std_logic;
42
43  begin
44  decoderInput <= IRout(20 downto 19);
45
46  U0: decoder4bits port map(
47        input  => decoderInput,
48        output => decoderOutput
49  );
50
51  U1: conFFSubComponent1 port map(
52        decoderOutput => decoderOutput,
53        BusMuxOut => BusMuxOut,
54        conFFOutput => orGateToFlipFlop,
55        busOrOut => busOrOutInternal
56  );
57
58  U2: flipFlop port map(
59        clk => clk,
60        D => orGateToFlipFlop,
61        Q => CONout
62  );
63  end architecture;
```