```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   library work;
5
6   entity reg_Zero_tb is
7   end;
8
9   architecture behaviour of reg Zero tb is
10
11  signal clk tb, clr tb   : std logic;
12  signal Rin_tb, BAout_tb : std_logic;
13  signal BusMuxOut tb     : std logic vector(31 downto 0);
14  signal BusMuxIn_tb      : std_logic_vector(31 downto 0);
15
16  component reg_Zero IS
17     PORT(
18        clk, clr, Rin, BAout : IN STD_LOGIC;
19        BusMuxOut : IN STD LOGIC VECTOR(31 DOWNTO 0);
20        BusMuxIn : OUT STD_LOGIC_VECTOR(31 DOWNTO 0)
21        );
22  END component;
23
24  begin
25     DUT1 : reg Zero port map(
26        clk   => clk_tb,
27        clr   => clr tb,
28        Rin   => Rin_tb,
29        BAout => BAout tb,
30        BusMuxOut => BusMuxOut_tb,
31        BusMuxIn  => BusMuxIn tb
32     );
33
34     sim_process: process
35     begin
36        clk_tb <= '0';
37        wait for 1 ns;
38        BusMuxOut_tb <= x"07ff8000";
39        clk tb <= '1';
40        clr_tb <= '0';
41        Rin tb <= '1';
42        BAout_tb <= '1';
43        BusMuxOut tb <= x"ffff0000";
44        wait for 9 ns;
45        clk tb <= '0';
46        BAout_tb <= '1';
47        BusMuxOut tb <= x"07fb8000";
48        wait for 10 ns;
49        clk tb <= '1';
50        wait for 10 ns;
51        BAout tb <= '1';
52        wait;
53     end process sim process;
54  end behaviour;
55
```