```
1   LIBRARY ieee  ;
2   LIBRARY std  ;
3   USE ieee.std_logic_1164.all  ;
4   USE ieee.std_logic_textio.all  ;
5   USE ieee.std_logic_unsigned.all  ;
6   USE std.textio.all  ;
7   ENTITY RegistersTB  IS
8   END ;
9
10  ARCHITECTURE RegistersTB_arch OF RegistersTB IS
11    SIGNAL BusMuxIn14   :  std_logic_vector (31 downto 0)  ;
12    SIGNAL BusMuxIn5   :  std_logic_vector (31 downto 0)  ;
13    SIGNAL BusMuxIn15   :  std_logic_vector (31 downto 0)  ;
14    SIGNAL Rin   :  std_logic_vector (15 downto 0)  ;
15    SIGNAL clr   :  STD_LOGIC  ;
16    SIGNAL BusMuxIn6   :  std_logic_vector (31 downto 0)  ;
17    SIGNAL BusMuxIn7   :  std_logic_vector (31 downto 0)  ;
18    SIGNAL BusMuxIn8   :  std_logic_vector (31 downto 0)  ;
19    SIGNAL BusMuxIn9   :  std_logic_vector (31 downto 0)  ;
20    SIGNAL BusMuxOut   :  std_logic_vector (31 downto 0)  ;
21    SIGNAL clk   :  STD_LOGIC  ;
22    SIGNAL BusMuxIn0   :  std_logic_vector (31 downto 0)  ;
23    SIGNAL BusMuxIn10   :  std_logic_vector (31 downto 0)  ;
24    SIGNAL BusMuxIn1   :  std_logic_vector (31 downto 0)  ;
25    SIGNAL BusMuxIn11   :  std_logic_vector (31 downto 0)  ;
26    SIGNAL BusMuxIn2   :  std_logic_vector (31 downto 0)  ;
27    SIGNAL BusMuxIn12   :  std_logic_vector (31 downto 0)  ;
28    SIGNAL BusMuxIn3   :  std_logic_vector (31 downto 0)  ;
29    SIGNAL BusMuxIn13   :  std_logic_vector (31 downto 0)  ;
30    SIGNAL BusMuxIn4   :  std_logic_vector (31 downto 0)  ;
31    COMPONENT Registers
32      PORT (
33        BusMuxIn14  : out std_logic_vector (31 downto 0) ;
34        BusMuxIn5  : out std_logic_vector (31 downto 0) ;
35        BusMuxIn15  : out std_logic_vector (31 downto 0) ;
36        Rin  : in std_logic_vector (15 downto 0) ;
37        clr  : in STD_LOGIC ;
38        BusMuxIn6  : out std_logic_vector (31 downto 0) ;
39        BusMuxIn7  : out std_logic_vector (31 downto 0) ;
40        BusMuxIn8  : out std_logic_vector (31 downto 0) ;
41        BusMuxIn9  : out std_logic_vector (31 downto 0) ;
42        BusMuxOut  : in std_logic_vector (31 downto 0) ;
43        clk  : in STD_LOGIC ;
44        BusMuxIn0  : out std_logic_vector (31 downto 0) ;
45        BusMuxIn10  : out std_logic_vector (31 downto 0) ;
46        BusMuxIn1  : out std_logic_vector (31 downto 0) ;
47        BusMuxIn11  : out std_logic_vector (31 downto 0) ;
48        BusMuxIn2  : out std_logic_vector (31 downto 0) ;
49        BusMuxIn12  : out std_logic_vector (31 downto 0) ;
50        BusMuxIn3  : out std_logic_vector (31 downto 0) ;
51        BusMuxIn13  : out std_logic_vector (31 downto 0) ;
52        BusMuxIn4  : out std_logic_vector (31 downto 0) );
53    END COMPONENT ;
54  BEGIN
55    DUT  : Registers
56      PORT MAP (
57        BusMuxIn14   => BusMuxIn14  ,
58        BusMuxIn5   => BusMuxIn5  ,
59        BusMuxIn15   => BusMuxIn15  ,
60        Rin   => Rin  ,
61        clr   => clr  ,
62        BusMuxIn6   => BusMuxIn6  ,
```

```
63          BusMuxIn7    => BusMuxIn7   ,
64          BusMuxIn8    => BusMuxIn8   ,
65          BusMuxIn9    => BusMuxIn9   ,
66          BusMuxOut    => BusMuxOut   ,
67          clk    => clk   ,
68          BusMuxIn0    => BusMuxIn0   ,
69          BusMuxIn10    => BusMuxIn10   ,
70          BusMuxIn1    => BusMuxIn1   ,
71          BusMuxIn11    => BusMuxIn11   ,
72          BusMuxIn2    => BusMuxIn2   ,
73          BusMuxIn12    => BusMuxIn12   ,
74          BusMuxIn3    => BusMuxIn3   ,
75          BusMuxIn13    => BusMuxIn13   ,
76          BusMuxIn4    => BusMuxIn4    ) ;
77
78
79
80    -- "Constant Pattern"
81    -- Start Time = 0 ns, End Time = 2 us, Period = 0 ns
82      Process
83       Begin
84        clr  <= '1'  ;
85       wait for 2 us ;
86    -- dumped values till 2 us
87       wait;
88     End Process;
89
90       Process
91       Begin
92        BusMuxOut  <= "10101010101010101010101010101010"  ;
93       wait for 2 us ;
94    -- dumped values till 2 us
95       wait;
96     End Process;
97
98    -- "Clock Pattern" : dutyCycle = 50
99    -- Start Time = 0 ns, End Time = 2 us, Period = 100 ns
100     Process
101      Begin
102       clk  <= '0'  ;
103      wait for 50 ns ;
104   -- 50 ns, single loop till start period.
105      for Z in 1 to 19
106      loop
107          clk  <= '1'  ;
108         wait for 50 ns ;
109          clk  <= '0'  ;
110         wait for 50 ns ;
111   -- 1950 ns, repeat pattern in loop.
112      end  loop;
113       clk  <= '1'  ;
114      wait for 50 ns ;
115   -- dumped values till 2 us
116      wait;
117    End Process;
118
119      Process
120      Begin
121         Rin  <= "0000000000000001";
122      wait for 100 ns ;
123         Rin  <= "0000000000000010";
124      wait for 100 ns ;
```

```
125         Rin  <= "0000000000000100";
126      wait for 100 ns ;
127         Rin  <= "0000000000001000";
128      wait for 100 ns ;
129         Rin  <= "0000000000010000";
130      wait for 100 ns ;
131         Rin  <= "0000000000100000";
132      wait for 100 ns ;
133         Rin  <= "0000000001000000";
134      wait for 100 ns ;
135         Rin  <= "0000000010000000";
136      wait for 100 ns ;
137         Rin  <= "0000000100000000";
138      wait for 100 ns ;
139         Rin  <= "0000001000000000";
140      wait for 100 ns ;
141         Rin  <= "0000010000000000";
142      wait for 100 ns ;
143         Rin  <= "0000100000000000";
144      wait for 100 ns ;
145         Rin  <= "0001000000000000";
146      wait for 100 ns ;
147         Rin  <= "0010000000000000";
148      wait for 100 ns ;
149         Rin  <= "0100000000000000";
150      wait for 100 ns ;
151         Rin  <= "1000000000000000";
152      wait for 100 ns ;
153
154   -- dumped values till 2 us
155      wait;
156    End Process;
157
158
159   END;
160
```