```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.ALL;
3
4   ENTITY reg_Zero IS
5      PORT(
6         clk, clr, Rin, BAout : IN STD_LOGIC;
7         BusMuxOut : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
8         BusMuxIn : OUT STD_LOGIC_VECTOR(31 DOWNTO 0)
9         );
10  END ENTITY reg_Zero;
11
12  architecture behaviour of reg_Zero is
13
14  signal regToAnd : std_logic_vector(31 downto 0);
15
16  component reg_32 IS
17     PORT(
18        clk, clr, Rin : IN STD_LOGIC;
19        BusMuxOut : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
20        BusMuxIn : OUT STD_LOGIC_VECTOR(31 DOWNTO 0)
21        );
22  END component;
23
24  component andGate_32vs1 is
25     port(
26        A     : in std_logic;
27        B     : in std_logic_vector(31 downto 0);
28        S     : out std_logic_vector(31 downto 0)
29     );
30  end component;
31
32  begin
33  U0: reg_32 port map(
34     clk => clk,
35     clr => clr,
36     Rin => Rin,
37     BusMuxOut => BusMuxOut,
38     BusMuxIn => regToAnd
39  );
40  U1: andGate_32vs1 port map(
41     A => BAout,
42     B => regToAnd,
43     S => BusMuxIn
44  );
45
46  end architecture;
```