```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.ALL;
3
4   ENTITY reg_IR IS
5      PORT(
6         clk, clr, Rin : IN STD_LOGIC;
7         BusMuxOut : IN STD LOGIC VECTOR(31 DOWNTO 0);
8         BusMuxIn : OUT STD_LOGIC_VECTOR(31 DOWNTO 0)
9         );
10  END ENTITY reg_IR;
11
12  ARCHITECTURE arc OF reg_IR IS
13  BEGIN
14     SingleRegister:
15     PROCESS (clk, clr, Rin, BusMuxOut)
16     BEGIN
17        IF (rising edge(clk) AND (Rin = '1')) THEN
18           IF (clr = '0') THEN
19              BusMuxIn <= (others => '0' );
20           ELSIF(clr = '1' and BusMuxOut(18) = '1') THEN
21              BusMuxIn(17 downto 0) <= BusMuxOut(17 downto 0);
22              BusMuxIn(31 downto 18) <= "11111111111111";
23           ELSE
24              BusMuxIn(17 downto 0) <= BusMuxOut(17 downto 0);
25              BusMuxIn(31 downto 18) <= "00000000000000";
26           END IF;
27        END IF;
28     END PROCESS;
29  END ARCHITECTURE arc;
30
```