

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity selectAndEncodeLogic is
5      port(
6          IRin                : in std_logic_vector(31 downto 0);
7          Gra, Grb, Grc, Rin, Rout, BAout : in std_logic;
8          BusMuxOut           : in std_logic_vector(31 downto 0);
9          C sign extended     : out std_logic_vector(31 downto 0);
10         r0in_r15in_Decoded    : out std_logic_vector(15 downto 0);
11         r0out_r15out_Decoded  : out std_logic_vector(15 downto 0)
12     );
13 end entity;
14
15 architecture behaviour of selectAndEncodeLogic is
16
17     component selectAndEncodeSubComponent1 is
18         port(
19             IRin                : in std_logic_vector(31 downto 0);
20             Gra, Grb, Grc       : in std_logic;
21             output              : out std_logic_vector(3 downto 0)
22         );
23     end component;
24     component selectAndEncodeSubComponent2 is
25         port(
26             input               : in std_logic_vector(15 downto 0);
27             Rin, Rout, BAout    : in std_logic;
28             r0in_r15in_Decoded : out std_logic_vector(15 downto 0);
29             r0out_r15out_Decoded : out std_logic_vector(15 downto 0)
30         );
31     end component;
32     component selectAndEncodeSubComponent3 is
33         port(
34             input               : in std_logic_vector(31 downto 0);
35             output              : out std_logic_vector(31 downto 0)
36         );
37     end component;
38     component decoder16bits is
39         port (
40             input  : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
41             output : OUT STD_LOGIC_VECTOR(15 downto 0)
42         );
43     end component;
44
45     signal decoderInput  : std_logic_vector(3 downto 0);
46     signal decoderOutput : std_logic_vector(15 downto 0);
47
48 begin
49
50     U0: selectAndEncodeSubComponent1 port map(
51         IRin  => IRin,
52         Gra   => Gra,
53         Grb   => Grb,
54         Grc   => Grc,
55         output=> decoderInput
56     );
57
58     U1: decoder16bits port map(
59         input  => decoderInput,
60         output => decoderOutput
61     );
62
63     U2: selectAndEncodeSubComponent2 port map(
64         input      => decoderOutput,
65         Rin        => Rin,
66         Rout       => Rout,
67         BAout      => BAout,
68         r0in_r15in_Decoded => r0in_r15in_Decoded,
69         r0out_r15out_Decoded => r0out_r15out_Decoded
70     );
71     U3: selectAndEncodeSubComponent3 port map(

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```
72         input => IRin,  
73         output => C_sign_extended  
74     );  
75 end architecture;  
76  
77  
78 --CONFIRMED TO WORK
```