```
1   --CONFIRMED TO WORK
2
3   library ieee;
4   use ieee.std_logic_1164.all;
5
6   library work;
7
8   entity memorySubsystem_tb is
9   end;
10
11  architecture behaviour of memorySubsystem tb is
12
13  signal BusMuxOut tb, BusMuxInMDR tb       : std logic vector(31 downto 0);
14  signal MDRin_tb, MARin_tb, clock_tb, clear_tb, mdrReadSig_tb, readSig_tb, writeSig_tb  :
    std logic;
15
16  component memorySubsystem is
17     port(
18        BusMuxOut      : in std logic vector(31 downto 0);
19        BusMuxInMDR : inout std_logic_vector(31 downto 0);
20        MDRin, MARin, clock, clear: in std logic;
21        readSig, writeSig, mdrReadSig: in std_logic
22     );
23  end component;
24
25  begin
26     DUT1 : memorySubsystem port map(
27        BusMuxOut   => BusMuxOut_tb,
28        BusMuxInMDR => BusMuxInMDR tb,
29        MDRin => MDRin_tb,
30        MARin => MARin tb,
31        clock => clock_tb,
32        clear => clear tb,
33        readSig => readSig_tb,
34        writeSig => writeSig tb,
35        mdrReadSig => mdrReadSig_tb
36     );
37     clock_process: PROCESS
38     begin
39        clock_tb  <= '0';
40        wait for 5 ns;
41        clock_tb <= '1';
42        wait for 5 ns;
43     end process clock_process;
44     sim process: process
45     begin
46
47  --     BusMuxOut_tb <= x"00000000";
48  --Set up MDRMux, MDR and Data Line
49        BusMuxOut_tb <= x"ffff0000";
50        clear tb <='1';
51        mdrReadSig_tb  <='0';
52        MDRin tb       <='1';
53        readSig_tb     <='0';
54        writeSig tb    <='0';
55        MARin_tb       <='0';
56        wait on clock tb;
57        wait on clock_tb;
58        wait on clock tb;
59        wait on clock_tb;
60  --Set up Address in MAR
61        mdrReadSig_tb  <='1';
62        MDRin tb       <='0';
63        readSig_tb     <='0';
64        writeSig tb    <='0';
65        MARin_tb       <='1';
66        BusMuxOut tb <= x"00000001";
67        wait on clock_tb;
68        wait on clock tb;
69  --Write to Ram
70        mdrReadSig_tb  <='1';
```

```
71          MDRin_tb        <='0';
72          readSig_tb      <='0';
73          writeSig_tb     <='1';
74          MARin_tb        <='0';
75          wait on clock_tb;
76          wait on clock_tb;
77          wait on clock_tb;
78          wait on clock_tb;
79          wait on clock_tb;
80          wait on clock_tb;
81          writeSig_tb     <='0';
82          wait on clock_tb;
83          wait on clock_tb;
84    --Set dataLine to 0
85          BusMuxOut_tb <= x"00000000";
86          mdrReadSig_tb   <='0';
87          MDRin_tb        <='1';
88          readSig_tb      <='0';
89          writeSig_tb     <='0';
90          MARin_tb        <='0';
91          wait on clock_tb;
92          wait on clock_tb;
93    --Set up address in MAR
94          BusMuxOut_tb <= x"00000001";
95          mdrReadSig_tb   <='1';
96          MDRin_tb        <='0';
97          readSig_tb      <='0';
98          writeSig_tb     <='0';
99          MARin_tb        <='1';
100         wait on clock_tb;
101         wait on clock_tb;
102   --Read from RAM
103
104         mdrReadSig_tb   <='1';
105         MDRin_tb        <='0';
106         readSig_tb      <='1';
107         writeSig_tb     <='0';
108         MARin_tb        <='1';
109         wait on clock_tb;
110         wait on clock_tb;
111         wait on clock_tb;
112         wait on clock_tb;
113         wait on clock_tb;
114         wait on clock_tb;
115         wait;
116      end process sim_process;
117   end behaviour;
```