```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity ram_tb is
5   end;
6
7   architecture behaviour of ram tb is
8
9   signal address tb : std logic vector(8 downto 0);
10  signal clock_tb   : std_logic;
11  signal data tb    : std logic vector(31 downto 0);
12  signal rden_tb    : std_logic;
13  signal wren tb    : std logic;
14  signal q_tb          : std_logic_vector(31 downto 0);
15
16  component ram is
17     port(
18        address  : IN STD_LOGIC_VECTOR (8 DOWNTO 0);
19        clock    : IN STD LOGIC  := '1';
20        data     : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
21        rden     : IN STD LOGIC  := '1';
22        wren     : IN STD_LOGIC ;
23        q        : OUT STD LOGIC VECTOR (31 DOWNTO 0)
24     );
25  end component;
26
27  begin
28     DUT1 : ram port map(
29        address => address tb,
30        clock => clock_tb,
31        data => data tb,
32        rden => rden_tb,
33        wren => wren tb,
34        q => q_tb
35     );
36
37     sim process: process
38     begin
39
40        wait for 1 ns;
41        clock tb <= '0';
42        address_tb <= "000000001";
43        data tb <= x"0000ffff";
44        rden_tb <= '1';
45        wren tb <= '1';
46        wait for 9 ns;
47        clock tb <= '1';
48        wait for 10 ns;
49        clock tb <= '0';
50        wren_tb <= '0';
51        wait for 10 ns;
52        clock_tb <= '1';
53        address tb <= "000000001";
54        rden_tb <= '1';
55        wait;
56     end process sim_process;
57  end behaviour;
```