CS223 : Assignment 3, Date of Demonstration 9th February, Lab Timing (2PM-5PM), 12% (6%+ 6%) weight

Part I (Breadboard and IC part)

Demonstrate a functionality of **4 Bit ALU (in build ALU IC 74181)** using Breadboard, ICs and Hookup Wires. Use in build ALU IC. Use 7 Segment LEDs for showing both inputs and out put, DIP switches for extra inputs or control inputs. **Caution: don't connect 7 Segment LED without resistors.**

Part II (VHDL and FPGA)

Implement a **4 Bit ALU (similar to IC 74181)** using HDL (either VHDL or Verilog, preferred VHDL), synthesize and simulate your design entry. After that Download bit file of your design to FPGA board and demonstrate the working of your design on FPGA.

Grade will be based on Functionality, quality (less resources (LUTs, SR, DSP Slices), low delay/high frequency) of design.

Evaluation Procedure

All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please **show your ID card** at the time of demonstration (as it is difficult to remember faces of all the 90 students of your batch).

Grading will be based on (a) Correctness, (b) Quality of design, (c) Wire optimization, (d) Optimum number of chip used,(e) Cleanliness in design (Wire and Chips should be organized to look good), (f) Use of proper Comment/Naming/Labeling of the wires and (g) Questionnaire and explanation.

For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires), performance, comments, and questionnaire and explanation.