CS223 : Assignment 4, Date of Demonstration 23rd Feb 2018, Lab Timing (2PM-5PM), 14% (7%+ 7%) weight

Part I (Breadboard and IC part)

Design and Implement a 8 bit unsigned multiplier (using ICs and breadbard).

Reference: "***RTL design for Multiplier***", Chapter 8, Section 8.7 of "Digital Design" 4th Edition Book by M. Moris Mano. HDL code is almost provided, but need to use properly.
Reference: "***Multiplier Design***", Chapter 3, Section 3.3 of "Computer Organization and Design-ARM edition" by L. Henessy and D Paterson.
Reference: Algorithm discussed in http://jatinga.iitg.ernet.in/~asahu/cs221/Lects/Lec19.pdf and **Assignment is same as last year assignment :)** **http://jatinga.iitg.ernet.in/~asahu/cs223-2017/**

Assume both the inputs are unsigned 8 bit integer and produce a 16 bit unsigned integer output

- Use two 4 bit Adders/ALUs to do addition operations
- Use DIP switches for inputs
- Use combination of both SIPO and PISO to make full flegged universal shift register (8 bit)
- For multiplicant (A of AxB), you can use two 4 bit PIPO registers
- For controller you can use a mod 8/16 counter
- Combination of D-FFs/Latches can be used as register if necessary
- Display all the outputs in 7 Seg LEDs, except the carry out. If you are not getting sufficient number of Seven Segment LEDs then used LEDs of Breadboard for output. **Caution: don't connect 7 Segment LED without resistors.**

Part II (VHDL and FPGA)

Design and Implement a 8 bit unsigned multiplier using HDL (either VHDL or Verilog, preferred VHDL), synthesize and simulate your design entry. After that Download bit file of your design to FPGA board and demonstrate the working of your design on FPGA.

Grade will be based on Functionality, quality (less resources (LUTs, SR, DSP Slices), low delay/high frequency) of design.

Evaluation Procedure

All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please **show your ID card** at the time of demonstration (as it is difficult to remember faces of all the 90 students of your batch).

Grading will be based on (a) Correctness, (b) Quality of design, (c) Wire optimization, (d) Optimum number of chip used,(e) Cleanliness in design (Wire and Chips should be organized to look good), (f) Use of proper Comment/Naming/Labeling of the wires and (g) Questionnaire and explanation.

For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires), performance, comments, and questionnaire and explanation.