CS223 : Assignment 2, Date of Demonstration 25th Jan 2018 Thursday (with Friday Time Table), Lab Timing (2PM-5PM), 10% (5%+ 5%) weight

Part I (Breadboard and IC part)

Implement and Demonstrate a **4 Bit Binary Counter** using Breadboard, ICs and Hookup Wires. You are not allowed to use inbuilt counter ICs. Use FFs, Gates and other components to design your Counter. Use manual clock (using switches) or automatic clock available in the breadboard for demonstration purpose. Automatic clock have higher weight-age.
New additional information: any basic counter working demo will have 70% of marks, 30% of marks are for additional features (up-down counter, synchronous, present, clear, loading, etc) and optimization.

Part II (VHDL and FPGA)

Implement a **8 Bit Binary Counter** using HDL (either VHDL or Verilog, preferred VHDL), synthesize and simulate your design entry. After that Download bit file of your design to FPGA board and demonstrate the working of your design on FPGA.

Implement both behavioral model (using +, mod operations) and structural model (using FFs, Gates and interconnection) for your counter. Implement as many extra added features (preset, load, clock, clear) to your counter. Also try to use manual clock (using switches) or automatic clock available in the FPGA board (you may need to scale down to 1Hz). Automatic clock have higher weight-age.

Evaluation Procedure

All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please **show your ID card** at the time of demonstration (as it is difficult to remember faces of all the 90 students of your batch).

Grading will be based on (a) Correctness, (b) Quality of design, (c) Wire optimization, (d) Optimum number of chip used,(e) Cleanliness in design (Wire and Chips should be organized to look good), (f) Use of proper Comment/Naming/Labeling of the wires and (g) Questionnaire and explanation.

For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires), performance, comments, and questionnaire and explanation.