Review and Simulation - Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability

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***Abstract*—This paper focuses on the design of Three-Stage OTA which is designed to operate in Subthreshold region. This paper is designed for the development of ultra-low-power amplifiers drawing low voltage from supply and would require low area but has the capability to drive high capacitive loads. Moreover a slew rate enhancer circuit is used at the output stage for performing high speed applications given the constraint of low power.**

***Index Terms*—CMOS analog integrated circuits, low-power design, multistage amplifiers, OTA, subthreshold operation.**

I. INTRODUCTION

Most of the analog circuits faces a important task of minimizing the power consumption when designed for battery operated applications. For achieving an ultra-low-power demand, MOS transistors is biased in such a way that it operates in subthreshold region [1]. This methodology of working of the MOS in subthrehold for achieving low power demand is adopted since 1970s. The method is used more preferably when working for low power and low voltage operations. There are trade offs that comes into picture when proposing this subthreshold mechanism. As an example we are able to achieve low-power consumption, increased allowable signal swing, high transconductance efficiency as g_m is related exponentially to V_{gs}, but this comes at the cost of reduced bandwidth and large drain current mismatch. Also lower bandwidth is compensated by the high MOS transition frequency.

A technique wherein the bulk is used an input terminal is adopted for the devices operating in saturation. The method being extended to subthreshold region which meets our requirement of increased input swing. Drawback of this method is that bulk transconductance is lower than the gate transconductance. Even there are methods that use bulk of differential pair as a control terminal to set the current which eliminates the need of additional transistor that is used as a tail current source to set the current in the circuit.

Subthreshold region finds its application in wireless sensor networks, biomedical application and also finds its place where speed isn't a factor to be looked upon. For these reasons OTAs implemented in subthresold region driving from a 1V supply and current in order of few nano amperes finds its place.

Gain of the amplifier (Common source stage) working in subthreshold region depends on its technological parameter. Thus, the gain is independent of the aspect ratios of the transistors. Since, low voltage is provided, therefore a cascode topology cannot be adopted to increase the gain. Hence, a cascade of three stage is implemented to achieve the desired gain. Had this three stage network been not adopted the gain comes out to be around 70dB but by adopting this method gain comes to be higher than 100dB.

In this paper attempt has been made to meet the requirement of consuming low power, operated at low voltage and able to drive high capacitive loads. The paper implements a three-stage OTA with 0.35μm technology. It consumes ultra low power of 195nW drawing 1V from the supply. The output stage is able to drive capacitive loads upto 200pF. By achieving these targets, this shows a significant improvement among all earlier reported papers in this field. The paper is organized as follows. Section II,III and IV describe the Three-Stage OTA and design procedure for implementing it. Also looks at various concepts that needs to be attended before implementing. Simulation results till whatever possible is given in part V. Conclusion drawn from this is presented in part VI.

II. TWO-STAGE OTA

In order to dive into Three-stage OTA let's first visit Two-stage OTA and understand how it works. OTA consist of cascade of different stages(refer fig 2) [3]. At first we have voltage to current conversion stage also known as the transconductance stage followed by a current to voltage stage known as the load stage. The first stage consist to differential amplifier pair which converts the differential input applied to it to differential currents. This current is fed to the current mirror being used as a load which gives voltage as the output. The

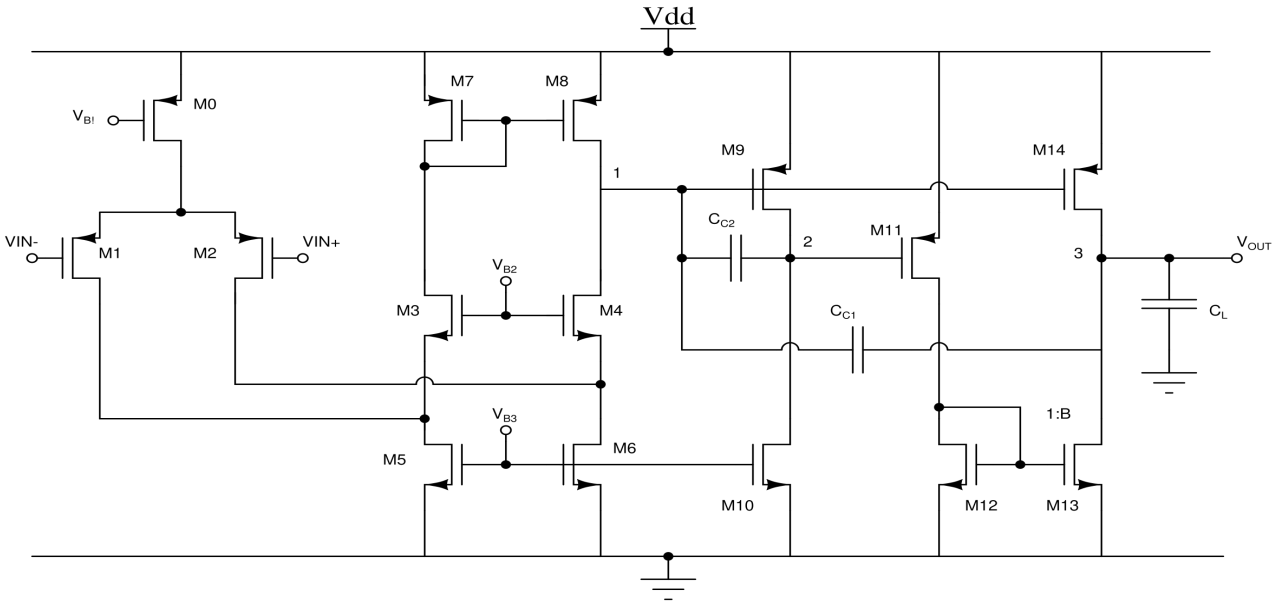

Fig. 1. Schematic of the amplifier

second stage then consist of a common source stage wherein M6 converts the gate voltage to the drain current. This current the drives the current sink load being connected at the output node. This was a brief description of two stage OTA let's now dive into Three-stage OTA.

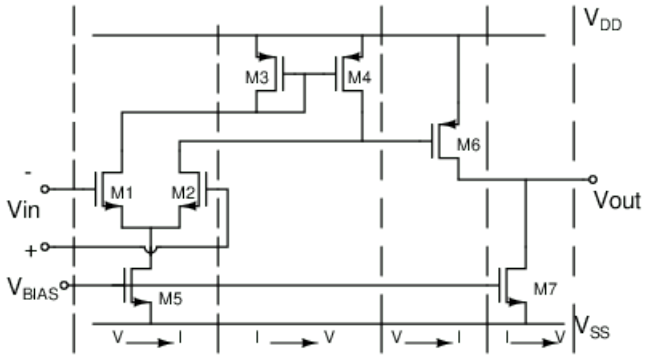

Fig. 2. Classical two stage CMOS OP AMP broken into Voltage to current and current to voltage stages

III. SUBTHRESHOLD THREE-STAGE OTA

The proposed circuit is broken down into three stages for observation. First stage consists of folded cascode amplifier. It consists of transistors M_1 to M_8. M_1 and M_2 forms a differential pair. Here PMOS is used as differential pair to extend the ICMR down to negative rail and to reduce the flicker noise. The differential current obtained from the differential pair is fed to current mirror comprising of M7 and M8. M_3 to M_6 pair is used to provide low signal swing at the output of the input stage.

As already discussed above the second stage comprises of the common source stage consisting of M_9 and M_{10}. Also we know that common source stage takes voltage as input and gives out current which is followed upon to the next stage.

The last non inverting stage is of a current buffer which is realized by the help of M_{11} - M_{14}. Please make a note that the gate of M_{14} is connected at the output first stage. This is done in order to implement a feed forward transconductance stage along with a class AB output stage capable of driving the load capacitance C_L.

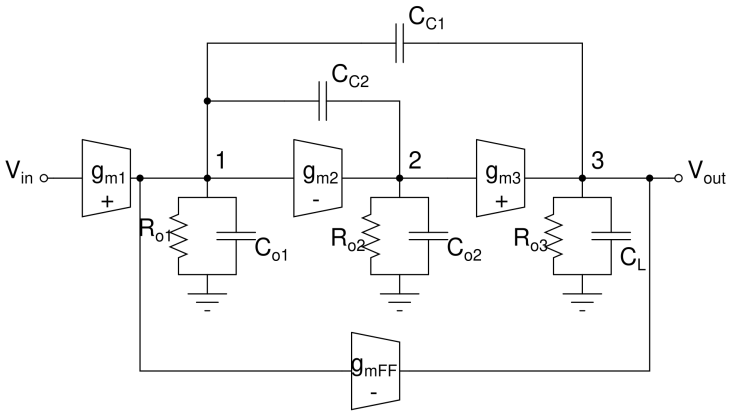

Fig. 3. Block diagram of the amplifier

Fig.3 represents the simplified block diagram of the schematic of three stage OTA depicted in fig.1. g_{mi}, r_{oi}, I_i and c_{oi} represents the i-th stage transconductance, resistance, current and equivalent output capacitance. g_{mFF} is the feed forward stage implemented by M_{14}. The Feed forward stage gives wider bandwidth in comparison to miller compensation technique and is even easier to stabilize. The current associated with first stage is I_1 and is equal to the drain current of M_0.

The first stage bias current I_{B1} is given by,

$$I_{B1} = I_{M0}(= I_1) + 2I_{M5,6} \tag{1}$$

where, I_{M0} is the bias current contribution of the differential input which includes the current through M1 and M2. I_{M5} is the current contributed by the folded section and it includes the current through M5. A similar fashion adopted for M6. Since M5 and M6 are matched so twice of the current flowing through M5 is taken into account. The current of the second stage is given by,

$$I_{B2} = I_{M10} = I_2 \tag{2}$$

The current through the last stage is given by,

$$I_{B3} = I_{M12} + IM13 = (1 + \beta)I_3 \tag{3}$$

where I_3 is the current assumed through M12 and due to current mirroring $1/\beta$ I_3 is the current flowing through M13.

A. Frequency compensation technique

A proper frequency compensation technique needs to be realized for having adequate stability margins.There are several ways to attain this but two of them are most popularly used. Nested Miller (NM) compensation technique and Reverse Nested Miller(RNM) compensation technique. Both of these aim to keep one dominant pole near to the origin and the other one as far apart as it could be. This phenomenon is known as pole splitting.This can be illustrated by the following.Consider small signal model of the circuit shown in fig.5 without the miller capacitance. The pole locations are given by

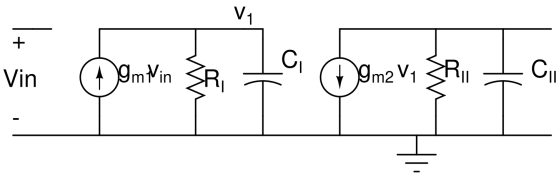

Fig. 4. Small signal model of uncompensated OTA

$$P_I = \frac{-1}{R_I C_I} \& P_{II} = \frac{-1}{R_{II} C_{II}} \tag{4}$$

where R_I = r_{o2} || r_{o4} , $R_I I$ = r_{o6} || r_{o7} , C_I = C_{DB4} + C_{DB2} + C_{SG6} and C_{II} = C_L. Refer fig.2. Now, after adopting miller compensation the poles are given by,

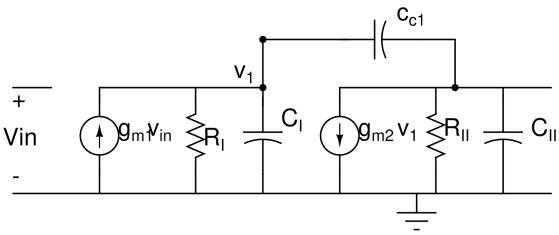

Fig. 5. Small signal model of compensated OTA

$$P_I = \frac{-1}{R_I R_{II} g m_{II} C_c} \& P_{II} = \frac{-g m_{II}}{C_{II}} \tag{5}$$

where, each notation values are same as previous and gm_{II} is equal to the transconductance of M1 or M2. From equations it can be seen that the value of P_I in compensated technique is decreased and it moves towards origin whereas the value of P_{II} is increased as the effect of gm_{II} dominates in comparison to C_{II}. $\therefore$ P_{II} moves away from the origin. Hence known as pole splitting. The advantage of this phenomenon is that desired phase margin and settling time can be achieved.

A reverse nested miller topology consist of capacitors connected from the output of first stage to the output of following stages. Finally, it can be shown that RNMC topologies finds inherent bandwidth potential over NMC topology. For having an improved bandwidth, compensation capacitors need to be connected in negative feedback configuration. Thus, there should be an inverting configuration for the second stage and and a non inverting one for the third stage. Among RNMC topology, networks adopting nulling resistor gives more potential bandwidth, but requires a large chip area and also leads to excessive noise. There this paper implements a pure RNMC networking consisting of two compensation capacitors gm_I, gm_{II} and a feed forward transconductance gm_{FF}.

B. Small Signal Behaviour and Stability Constraints

[2] Fig.3 represents the block diagram of the amplifier and Fig.6 represents its small signal equivalent model. From fig.6 calculation of voltage gain is done. The equations accounting for voltage gain is given by

$$\frac{V_{out}}{r_{o3}} + V_{out} S C_3 + (V_{out} - V_1) S C_{c1} + g m_{FF} V_1 = g m_3 V_2 \tag{6}$$

$$\frac{V_2}{r_{o2}} + V_2 S C_2 + (V_2 - V_1) S C_{C2} + g_{m2} V_1 = 0 \tag{7}$$

$$\frac{V_1}{r_{o1}} + V_1 S C_1 = (V_2 - V_1) S C_{C2} + (V_{out} - V_1) S C_{c1} + g_{m1} V_{in} \tag{8}$$

Solving these equations we get the loop gain transfer function as,

$$A(s) = \frac{-g m_1 r_{o1} g m_2 r_{o2} g m_3 r_{o3}}{[1 + (r_{o1} g m_2 r_{o2} g m_3 r_{o3} C_{c1}) s]} \cdot \frac{N(s)}{D(s)} \tag{9}$$

where the numerator and denominator is given by,

$$N(s) = 1 + [\frac{C_{c2}}{g m_2}(\frac{g m_{FF}}{g m_3} - 1) + \frac{C_{c1}}{g m_2 g m_3 R_{o2}}] s - \frac{C_{c1} C_{c2}}{g m_2 g m_3} s^2 \tag{10}$$

$$D(s) = 1 + [\frac{C_{c2}}{g m_3}(\frac{C_L}{C_{c1}} + 1) + \frac{C_{c2}}{g m_2}(\frac{g m_{FF}}{g m_3} - 1)] s - \frac{C_{c2} C_L}{g m_2 g m_3} s^2 \tag{11}$$

For calculation of open loop gain, A_o , put s=0 in equation 9. The result yields,

$$A_o \approx -g m_1 r_{o1} g m_2 r_{o2} g m_3 r_{o3} \tag{12}$$

For calculation of the dominant pole, method adopted is look for the denominator of the transfer function and take inverse of the coefficient of s, after neglecting the terms in

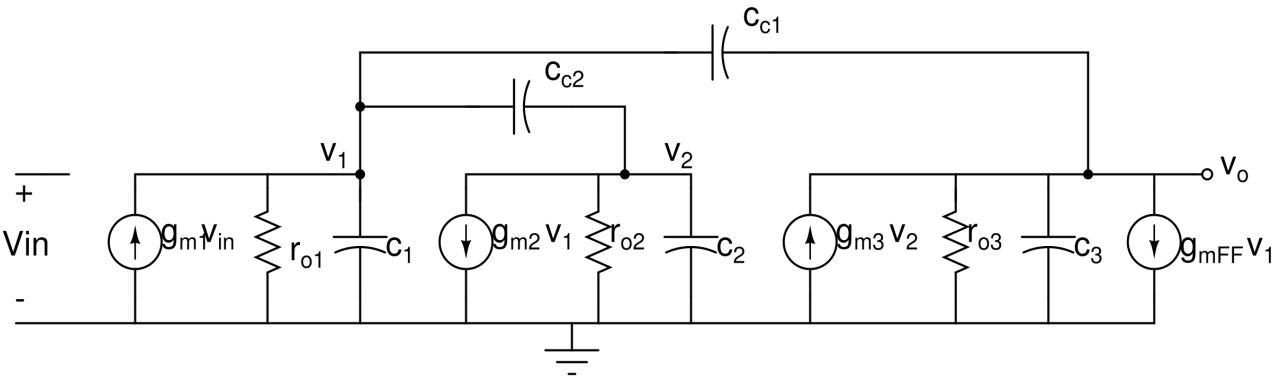

Fig. 6. Small signal model of three-stage OTA

comparison. If we have,

$$D(s) = 1 + as + bs^2 = (1 - \frac{s}{p1})(1 - \frac{s}{p2}) \tag{13}$$

if p1 is dominant pole, i.e. p1 >> p2, then equation reduces to,

$$D(s) = 1 + as + bs^2 = (1 - \frac{s}{p1} + \frac{s^2}{p1p2} \tag{14}$$

By comparing we can see that p1 being dominant pole is equal to the inverse of the coefficient of s.

But here it would be a tough task to calculate , hence we will look into it intuitively, We know that,

$$\omega p_1 = 1/RC \tag{15}$$

where R is the effective resistance looking from node 1 and C is the effective capacitance looking from node1.
$\therefore$ R = r_{o1}
For calculating effective capacitance, it is equal to gain times C_{c2} in addition to gain times C_{c1}.
$\therefore$ C= $gm_2\ r_{o2}\ C_{c2}$ + $gm_2\ r_{o2} gm_3\ r_{o3}\ C_{c1}$.
Neglecting terms, we get C=$gm_2\ r_{o2} gm_3\ r_{o3}\ C_{c1}$. $\therefore$

$$\omega p_1 \approx \frac{1}{r_{o1} gm_2 r_{o2} gm_3 r_{o3} C_{c1}} \tag{16}$$

For calculation of UGB frequency equate A(s)=1 by substituting s=jω.
So,

$$\omega_{GBW} = \frac{-gm_1 r_{o1} gm_2 r_{o2} gm_3 r_{o3}}{r_{o1} gm_2 r_{o2} gm_3 r_{o3} C_{c1}} = \frac{gm_1}{C_{c1}} = \frac{I_1}{\eta V_T C_{c1}} \tag{17}$$

It is apparent from these equations that there are two zeroes one in the left half plane and other in the right half plane and two non dominant complex conjugate poles both on left half plane.
Assuming as usual that gm_{FF} = gm_3 and intrinsic gain of stage 2 i.e. $g_{m2}r_{o2} >> 1$, the numerator then reduces to,

$$N(s) = 1 + [\frac{C_{c2}}{gm_2}(\frac{gm_3}{gm_3} - 1) + \frac{C_{c1}}{gm_2 gm_3 R_{o2}}]s - \frac{C_{c1}C_{c2}}{gm_2 gm_3} s^2 \tag{18}$$

$$N(s) = 1 + \frac{C_{c1}}{gm_2 gm_3 r_{o2}} s - \frac{C_{c1}C_{c2}}{gm_2 gm_3} s^2 \approx 1 - \frac{C_{c1}C_{c2}}{gm_2 gm_3} s^2 \tag{19}$$

From the value of N(s) obtained, we have two zeroes placed at the same position whose value is obtained by substituting s=jω and equating it to zero,

$$1 - \frac{C_{c1}C_{c2}}{gm_2 gm_3} (j\omega)^2 = 0 \tag{20}$$

Solving we get,

$$|\omega_{z1,z2}| = \sqrt{\frac{gm_2 gm_3}{C_{c1C_{c2}}}} \tag{21}$$

Being a high value, its effect on the phase contribution is negligible. Also, the gain contribution can be made negligible if | $\omega_{z1,z2}$ | is greater than the GBW product expressed in eq.17.

$$|\omega_{z1,z2}| = \sqrt{\frac{gm_2 gm_3}{C_{c1C_{c2}}}} > \omega_{GBW} \tag{22}$$

squaring both sides,

$$\frac{gm_2 gm_3}{C_{c1C_{c2}}} > \frac{{gm_1}^2}{C_{c1}^2} \tag{23}$$

Rearranging,

$$C_{c2} < \frac{gm_2 gm_3}{{gm_1}^2} C_{c1} = \frac{I_2 I_3}{{I_1}^2} C_{c1} \tag{24}$$

Now, for calculating the phase margin, if
N(s) = 1
D(s) = 1 + a_1s + $a_2 s^2$
phase margin is expressed as,

$$\phi = 90 - tan^{-1}(\frac{a_1 \omega_{GBW}}{1 - a_2 \omega_{GBW}^2}) = tan^{-1}(\frac{1 - a_2 \omega_{GBW}^2}{a_1 \omega_{GBW}}) \tag{25}$$

We have that the zeroes are neglected in the transfer function. So, we can set N(s)=1 and assuming that $C_L >> C_{c1}$ in D(s). By comparing equation (11) with standard equation of D(s) = 1 + a_1s + $a_2 s^2$, the phase margin is evaluated using,

$$tan\phi = \frac{1 - \frac{C_{c2}C_L}{gm_2 gm_3} * \frac{g_m^2}{C_{c1}^2}}{[\frac{C_{c2}}{gm_3}(\frac{C_L}{C_{c1}} + 1) + \frac{C_{c2}}{gm_3}(\frac{gm_{FF}}{gm_3} - 1)] * \frac{gm_1}{C_{c1}}} \tag{26}$$

Applying gm_{FF} = gm_3 and $C_L >> C_{c1}$,

$$tan\phi \approx \frac{gm_2 gm_3 C_{c1}^2 - gm_1^2 C_{c2} C_L}{gm_1 gm_2 C_{c2} C_L} \tag{27}$$

From here, C_{c1} can be calculated by assuming gm_1/gm_2 to be lower in comparison to tanϕ,

$$C_{c1} = \sqrt{\frac{gm_1 C_{c2} C_L}{gm_3}(\frac{gm_1}{gm_2} + tan\phi)} \approx \frac{\sqrt{C_{c2} C_L tan\phi}}{\sqrt{\frac{gm_3}{gm_1}}} \tag{28}$$

$$C_{c1} = \frac{\sqrt{C_{c2} C_L tan\phi}}{R} \tag{29}$$

$$where, R = \sqrt{\frac{gm_3}{gm_1}} = \sqrt{\frac{I_3}{I_1}}$$

Note that C_{c1} decreases if both of C_{c2} and I_1 / I_3 is reduced.

C. Amplifier Noise

Now, we look for the noise associated with the amplifier, In a multistage amplifier, majority of the noise is contributed by the first stage. The input noise spectral density will be the noise associated with M1,M2,M5,M6,M7,M8.

There would be no contribution of noise due to M3 and M4 as this is a part of the folded cascode topology, and we know that the transistor biased by some voltage does not contribute to noise. Hence, M3 and M4 won't contribute to noise.

Let's assume the noise PSD is given by S_{nM}. Initially noise at input of M5 is given by S_{nM5}. To convert it form input gate stage to output drain stage, we know that I = gm*Vgs, so multiplying this by gm^2 we get $gm_5{}^2$ S_{nM5}. squaring is done because we have equation is form of PSD which is a squared quantity. To convert this noise value to the input of say M1, we need divide it by gm of input transistor M1. Thus obtaining

$$S_{n,in} = (\frac{gm_5}{gm_6})^2 S_{nM5}$$

Overall input noise is given by ,

$$S_{n,in} = 2[S_{nM1,2} + (\frac{g_{mM5,6}}{g_{mM1,2}})^2 S_{n,M5,6} + (\frac{g_{mM7,8}}{g_{mM1,2}})^2 S_{n,M7,8}] \tag{30}$$

We know that noise consists mainly of thermal and flicker noise. Thus their overall contribution is subthreshold region is represented by

$$S_{vw} = \frac{2q}{I_D}(\eta V_T)^2 + \frac{K}{WL}\frac{1}{f} \tag{31}$$

where the alphabets have their usual meaning. q refers to the charge by an electron, K being the fabrication process parameter and f is frequency. Thus, putting the values we get,

$$S_{n,in} = 4\frac{q\eta^2 V_T^2}{I_{M1,2}}[1 + (\frac{I_{M5,6}}{I_{M1,2}})^2 + (\frac{I_{M7,8}}{I_{M1,2}})^2] + 2\frac{K}{f}[\frac{1}{WL_{1,2}} + \frac{I_{M5,6}^2}{I_{M1,2}^2 WL_{5,6}} + \frac{I_{M7,8}^2}{I_{M1,2}^2 WL_{7,8}}] \tag{32}$$

where gm_i ratios from equation 31 is replaced by the current I_i ratios in equation 32.

IV. OTA DESIGN

For designing the values, normal design procedure as we did while the transistors were working in saturation or strong inversion region cannot be adopted here. The Subthreshold region finds a different set of design procedure. Given that the application consumes ultra low power so, we need to minimize the power requirement for a given speed performance. We have from equation 17,

$$\omega_{GBW} = \frac{I_1}{\eta V_T C_{c1}} \tag{33}$$

Inserting the value of C_{c1} from equation 29, we get,

$$\omega_{GBW} = \frac{\sqrt{I_1 I_3}}{\eta V_T \sqrt{C_{c2} C_L tan\phi}} \tag{34}$$

From the equation it is clear that to maximize the GBW product, lower value of C_{c2} is required. For designing such that it comes ultra low power, we start by taking total current I_T as the total amplifier bias current. Now, as defined earlier in section III about the stage bias currents. I_{B1} = $2I_1$, I_{B2} = I_2 , I_{B3} = (1 + β) I_3. Adding them to obtain total current,

$$I_T = I_{B1} + I_{B2} + I_{B3} = 2I_1[1 + \frac{I_2}{I_1} + (1+\beta)\frac{I_3}{I_1}] \tag{35}$$

From 34, and multiplying and dividing by $\sqrt{I_1}$,

$$\omega_{GBW} = \frac{\sqrt{I_1 I_3}}{\eta V_T \sqrt{C_{c2} C_L tan\phi}} * \frac{\sqrt{I_1}}{\sqrt{I_1}} = \frac{R.I_1}{\eta V_T \sqrt{C_{c2} C_L tan\phi}} \tag{36}$$

Substituting the value of I_1 from 35, we have,

$$\omega_{GBW} = \frac{I_T}{\eta V_T \sqrt{C_{c2} C_L tan\phi}.\frac{1}{(2+\frac{I_2}{I_1})\frac{1}{R} + (1+\frac{1}{\beta})R}} \tag{37}$$

For a given bias value of current, ω_{GBW} = can be maximized by minimizing the denominator with respect to R.

$$\frac{d}{dR}((2 + \frac{I_2}{I_1})\frac{1}{R} + (1 + \frac{1}{\beta})R) = 0 \tag{38}$$

Solving we get,

$$R^2 = \frac{I_3}{I_1} = \frac{2 + I_2/I_1}{1 + 1/\beta} \approx 2 + \frac{I_2}{I_1} \tag{39}$$

where β is assumed to be much higher than 1. From previous equation we get the value of I_3 which is equal to

$$I_3 = 2I_1 + I_2 \tag{40}$$

$\therefore$ I_T which was equal to

$$I_T = 2I_1 + I_2 + I_3 = 2I_3 \approx 2I_{B3} \tag{41}$$

$$\omega_{GBW} = \frac{1}{2\eta V_T}\frac{I_T}{\sqrt{C_{c2} C_L tan\phi(2 + \frac{I_2}{I_1})}} \tag{42}$$

Now after all the equations has been derived, let's look for the values of current. We have the ratio of I_2 / I_1 has to be greater than 1. let's assume this value between 4 to 7. say 5. We won't take much larger values as it would lead to excessive reduction of gain bandwidth product. From equation 42, given

all the values and the ratio of I_2 / I_1, we can calculate I_T. From the value of I_T, all other currents can be known based on the above relation.
Regarding the noise impacting the desired target specifications, if the thermal noise is within the limit then the flicker noise can be reduced by increasing the transistor area of the input stage as input stage is the one contributing noise in multistage amplifiers. Now if the thermal noise component is beyond the limit, it can be minimized by increasing the first stage bias current. This leads to minimum power consumption.

V. EXPERIMENTAL RESULTS

A. Implementation

Experiment is carried out trying to achieve gain and phase margin and not for the low power calculations, since we are using a supply of 1.8V. The design of the OTA has been implemented on CADENCE VIRTUOSO simulation tool based on gpdk180nm technology. The transistors have minimum channel length of 180nm. The threshold value of transistors are nearly 485mV. Let the design under following specification. Greater than 1MHz unity gain bandwidth, capacitive load upto 200pF and for a phase margin of 55° along with an achievable gain of 100dB. Let the total current flowing in through the supply is 10 μ A. As per our calculations done above,

$$I_T = 10\mu A = 2I_3 => I_3 = 5\mu A \tag{43}$$

We have the relation I_3 = 5 I_1 and I_2 = 7 I_1 , Thus,

$$I_1 = 0.71\mu A and I_2 = 3.57\mu A. \tag{44}$$

From equation 42, putting the values of I_T = 10uA , ω_{UGB} = 1MHz, η =1, V_T= 25mV, C_L = 20pF, tanϕ =1.5, ratio of I_2/I_1 =5, we get the value of C_{c2},

$$C_{c2} = 190pF. \tag{45}$$

After C_{c2} is obtained, value of C_{c1} can be obtained from eqn 29. where the value of R is $\sqrt{7}$

$$C_{c1} = 28.56pF \tag{46}$$

Since C_{c1} and ω_{UGB} is known, g_{m1} can be calculated from equation 17.

$$g_{m1} = 30\mu A \tag{47}$$

Thus after knowing current values through transistors and keeping Vgs in a way that transistors remain in saturation, we can calculate W/L of the transistors. The values of W/L are presented in the table along with.

Transistors dimensions	
TRANSISTOR	DIMENSION(μm/μm)
M0	2/0.5
M1,M2	12/0.35
M3,M4,M7,M8,M11,M12	1/0.5
M5,M6	2/0.5
M9,M10	4/0.5
M13,M14	6/0.5

Small signal parameters	
parameter	values
g_{m1}	30uA/V
g_{m2}	1.3uA/V
g_{m3}	2.1uA/V
g_{mFF}	2uA/V
C_{c1}	28.5pF
C_{c2}	190pF

B. Simulation results

Simulation of the experiment is carried out taking the values as mentioned in the previous section. AC analysis is performed for obtaining gain of the circuit and phase margin along with that confirming the value of unity gain band width frequency. Transient analysis is performed for an input voltage of 100mV peak amplitude.The results obtained from transient response shows that load capacitor charges instantly but discharges gradually as it discharges through the current mirror path of M12 and M13 contributing high resistance. Due to this high resistance, time constant is of higher value, thereby discharges slowly. The table showing the values obtained and the graph is presented along.

Amplifier performance parameters	
performance parameter	value
Power supply(V)	1.8
Loading capacitance (pF)	20
Gain(dB)	73.47
Phase Margin	42 °

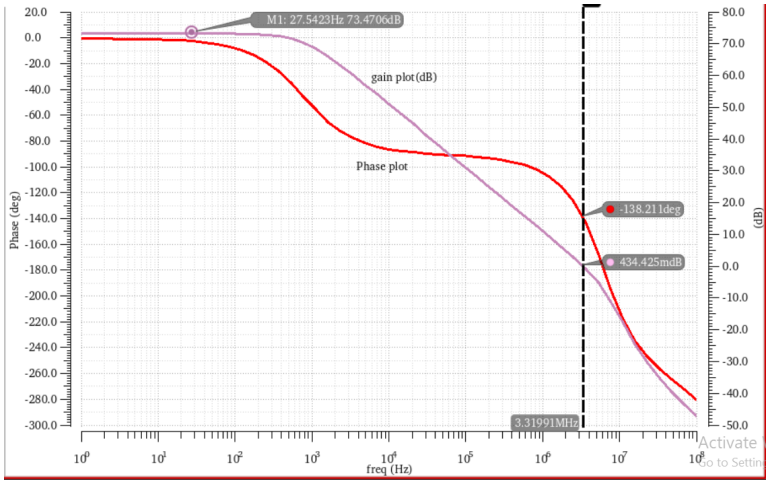

Fig. 7. Plot showing phase, Gain and f_{UGB}

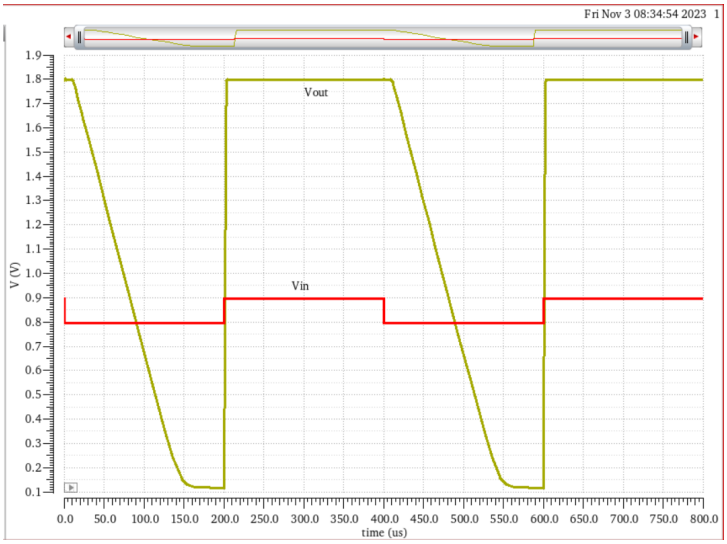

Fig. 8. Plot showing transient response analysis

VI. CONCLUSION

The paper aims to present the design of an ultra-low-power subthreshold three-stage OTA. Various parameters have been exploited to take the best out of it keeping in mind the trade offs that come into picture. The paper provides a 120-dB DC gain which is possible due to cascading of three stages. The design has been carried out in 0.35μ technology and occupying an area of 4.4*10^{-3} mm^2. Circuit consisting of three stage is carried along with a pure Reverse Nested Miller network. Nulling resistor has not been implemented in order to save the silicon area. It is able to drive capacitive loads upto 200pF, with 20KHz unity gain frequency consuming only 195nW power.

Apart from the above results obtained in paper I tried to simulate the circuit to whatever extent possible. Taking power supply voltage to be 1.8V, a DC gain of 74dB was obtained with a phase margin of 42 °.

The Design methodologies and values obtained here is best among all the papers in this field till date. It confirms that the amplifier is ready for best in use considering driving high capacitive loads by consuming very less power.

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