VISVESVARAYA TECHNOLOGICAL UNIVERSITY

BELAGAVI - 590018

Project Report

on

"LOW NOISE AMPLIFIER DESIGN FOR WIRELESS BODY AREA NETWORK APPLICATIONS"

Submitted in partial fulfilment of the requirements for the VIII Semester

Bachelor of Engineering

in

ELECTRONICS AND COMMUNICATION ENGINEERING

For the Academic Year

2020-2021

BY

SACHIN P B	**1PE17EC110**
SAURABH SUMAN	**1PE17EC122**
MATLI VENKATA SAI MOHIT MAYUR	**1PE17EC074**

UNDER THE GUIDANCE OF

MURALIDHAR S

Assistant Professor, Dept. of ECE, PESITBSC

Department of Electronics and Communication Engineering

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the project work entitled "LOW NOISE AMPLIFIER DESIGN FOR WIRELESS BODY AREA NETWORK APPLICATIONS" carried out by "SACHIN P B, SAURABH SUMAN, MATLI VENKATA SAI MOHIT MAYUR, bearing USN's 1PE17EC110, 1PE17EC122, 1PE17EC074" respectively in partial fulfillment for the award of Degree of Bachelors (Bachelors of Engineering) in Electronics and Communication Engineering of Visvesvaraya Technological University,Belagavi during the year 2020-2021. It is certified that all corrections/ suggestions indicated for internal assessment have been incorporated in the report. The project report has been approved as it satisfies the academic requirements in respect of project work prescribed for the said Degree.

Signature of the Guide	Signature of the HOD	Signature of the Principal
Muralidhar S	**Dr. Subhash Kulkarni**	**Dr. Subhash Kulkarni**
Assistant Professor	**HOD**	**Principal, PESIT-BSC**

External Viva

Name of the Examiners	**Signature with Date**
1.	
2.	

ACKNOWLEDGEMENTS

The satisfaction and euphoria that accompany the successful completion of any task would be incomplete without the mention of people who made it possible, whose constant guidance and encouragement crowned our effort with success.

We are indebted to our Guide, Muralidhar S, Department of Electronics and Communication Engineering, PESIT - Bangalore South Campus, who has not only coordinated our work but also given suggestions from time to time.

We would like to express our gratitude to Dr. Subhash Kulkarni, Principal and ECE Head of Dept. PESIT Bangalore South Campus, for providing us with the relevant infrastructure.

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Sachin P B
Saurabh Suman
Matli Venkata Sai Mohit Mayur

ABSTRACT

Wireless Body Area Network(WBAN) is a wireless network of wearable computing devices that may be implemented or mounted on the human body.Low Noise Amplifier(LNA) is the first functional block in WBAN receiver.In order to maintain the required SNR,high gain LNA is desirable which further reduces the overall Noise Figure(NF) of the receiver block.In this project work we are exploring and targeting to design LNA to meet balance amongst these parameters,in particular high power gain and if low power consumption.

After conducting the Literature survey,we have observed that most Low Noise Amplifiers suffer from higher Noise Figure,high power and reduced stability.To overcome these potential problems,an attempt will be made to improve the above mentioned parameters.

Keywords: Low Noise Amplifier,WBAN,S Parameter,Topologies,Noise Figure,Power gain,Power Consumption,Stability

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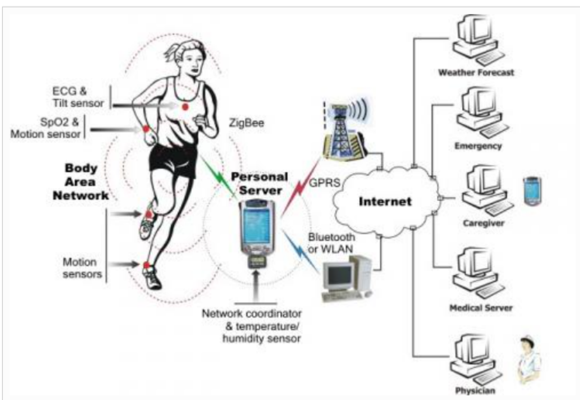
Chapter 1

INTRODUCTION

1.1 WIRELESS BODY AREA NETWORK(WBAN)

WBAN is a wireless network which is comprised of wearable devices that have the ability to measure and gather data regarding the physiological condition of the user.The network typically expands over the whole body and the nodes are connected through a wireless communication channel.A WBAN connects independent nodes (e.g. sensors and actuators) that are situated in the clothes, on the body or under the skin of a person.
A WBAN offers many promising new applications in the area of remote health monitoring,sports and many other all of which make advantage of the unconstrained freedom of movement a WBAN offers. In the medical field, for example, a patient can be equipped with a wireless body area network consisting of sensors that constantly measure specific biological functions, such as temperature, blood pressure, heart rate, electrocardiogram (ECG), respiration, etc. The advantage is that the patient doesn't have to stay in bed, but can move freely across the room and even leave the hospital for a while. This improves the quality of life for the patient and reduces hospital costs. In addition, data collected over a longer period and in the natural environment of the patient, offers more useful information, allowing for a more accurate and sometimes even faster diagnosis.

Figure 1.1: WIRELESS BODY AREA NETWORK

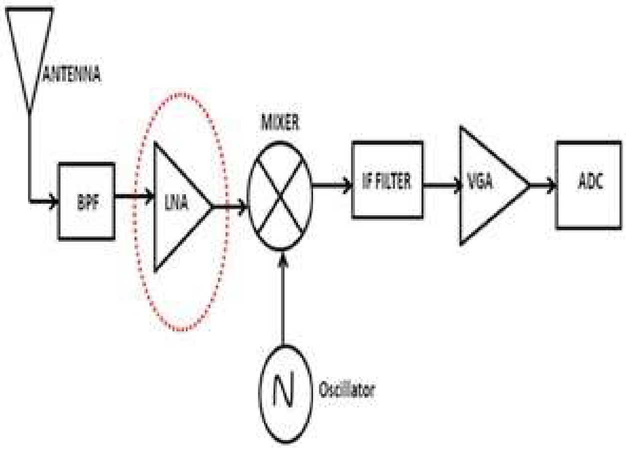


1.2 LOW NOISE AMPLIFIER

Low-Noise Amplifier is the typically the first stage of the receiver, whose main function is to provide enough gain to overcome the noise of subsequent stages.Apart from providing this gain while adding as little noise as possible, an LNA should accommodate large signals without distortion, and frequently must also present a specific impedance to the input source

A low-noise amplifier (LNA) is an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio. An amplifier will increase the power of both the signal and the noise present at its input, but the amplifier will also introduce some additional noise. LNAs are designed to minimize that additional noise. Designers can minimize additional noise by choosing low-noise components, operating points, and circuit topologies. Minimizing additional noise must balance with other design goals such as power gain and impedance matching.LNAs are found in radio communications systems, medical instruments and electronic test equipment.

Figure 1.2: BLOCK DIAGRAM OF RECEIVER



Chapter 2

LITERATURE SURVEY

1 2019 This paper designed a wireless body area network circuit using LNA that can work at low supply voltage using 130nm CMOS technology. This paper mainly aims at good gain and good linearity

2 2016 The paper proposes a Folded Cascode (FC) Low Noise Amplifier (LNA) for low voltage and high gain RF applications. This paper mainly focuses on low voltage high gain RF applications.

3 2018 The paper aims to achieve a low noise figure, reasonable power gain and low power consumption in 3-10 GHz. Improved PI-network and T-network are used to obtain a high and smooth power gain.

2.1 PROBLEM STATEMENT

After conducting the Literature survey, we have observed that most Low Noise Amplifiers suffer from higher Noise Figure, high power and reduced stability. To overcome these potential problems, an attempt will be made to improve the above mentioned parameters.

Chapter 3

SOFTWARE SPECIFICATIONS

3.1 SOFTWARE ENVIRONMENT DETAILS

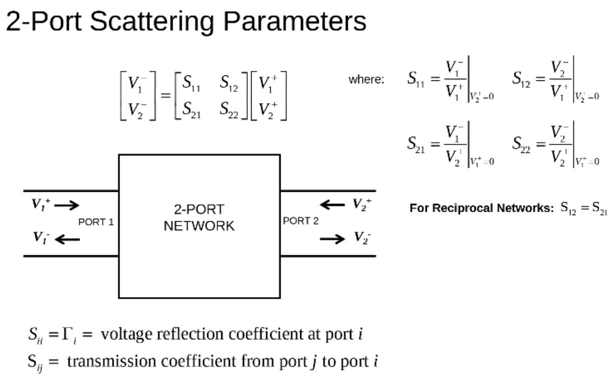
The software environment is CADENCE under which VIRTUOSO platform is used. Virtuoso platform includes tools for designing full-custom integrated circuits,which can be used schematic entry,behavioural modeling,circuit simulation,custom layout,physical verification,extraction and back annotation and provides complete design environment for front and back end design.It also offers various packages like analoglib,GPDK 180 etc,where 180 indiactes the feature size. It is mainly used for analog,mixed-signal,RF and other standard-cell designs.It is also used for memory cells and FPGA designs.The schematic of design is done in schematic editor window.In the Virtuoso platform,RF Spectre simulator is used in order to simulate the circuit.The Cadence Spectre RF option provides numerous analyses built on silicon-proven simulation engines in both the time and frequency domains.The wide range of analysis enables verification of mixers,power amplifiers,filters etc.

Chapter 4

BASICS OF RF DESIGN

4.1 S-PARAMETERS

Figure 4.1: S PARAMETER



S parameters describe the response of an N port network to signal incident to any or all of the ports.The advantage of using S parameters is that matched loads are much easier to use at high signal frequencies and also quantities are measured in terms of power.
Here
S11 is input reflection coefficient
S12 is reverse transmission gain
S21 is forward transmission gain
S22 is output reflection coefficient

4.2 GAIN

Gain is basically the ratio of amplified output signal to the applied input signal and is given by

$$A_v = \frac{V_{out}}{V_{in}}$$

There are 3 different types of gains:
Transducer Power Gain(GT) is the ratio of power delivered to the load to power available from the source.

$$G_T = \frac{P_{load}}{P_{source,max}}$$

Available Power gain is the ratio of power available from the network to the power available from the source.

$$G_A = \frac{P_{load,max}}{P_{source,max}}$$

Operating Power Gain(Gp)is the ratio of power delivered to the load to power input to the network.

$$G_P = \frac{P_{load}}{P_{input}}$$

4.3 NOISE FIGURE

The noise figure is the ratio of input SNR to output SNR.

$$F = \frac{SNR_{in}}{SNR_{out}}$$

The noise figure NF is defined as the noise factor in db:

$$NF = 10log_{10}(F)$$

$$NF = 10log_{10}\frac{SNR_{in}}{SNR_{out}}$$

$$NF = SNR_{in,dB} - SNR_{out,dB}$$

4.4 STABILITY

Stability is affected by parameters such as:
• Presence of feedback path between output and input.
• Very high gain
These may cause the circuit to ossilate for some values of load and source impedence.Hence a circuit has to satisfy the stem stability fator to exhibit unconditional stability,which is defined as,

$$K = \frac{1 + |\delta|^2 + |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{22}|}$$

where,
S11 is the input reflection coefficient
S22 is the output reflection coefficient.

Chapter 5

DIFFERENT TYPES OF LNA TOPOLOGIES

Figure 5.1: DIFFERENT TYPES of LNA TOPOLOGIES

Type	Benefits	Drawbacks
Common Source (CS) Resistive termination	If R1 is connected to 50ohm it gives good input matching	Generates thermal noise due to presence of R1 and it will contribute to total NF
Common Gate(CG) Configuration	Looking into the M1 source Rin is 1/gm this can be made 50ohm easily by sizing of M1.	Gm cannot be increased very high and it puts lower bound.
CS Shunt Series feedback	Attenuating problem is very less so it can be used as Broad band amplifiers	Feedback RF contributes thermal noise.
ISD Configuration	Since no resistor physical so no thermal noise. Inductors at source with Cgs gives the real impedance.	Performance is good if size of the inductors neglected.
Cascode ISD Configuration	Due to isolation of I/P and O/P, can achieve higher gain and lower Noise Figure	Cascode transistor may contribute noise.

5.1 COMMON SOURCE (CS) RESISTIVE TERMINATION

In this topology resistors at input terminal aids to accomplish 50 ohm impedance matching but it adds thermal noise to the circuit.

Figure 5.2: COMMON SOURCE (CS) RESISTIVE TERMINATION:

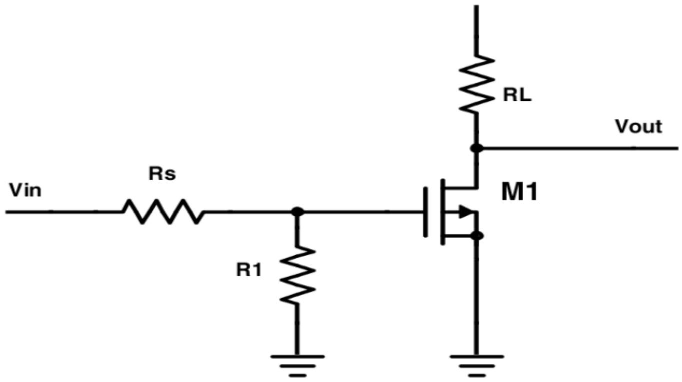


Figure 2.4 Common source (CS) resistive termination

5.2 COMMON GATE (CG) CONFIGURATION

Common gate configuration benefits to achieve less power consumption but has gain limitations.

Figure 5.3: COMMON GATE (CG) CONFIGURATION

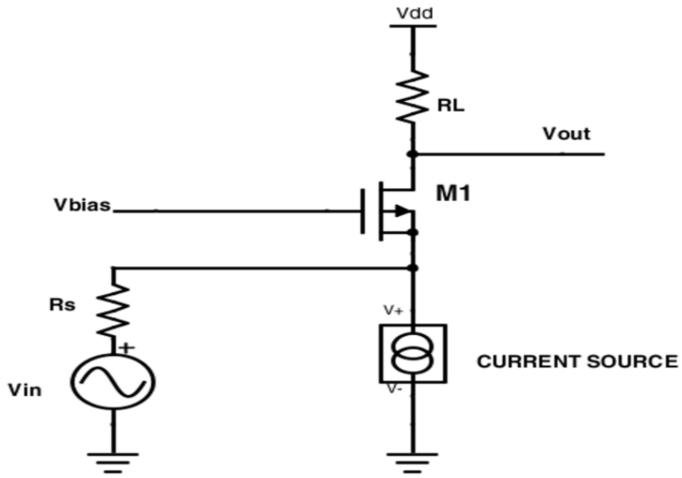


Figure 2.5 Common gate (CG) Configuration

5.3 CS SHUNT SERIES FEEDBACK

Amplifier using shunt-series feedback often have extraordinary high power dissipation compared to others with similar noise performance.It is difficult to achieve good trade off between gain and Noise figure.

Figure 5.4: CS SHUNT SERIES FEEDBACK

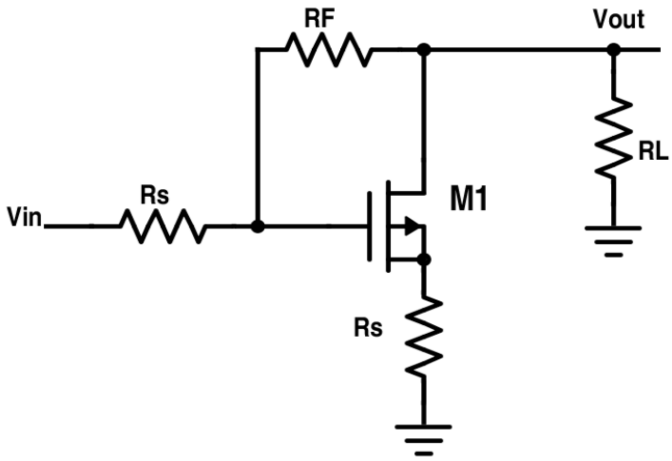


Figure 2.6 CS Shunt series feedback

5.4 CASCODE INDUCTIVE SOURCE DEGENERATION

Cascode ISD configuration provides good insolation between input and output stage which aids for NF and low power consumption.Hence this configuration can be used to achieve the design specifications.

Figure 5.5: CASCODE INDUCTIVE SOURCE DEGENERATION

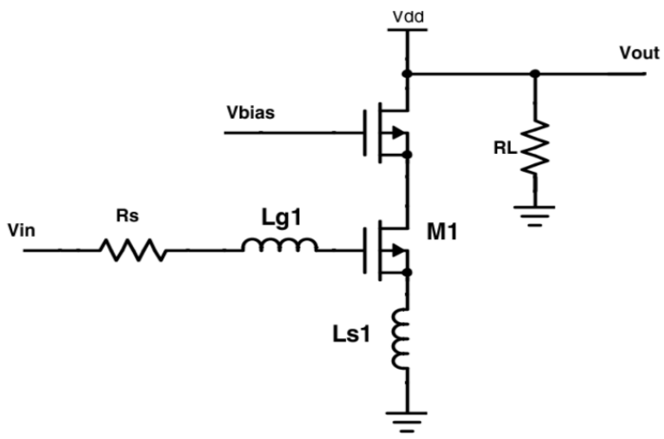


Figure 2.8 Cascode inductive source degeneration

Chapter 6

DESIGN

6.1 PROPOSED DESIGN

Figure 6.1: SCHEMATIC

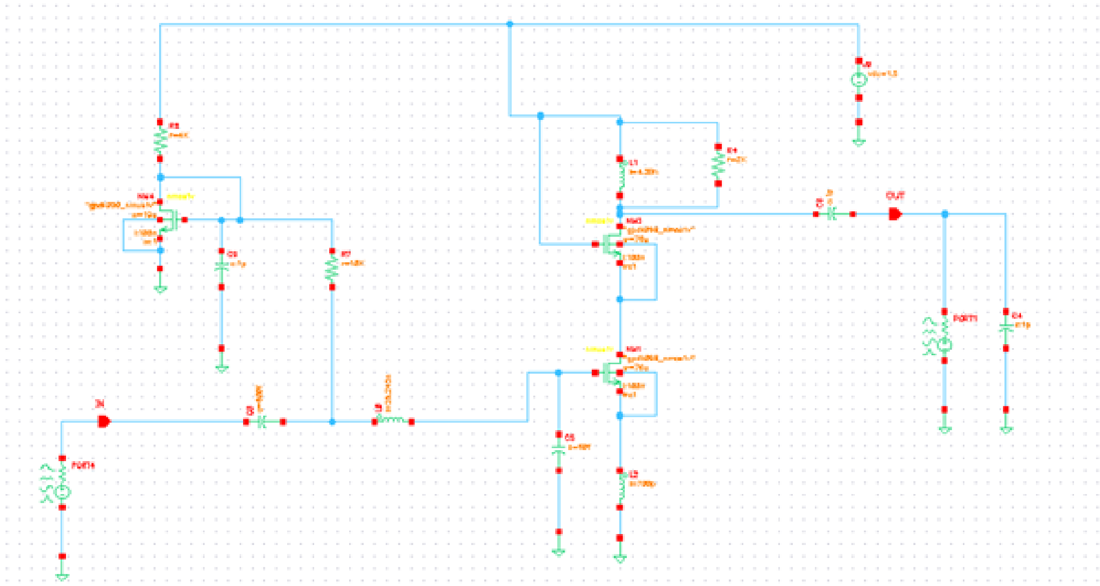


Figure 6.2: TARGET SPECIFICATIONS

Parameters	Target Specifications
Frequency	2.4 GHz
Supply Voltage	1 V
Noise Figure	<1.2 dB
Power Dissipation	<2 mW
Power Gain	>16 dB

POWER CONSTRAINT:
The power dissipated in the circuit is given by:

$$P = I_d \times V_{dd}$$

Since our design target for power consumption is 2 mW and the Voltage supply, VDD selected is 1 V, the IDD value comes out be 1 mA.

INPUT IMPEDANCE:

The input impedance is given by the equation:

$$Z_{in} = \frac{g_m \times L_s}{C_{gs}}$$

Since we have to match with a 50ohms antenna, the Zin = 50 ohms Initially, we have started the design with the degeneration inductance ”LS” to be 1 nH.

QUALITY FACTOR:

The quality factor is given by:

$$Q = \frac{f_0}{BW}$$

Since our operating frequency is 2.4 GHz and the bandwidth is taken as 300 MHz, we get a quality factor of 8.

We have the equation:

$$Q = \frac{\omega(L_g + L_s)}{R_s}$$

From the above equation, we obtain Lg to be 25.5 nH.

CENTER FREQUENCY:

We need to tune the circuit to 2.4 GHz, therefore we use the equation:

$$\omega_0^2 = \frac{1}{(L_g + L_1)(C_{gs} + C_{pad})}$$

After substituting the required values, we choose ”Cgs” = 106 fF and ”Cpad” = 60fF

Load inductance can be found out from the output network by considering the parasitic and load capacitances.

$$L_d = \frac{1}{C_{out} \times \omega_0^2}$$

Since our Cout= 1pF, we obtain a Load inductance of 4.39 nH.

Vdd=1V,Id can be found from power constraint

The gm of the MOSFET is given by the equation:

$$g_m = \sqrt{2 \times \mu_n C_{ox} \times I_D \times \frac{W}{L}}$$

The gm of the MOSFET was calculated from the above equation and it came out to be 40.14 mS.

WIDTH CAN BE CALCULATED FROM THE Id EQUATION:

The drain current equation at saturation is given by:

$$I_D = \frac{1}{2} \times k_n'(V_{dsat})^2 \times \frac{W}{L}$$

Here, L = 90 nm
Therefore, we get W=74 micro meters
This Width value should be adjusted after finding the right VDsat value after the first simulation.

$$\frac{W}{L} = \frac{2I_D}{k_n' \times (V_{dsat})^2}$$

TRANSITION FREQUENCY:

Using the gm found out in the above equation we can find the transition frequency using the following equation:

$$\omega_T = \frac{g_m}{C_{gs}}$$

was calculated to be 378 GHz and therefore the transition frequency, fT = 60 GHz.

NOISE FIGURE:

The minimum noise factor can be estimated using the following equation:

$$F_{min} \approx 1 + 2.4\frac{\gamma}{\alpha}[\frac{\omega}{\omega_T}]$$

The minimum noise factor for our circuit was calculated to be 1.224.
We know that, Noise figure can be calculated from the noise factor as:
Therefore, the minimum noise figure for this circuit is estimated to be 0.877 dB.

CURRENT MIRROR BIAS CIRCUIT DIMENSIONS:

We use a Current mirror circuit to provide current to the main amplifier circuit. We need to allow only a small amount of current to flow through the current mirror to minimize the power dissipation. Therefore, in this circuit we let only 25 percent of ID pass through the current mirror. Since our ID is 2 mA, 0.5 mA will flow into the current mirror. In order to do this, we have to make the transistor width of the current mirror to be 25 percent of the transistor width in the main circuit. Since we selected the MOS width to be 74 micrometer initially, the MOS in the current mirror should have a width of about 18.5 um.

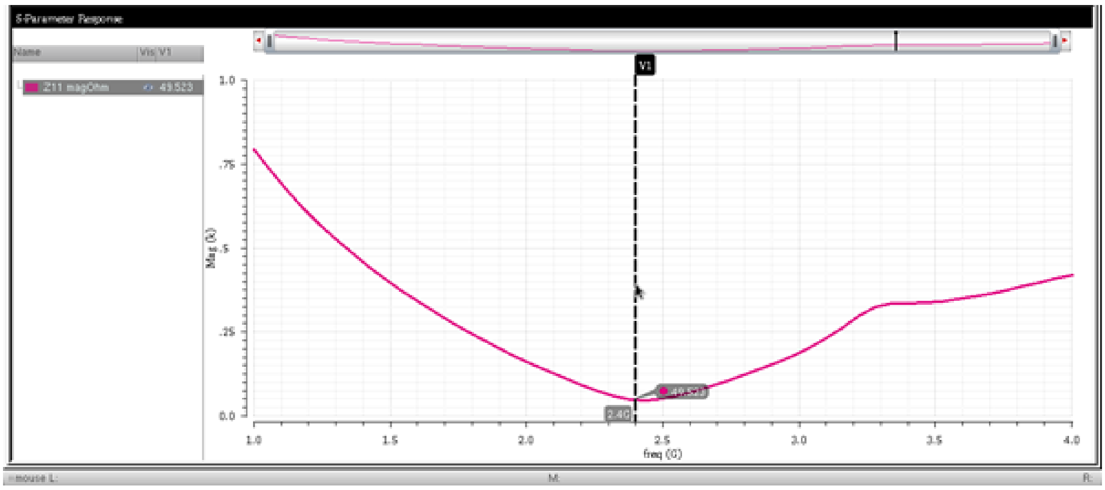
Chapter 7

SIMULATION RESULTS

7.1 IMPEDANCE

The LNA has been designed to have impedance match of 50 ohms and we obtained input impedance to be 49.5 ohm which is a accepted value and leads impedance match of LNA and antenna.

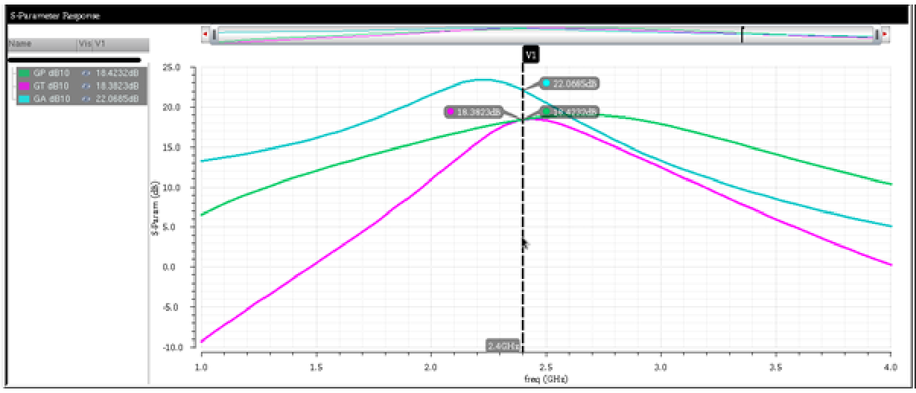
Figure 7.1: GRAPH OF Z11



7.2 POWER GAIN

The 3 different power gain parameters GP,GA,GT is shown in the diagram and we have achieved good power gain for our LNA.

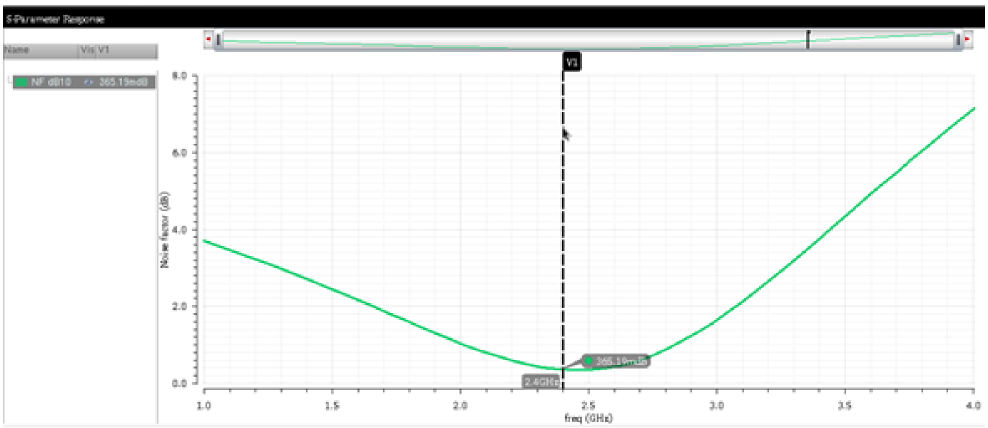
Figure 7.2: GRAPH OF POWER GAIN



7.3 NOISE FIGURE

Noise figure is defined as the ratio of signal to noise ratio at the output to that at the input.We have designed LNA to have a noise figure of 0.36 Db and it better than our reference paper.

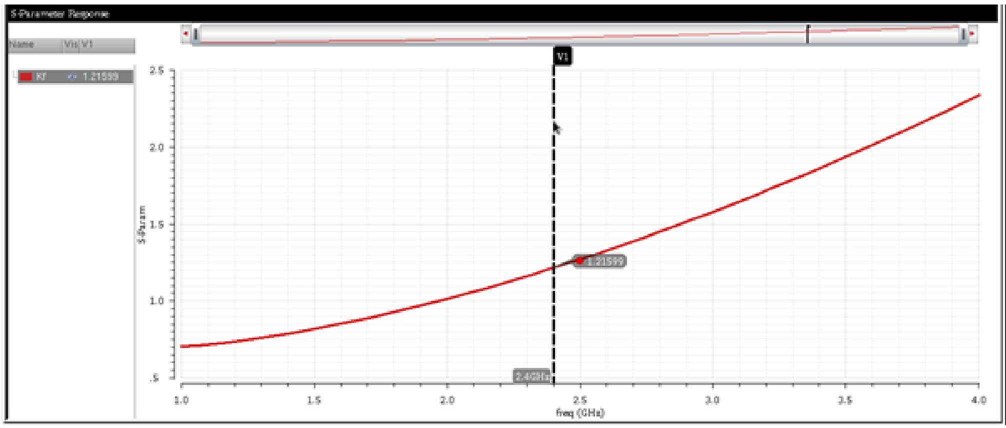
Figure 7.3: GRAPH OF NF



7.4 STABILITY

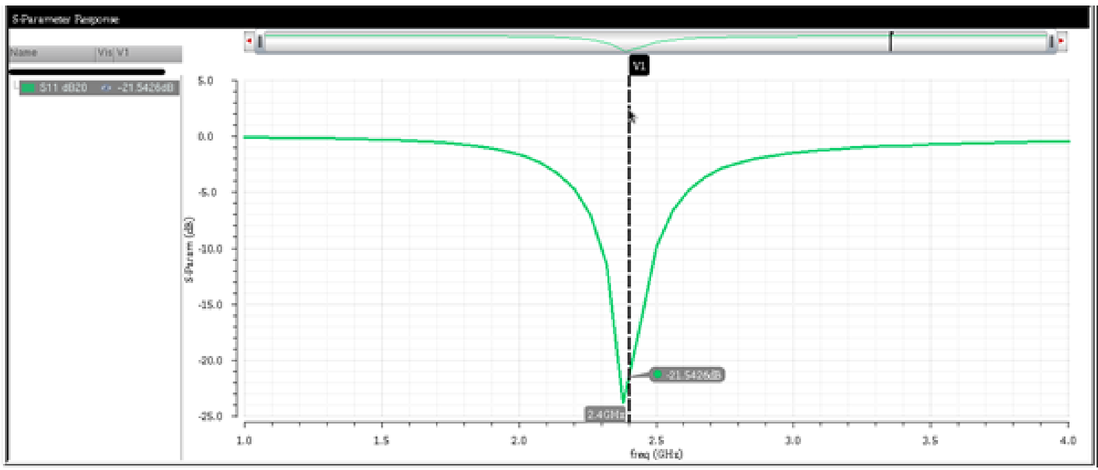
Our LNA has Kf value to be 1.21 at 2.4 Ghz which indicates our LNA is stable.

Figure 7.4: GRAPH OF STABILITY



7.5 S PARAMETER ANALYSIS

Figure 7.5: GRAPH OF S11



Due to the usage of cascode configuration we have have obtained good reverse isolation of -32.82 DB

Figure 7.6: GRAPH OF S12

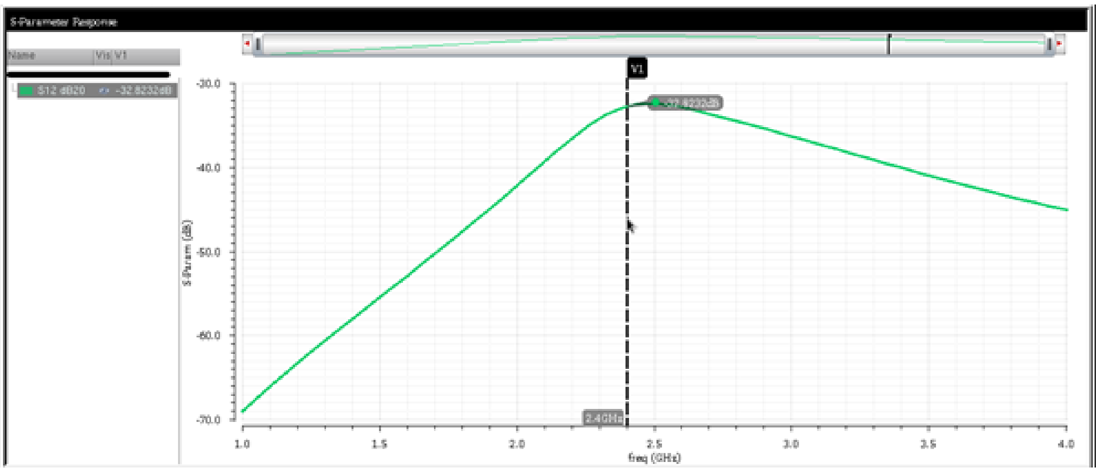
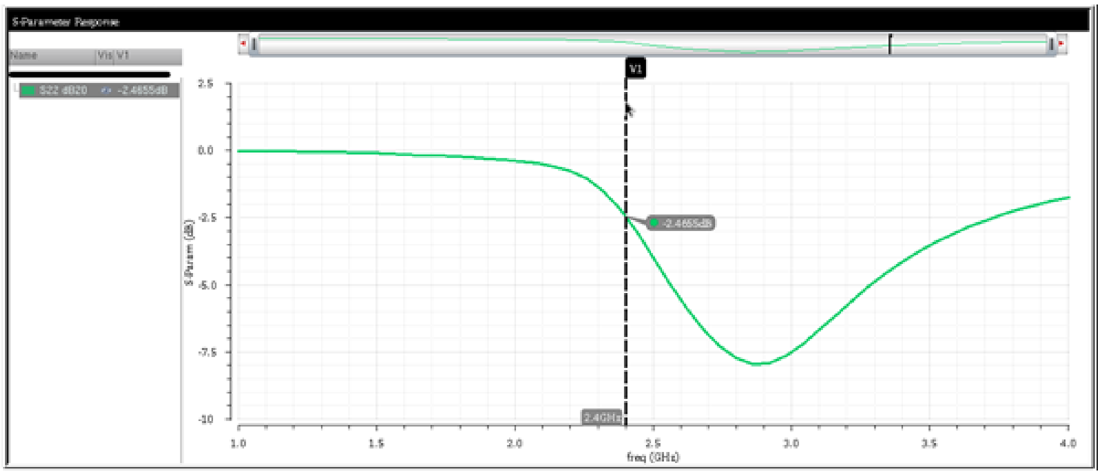


Figure 7.7: GRAPH OF S22



Our LNA has a forward gain of 18.38 DB which is large enough gain to cancel out noise from subsequent stages.

Figure 7.8: GRAPH OF S21

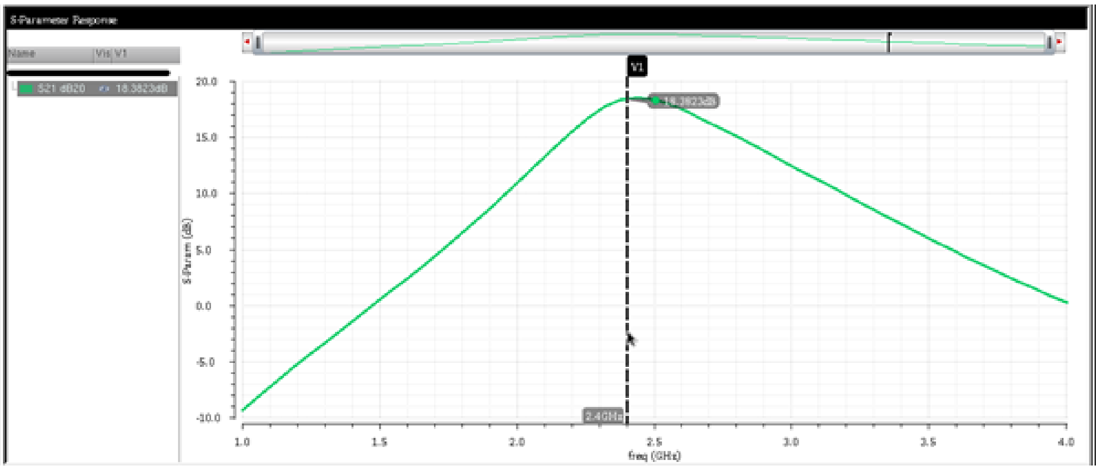


Figure 7.9: PERFORMANCE COMPARISON WITH OTHER PAPERS

Parameters	[5]	[8]	[9]	[10]	Our Work
Frequency (GHz)	2.4	2.4	2.4	2	2.4
Vdd (V)	0.5	0.5	1.8	1.8	1.0
Pdc (mW)	1.44	2.1	11.96	6.055	1.79
S11 (dB)	-27.72		-5.054	-6.61	-21.54
NF (dB)	1.7	1.5	2.17	2.049	0.35
Technology (nm)	130	180	180	180	90

Chapter 8

CONCLUSION

In this project, the design of a Low Noise Amplifier for Wireless Body Area Network applications is presented. The LNA is designed using Cascode Inductive Source Degeneration configuration in the Cadence environment with 90 nm CMOS technology. Since this LNA is used for WBAN applications, it should ideally dissipate lesser power and have a low noise figure.
This LNA operates at a frequency of 2.4 GHz. Trade-off between the S-Parameters, Noise Figure and Power have been optimized by performing multiple iterations in the design. All the other design targets are satisfied and the circuit is unconditionally stable.
This LNA dissipates very less power (=1.79 mW) and has a very good noise figure (=0.35 dB) which is better than the existing circuits. The isolation between input and output port is good which is signified by the reverse voltage gain (S12) of -32.823. Comparatively, this circuit has a better overall performance.

Chapter 9

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6. INTRODUCTION TO RFIC by Prof. Sankaran Aniruddhan - Reference video lectures by professor Aniruddhan

Appendix A

REVIEW PROCESS

A.1 PHASES OF REVIEW

Project was evaluated at phases with major checkpoints as follows :

1st Review : ***Defining Problem Statement and Literature Survey Review***

1. Clarity in understanding of the problem statement.
2. Completion of Literature Survey.
3. Technical understanding of domain.
4. Timeline for completion of project using Gantt chart.

2nd Review : ***Hands on Cadence and Theoretical aspects of designing LNA***

1. Hands on Cadence.
2. Understanding how RF analysis works.
3. Constructing sample LNA to understand how designing works.

3rd Review : ***Project Progress and Finishing plan Review***

1. 70% implementation
2. Completed design and schematic
3. Work on simulation started.
4. Final demonstration plan.

4th Review : ***Module completion and Integration Review***

1. 100% Module implementation.
2. Completion of Project.
3. Presentation of our design and values obtained.
4. Adherences to project plan.