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# EE537 Circuit Simulation Lab

## Experiment 8

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### 1 Design of an inverting amplifier using a two stage OTA

Design an inverting amplifier using a 2 stage miller compensated OTA. Fig. 1 shows the schematic of the inverting amplifier to be designed.

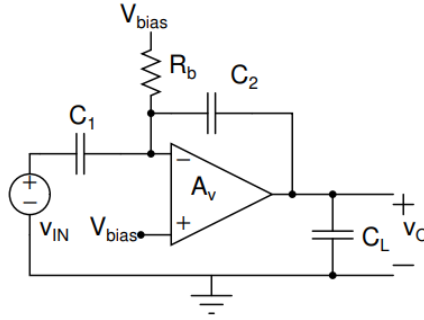


Figure 1: Inverting amplifier with capacitive voltage feedback

Target specifications:

Spec.	Value
Midband gain	20 dB
Bandwidth	> 1 MHz
Input capacitance	1 pF
Load capacitance	10 pF
Slew rate	$\geq 10 \text{ V}/\mu\text{s}$
Gain error	0.1 %
Phase margin	$\geq 65^\circ$
Operating temperature range	0 °C to 70 °C

Figure 2: Specification Table

### 2 Implement the 2 stage using a miller compensated 2 stage OTA

A Two stage uncompensated OTA is as shown below

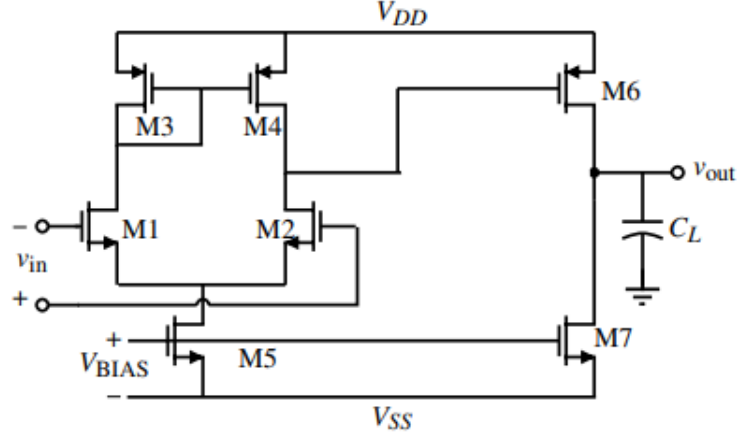


Figure 3: Two stage uncompensated OTA

Small signal model of Two stage uncompensated OTA

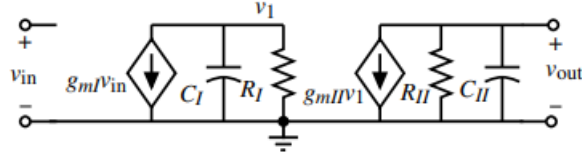


Figure 4: Small signal of Two stage OTA

Applying small signal method to solve the circuit

$$g_{mI}V_{in} + sC_1V_1 + \frac{V_1}{R_I} = 0 \quad (1)$$

$$g_{mII}V_1 + sC_1V_{out} + \frac{V_{out}}{R_{II}} = 0 \quad (2)$$

where,  $g_{mI} = g_{m1}$  and  $g_{mII} = g_{m6}$  Solving above equations we get,

$$A_{v_o} = -g_{m1}g_{m6}R_IR_II, P_I = \frac{-1}{R_IC_I}, P_{II} = \frac{-1}{R_{II}C_{II}} \quad (3)$$

where  $R_I$  equals  $r_{o2}||r_{o4}$  and  $R_{II}$  equals  $r_{o6}||r_{o7}$  and  $C_I$  and  $C_{II}$  include parasitics capacitances at input and output terminals.

**NOTE** These values of poles are so close to each other that they do not lead to a phase margin of  $45^\circ$ .

Hence, we need a miller compensation technique to achieve a phase margin of more than  $45^\circ$  by doing pole splitting.  $\therefore$  we look at the Miller Compensation network,

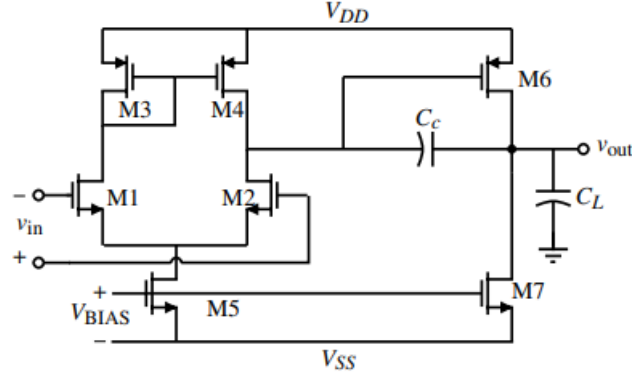


Figure 5: Miller Compensated Two Stage OTA

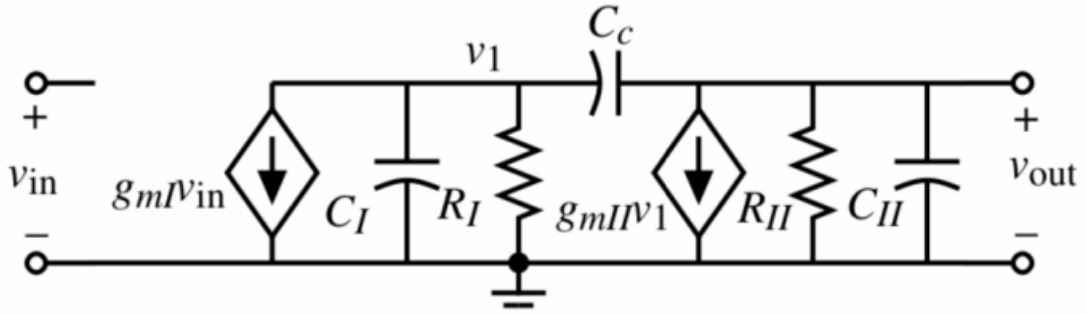


Figure 6: Small signal of Miller compensated Two stage OTA

From the small signal model

$$\frac{V_{out}}{r_{o2}} + SC_{o2}V_{out} + gm_2V_1 + (V_{out} - V_1)SC_C = 0 \quad (4)$$

$$(V_{out} - V_1)SC_C = \frac{V_1}{r_{o1}} + V_1SC_1 + gm_1V_{in} \quad (5)$$

Solving these small signal equations,

$$\frac{V_{out}}{V_{in}} = \frac{gm_I gm_{II} R_I R_{II} (1 - \frac{SC_c}{gm_{II}})}{1 + S[R_I(C_{o1} + C_c) + R_{II}(C_{o2} + C_c) + gm_2 R_I R_{II} C_c] + s^2 R_I R_{II} (C_{o1} C_{o2} + C_{o2} C_c + C_{o1} C_c)} \quad (6)$$

For DC gain,

$$A_{vo} = gm_I gm_{II} R_I R_{II}, P_I = \frac{-1}{gm_2 r_{o1} r_{o2} C_c}, P_{II} = \frac{-gm_2}{C_L} \quad (7)$$

where  $R_I$  equals  $r_{o2} || r_{o4}$  and  $R_{II}$  equals  $r_{o6} || r_{o7}$ .

**NOTE** Since,  $C_c$  comes in denominator of pole 1 and the value of  $C_c$  is large in the orders of  $\mu A$ ,  $\therefore$  pole 1 has a lower value and moves towards origin. On the other hand, pole II has  $gm_2$  in numerator as compared to having  $r_{o6}$  in denominator previously, increases its value and thus pole II moves away from the origin and beyond the UGB frequency, which is given as ,

$$\omega_u = \frac{gm_1 r_1 gm_2 r_2}{r_1 gm_2 r_2 C_c} = \frac{gm_1}{C_c} \quad (8)$$

Thus, we see that pole has been splitted and a phase margin of greater than  $45^\circ$  can be achieved. The same has been shown in phase plot.

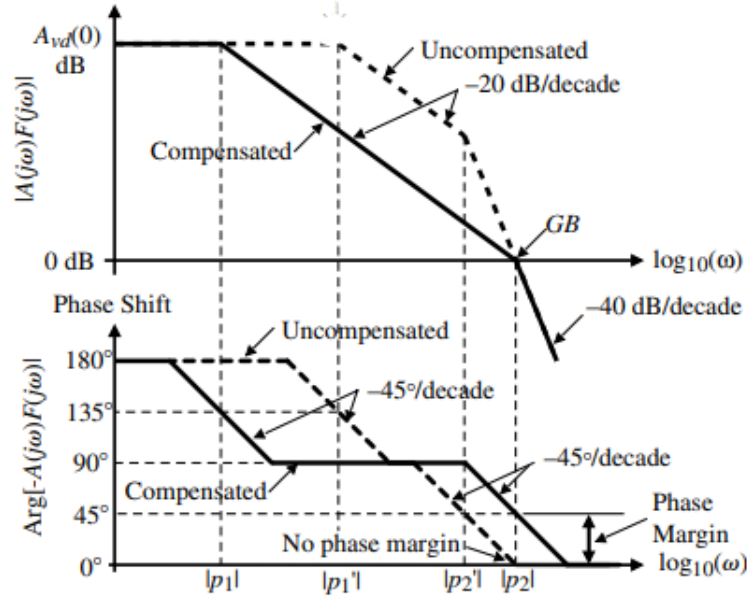


Figure 7: Phase plot showing a margin of  $45^\circ$

### 3 Calculations used for all the specifications

#### 3.1 Relation between pole and zeroes frequency with respect to UGB frequency

For 2 poles and 1 zero we have a general transfer function of the form

$$L(S) = -\frac{A_0(1 - \frac{S}{Z_1})}{(1 + \frac{S}{P_1})(1 + \frac{S}{P_2})} \approx \frac{-A_0}{(1 + \frac{S}{P_1})(1 + \frac{S}{P_2})} \quad (9)$$

where,  $A_o$ = open loop DC Gain. Given the assumption that Zero is very far away so we can neglect Zero,  $\therefore$  the above equation summarizes as

$$L(S) = -\frac{A_0}{(1 + \frac{S}{P_1})(1 + \frac{S}{P_2})} \approx \frac{-A_0}{(1 + \frac{S}{P_1})(1 + \frac{S}{P_2})} \quad (10)$$

Give the phase margin as  $65^\circ$ ,

$$PM = 180 - \tan^{-1}\left(\frac{w_u}{w_{p1}}\right) - \tan^{-1}\left(\frac{w_u}{w_{p2}}\right) \quad (11)$$

$$65^\circ = 180^\circ - 90^\circ - \tan^{-1}\left(\frac{w_u}{w_{p2}}\right)$$

$$\tan^{-1}\left(\frac{w_u}{w_{p2}}\right) = 25^\circ$$

By solving this we get

$$\omega_p = 2.2\omega_u \quad (12)$$

In simulations took  $w_p=4w_u$ , thus obtaining a phase margin of  $75^\circ$

It is give that  $\omega_z$  is 10 times the UGB frequency, Thus,

$$\omega_p = 10\omega_z \quad (13)$$

### 3.1.1 Calculating UGB frequency ( $W_u$ )

We know that  $A\beta = 1$

Where  $A_o$  is the open loop DC gain and the capacitor expression forming the  $\beta$  network  
Substituting  $S=j\omega$  and taking mod of the expression, we get,

$$\frac{A.P_1}{|j\omega|} * \frac{C_2}{C_1 + C_2} = 1 \quad (14)$$

$$\omega_u = A * \frac{C_2}{C_1 + C_2} * P_1 \quad (15)$$

$$\omega_u = \frac{g_{m1}(ro1||ro2)g_{m7}(ro6||ro7)}{g_{m7}C_c(ro6||ro7)(ro2||ro4)} * \frac{c_2}{C_1 + C_2} \quad (16)$$

By solving above equation we get -

$$W_u = \frac{g_{m1}}{C_c} * \frac{C_2}{C_1 + C_2} \quad (17)$$

### 3.2 Calculating Miller capacitance $C_c$

We have,  $w_z=10w_u$ , Substituting the values,

$$\frac{g_{m7}}{C_c} = 10 * \frac{g_{m1}}{C_c} * \frac{C_2}{C_1 + C_2} \quad (18)$$

$$g_{m7} = g_{m1} \quad (19)$$

We have,  $w_{p2}=4w_u$ , Substituting the values,

$$\frac{g_{m7}}{C_L} = 4 * \frac{g_{m1}}{C_c} * \frac{C_2}{C_1 + C_2} \quad (20)$$

$$C_c = 0.4C_L \quad (21)$$

given,  $C_L = 10\text{pF}$ , we have,  $C_c = 4\text{pF}$

### 3.3 Calculation of (W/L) of M5,M6 and M7

Given that,

$$SR = \frac{10V}{\mu S} = \frac{I_{d5}}{C_c} = \frac{I_{d6}}{C_c + C_L + \frac{C_1 C_2}{C_1 + C_2}} \approx \frac{I_{d6}}{C_c + C_L} \quad (22)$$

Now, Substituting the value of  $C_c$ ,

$$I_{d5} = 10^7 * 4 * 10^{-12} = 40\mu A \quad (23)$$

and Substituting the value of  $C_c$  and  $C_L$ ,

$$I_{d6} = 10^7(C_c + C_L) = 10^7(4 * 10^{-12}) = 140\mu A \quad (24)$$

We know that  $I_{d5}$  is given by the square law equation,

$$I_{d5} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_5 (V_{GS} - V_{th})^2 = 40\mu A \quad (25)$$

Substituting the values, we get  $(W/L)_5$

$$40\mu A = \frac{300\mu}{2} \left(\frac{W}{L}\right)_5 (0.1)^2 \quad (26)$$

$$(W/L)_5 = 80/3 \quad (27)$$

We know that  $I_{d6}$  is given by the square law equation,

$$I_{d6} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_6 (V_{GS} - V_{th})^2 = 140\mu A \quad (28)$$

Substituting the values, we get  $(W/L)_5$

$$140\mu A = \frac{300\mu}{2} \left(\frac{W}{L}\right)_6 (0.1)^2 \quad (29)$$

$$(W/L)_6 = 280/3 \quad (30)$$

We Know that  $W/L_7$  is 2 times the  $W/L_6$ ,

$\therefore$ ,

$$(W/L)_7 = 560/3 \quad (31)$$

### 3.4 Calculation of (W/L) of M1, M2, M3 and M4

We know that  $I_{d1,2}$  is given by the square law equation,

$$I_{d1,2} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_{1,2} (V_{GS} - V_{th})^2 = I_{d5}/2 = 20\mu A \quad (32)$$

Substituting the values, we get  $(W/L)_{1,2}$

$$20\mu A = \frac{300\mu}{2} \left(\frac{W}{L}\right)_{1,2} (0.1)^2 \quad (33)$$

$$(W/L)_{1,2} = 40/3 \quad (34)$$

We Know that  $W/L_{3,4}$  is 2 times the  $W/L_{1,2}$ ,

$\therefore$ ,

$$(W/L)_{3,4} = 80/3 \quad (35)$$

## 4 Plots required to verify the achieved specifications

### 4.1 AC GAIN AND PHASE

First, we constructed a miller compensated open loop circuit to verify the phase margin of the system. Schematic and the results are as shown below.

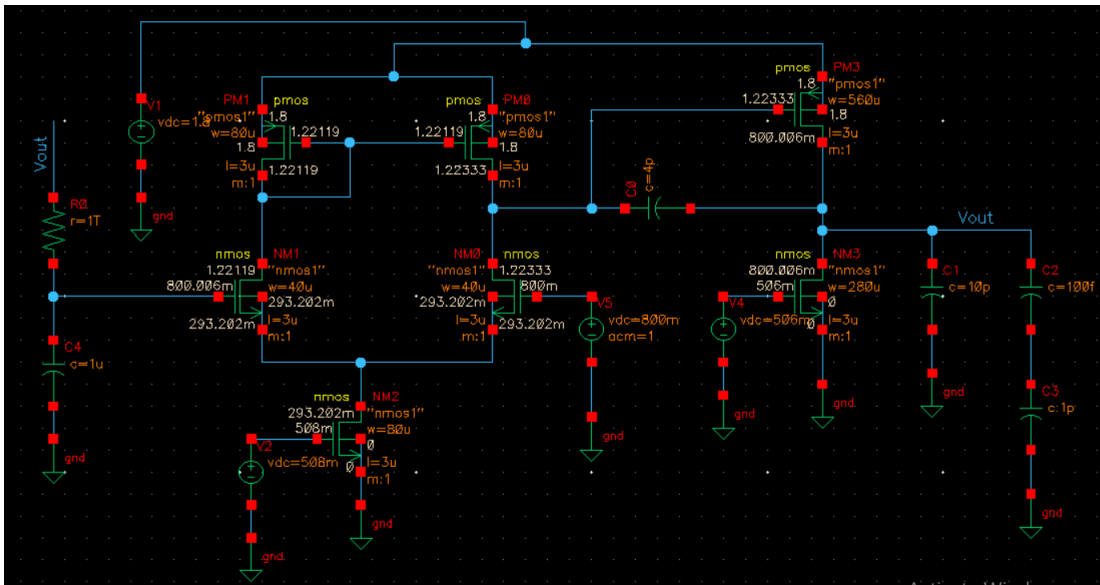


Figure 8: Schematic of Open loop Compensated OTA

Here is the plot showing the resultant phase margin achieved.

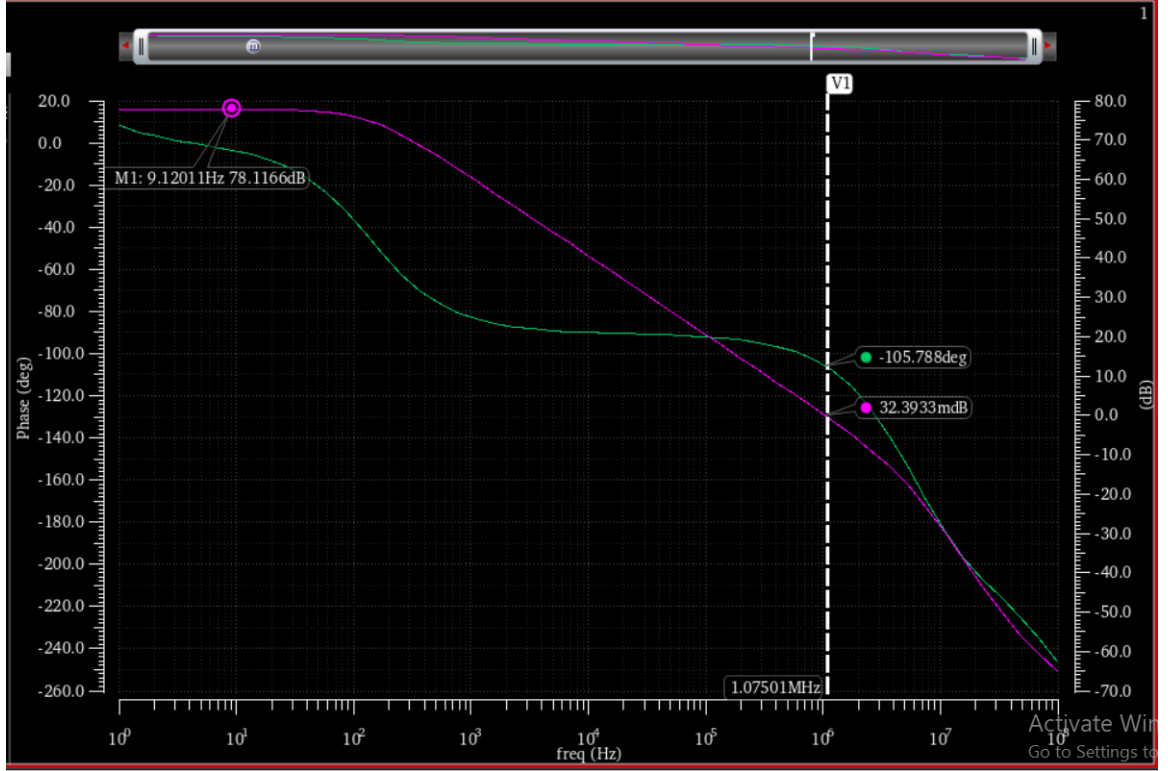


Figure 9: Frequency plot showing AC gain and phase

From the plot it can be seen that the open loop gain is around 78dB and the phase margin is  $(180+(-105.78))^{\circ} = 74.22^{\circ}$ .

## 4.2 Mid band gain and Bandwidth

Next, Coming to closed loop circuit, Schematic and the results are as shown below.

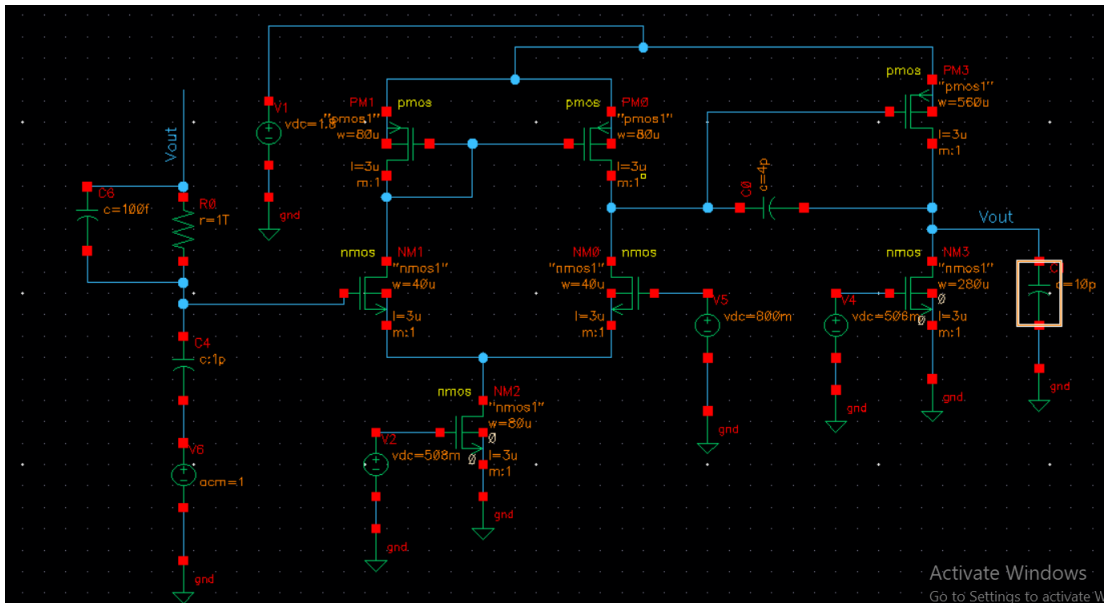


Figure 10: Schematic of closed loop Compensated OTA

Here is the plot showing the resultant phase margin achieved.

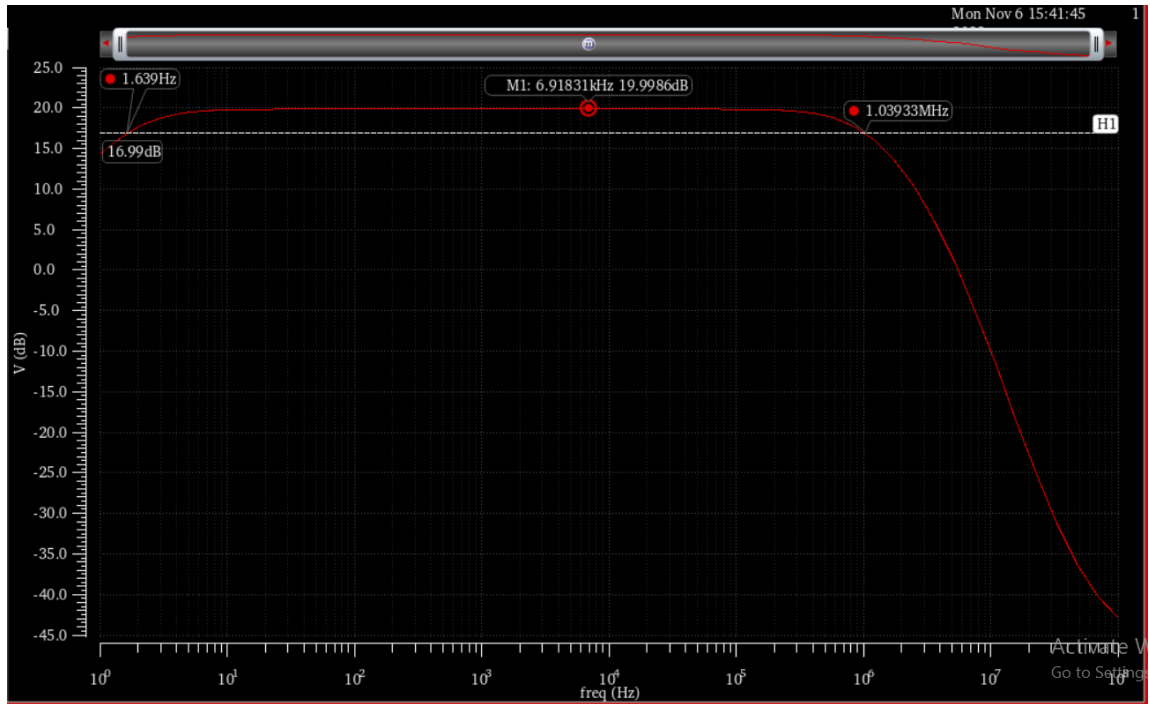


Figure 11: Frequency plot showing mid band gain and bandwidth

From the plot it can be seen that the mid band gain comes out to be 19.99dB and the bandwidth to be 1.04MHz which is greater than 1MHz.

### 4.3 SLEW RATE VERIFICATION

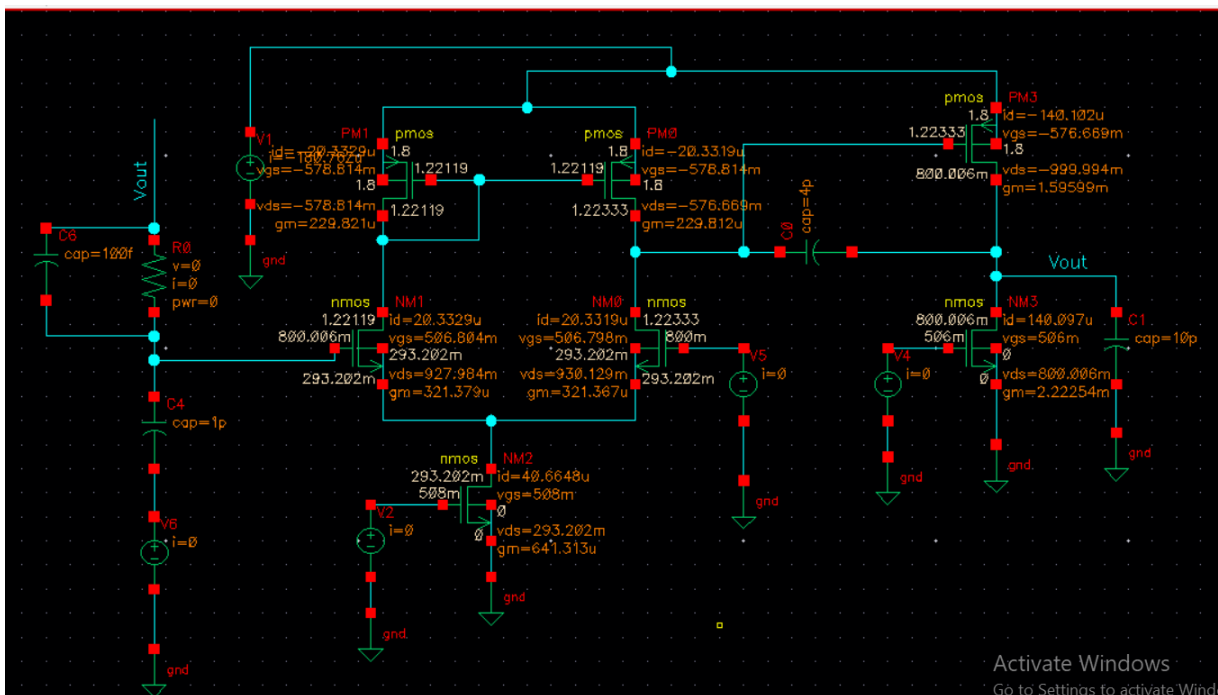


Figure 12: DC analysis of the Closed Loop circuit.



From the DC aalysis obtained, it can be seen that  $I_{d5}$  is equal to  $40\mu A$  and  $I_{d6}$  is equal to  $140\mu A$ . From the slew rate expression,

$$Slewrate = I_{d5}/C_c = 40\mu A/4pF = 10V/\mu S \quad (36)$$

$$Slewrate = I_{d6}/(C_c + C_L) = 140\mu A/14pF = 10V/\mu S \quad (37)$$

Thus slew rate is  $10V/\mu S$ .

#### 4.4 Calculation of % gain error:

$$A_{CL} = \frac{A}{1 + A\beta} \quad (38)$$

$$\Delta A_{CL} = \frac{-1}{\beta(1 + A\beta)} \quad (39)$$

$$\%gainerror = \frac{\Delta A}{A} * 100 = \frac{1}{A\beta} * 100 \quad (40)$$

$$\text{loop gain, } A\beta = 78.11\text{dB} = 8044.51$$

$$\%gainerror = \frac{1}{8044.51} * 100 = 0.0124\% \quad (41)$$

**NOTE :** The experiment is carried out at  $27^\circ C$  which is inside the given range.