EE663: PLL Course Project

Phase 2

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AIM: Design a complete PLL at the transistor level in Cadence Design Suit using a TSMC 65nm CMOS technology.

1 Introduction

A phase-locked loop (PLL) is a circuit designed to align the output signal of an oscillator with a reference or input signal, ensuring synchronization in both frequency and phase within a given system. In the synchronized or locked state, the phase error between the output signal of the oscillator and the reference signal is either zero or remains constant. If a phase error accumulates, a control mechanism intervenes to minimize the phase error by acting on the oscillator. In this control system, the phase of the output signal becomes locked to the phase of the reference signal, hence the term "phase-locked loop." The project aims to develop a square-wave output frequency generator, primarily utilizing the PLL as a frequency multiplier, achieved by multiplying the frequency of the reference oscillator.

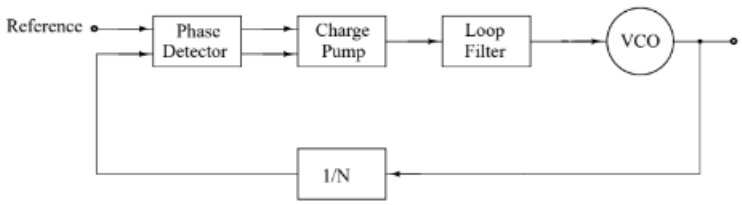

Figure 1: Block Diagram of phase-locked loop

2 Given Data:

- **Reference frequency:** 4×10^7
- **Output Frequency:** 1.28×10^9
- **Divider:** 32

3 Calculations:

- Assumed values:

  Phase margin(ϕ_m) = 65°

  K_{VCO} from Simulation = 2.37G.

- Calculation of b:

$$b = 2(tan^2\phi_m + tan\phi_m\sqrt{1 + tan^2\phi_m}) \tag{1}$$

$$b = 2(4.59 + 2.14\sqrt{5.59})$$

b=19.34

- Calculation of ω_{uloop}:

$$\omega_{uloop} = \frac{\omega_{ref}}{20} = \frac{2\pi 4\times 10^7}{20} = 12.56 \times 10^6 \text{ rad/sec}$$

- Calculation of ω_z:

$$\omega_z = \frac{\omega_{uloop}}{\sqrt{1+b}} \tag{2}$$

$$\omega_z = \frac{12.56\times 10^6}{\sqrt{1+19.34}}\text{=2.78M}$$

- Solving for I_o and capacitance, C_1

From simulation we have $K_{VCO} = 2.37$G

$$K_{vco} = \frac{N}{I_0} \times \frac{(b+1)^{1.5}}{b} \times C_1\omega_z^2 \tag{3}$$

$$K_{vco} = \frac{32}{I_0} \times \frac{(20.34)^{1.5}}{19.34} \times C_1(2.78 \times 10^6)^2 \tag{4}$$

$$\frac{K_{vco}I_0}{C_1} = 1.17 \times 10^{15} \tag{5}$$

$$C_1 = 2.02 \times 10^{-6} I_o \tag{6}$$

Considering $C_1 = 20$pF.
we get $I_o = 10\mu$A.

- Calculation of C_2:

$$b = \frac{C_1}{C_2} \tag{7}$$

$$19.34 = \frac{20p}{C_2} \tag{8}$$

Calculating, $C_2 = 1.03$pF.

- Calculation of Resistance, R:

$$\omega_Z = \frac{1}{RC_1} \tag{9}$$

$$2.78M = \frac{1}{R \times 20p} \tag{10}$$

Solving, we get R= 17.98Kω.

4 Design of Phase Frequency Detector (PFD)

In a PLL, the phase-frequency detector serves the crucial function of comparing the phases of the reference signal and the feedback signal. This detector transforms the phase difference into a voltage (or current), which is subsequently processed through a Low-Pass Filter (LPF) before being converted into the phase for the Voltage-Controlled Oscillator (VCO).

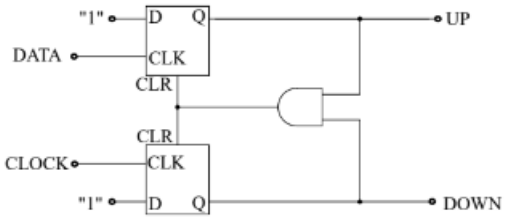

Figure 2: Circuit of PFD

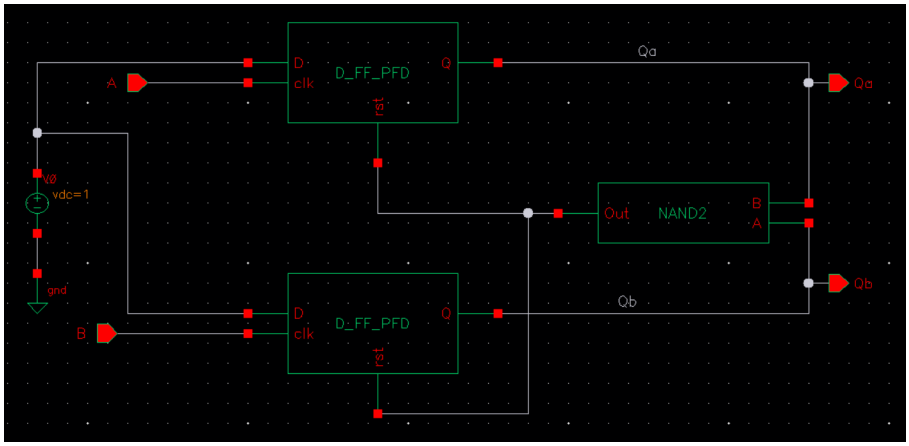

Figure 3: Schematic of PFD

Implementation of PFD has been car4ried out using D Flip flops and AND gate, Schematics of which has also been attached below.

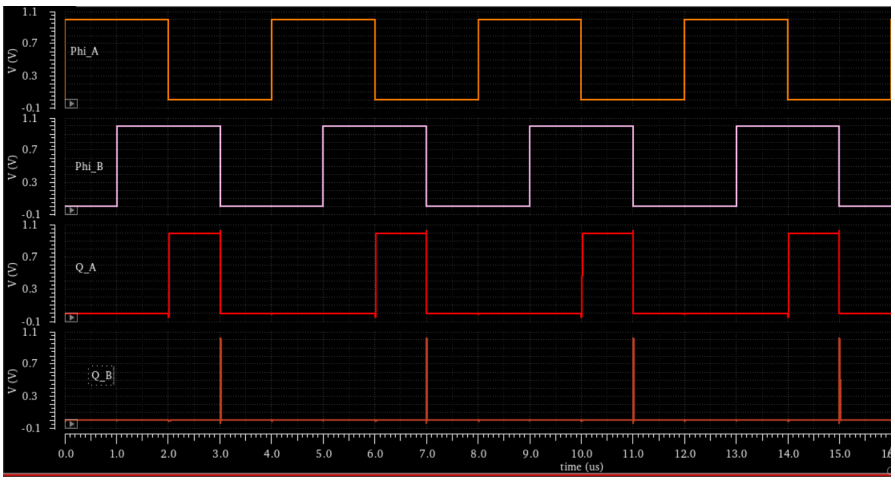

Figure 4: Output of PFD block

From the output wave form we can see the output Q_A goes high whenever it sees a phase

difference. Point to be noted is that it goes high for once in one complete clock cycle and remains low for other variation in that clock cycle.

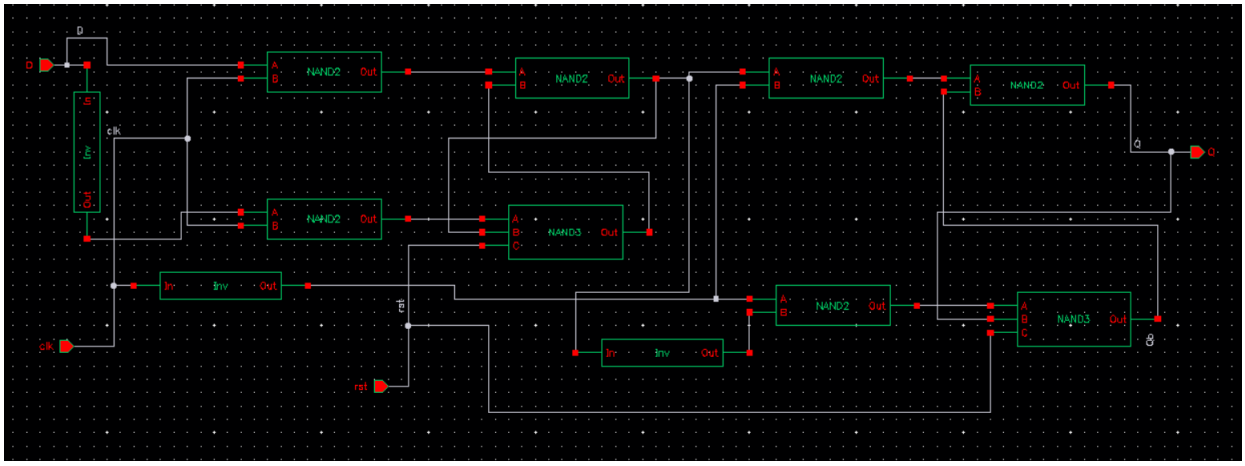

Figure 5: Schematic of D FF

D Flip Flop has been carried out by implementing master slave configuration and with the help of NAND gate.
Schematic of NAND has also been attached here which has been implemented by pmos and nmos transistors.

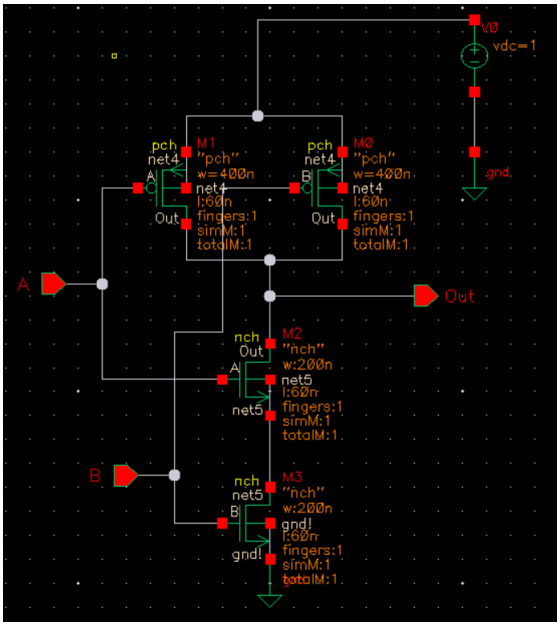

Figure 6: Schematic of NAND gate.

5 Design of the Charge Pump

The charge pump consists of two switches equipped with two symmetrical current sources. One current source is linked to a positive power supply, while the other is connected to a negative one. The switches alter their states based on the UP and DN signals. The output of the low-pass filter (LPF), determined by the UP and DN signals, is the Voltage-Controlled Oscillator (VCO) control signal.

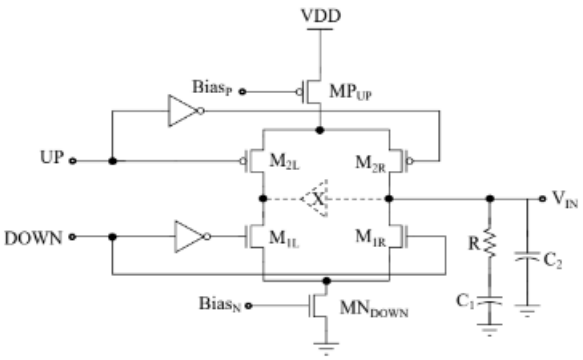

Figure 7: Circuit for charge pump with loop filter

Initially we made a buffer and the schematic of which has been attached. For the buffer as the name suggests output should follow the input. So, we performed transient analysis to verify the buffer. The results are attached here with.

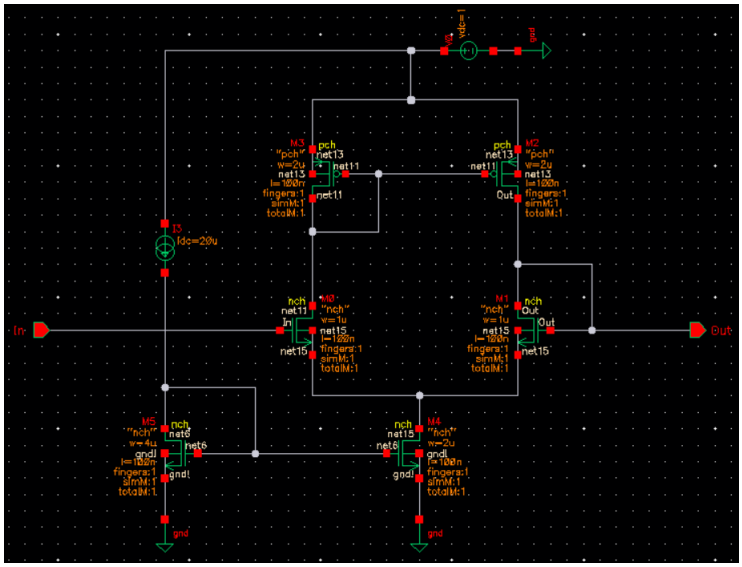

Figure 8: Schematic of Buffer

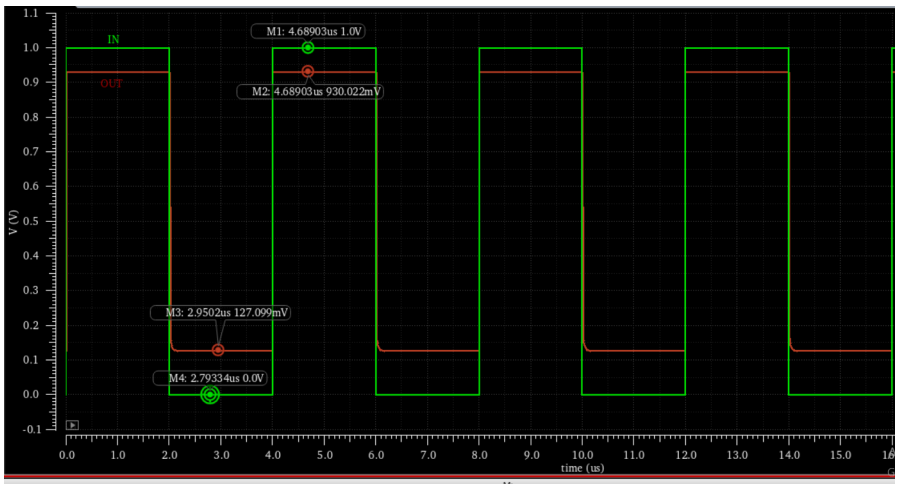

Figure 9: Output of BUFFER

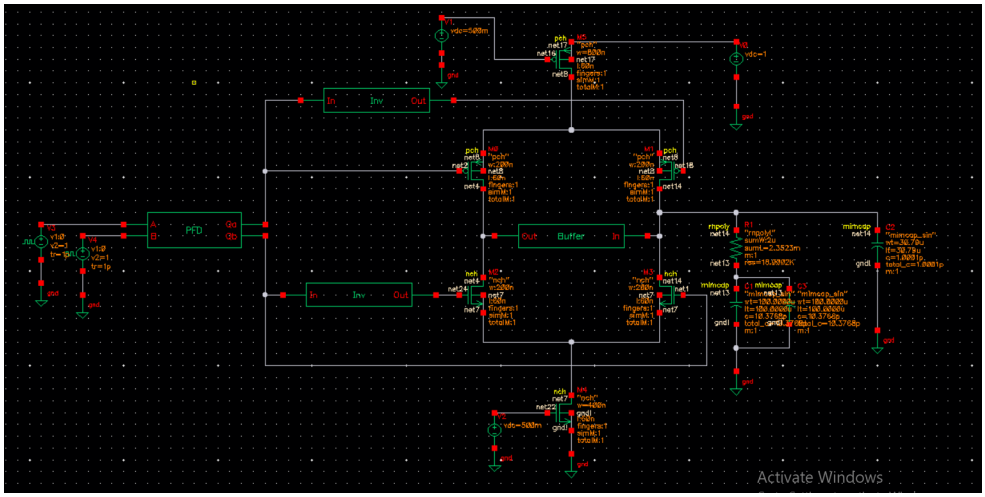

Figure 10: Schematic of Charge Pump with Loop Filter

Output of charge pump is a voltage developed across load capacitor. A similar kind of charging discharging curve is obtained.

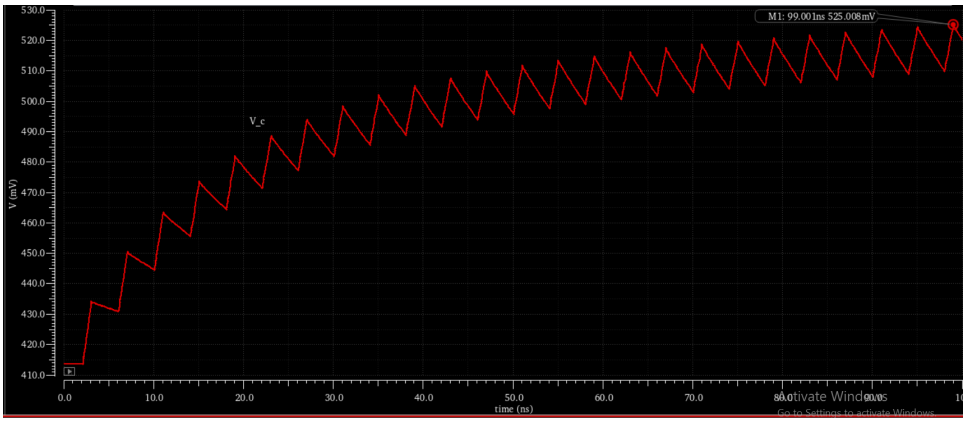

Figure 11: Output of Charge Pump with Loop Filter

6 Design of Voltage Controlled Oscillator (VCO)

VCOs play a pivotal role in the architecture of a PLL. The fundamental concept behind a VCO is to generate a clock signal while adhering to the Barkhausen criteria for oscillation. According to the Barkhausen criteria, the magnitude of the VCO's transfer function at the oscillation frequency is unity, and the phase is at -180 degrees and this negative phase is changed in possitive 180 defree phase by putting the 2 inverters in series at the output of the VCO.

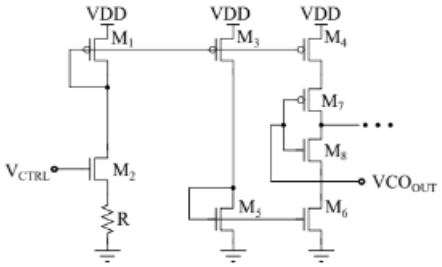

Figure 12: Circuit for voltage controlled oscillator

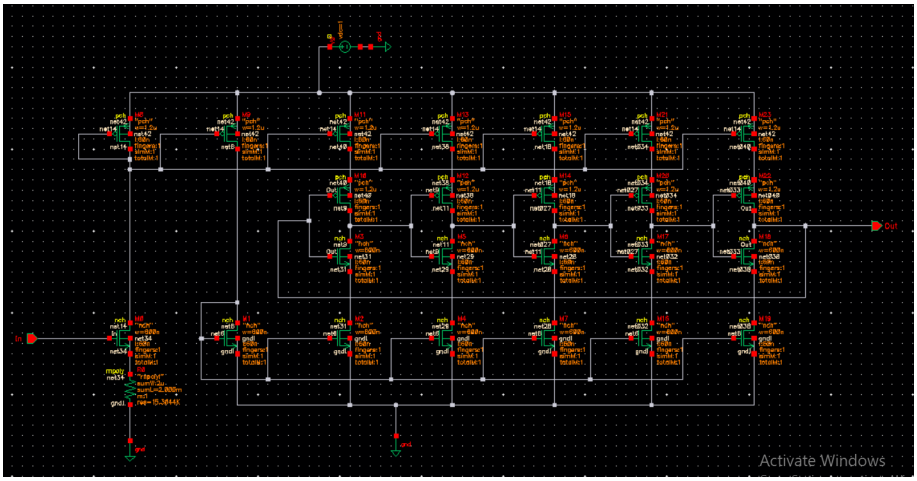

Figure 13: Schematic of VCO

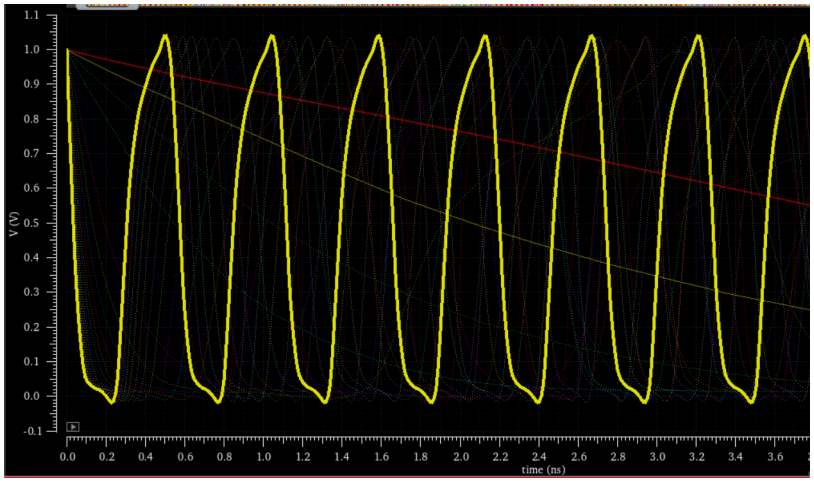

Figure 14: Output of VCO

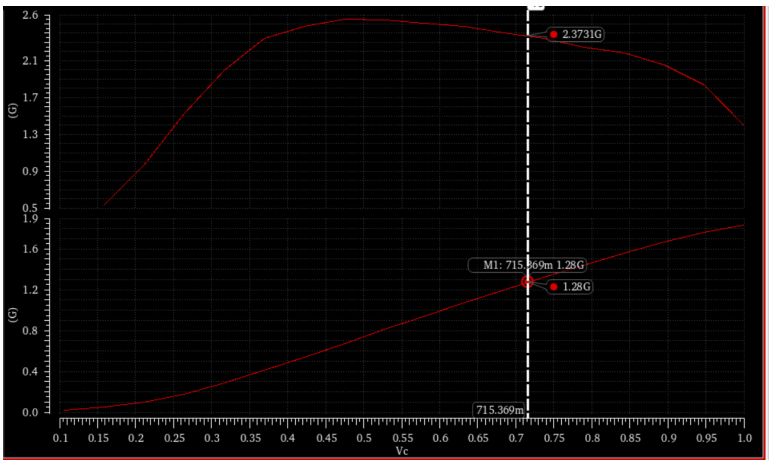

Figure 15: K_{vco} from simulation

From the simulation value of K_{VCO} is 2.37G.

7 Design of Divider network

Divider is used to divide the output frequency by the divider value. Divider has been implemented by the D Flip flop by connecting the Q_{bar} to the D input and cascading the stages to form the network. For implementing we have used 5 D flip flops to get the Divide by 32 network. Schematic and output has been attached herewith.

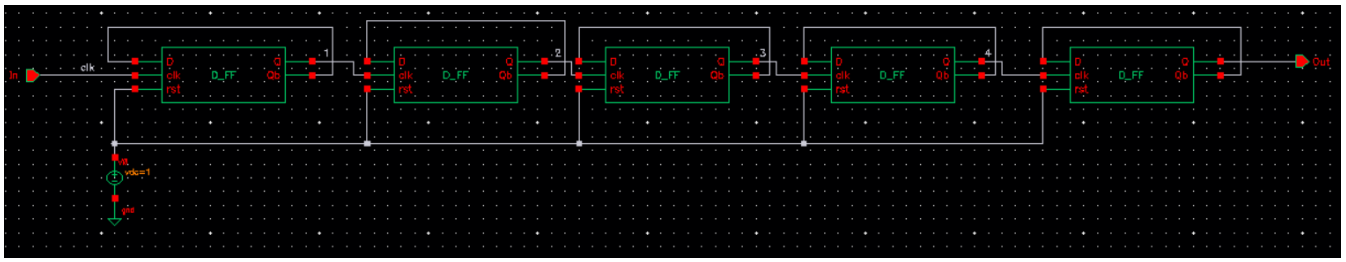

Figure 16: Schematic of Divider

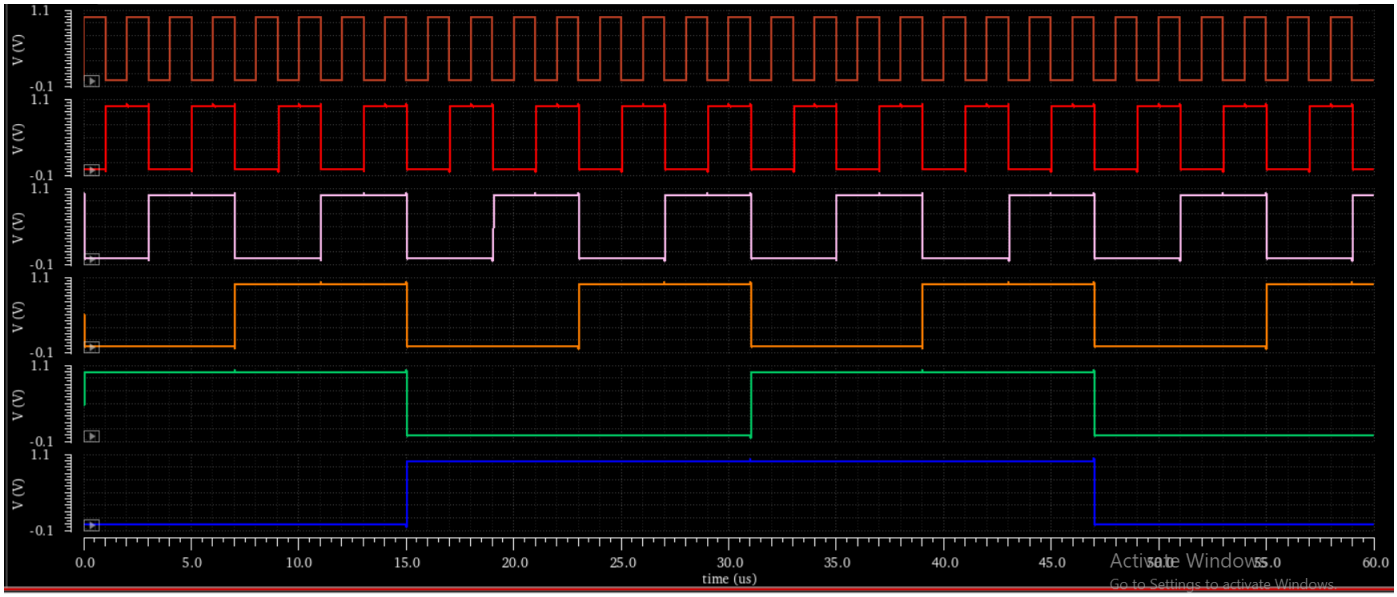

Figure 17: Output of Divider network

8 Phase Lock Loop (PLL)

Now all the blocks has been connected as per the block diagram and the final output is seen.

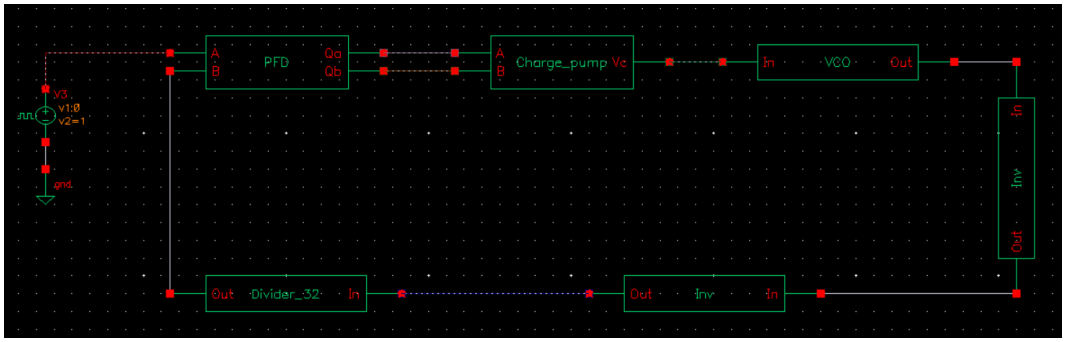

Figure 18: Schematic of PLL

So, finally we will be looking at all the outputs when the given reference frequency of 4×10^7 Hz is applied. Here the time period is 25n seconds which is given as input.

- output of PFD.

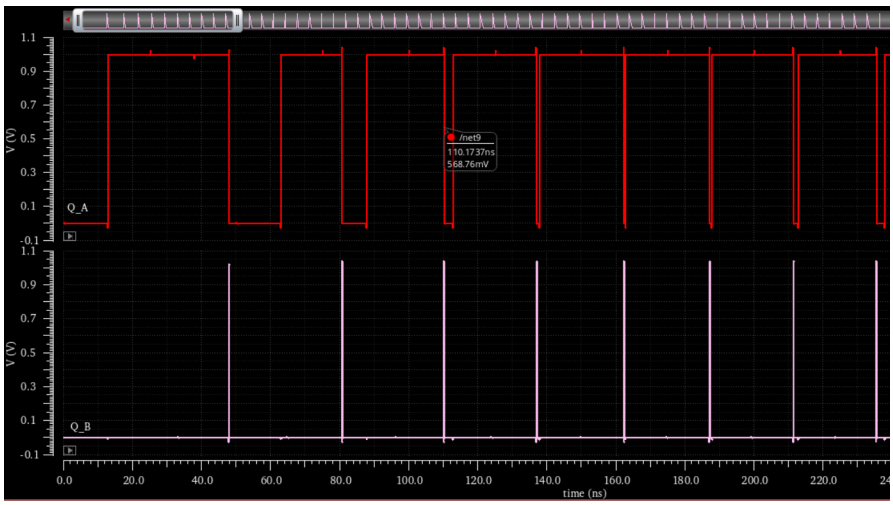

Figure 19: Output of PFD

- output of charge pump is the control voltage.

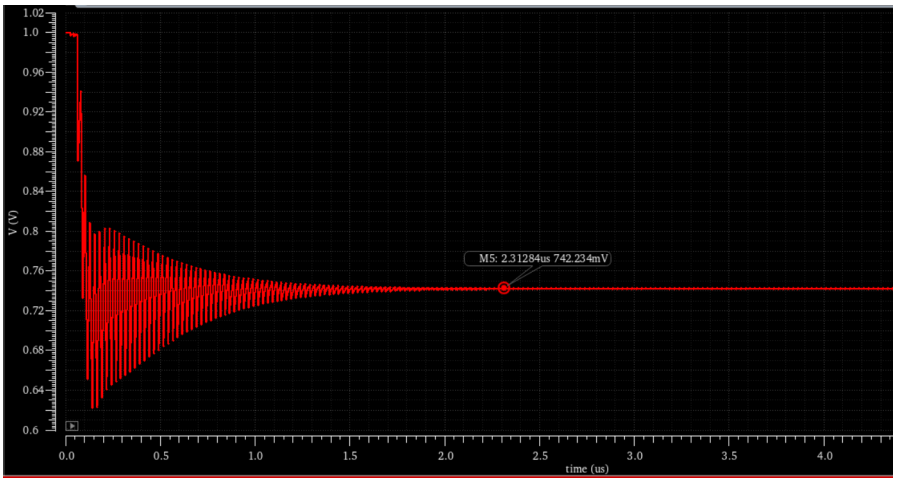

Figure 20: Control voltage

The value of control voltage comes out to be 742mV.

- output of VCO.

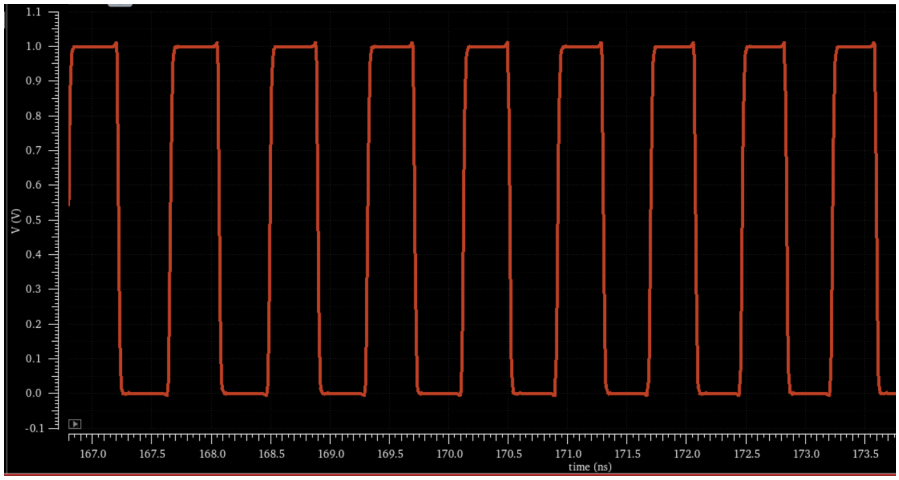

Figure 21: Output of VCO

The output of VCO is a sine waveform which is converted to the square waveform when passed through the inverter circuit. Two inverters are used to get a perfect pulse waveform output.

- Final locked Frequency.

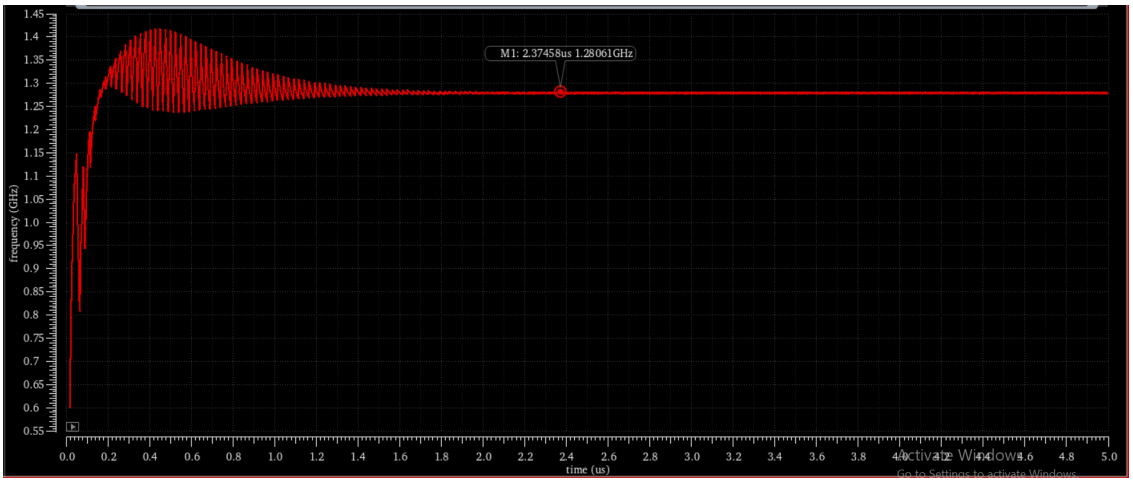

Figure 22: Output of PFD

Finally, the frequency is locked at 1.28GHz which is shown by the above waveform.

9 References

1.) Behzad Razavi, "Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level" , Cambridge University Press, 2020.

2.)Design of a phase locked loop based clocking circuit for high speed serial link applications by Ratan, Rishi , 2014-05-30T16:47:43Z (https://hdl.handle.net/2142/49509)

3.) P. K. Hanumolu, M. Brownlee, K. Mayaram and Un-Ku Moon, "Analysis of charge-pump phase- locked loops," in IEEE Trans. on Circuits and Syst. I: Regular Papers, vol. 51, no. 9, pp. 1665-1674, Sept. 2004.

4.) H. R. Rategh, H. Samavati and T. H. Lee, “A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver,” in IEEE J. of Solid-State Circuits,vol. 35, no. 5, pp. 780-787, May 2000.