4 Integrated Circuit Technology

Possible Future Transistor Options

- Advanced Channel Materials
  - III-V and Ge channel materials
- Multi-Gate Fin Transistors
  - Non planar architecture
- Tunnel Transistors
  - New transport mechanism

Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET

III-V Materials for NMOS Channel?

+ Low m* Γ valley ⇒ High υ_{inj}

- Low m* Γ valley ⇒ Low m^*_{DOS}
  ⇒ Low Q_{INV}

- 2-D Quantization:
  ⇒ Charge transfer from low mass Γ to high mass X & L valleys
  ⇒ Lowers υ_{inj}

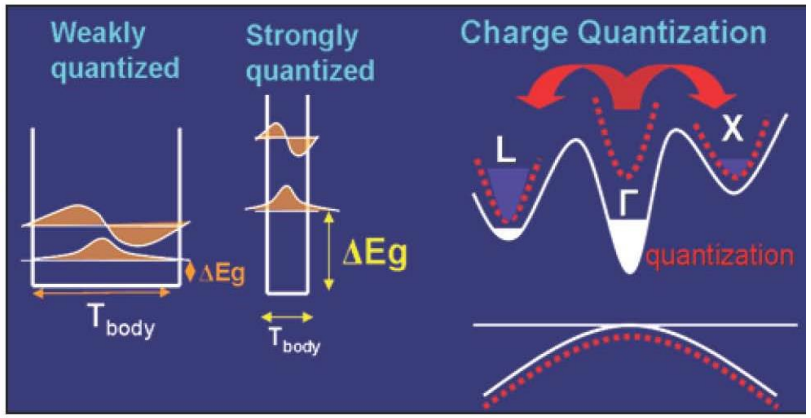
- Low Eg ⇒ Large Ioff (junction)

- High ε ⇒ Poor SCE

Projecting III-V NMOS performance based on simplistic models could lead to erroneous performance assessment.

Properties of some NMOS candidates

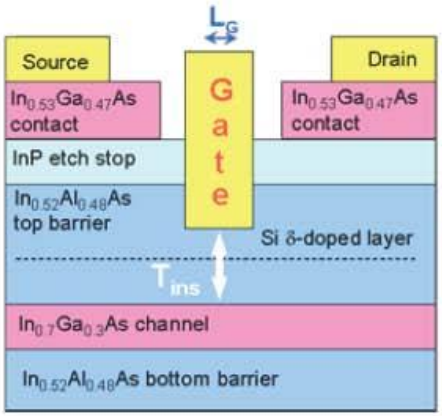
Material/Property	Si	Ge	GaAs	InAs	InSb
m_{eff}^*	0.19	0.08	0.067	0.023	0.014
μ_n (cm^2/Vs)	1600	3900	9200	40,000	77,000
E_G (eV)	1.12	0.66	1.42	0.36	0.17
ε_r	11.8	16	12.4	14.8	17.7



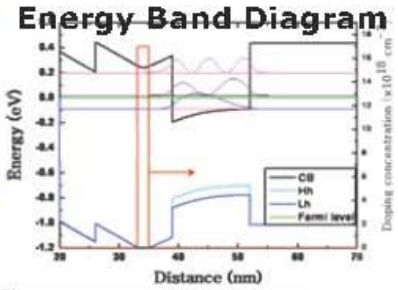
K. Saraswat et.al., IEDM 2006

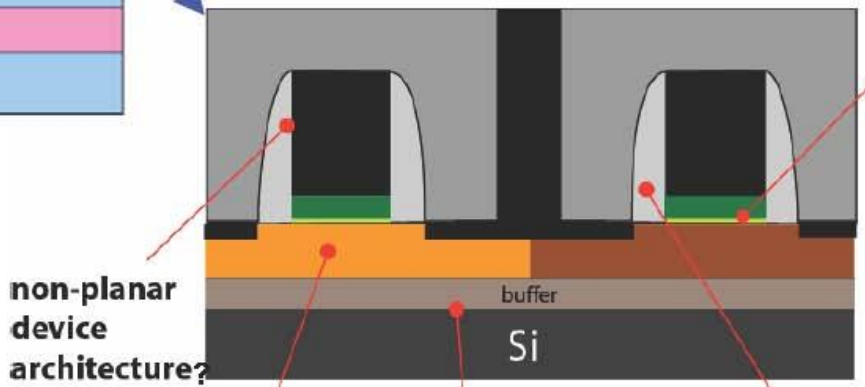
SCE: short channel effect

The Grand Challenges for III-V CMOS



- InGaAs Quantum Well channel
- InAlAs insulator (poor Jox)
- Ti/Pt/Au gate
- Non-self aligned contacts





high-K dielectric gate insulator

J. Del Alamo
IEDM 2007

non-planar device architecture?

III-V p-type channel device

Scalable, self-aligned, E-mode device architectures

III-V epitaxy on large-area Si wafers

Souce: Intel

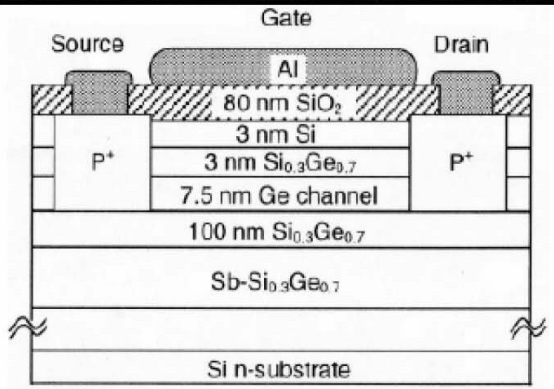
Ge Transistor- Back to the Future?

- **Advantages:**
  - + Best hole mobility (unlike III-V)
  - + Si(Ge) already used in logic tech
  - + Col-IV: Non-Polar
- **Challenges:**
  - - Reference device is highly strained silicon
  - - Poor HiK interface:
    - * Need better understanding
    - * Buried strained QW Ge
  - - Higher dielectric constant
    - * Poorer SCE
  - - Worse parasitic resistance
    - * Worse dopant activation

Material ⇒ Property ⇓	Si	Ge	GaAs	InAs	InSb
Electron mobility	1600	3900	9200	40000	77000
Hole mobility	430	1900	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric constant	11.8	16	12.4	14.8	17.7

K. Saraswat et.al., IEDM 2006.

Buried Strained Ge Quantum Well



(**U. Tokyo**, APL 2002)

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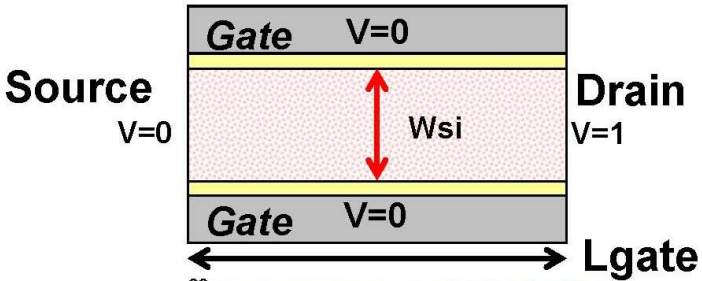
Multi-Gate Transistor Architecture

$$\frac{\partial^2\Phi}{\partial x^2}+\frac{\partial^2\Phi}{\partial y^2}=\frac{qN_A}{\varepsilon_{Si}}$$

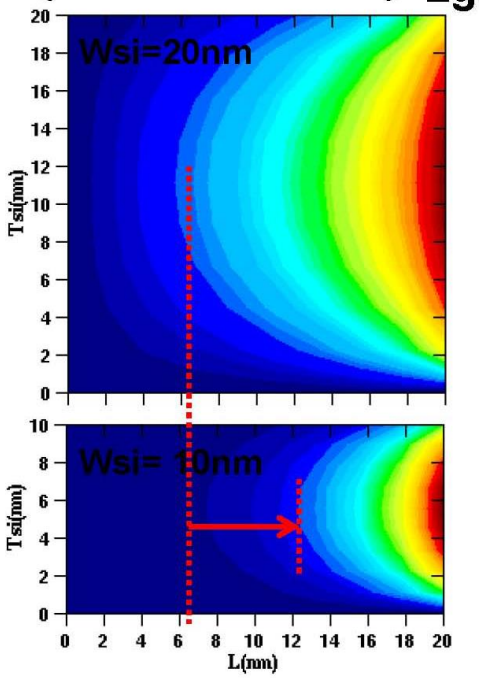


Multi-Gate Transistors have better SCE:

- Gates reduce spread of V_{drain} Enables lower threshold voltage ($\uparrow I_D$)
- Enable lower channel doping ($\uparrow\mu$)

Multi-Gate Transistors have lower E_{EFF}:

- Optimum gate work function is away from band-edge leading to lower Eeff ($\uparrow\mu$)



SCE: short channel effect(s)
E_{eff}: transverse (channel) electric field)

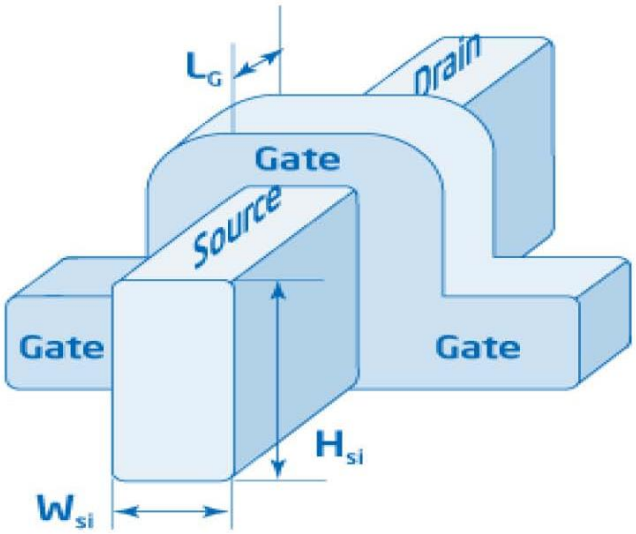
Souce: Intel

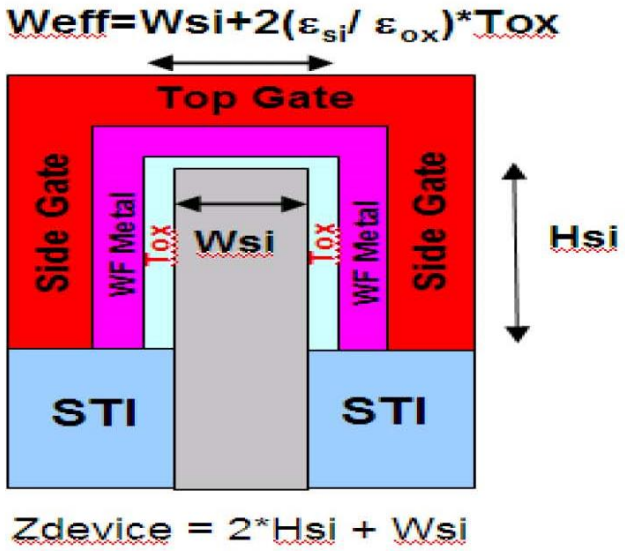
Multi-Gate Transistors Implementation

Multi-Gate Fin Transistor:

++ Self Aligned structure for S/D

-- Non-Planar structure



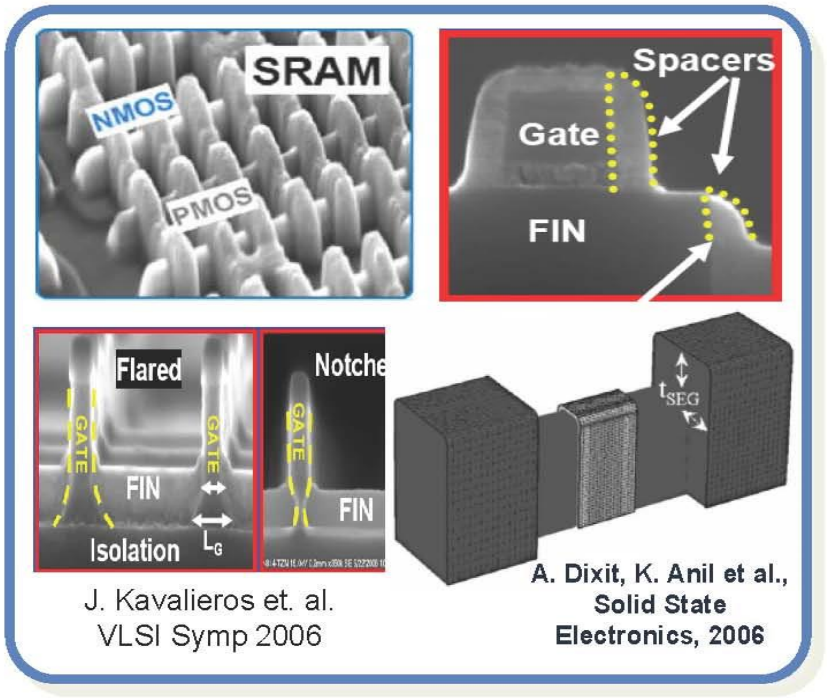


Multi-Gate Fin Transistor

Souce: Intel

Top Challenges for Multi-Gate Fin Transistors

- **Implement High Strain in Fins?**
  - Planar Ref= Highly strained
  - 4-5x p-mobility enhancement
  - High level of fin strain NOT published to date
- **High Parasitics in Fin Transistors**
  - Narrow fins lead to high Rext
  - Fin architecture may also lead to higher fringe capacitance
- **Manufacturing worthy Patterning**
  - Fin, Gate and Spacer patterning will be extremely challenging in a manufacturing environment
- **Design**
  - Device Z increments quantized



- **Best published drive currents for Multi-Gate Fin Transistors are <u>significantly lower</u> than best published planar transistors to date**
- **Many significant challenges remain to be resolved for Fin Transistors**

Souce: Intel

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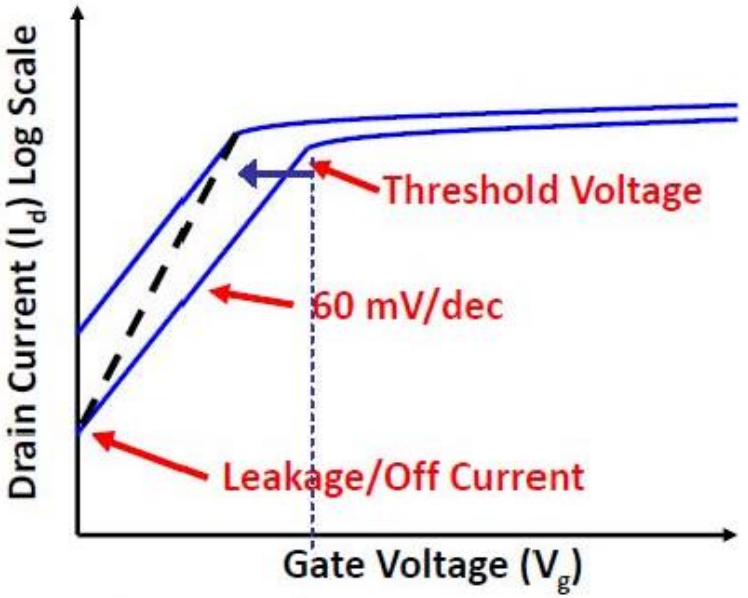
Why we Need to Beat Sub-Threshold Slope of 60mV/decade?

$I_D \sim (V_{CC}-V_{TH})$

At very low Vcc we need small V_{TH} for reasonable drive

BUT

Sub-threshold slope is limited by thermal kT/q limit
➔ Ioff increases exponentially with V_{TH} scaling.



$$S = \left(\frac{d\log I_d}{dV_g}\right)^{-1} = 2.3\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right) \geq 2.3\frac{kT}{q}$$

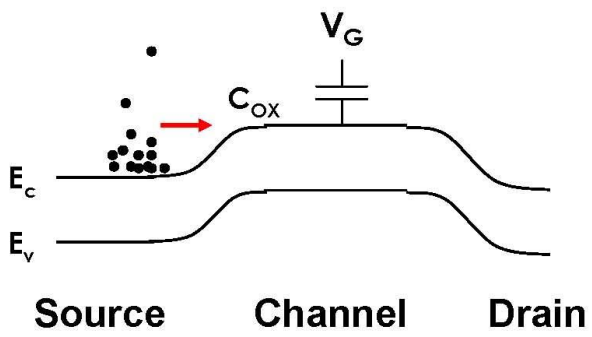
HOW TO BEAT kT/q limit?

Leakage current increases *exponentially* as device is scaled

Souce: Intel

Ultimate Frontier: Overcoming Thermal kT/q Limit

C. Hu, STEEP Program



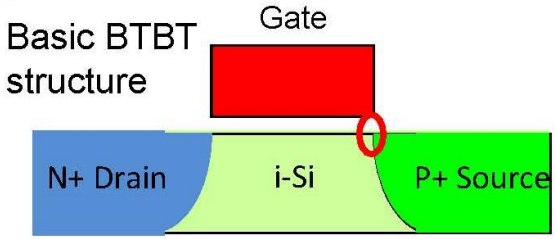
Electrons go over a potential barrier. Leakage current is determined by the Boltzmann distribution or 60 mV/decade, limiting MOSFET, bipolar, graphene MOSFET…

How to overcome the limit:

Let electrons go through the energy barrier, not over it → Tunneling

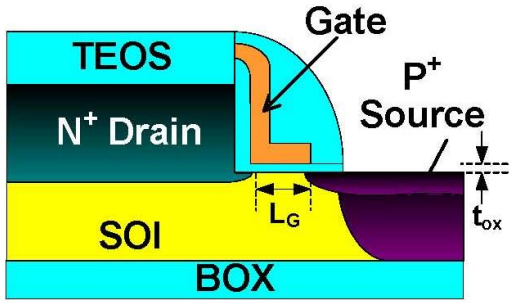
Souce: Intel

Tunnel Transistor Concept and Challenges

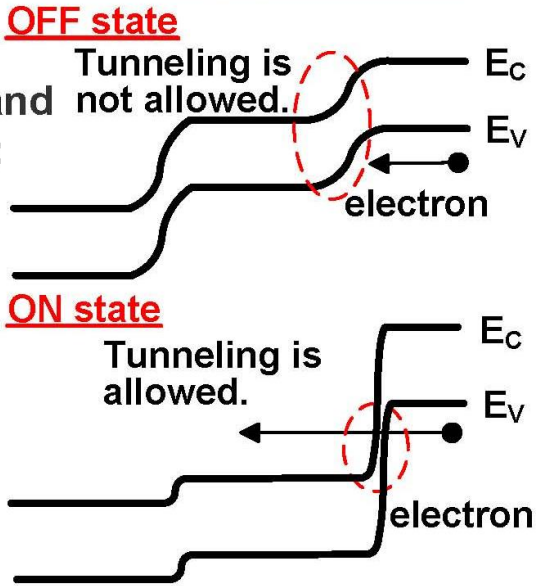


- Device behaves like reverse bias pin diode
- Positive Vgs induces electron electron channel
- Band bending allows tunneling at source channel interface ➔ Gate controlled band tunneling
- BTBT Transistor suffer from extremely poor drive current
  ➔ **Need materials with more efficient tunneling**

Structure:



Energy-band Diagrams:



W. Y. Choi *et al.* *IEEE-EDL* vol. 28, pp. 743-745, 2007

BTBT: band-to-band tunneling