5 3D Technology for Increased Integration Density

5.1 Motivation and Overview

5.2 Selected 3D-Integration Approaches

5.3 Fabrication of Through Silicon (Hole) Vias [TSV, (THV)]

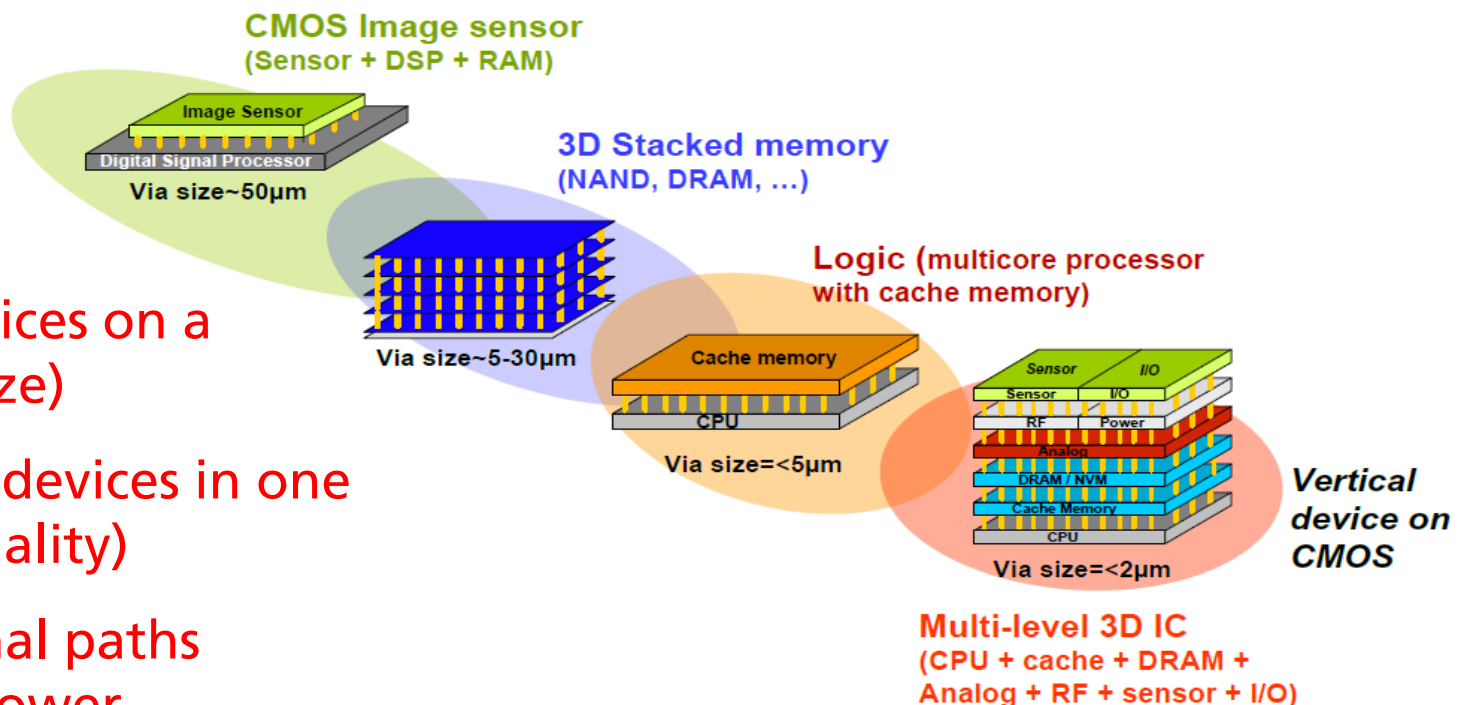
Dr.-Ing. Lutz Hofmann

Definition in general

3D-integration implies any stacking of integrated devices (ICs, MEMS) and their vertical mechanical and electrical connection.

In order to:

- Combine more devices on a smaller space (→ size)
- Combine different devices in one system (→ functionality)
- Enable shorter signal paths (→ performance, power consumption)



Picture source: CEA Leti "3D Activities and Roadmap", presented at EMC-3D European Technical Symposium Minatec June 29th, 2007

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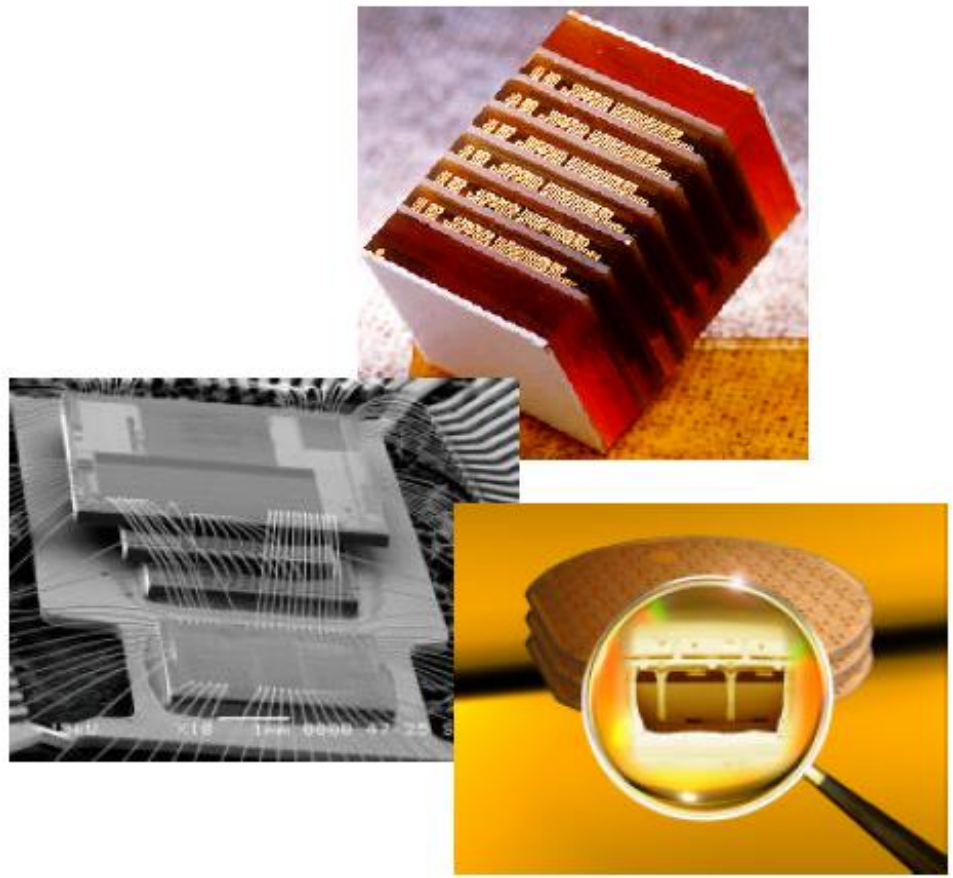
3D System Integration

Potential:

- Increased integration density
- Increased performance
- More functionality
- Reduced power consumption
- Minimum volume and weight
- Mixed Technologies: 3D SoC



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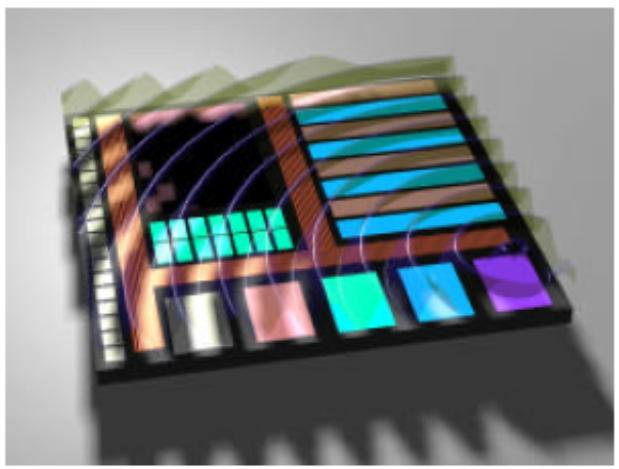
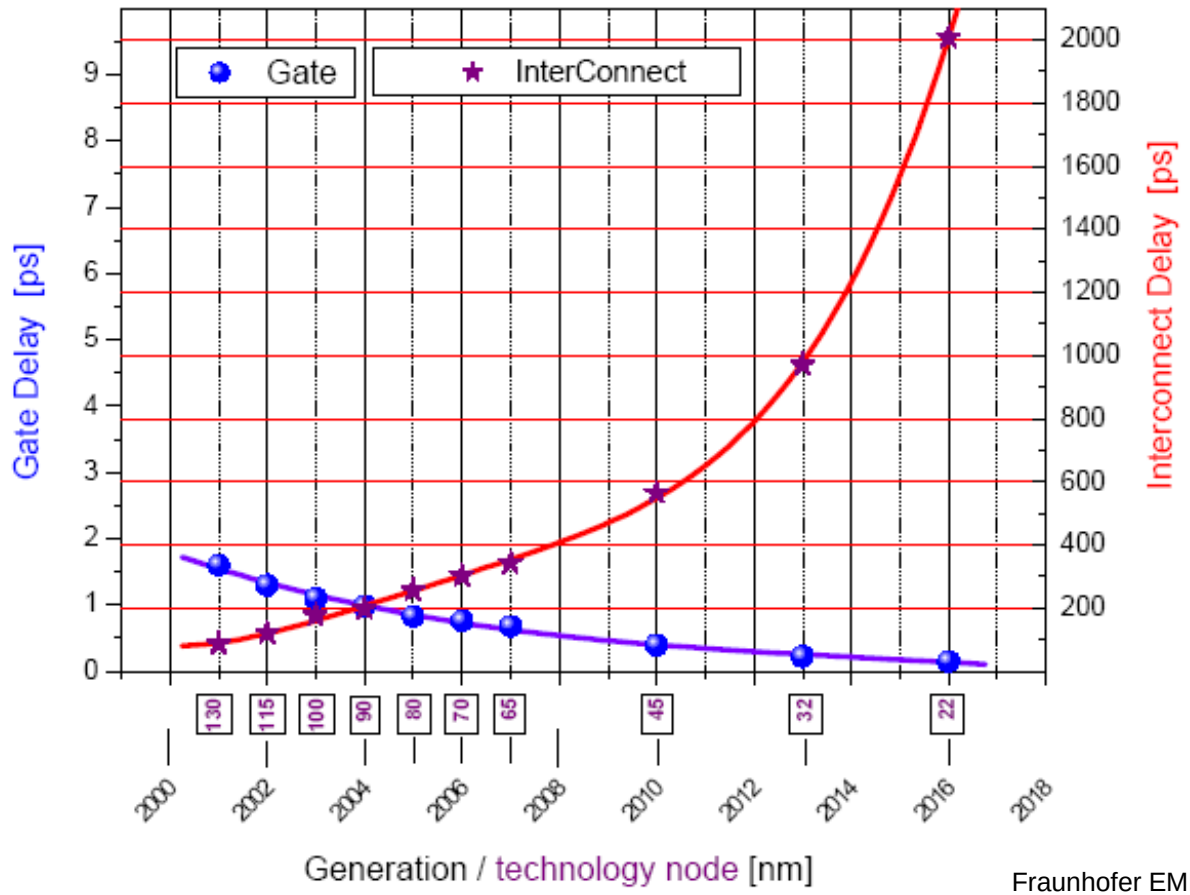
Wiring crisis on-chip





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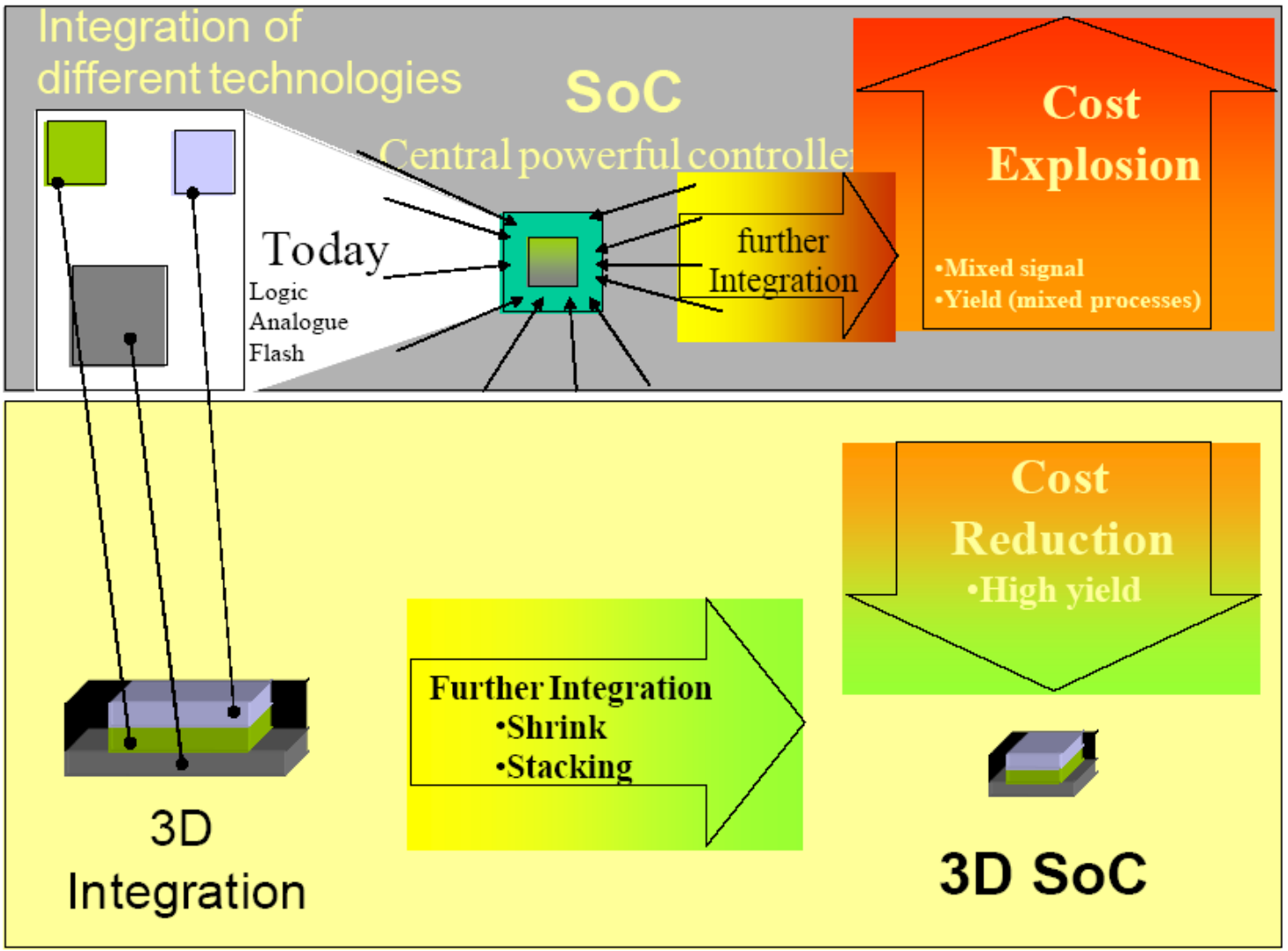
Scenario Mixed Technologies



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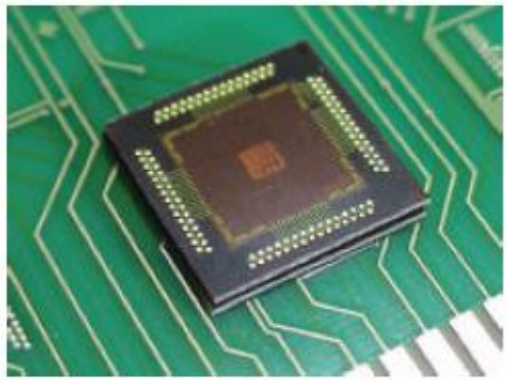
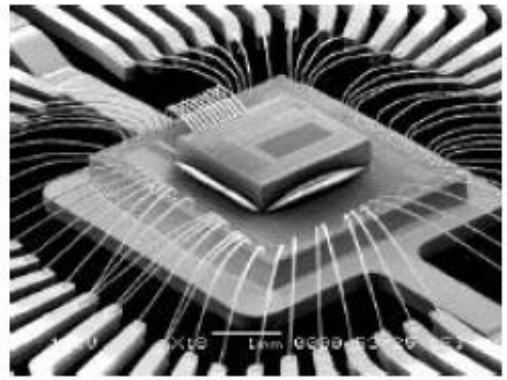
3-D System Integration





Concepts:

- **Stacked Packages**
- **Stacked Chips**
- **Vertical System Integration**
  - Stacking of Wafers
  - Chip-to-Wafer Stacking

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Vertical System Integration

Wafer-to-Wafer

- Planar IC Technologies
- Thinning and Bonding
- InterChip Metallization

Dicing, Packaging

Chip-to-Wafer

Waferscale Processing
(complete IC-fabrication)

Chip-to-Wafer
Aligned Bonding

Testing, Thinning,
Separation

Waferscale Processing
(InterChip Metallization)

Dicing, Packaging

Wafer to Wafer (W2W) stacking technology

Vertical system integration by stacking/ bonding complete wafers on top of over each other

- Fabrication of Wafers
- Wafer bonding and wafer Thinning
- Dicing/packaging
- Test of final device

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Advantage:

- „Parallel“ process → high throughput
- High alignment accuracy

Drawback:

- Test only at final device/chip
- Limit in heterogeneity (only same die size)

3D Wafer-to-Wafer Technology

InterChip Via Technology (ICV)

Vertical system integration by W2W stacking

CMOS compatible technology

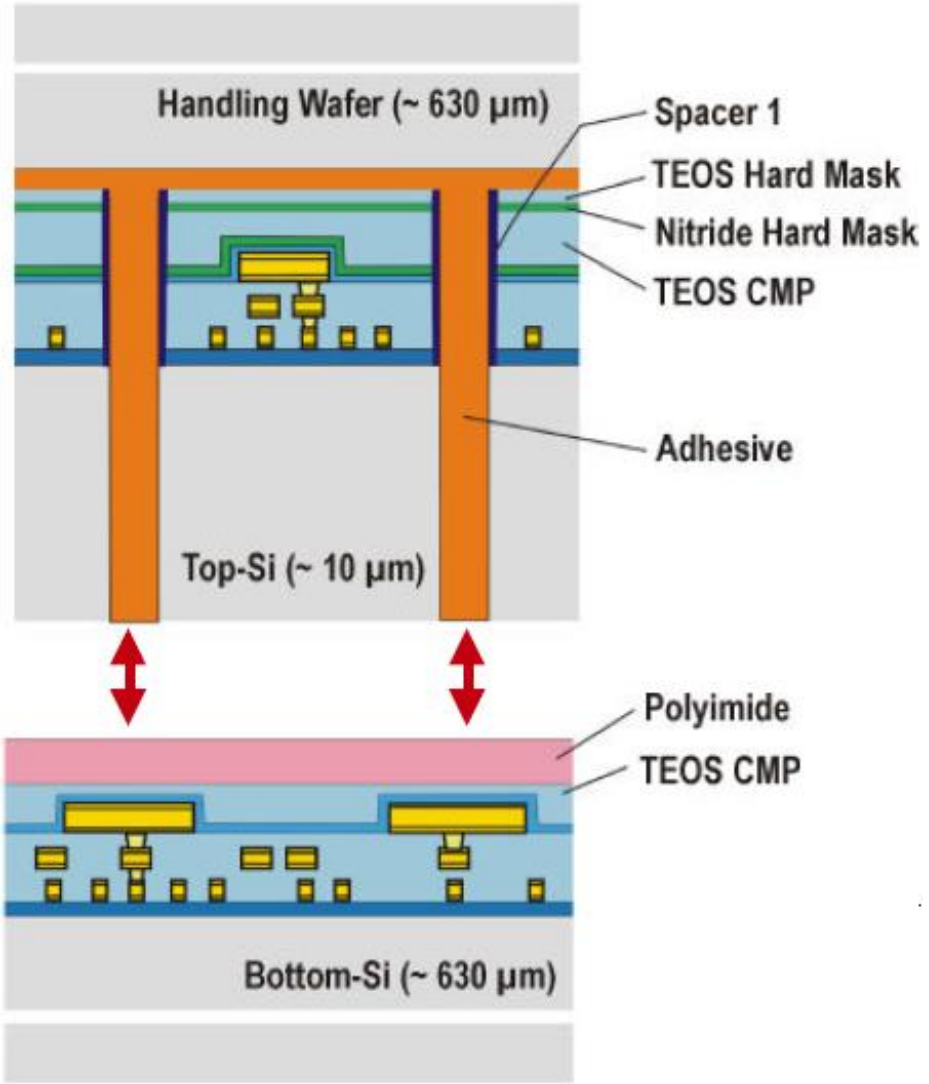
Without intervention to the basic IC process

Top-Chip:

- Via drilling/etching
- Bonding to handling wafer by adhesives
- Wafer thinning and ICV reveal

Bottom chip:

- Planarization via CMP
- Deposition of polyimide as bonding layer



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Different names same meaning: ***ICV*** ***Inter chip Via***

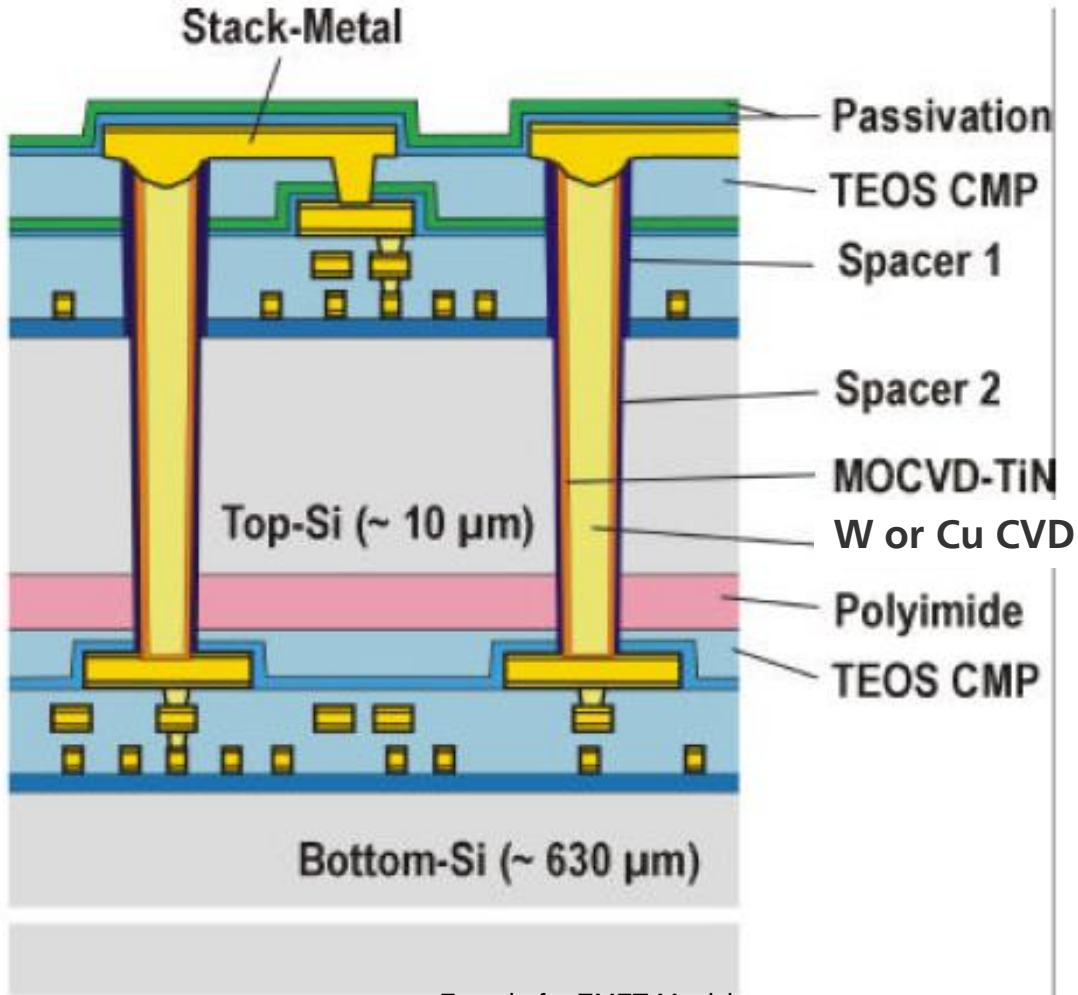
TSV ***Through Silicon Via***

THV ***Through Hole Via***

3D Wafer-to-Wafer Technology

InterChip Via Technology (ICV)

- Adhesive bonding of top-chip to bottom chip
- Release of handling wafer
- Etch through bond interface
- Isolation liner (CVD O_3/TEOS)
- Metallization by CVD TiN/W or TiN/Cu
- Top metallization by Through-Mask Electroplating



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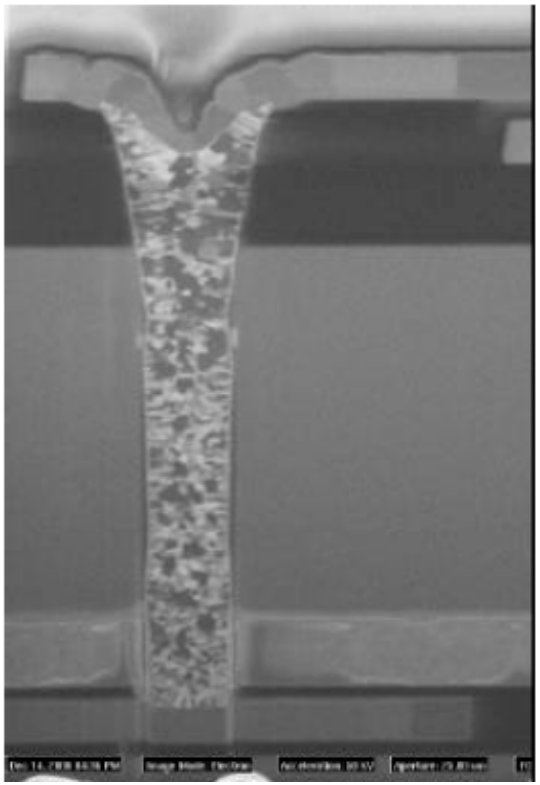
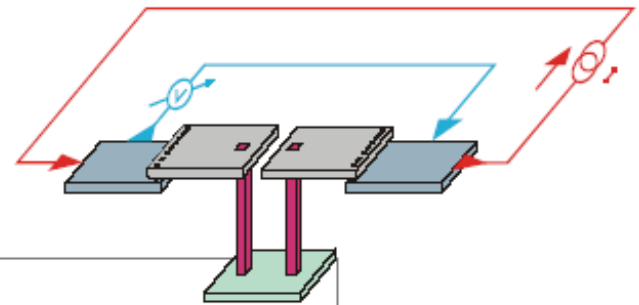
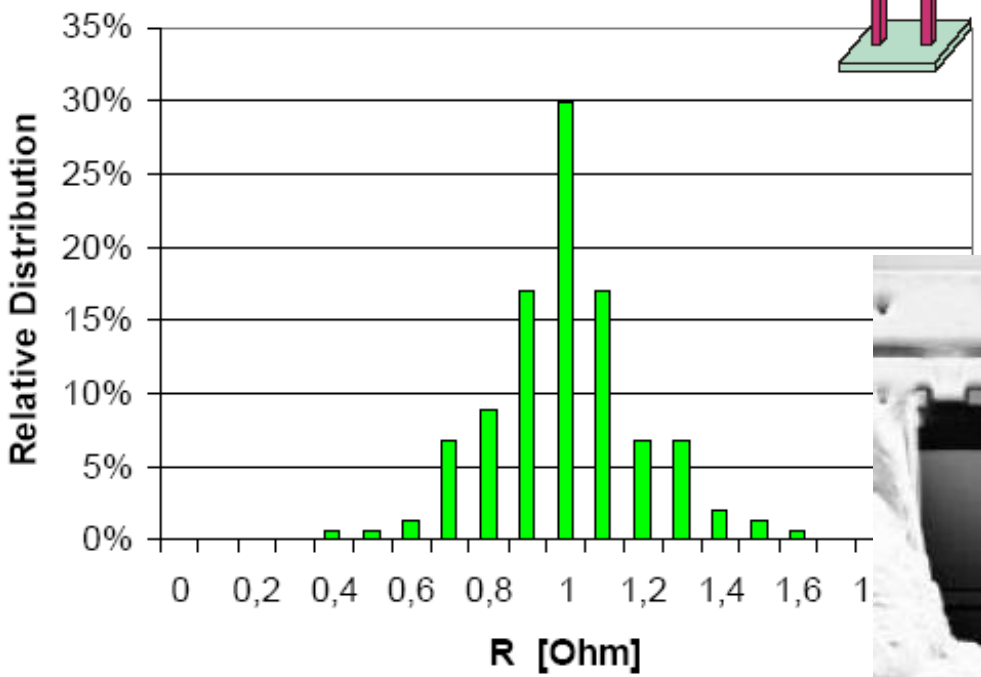
3D Wafer-to-Wafer Technology

InterChip Via – *Tungsten ICV Resistance*







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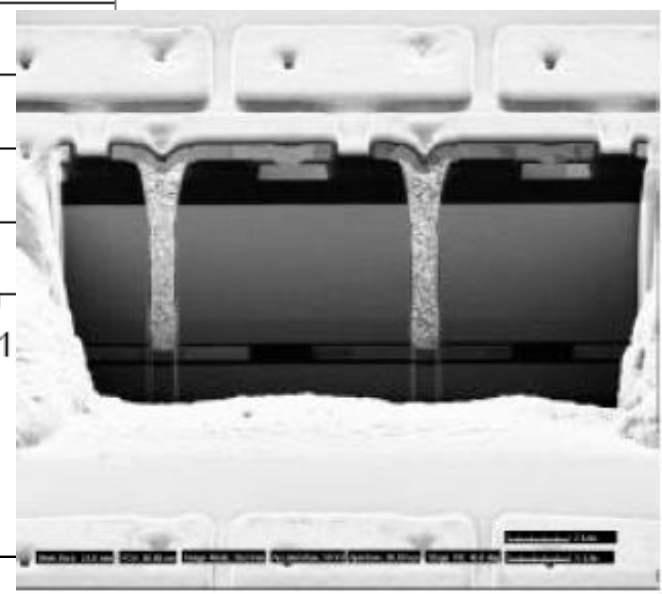

FIB of a vertically integrated test chip structure, showing 2.5 x 2.5 µm² inter-chip vias

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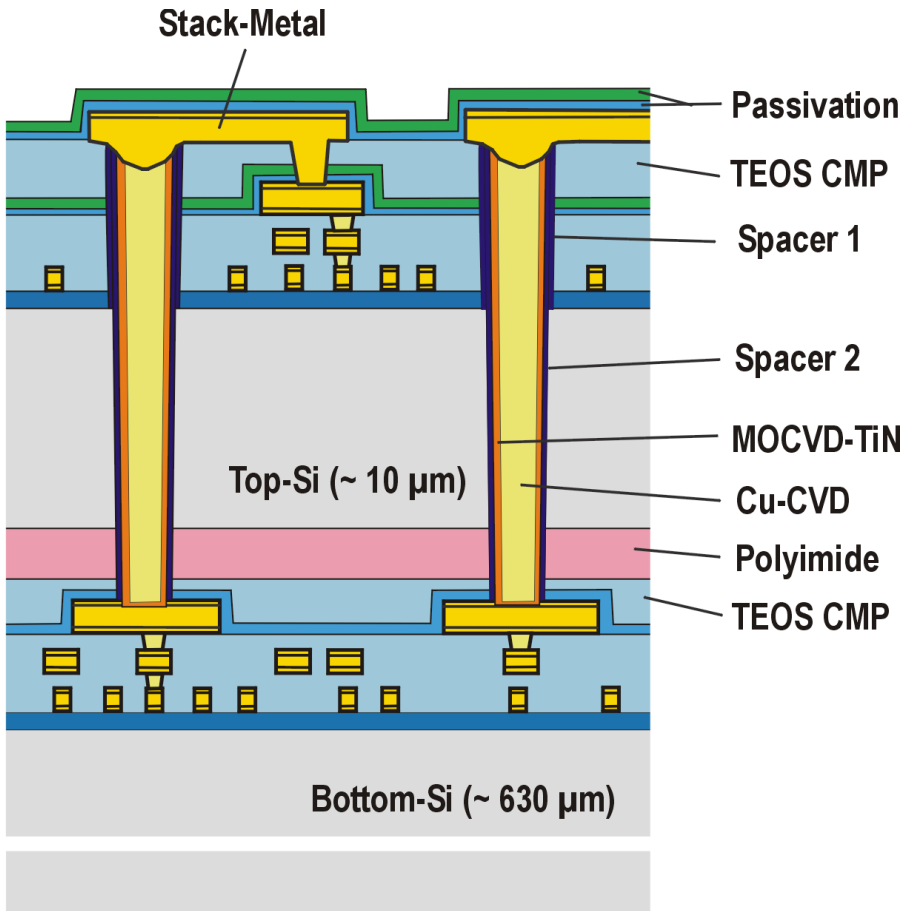
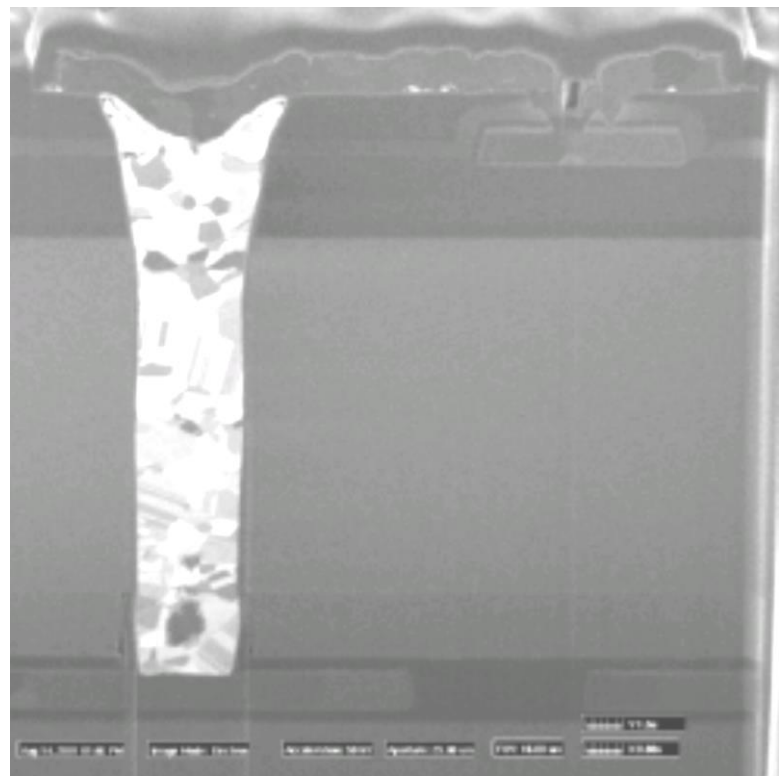
3D Wafer-to-Wafer Technology:



Interchip Via Technology with CVD-Cu ICV



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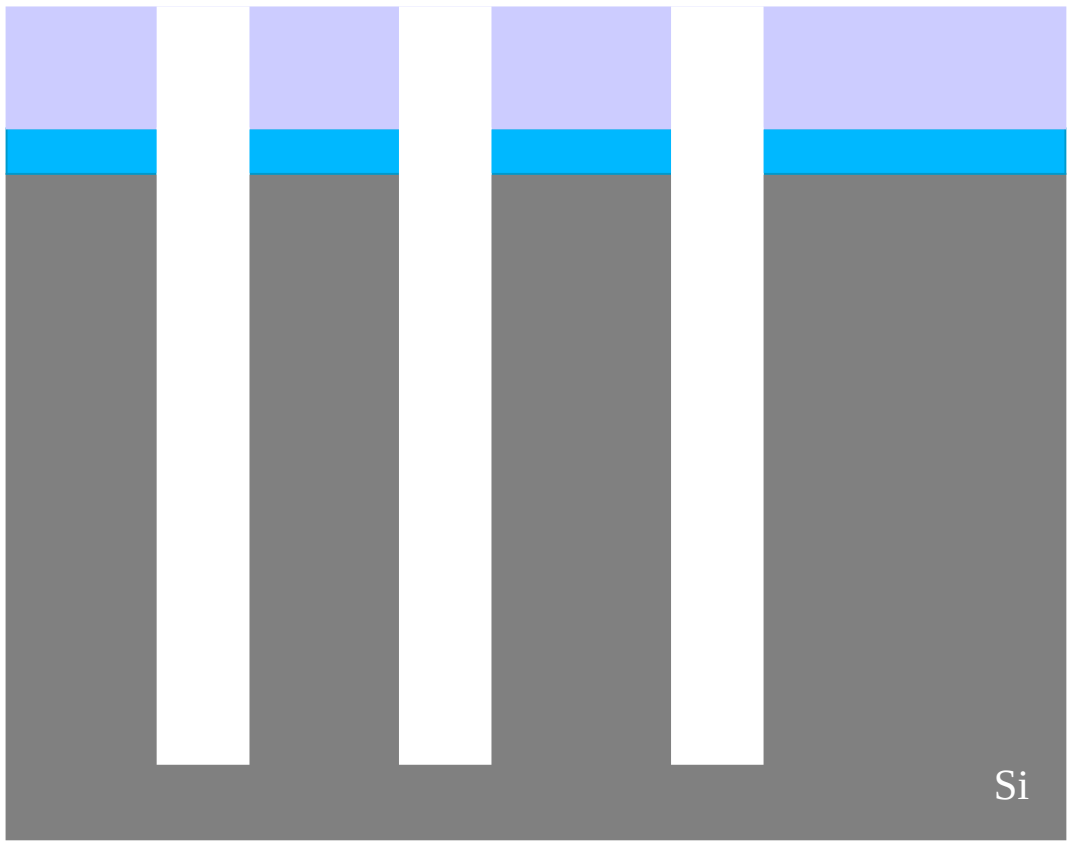
TSV/THV Process and Front Side Metallization

- THV-etch process
- Isolation
- Barrier deposition
- Copper deposition
- Cu and barrier CMP
- Dielectric deposition
- Dielectric etch (SD)
- Deposition of Barrier and Cu
- CMP
- Passivation deposition

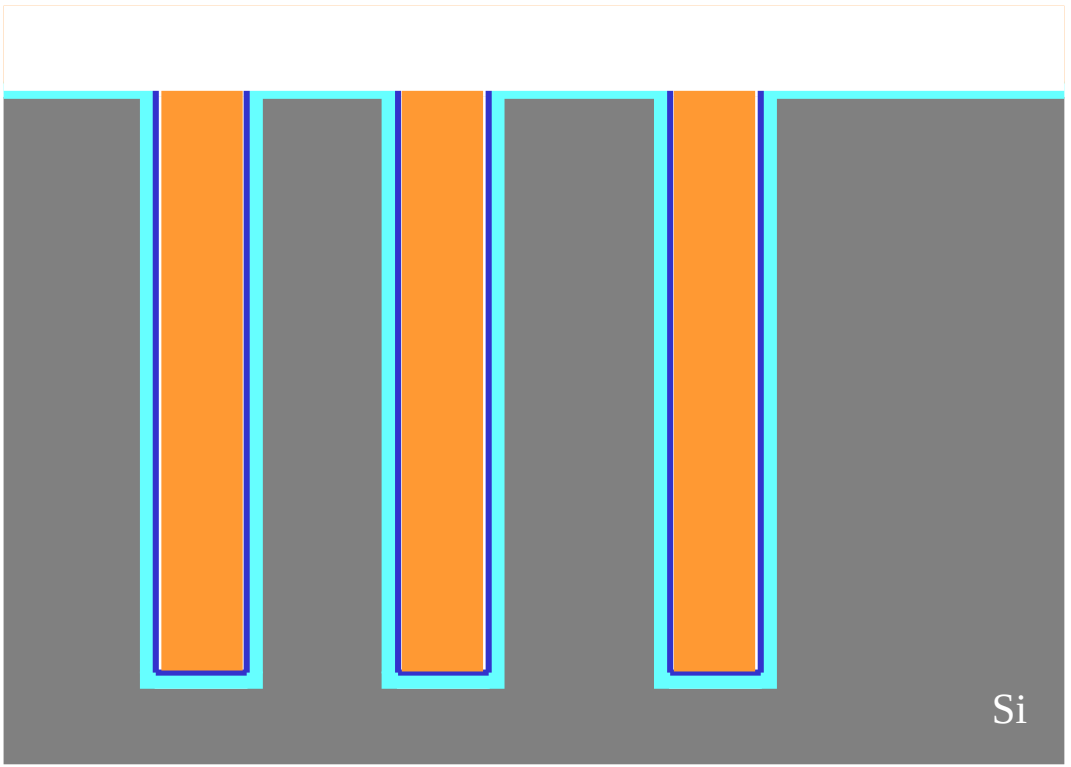
Technology Cu fill

1. TSV ETCH



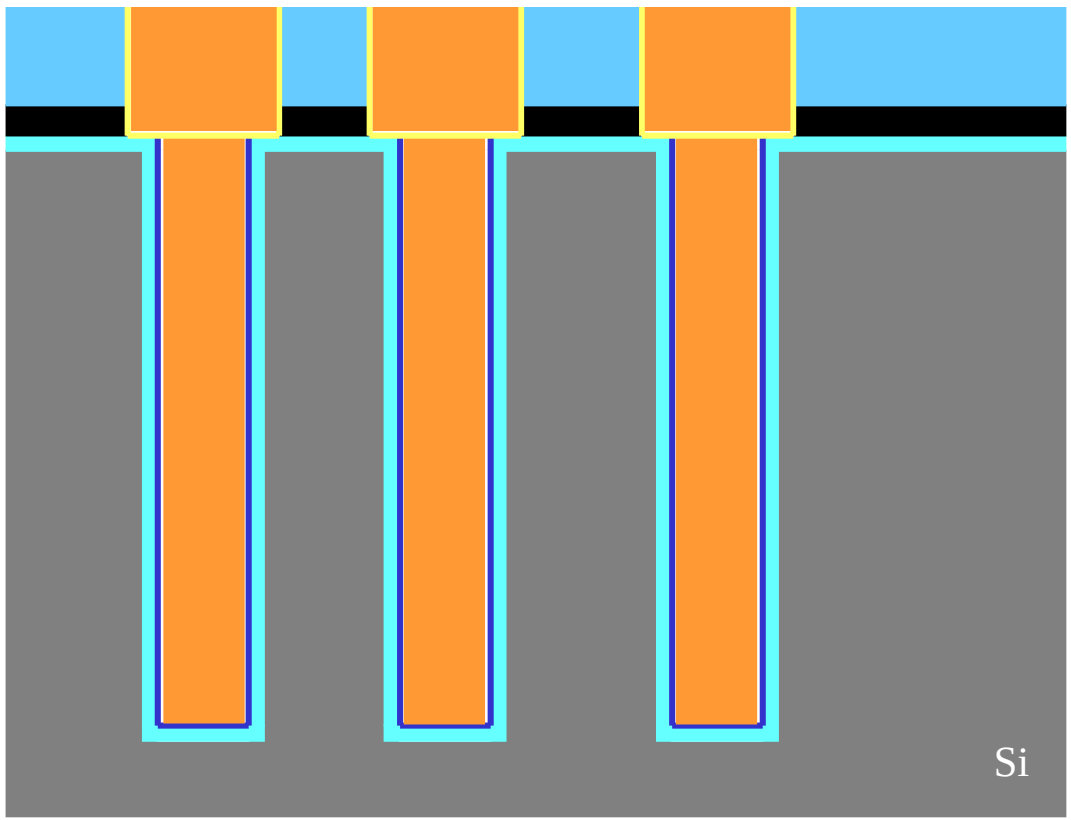
- Dielectric deposition
- Lithography (MASK-1)
- Dielectric opening
- THV etch (DRIE, BOSCH process)
- Removal of resist and hard mask
- Removing of polymer residues

2. TSV Fill



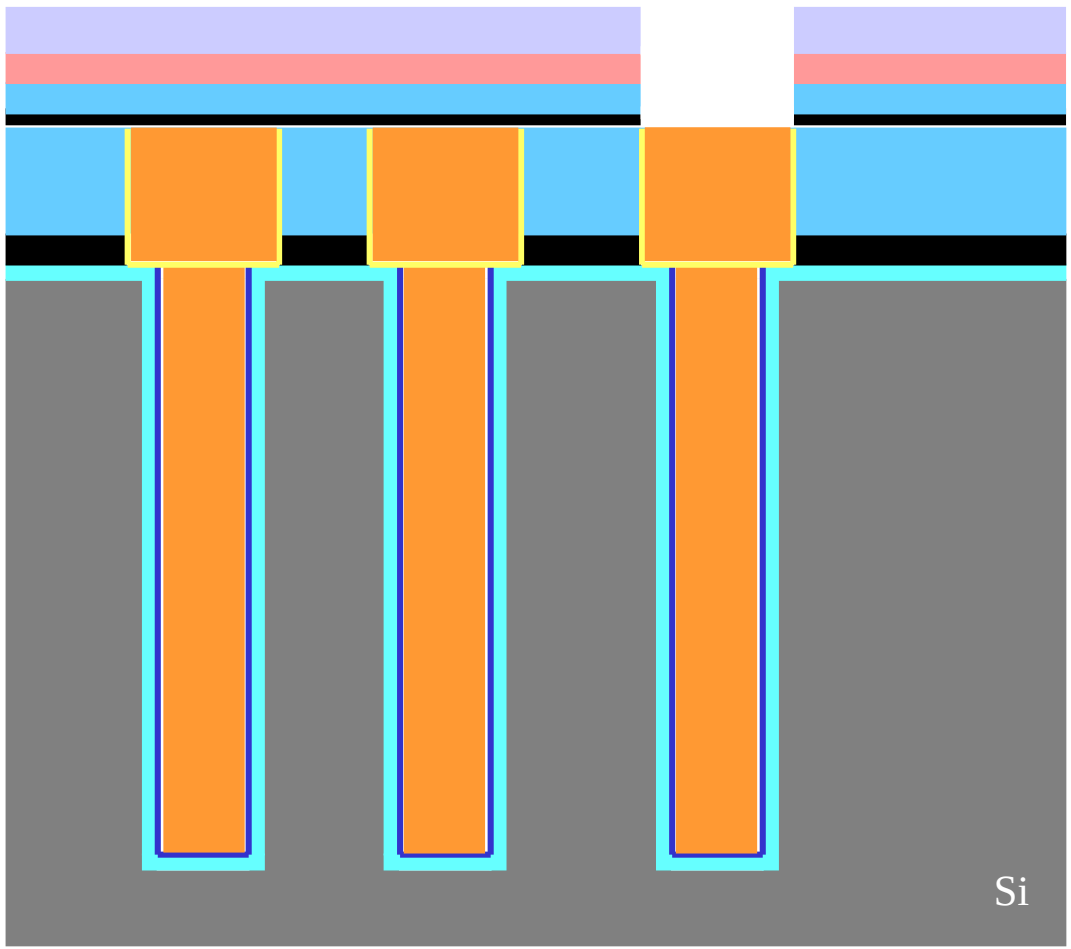
- Isolation
  - SiO_2 (Oxidation, LPCVD, PECVD or SACVD-TEOS)
  - Polymers
- Metal deposition
  - MOCVD TiN Barrier
  - iPVD or MOCVD Cu seed
  - Electroplating of Cu
- Planarization
  - Cu and Barrier CMP

3. Damascene Metallization



- SiC Etch Stop Layer
- Dielectric deposition
- Resist and Litho MASK-2
- Etch Dielectric
- Resist removal
- Opening of SiC
- PVD Barrier deposition
- PVD Cu Seed deposition
- Cu Plating
- CMP

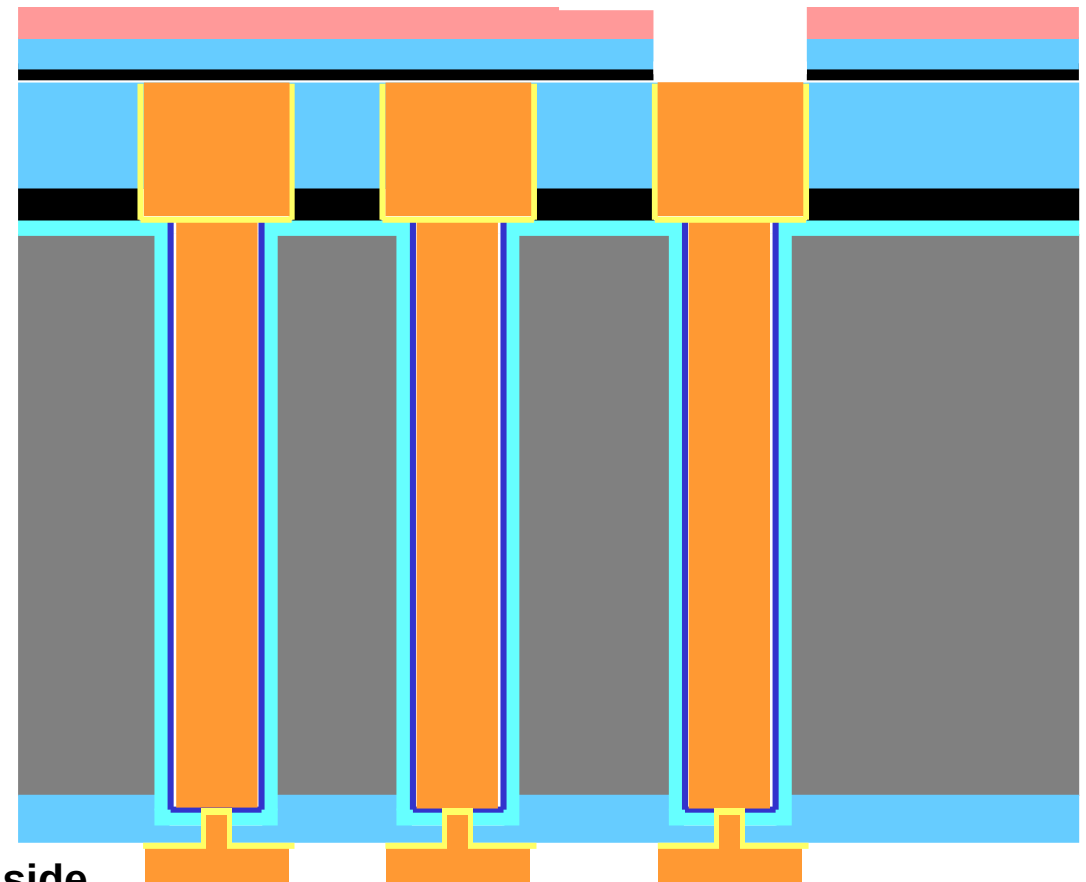
4. Pad Opening



- SiC Hard Mask Deposition
- Dielectric Deposition
- SiN Passivation
- Resist and Litho MASK-3
- SiN and Dielectric Etch
- Resist removal
- SiC Opening

Backside processing

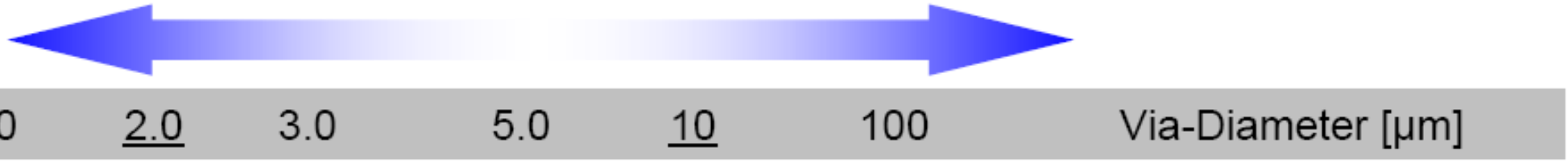
Front side

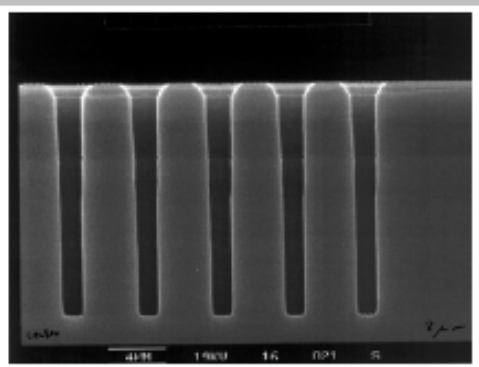


Back side

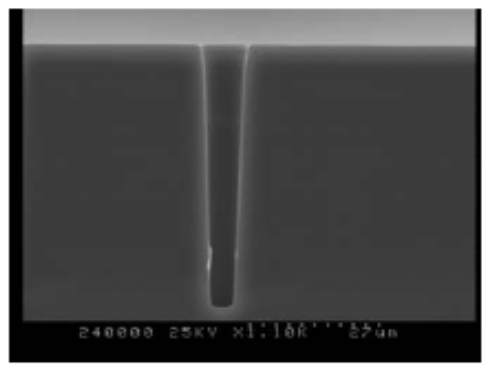
- Bonding front side to handling wafer (***not shown here***)
- Backside thinning
- Via reveal
- Backside Isolation
- Contact opening
- Metallization steps … (e.g. through mask ECD)

ICV: ICs, Memory Interposer

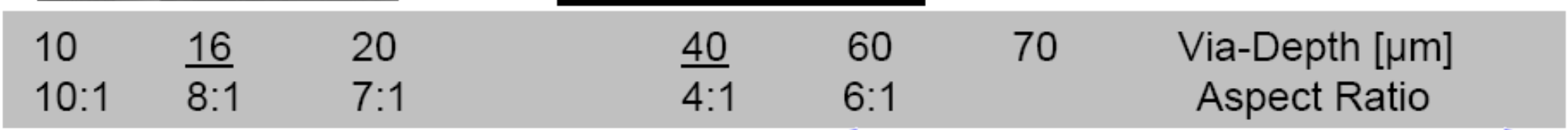




16 µm,
8:1



40 µm,
4:1



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MEMS, Image Sensor

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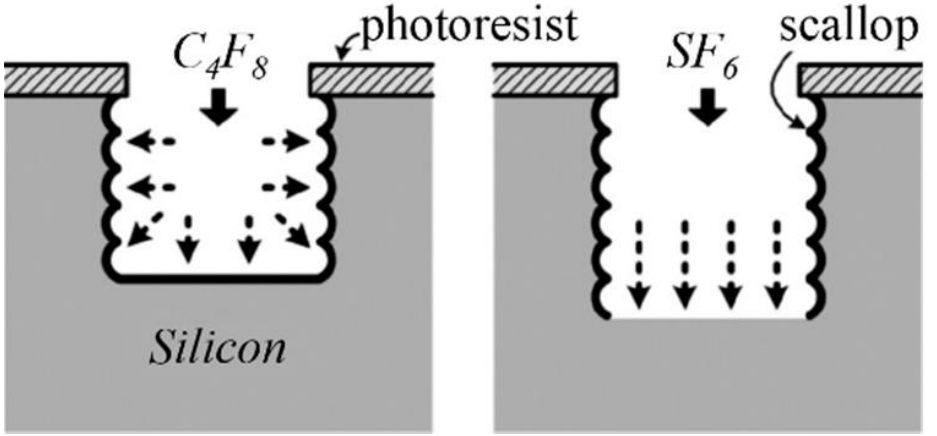
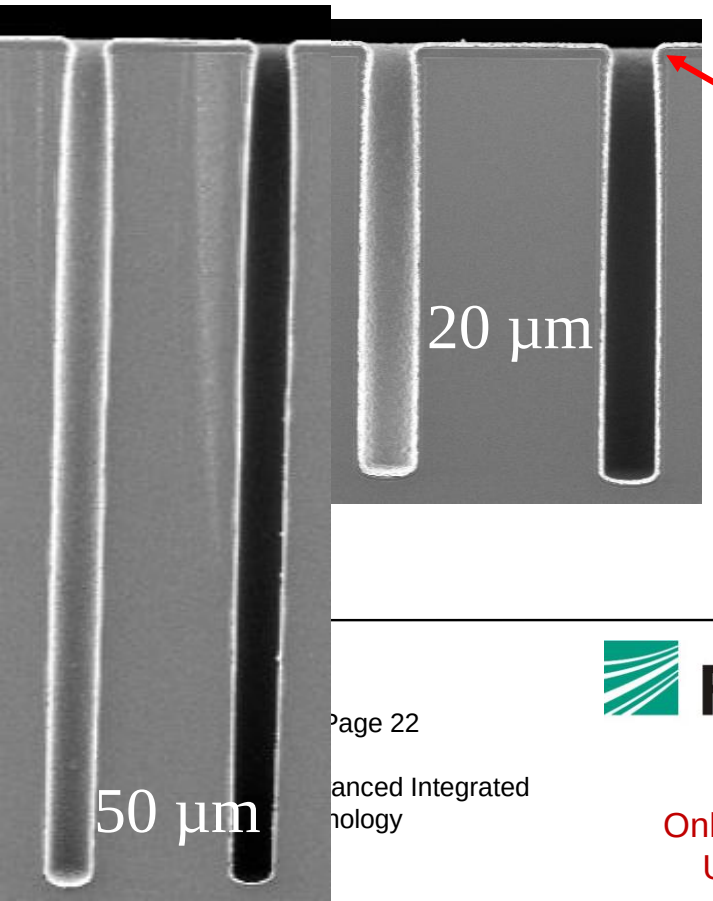
TSV Etching — Requirements and critical issues

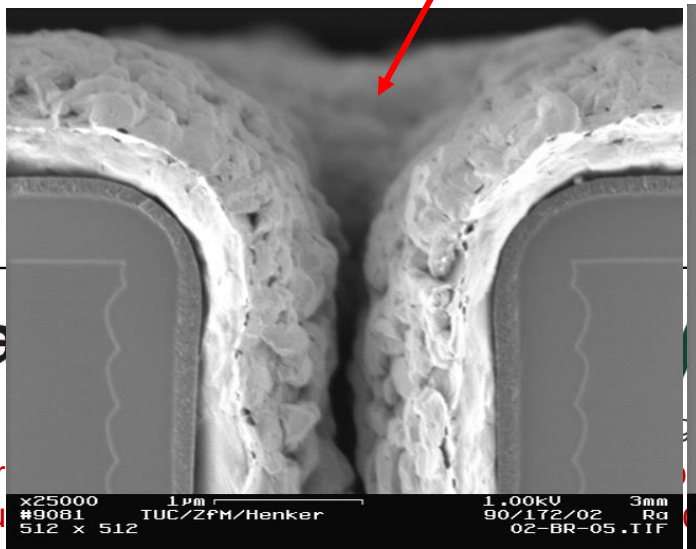
STS DRIE Si etch tool / Bosch process

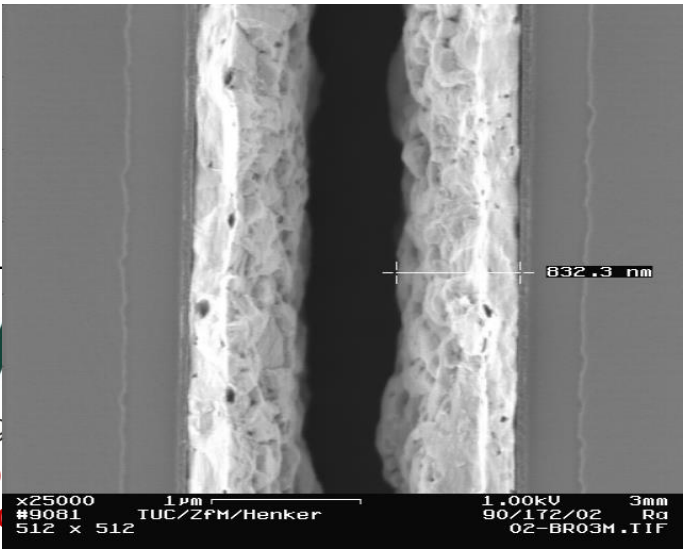
- Straight profile of TSV (~90°)
- Cyclic process (etching/passivation) → scallops form in the upper TSV region





- Standard-process → Overhang formation during deposition – processes (isolation, barrier, Cu)
- Premature closing of TSV entrance

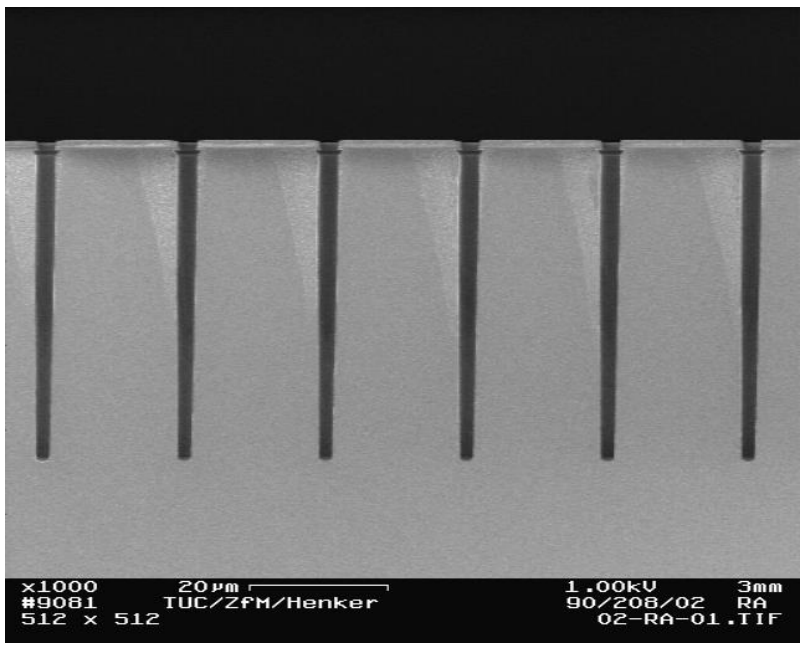


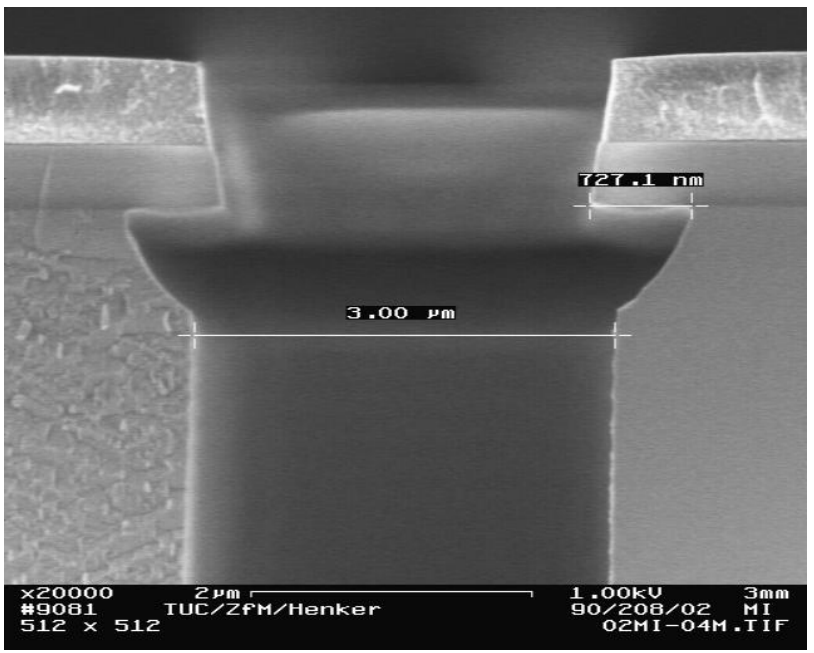


TSV Etching

Solution: Modification of the Bosch process

- tapered profile by changing the first etch cycles
- enlarged via entrance of TSV





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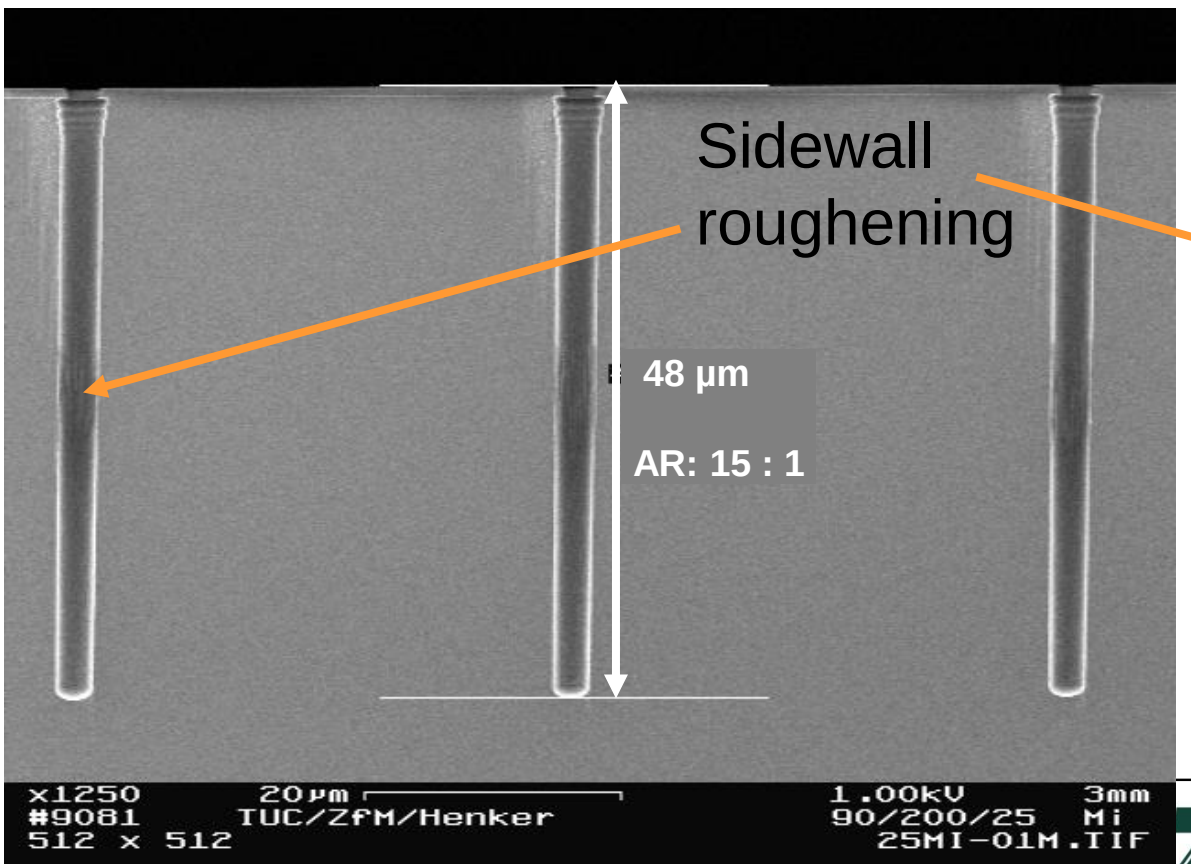
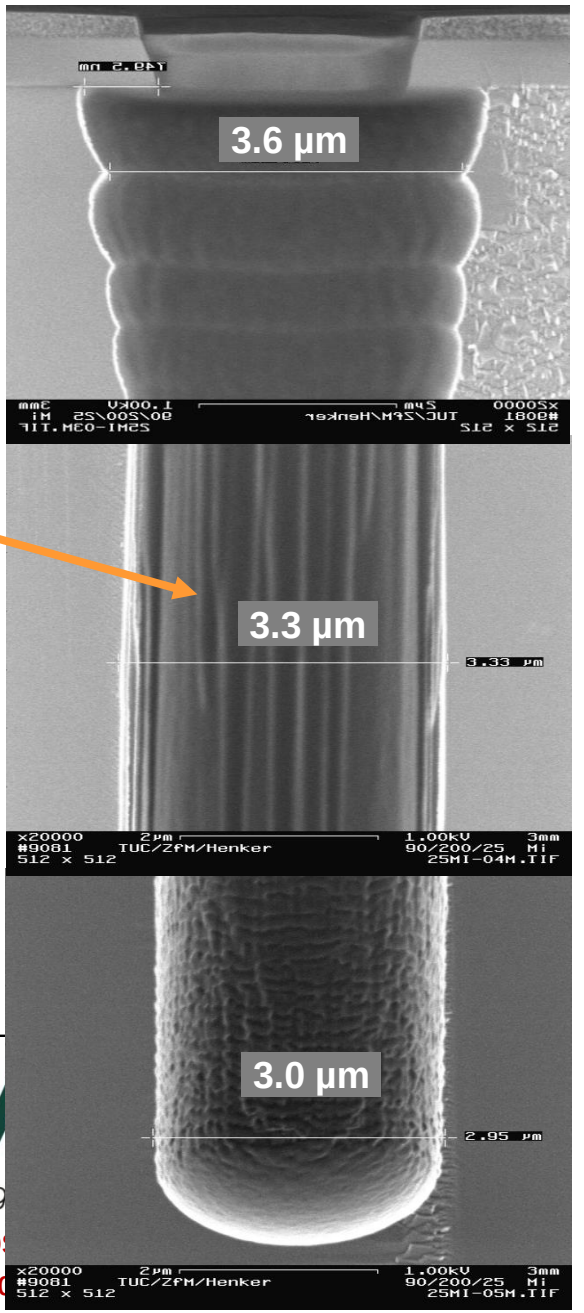
TSV Etching

Optimization of the taper process:

- 3 steps with decreasing cycle time
- still sidewall roughness





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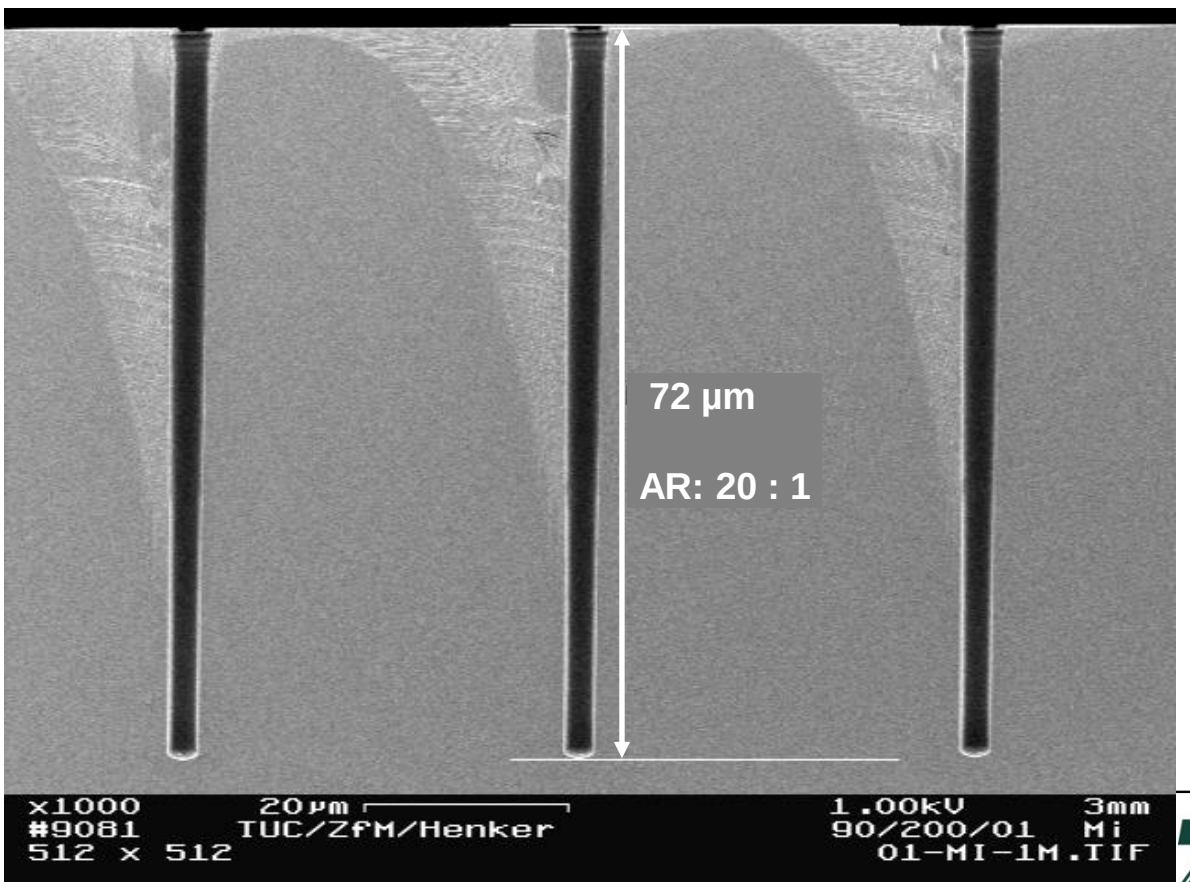
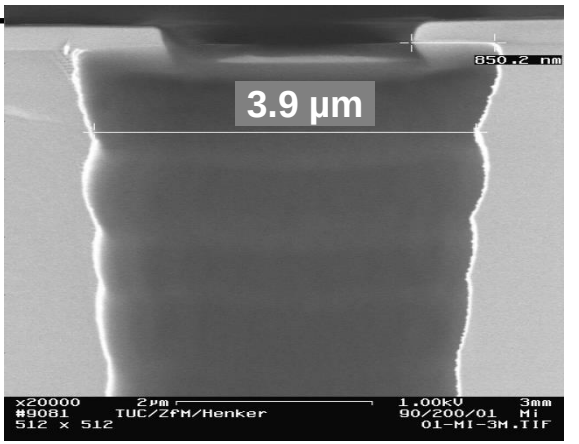
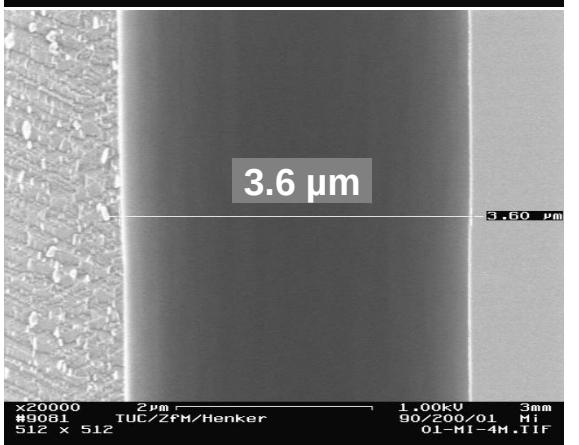
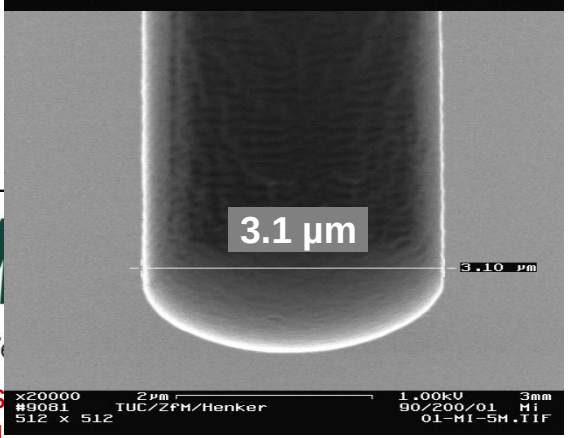
TSV Etching

Optimized process (cycle time, pressure, RF-power)
→ Reduced roughness









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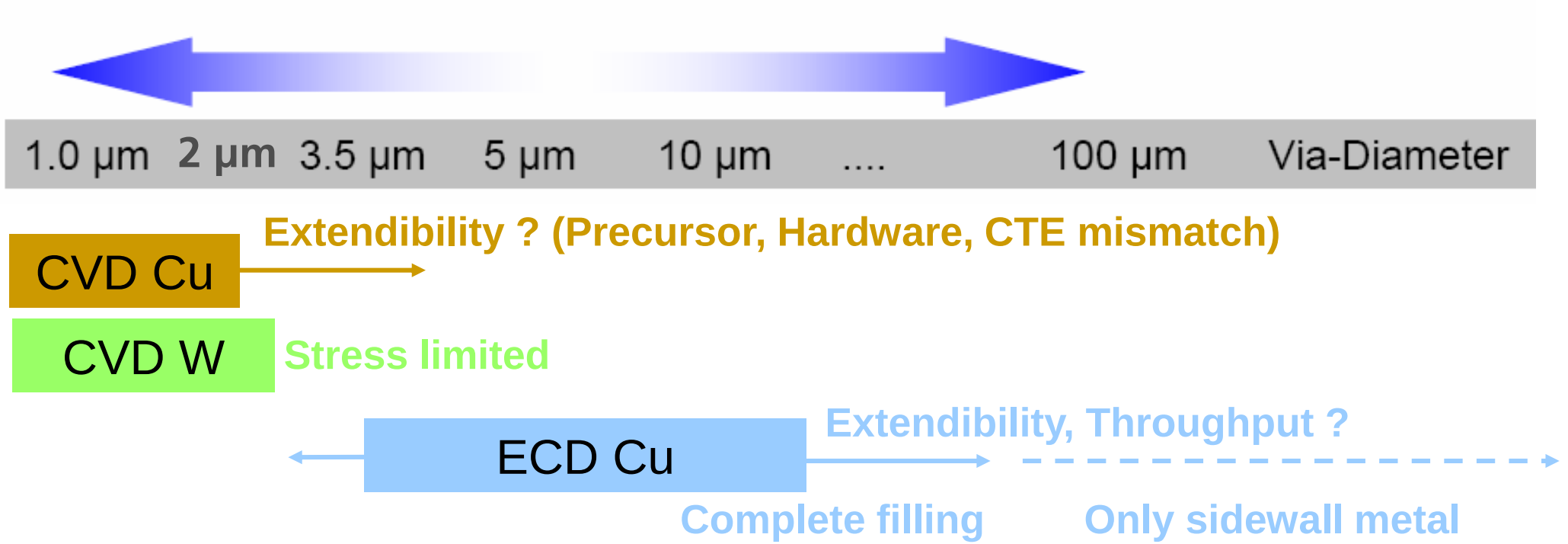
TSV Fill — Processes for different TSV diameter



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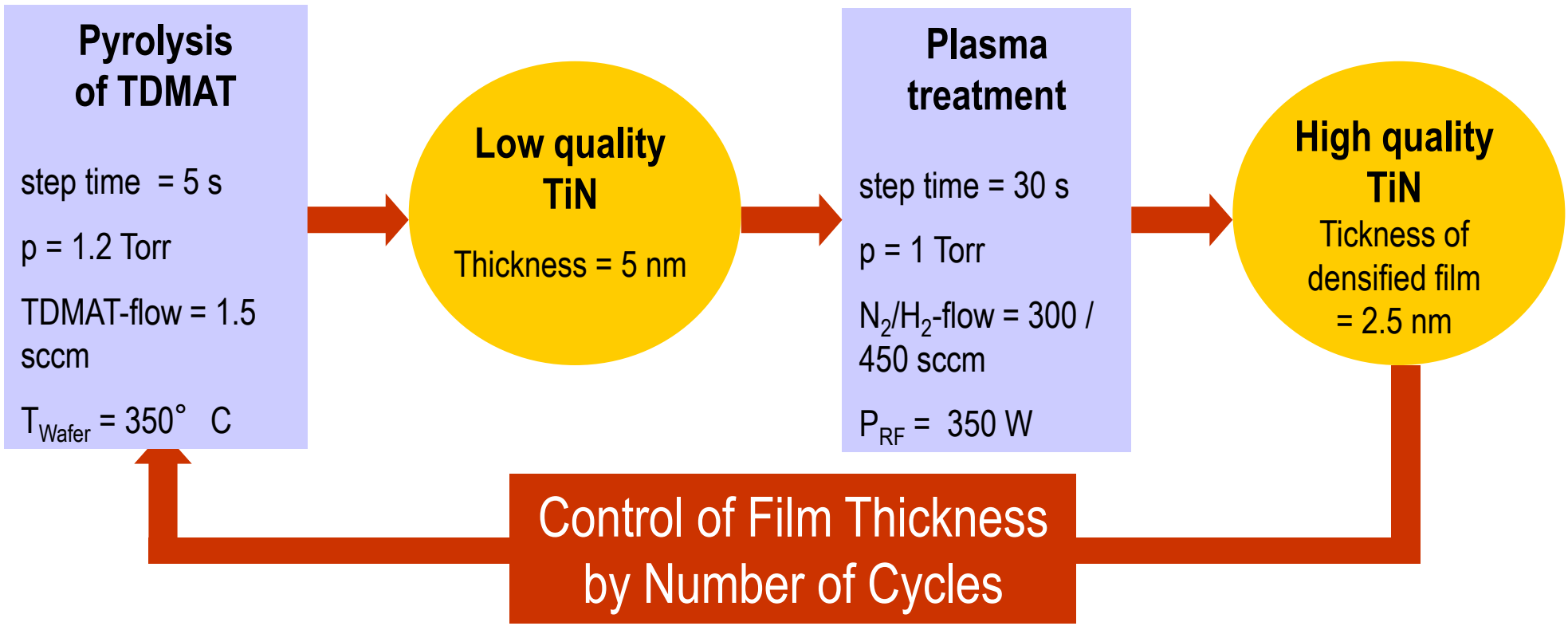
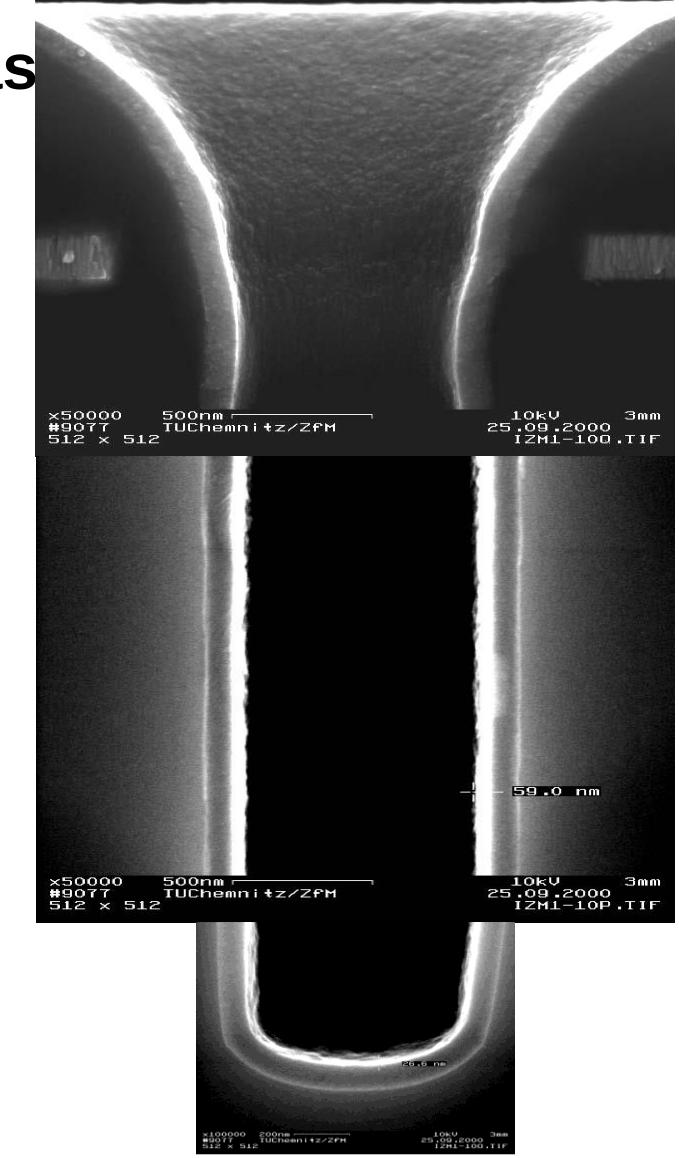
Principle of TiN-MOCVD with Plasma Densification



Step Coverage of MOCVD TiN in Interchip Vias

Via size (design)	1.6 µm	2.5 µm
Position / Aspect Ratio	~ 15	~ 8
Field top	81 nm = 100%	81 nm = 100%
via entrance	110 nm = 136%	103 nm = 127%
sidewall middle	59 nm = 73%	63 nm = 78 %
via bottom	27 nm = 33%	46 nm = 57%

- Step coverage in the upper via area: > 100% (plasma densification more efficient at planes perpendicular to the incident ions)
- Step coverage depends on via size
- Actual via width is about 400 nm smaller (oxide spacer); here: TiN thickness 84 nm for better visualisation
- Measurement error: about 10%



1.6 µm wide ICV (AR ~ 15)

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Step Coverage Copper CVD

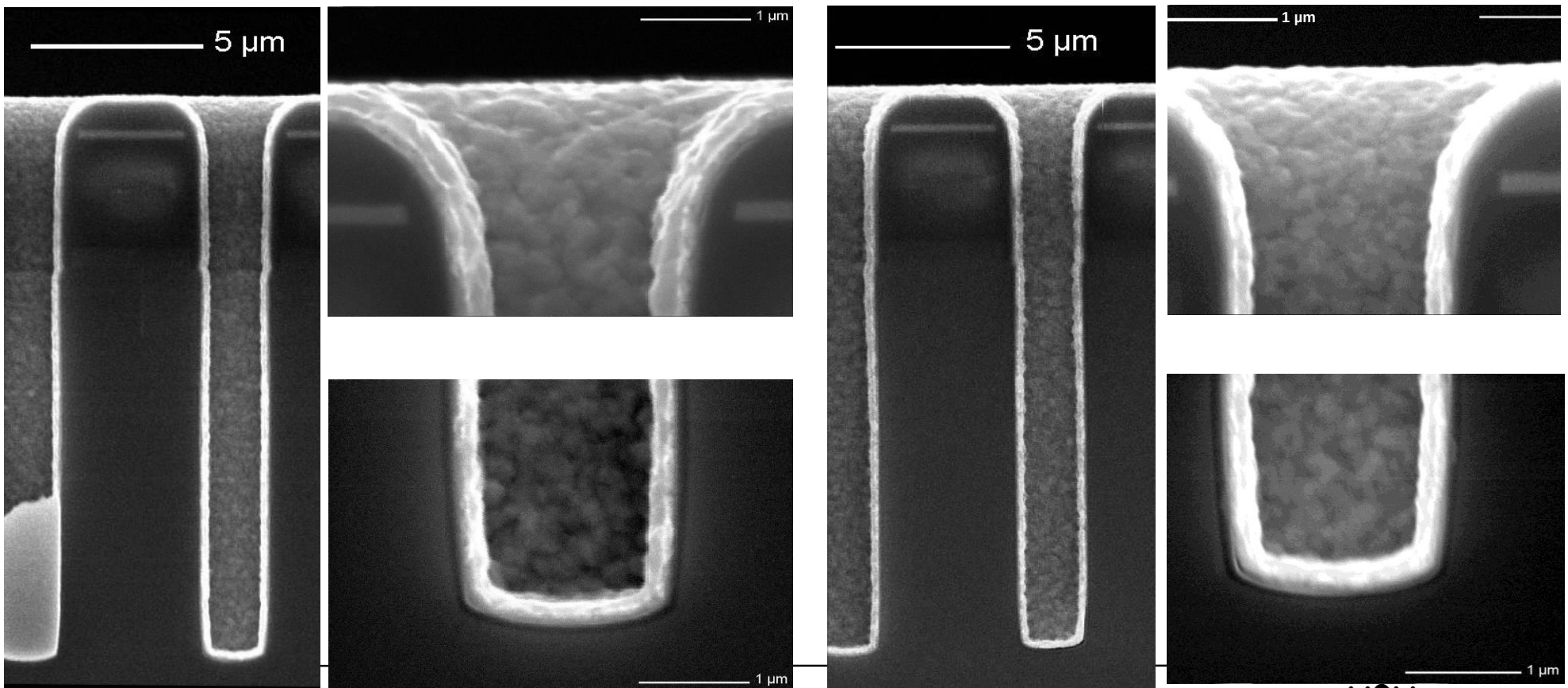
Comparison of two different deposition temperatures

200° C

Rate = 165 nm/min step coverage 65 %

170° C

Rate = 80 nm/min, step coverage ~ 100 %



AR = 8.5

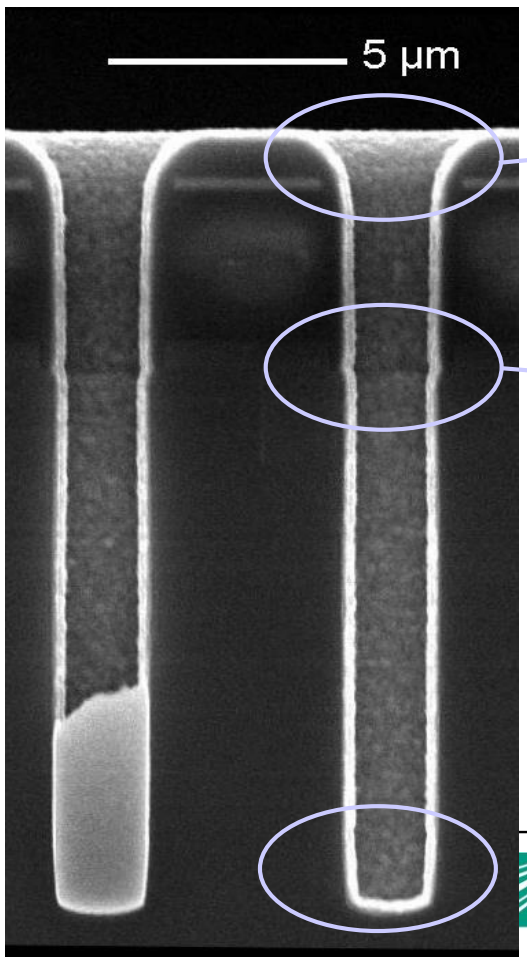
Optimum Process for Interchip Via
→ Low Temperature

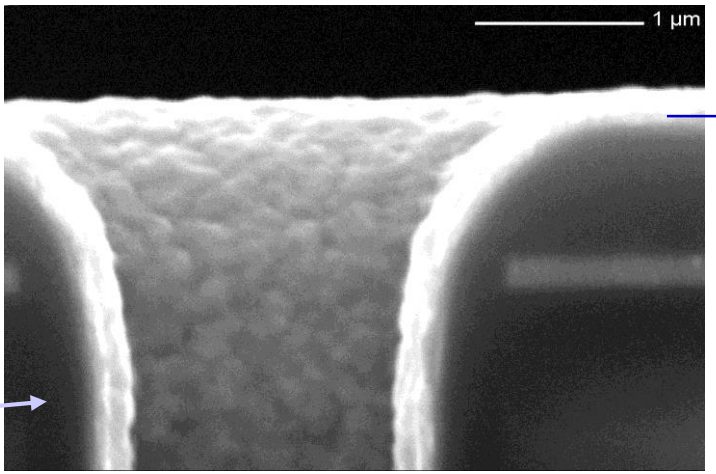
Conformal Seed

T_{wafer} = 170° C

Step coverage

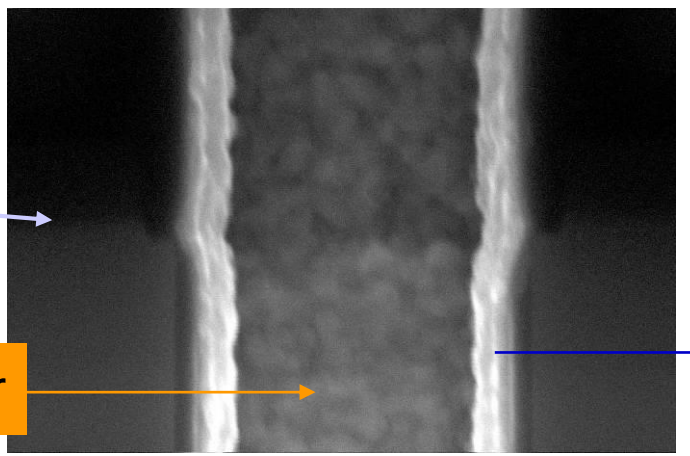
using Cu-CVD
aspect ratio = 8



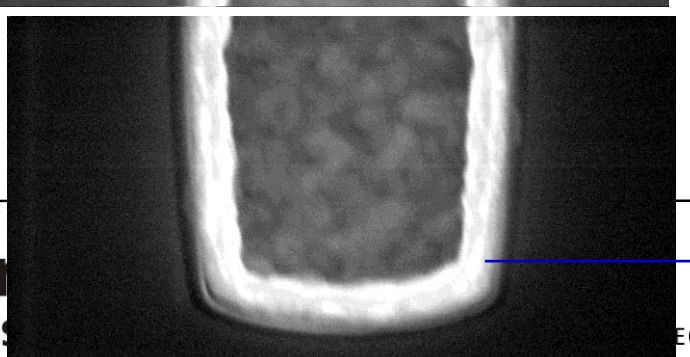


220 nm = 100%

CVD-Copper



220 nm = 100%



215 nm = 97.5%

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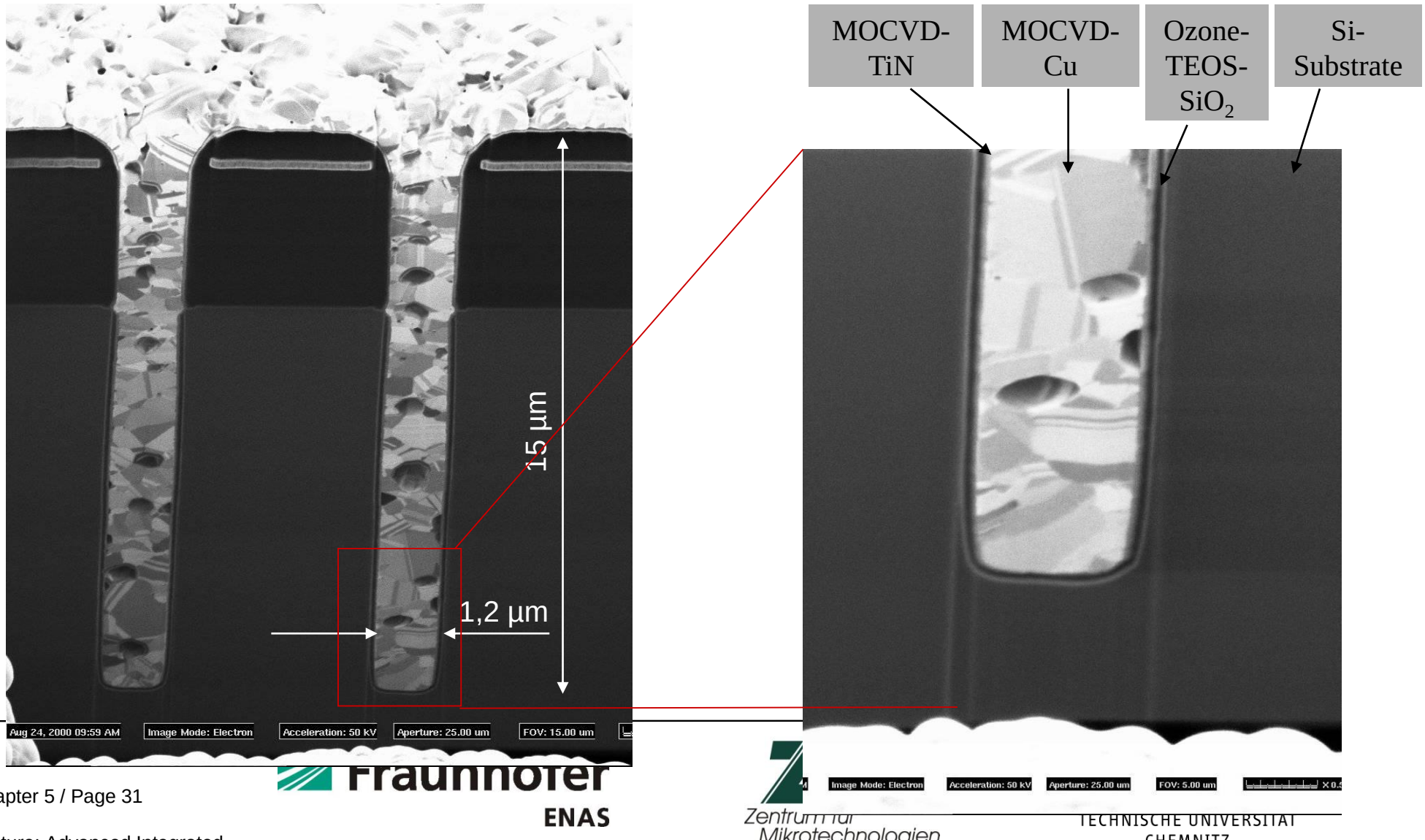
Optimum Process for CVD Interchip Via Fill

FIB cut of a via hole with AR of 12.5 after CVD-Cu fill and anneal



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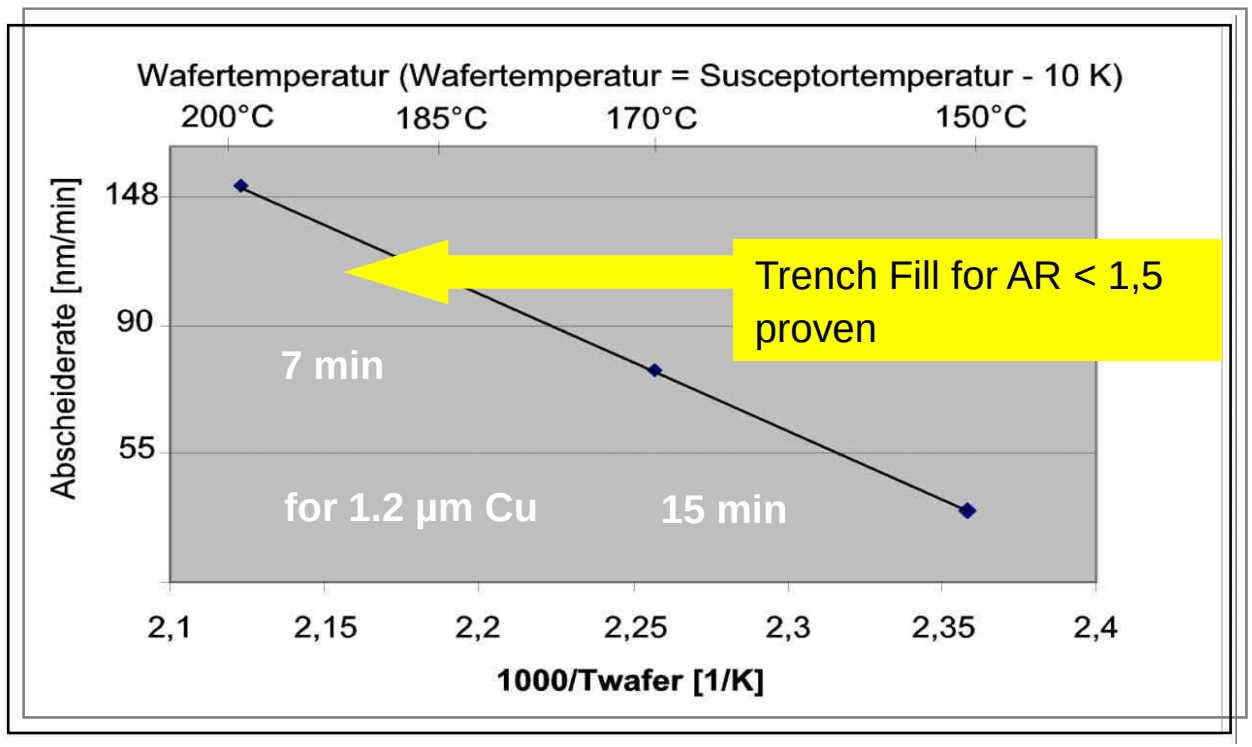
Requirements for Copper CVD in Interchip Vias

- High deposition rate (target thickness = 1.2 µm)
- Excellent step coverage / fill behaviour at AR ≥ 8

Both reqirements can not be fulfilled at same time:

Precursor flow limited (condensation of precursor for higher partial pressures).



Arrhenius plot for 0.8 g/min precursor flow

Cu-CVD with CupraSelect (Schumacher)

- Long filling process
  - condensation of by-products at chamber wall
  - Fill in 3 processes steps with t/3
  - pump process steps 3 times longer than the individual deposition steps (3xt)

TSV d ≤ 2 µm

- CVD barrier
- Cu CVD Fill

TSV d > 2 µm

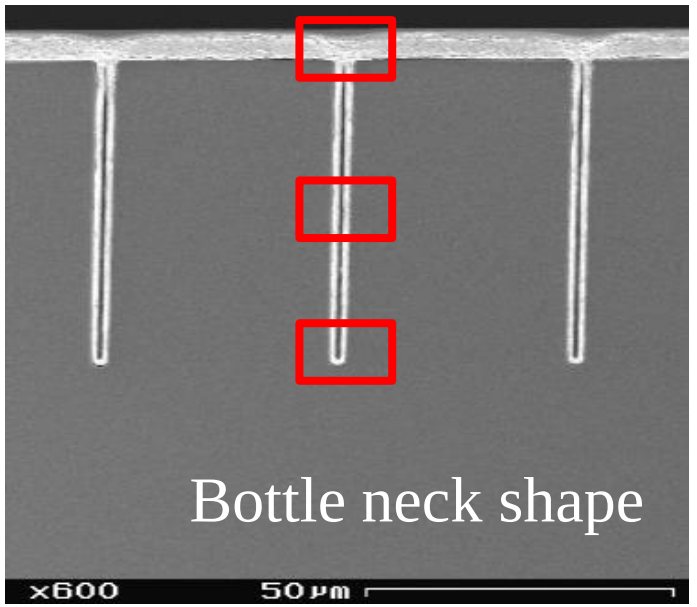
- CVD barrier
- CVD Cu seed layer
- Cu plating

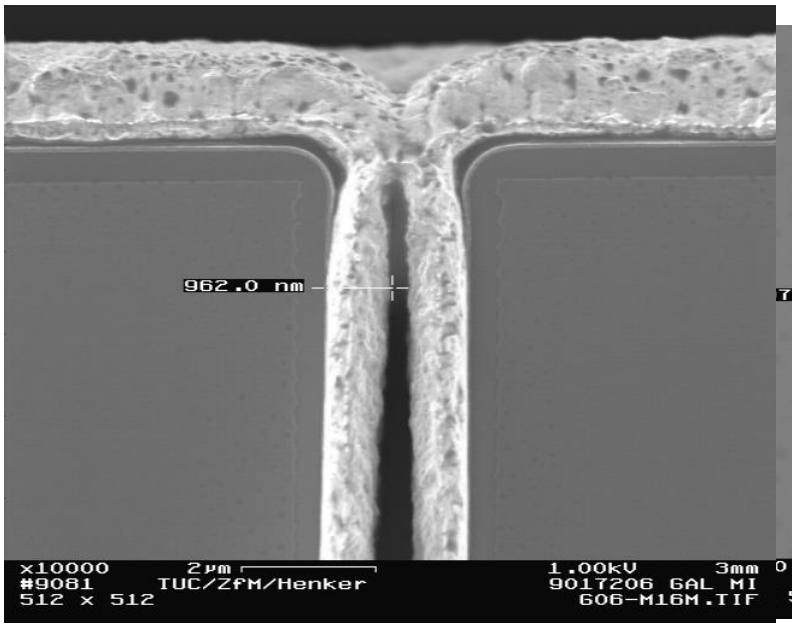
With smaller TSV and higher aspect ratios: lower step coverage
→ Lower temperature
→ Lower deposition rate → Low throughput

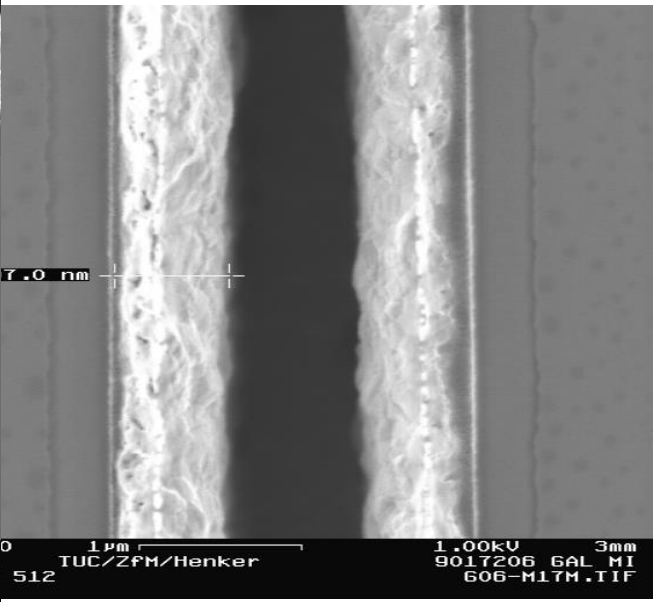
→ Special plating chemistry
→ Advanced process recipes
→ Throughput (for fill of large vias) ?

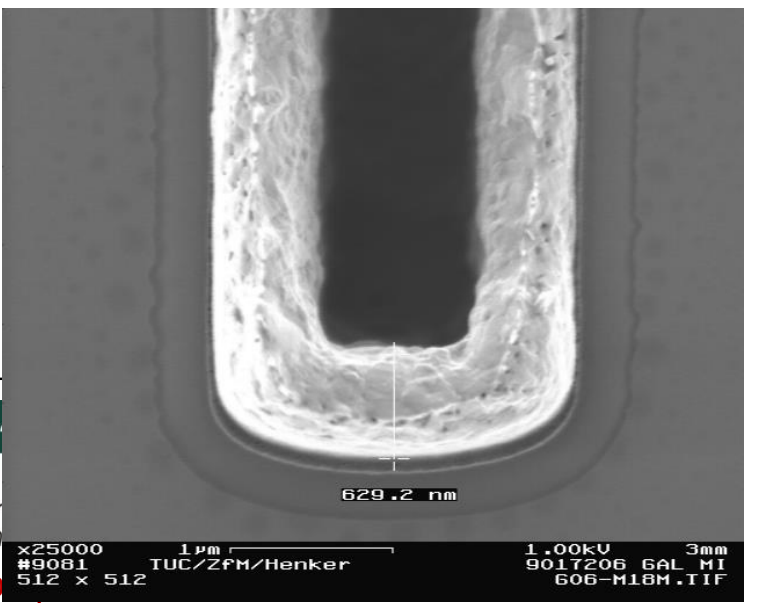
TSV Fill

Cu ECD









Plating also provides conformal Cu in high aspect ratio features, but complete fill is difficult and time consuming; only works with CVD seed

Potential for further development

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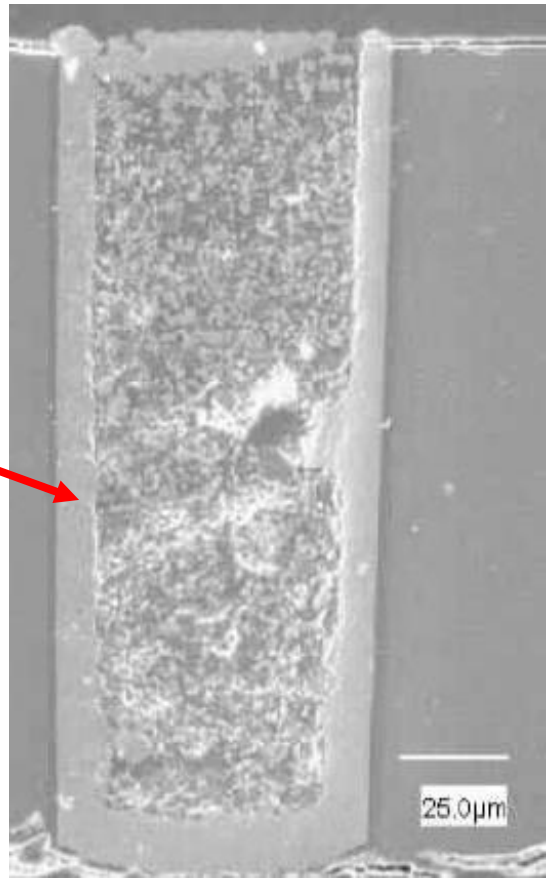
Partially Filled Vias with core fill

Cu-ECD only on sidewall



Composite Fill after Cu ECD

- Issue for complete fill (especially for larger diameter vias): mechanical reliability:
  - CTE mismatch (metal dependent)
- Partially filled vias:
  - Suitable for large and deep vias
  - Low cost core fill required (e.g. with polymers)
  - Extendable to smaller vias ??

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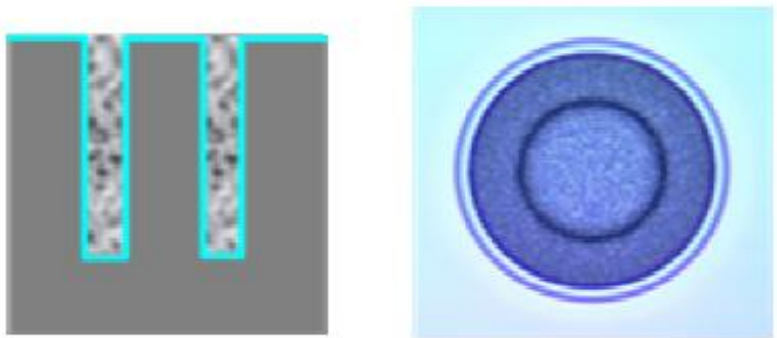
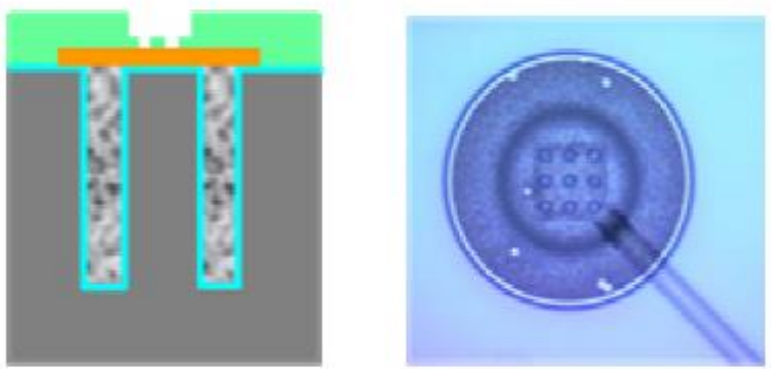
Annular-Shaped Via Approach

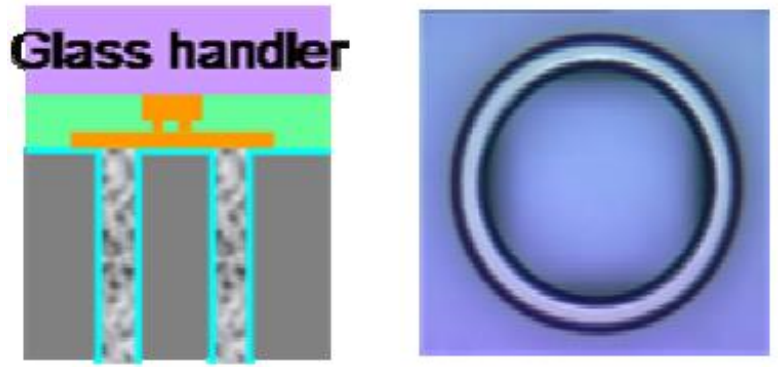
1 Deep Si RIE / Insulate / Metal Fill



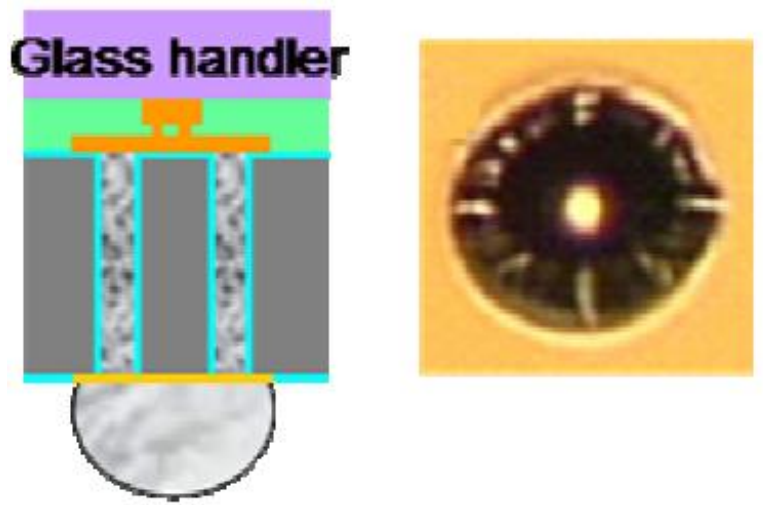
2 Build Wiring Levels



3 Laminate / Thin Wafer / Expose Vias



4 Backside Process / Add BLM & C4



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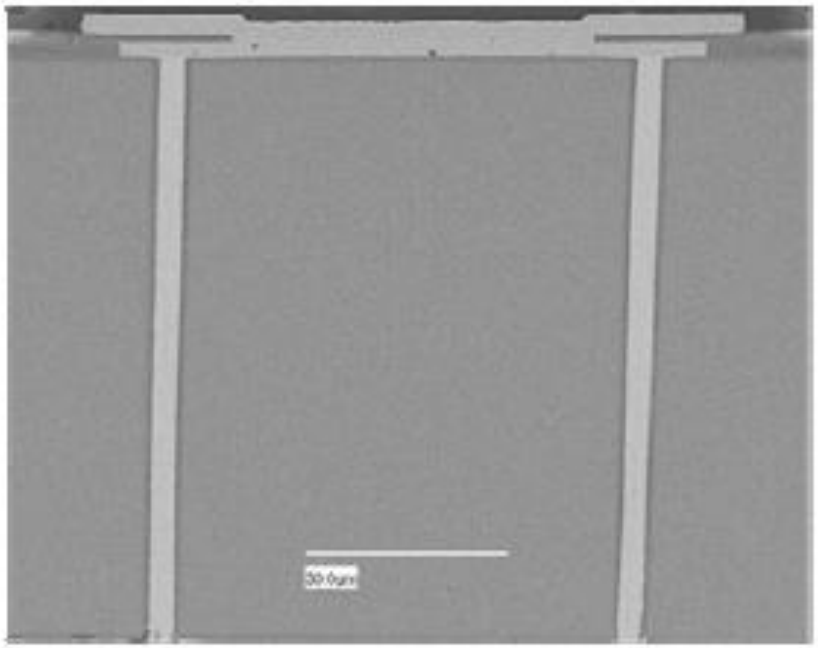
Annular-Shaped Via Approach

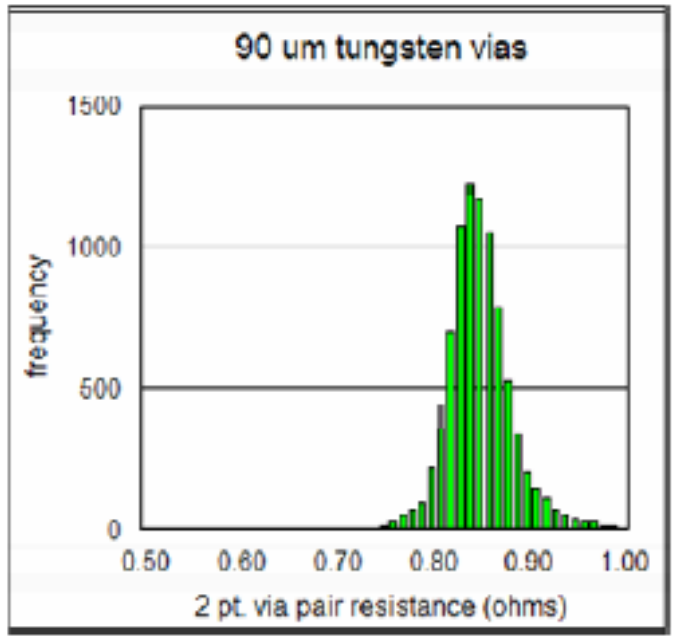


Vehicle B: 20 x 21 mm die

4 µm wide W ring with

50, 90, 150 µm diameter, resp.

→ 99.99..100% yield



mean = 0.851 ohms
sigma = 0.034 ohms
17,194 vias probed
yield = 99.99%

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TSV Fill: Summary and Trends