1. Please explain the term "equivalent scaling" ①

Equivalent scaling refers to 3-dimensional device structure improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of chip.

2. Please name three equivalent scaling measures applied in the interconnection system of ICs

- ~~Into~~ 1. Gate stack
  2. Electro static control
  3. Channel material.

3. Name three important trends in cMOS technology.

- 1) Production of many identical devices/circuits/chips by one process
  → Cost

2) Characteristic quantities:
   - wafer diameter
   → Die size
   → Number of transistors per die
   - Yield

3. New and improved products
   → Require continued increase of degree of Integration
   → Scaling down
   → Increase of die size

4. Define the term "3D integration. What is the motivation to use (or the potential of using) 3D integration technology?

→ 3D-integration implies any stacking of integrated devices (ICs, MEMS) and their vertical mechanical and electrical connection. In order to

→ Increased integration density
→ Increased performance
→ More functionality
→ Reduced power consumption
→ Minimum volume and weight
→ Mixed technologies ; 3D SoC

5. Please name the components of a copper plating bath for Electrochemical deposition and their meaning/function Which types of anodes can be used in ECD (electrochemical deposition)

Basic components: Component	chemical Basis	Meaning
Copper Sulfate	Metal salt	→ Provison of cupric ions → increase in conductivity
Sulfuric acid	Acid	
Additives		
Chlorine	Halogen	→ weak inhabitation of deposition → Necessary for operation of other additives
carrier (suppressor)	Polyether	→ Inhibition of deposit → uniformity of deposit
Brightener (accelerator)	Organic sulfur compound	→ Acceleration of deposition Brigth deposits
Leveler	Organic Nitrogen Compound	→ Strong inhabitation of deposition Smooth surfaces strong grain refiner

Anode types

→ Soluble copper anode (Provides cupric ions)

→ non soluble inert anode (ions are added from extanal source)

8. Please name the goals of ion implantation. In which process modules ion implantation is applied in the CMOS technology? Describe the chanelling effect and give potential measures to prevent this effect.

Goals

→ Doping

→ Modification of material propaties

→ Stoichiometric implantation

CMOS

Well formation

Channelling effect: Ions lose considerably less energy if they travel througth the crystal along low-index directions.

Prevention: → Inclination of ion beam against the surface normal of the wafer

→ Amorphous cover layers

→ Pre-amorphisation

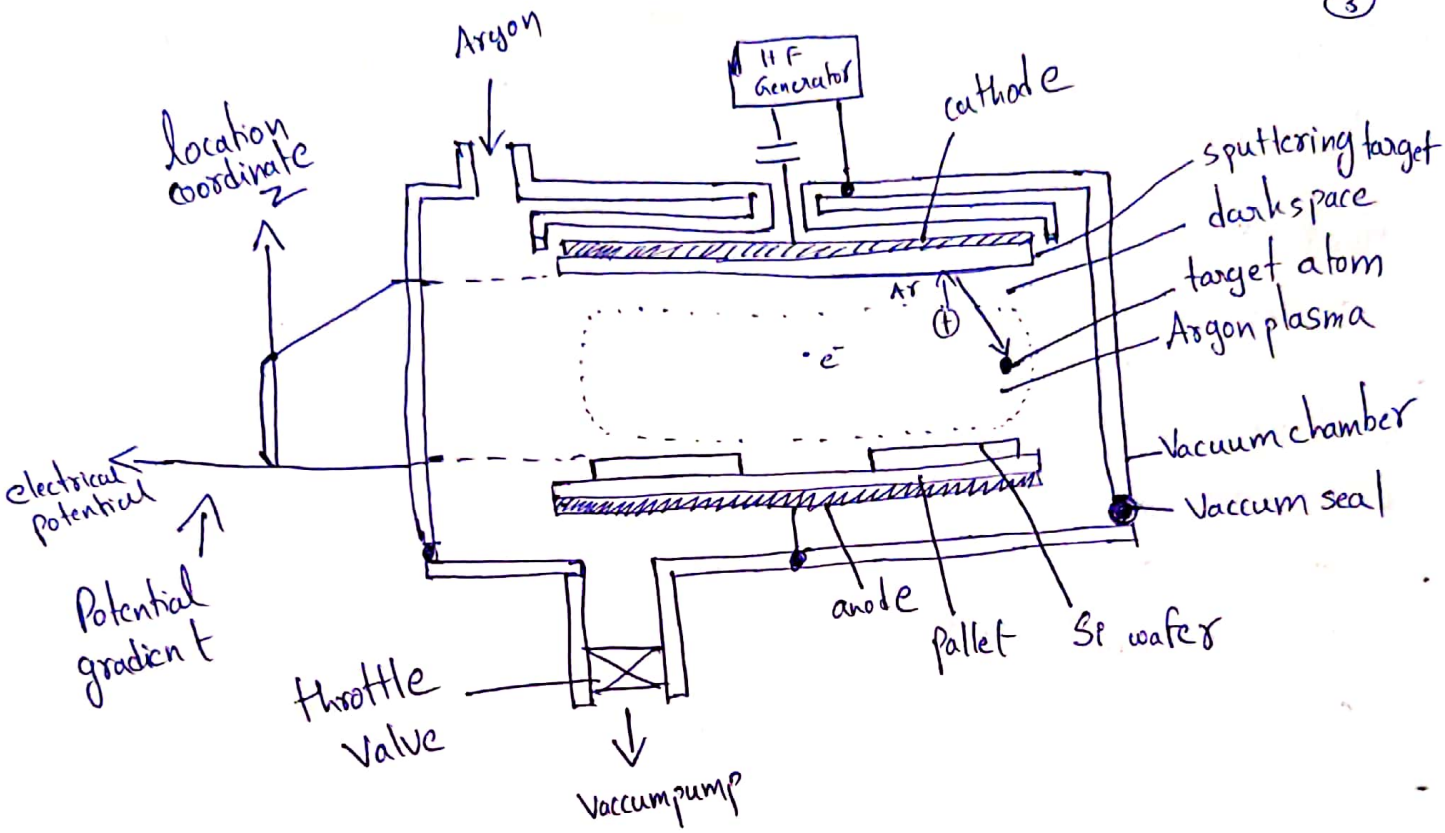
9. What are the objectives of post-annealing after ion implantation? Name the methods/processes of annealing applied in different technology nodes and sorta them by the extent of broadening of dopant profiles due to diffusion strating with the lowest dopant broadening.!

Objectives:

- High degree of dopant activation
- Achievement of superior crystal properties.

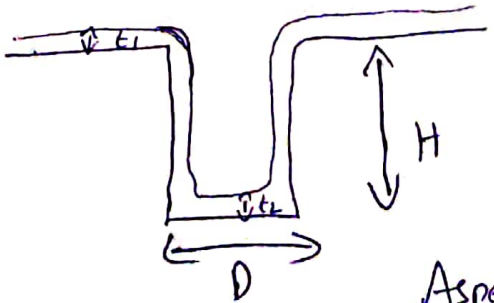
Method	Processtemp	Process time	Broadening of profiles during process time at T = 1100°C
Furnace	900 - 1100	min, h	1 µm (1000 s)
Rapid thermal processing	1000-1250	s	0.1 µm (10 s)
Flash lamp	1000 -1300	ms	0.01 µm (0.01 s)
Laser	1100 - 1400	µs	< 0.01 µm (0.01 s)

10. Draw a schematic cross-section of RF sputtering tool and name/mark the different parts. please draw the electrical potential versus z-axis of the reactor



11. Please define term step coverage by a schematic and the respective equation for calculation.
Please name three approaches for advanced sputtering techniques to improve the step coverage of sputtering process and briefly describe, how the improvement is acheived

Step coverage: The ratio of thickness of film along the walls of a step to the thickness of the film at the bottom of a step



sc: t_2/t_0

Aspect ratio H/D

Advanced tech

-> ionised metal deposition
-> Collimated sputtering
-> long throw sputtering

12. Please name the process steps in the technology flow of a through silicon / Hole via fabrication and front side metallization.

→ Shallow trench isolation
→ Twin well implants
→ Gate structure
→ lightly doped drain Implants
→ Sidewall spacer
→ Source / Drain implants
→ Contact formation
→ local interconnect
→ Via-1 / metal-1 formation
→ " 2 / " 2 "
→ " 3 / " 3 "
→ " 4 / " 4 "
→ Bond pad metal & passivation
→ parametric testing.

13. Which two basic metallization process sequences do exist for fabrication of the interconnect system? Name the conductor materials used in each of them for the Via and line, respectively.