3.9 Advanced Wet Chemical and Cleaning Processes

(A) Electrochemical Deposition (ECD)

also: electroplating (EP) or *electrodeposition*

(B) Electroless Deposition

Status: 27.06.2011

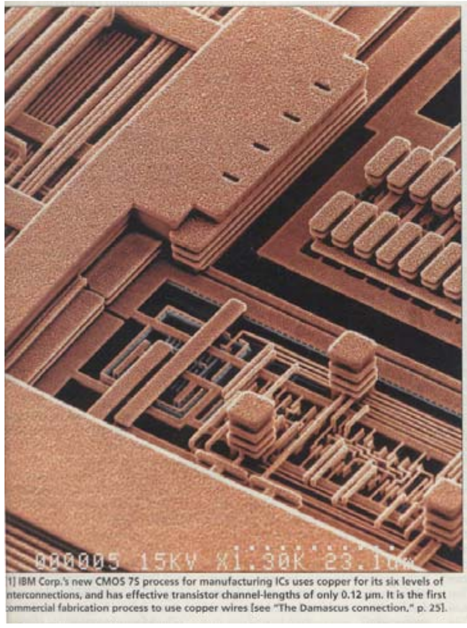
Electrochemical Deposition (ECD) and Electroless Deposition

1. Application of Copper ECD in Damascene Interconnect Systems
2. Equipment for ECD in Microelectronics Front End Processing
3. Basics of Electroless Deposition
4. Electroless Deposition of Copper Diffusion Barriers

Application of Copper ECD in Damascene Interconnects

Background

- Copper has replaced Aluminum in recent years because of higher conductuvity and better electromigration resistance
- Copper ECD has better ability to fill high aspect ratio trenches compared to PVD and CVD and moreover its less expansive
- Filling of multilayer structures in one step can be done (Dual Damascene)

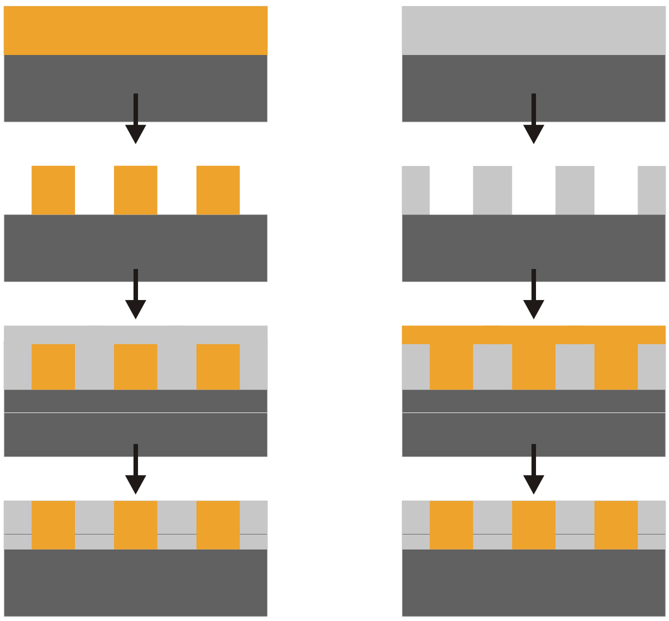


CMOS interconnects [IBM]

Advanced Integrated Circuit Technology

Basic Principle

Conventional Technology		Single Damascene Technology	
Metal deposition			Isolator Deposition
Metal structuring			Isolator structuring
Isolator Deposition			Metal deposition
Isolator back etch and planarization			Metal back etch and planarization



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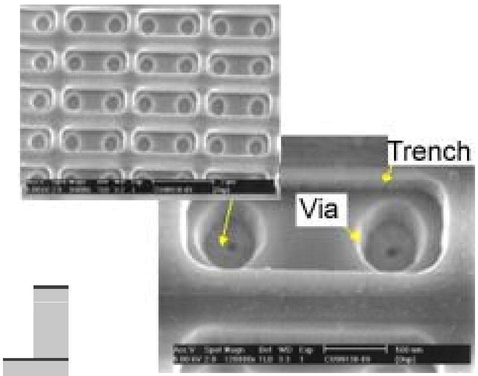
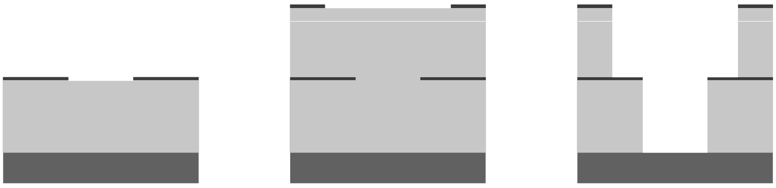
Dual Damascene Technology

- Barrier (Ta/TaN, Ti/TiN) and Cu-seed deposition e.g. by ionized PVD
- Vias and trenches filled in single step ECD

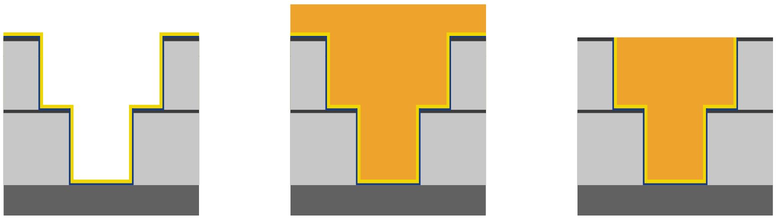


Trench and Vias [IMEC]



Isolator deposition and Hardmask deposition / Structuring (Layer 1+2)

Isolator structuring



Barrier and Seed layer deposition

Cu deposition

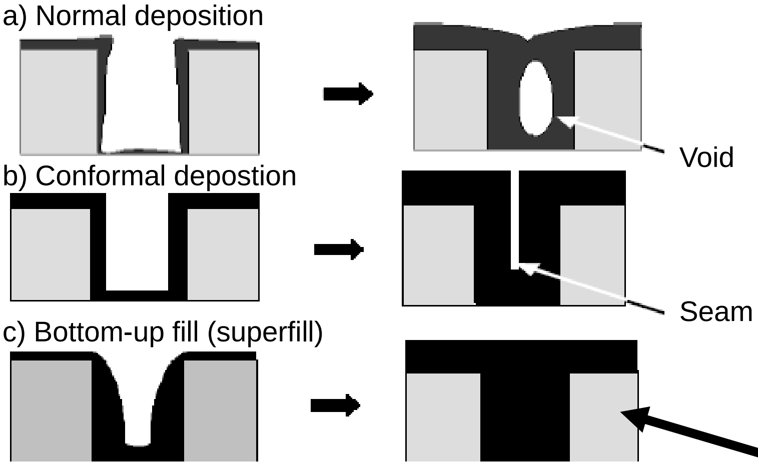
CMP

Fill characteristics – effect of plating additives

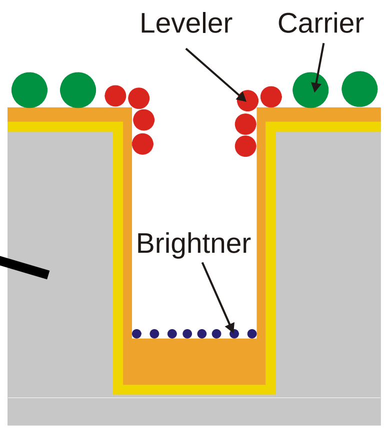
a) Normal deposition

b) Conformal depostion

c) Bottom-up fill (superfill)



Effect of additive composition on fill characteristic [6]



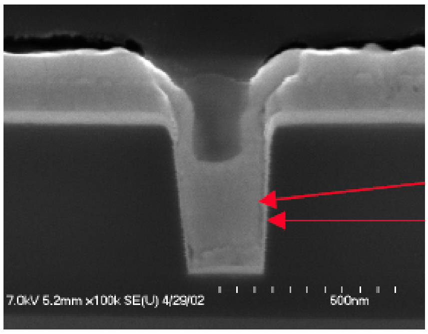
Bottom-up fill with optimized additive composition

a) High current density at trench edges leads to faster deposition at those sites
b) Excess suppressor concentration leads to conformal deposition
b) Optimized composition of additives leads to perfect trench-fill characteristic

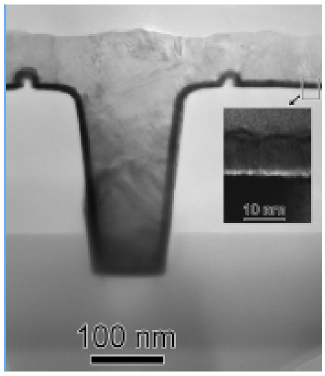
Seedless Plating onto barrier layers

- Background of Seedless plating
  - Defect free seed layers in high aspect ratio trenches are difficult to fabricate
  - Corrosion of thin seed layers in electrolyte
  - Decrease in conductivity in narrow trenches due to higher fraction of resisitive barrier layers

  -> Need for new barrier materials
- Requirements
  - Barrier behavior: Cu not immiscible with barrier
  - High conductivity
  - Good wetting of barrier layer with electrolyte
- Methods and Materials
  - Research is done on: Ru, Pt, Pd, Rh, Ir, Ag
  - Methods: ionized PVD, CVD, ALD



Seed layer in small trenches [7]



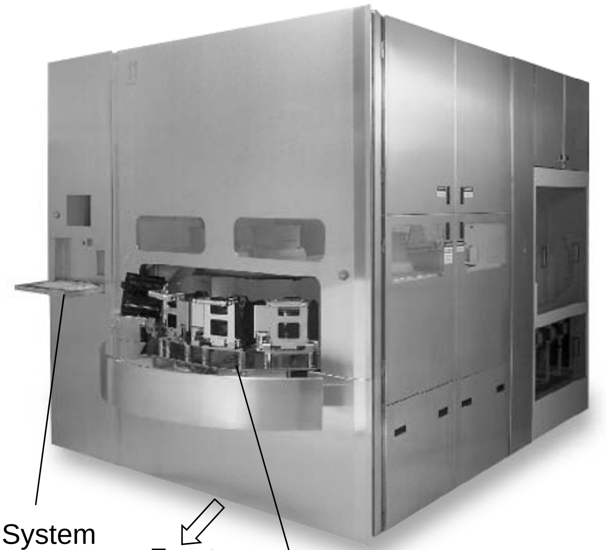
Seedless superfill on 15nm Ir (ALD) [7]

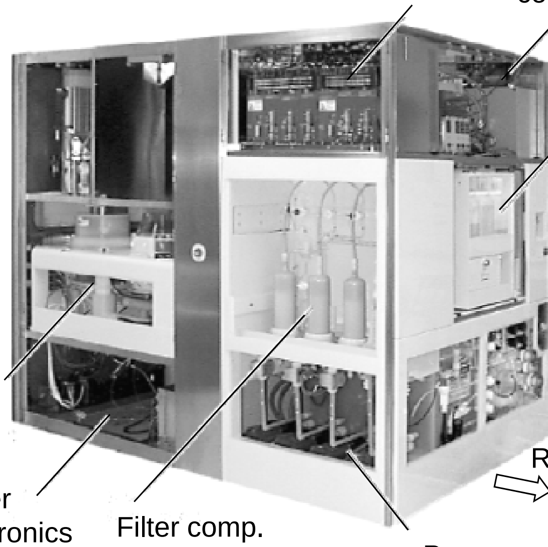
Equipment for Copper ECD

Basic facts

- Pre/post treatment cells for cleaning, rinsing and drying
- Plating cells:
  - Contain plating solution (cupric ion solution)
  - (Soluable) Anode
  - Cathode i.e. workpiece (Wafer) in a holder
- Two basic concepts of plating cells:
  - Vertical cathode-anode-arrangement used in older PCB-plating tools for high troughput
  - Horizontal cathode-anode-arrangement in new PCB tools and in Semiconductor fabrication for more precise deposition processes
- Main manufacturers of electroplating tools:
  - Novellus, Semitool, AMAT
  - Novellus introduced first 45/32nm node electrofill tool in 06/06 (Sabre Extreme)
- Bath chemistry suppliers:
  - Enthone (Cubath Viaform), Rohm&Haas (Ultrafill)

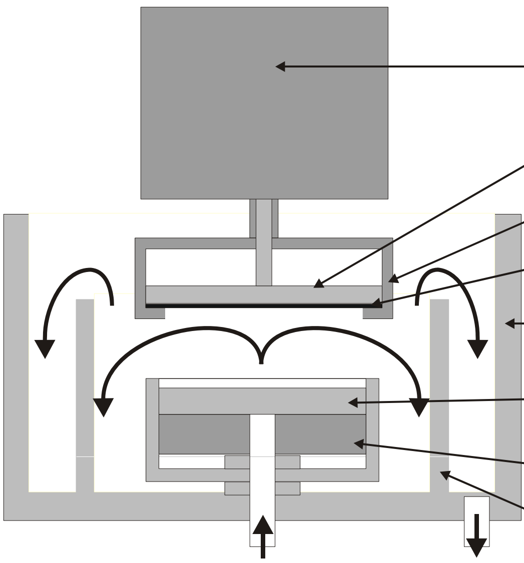
Semiconductor Copper ECD tool (Novellus Sabre Concept II)





Pictures taken from [5]

Fountain Plating Cell



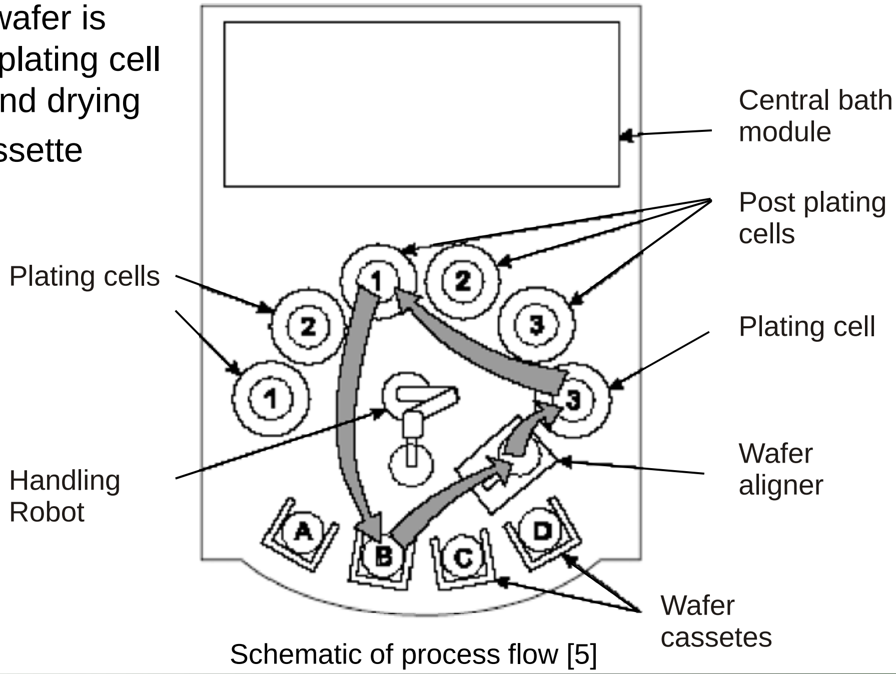
Principle of fountain plating cell

Plating cells and post plating cells in the process compartment [5]

Clamshell [5]

Process flow

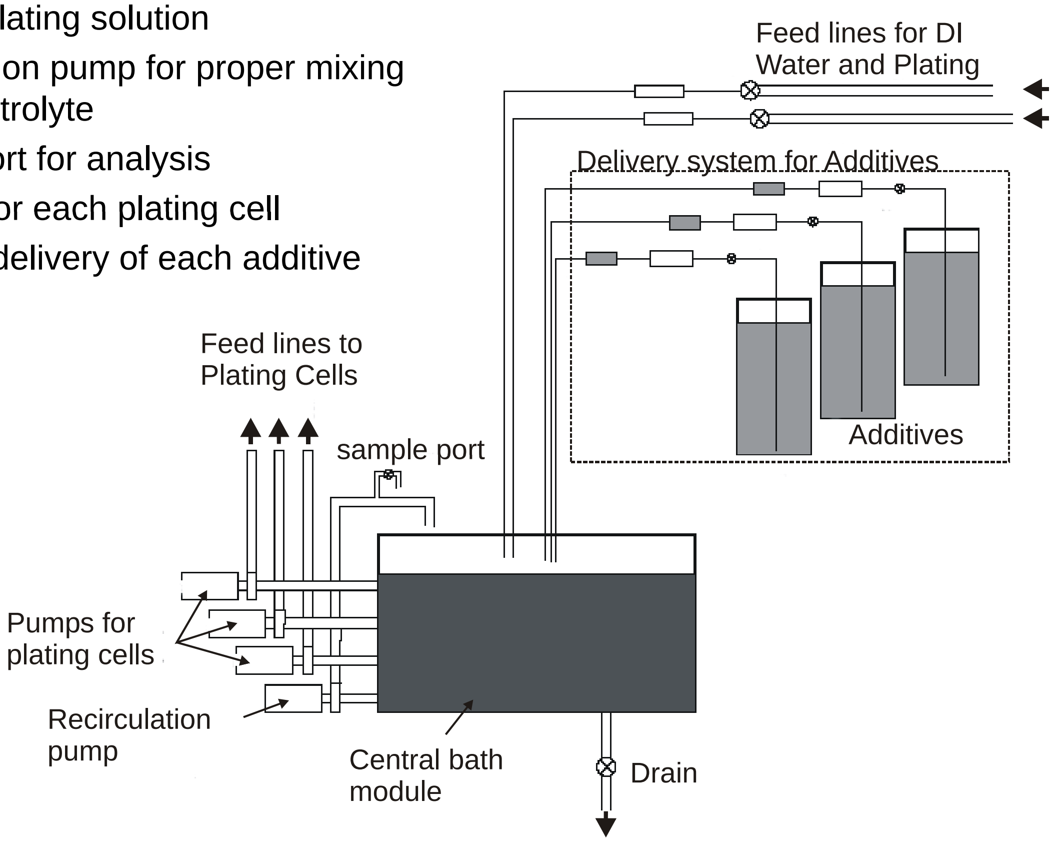
- Wafer cassettes are placed in the cassette nest
- Wafer picked by handling robot out of cassette and placed into wafer aligner
- Centering and alignment of wafer for processing
- Handling robot places wafer into clamshell of plating cell
- Wafer is submerged into the plating solution and DC current is applied
- After processing the wafer is transported to a post plating cell for cleaning, rinsing and drying
- Return of wafer to cassette



Schematic of process flow [5]

Dosing System

- Central bath module: 150l tank contains plating solution
- Recirculation pump for proper mixing of the electrolyte
- Sample port for analysis
- 3 pumps for each plating cell
- Separate delivery of each additive



Schematic of dosing system [5]

Electroless Deposition

Fundamentals

- Deposition process without any external power supply
- Two types of electroless deposition processes:

1. Reduction process
   - Reducing agent contained in the electrolyte
   - Electrons provided by oxidation of the reducing agent

$$\underset{\text{Metal ion}}{Me^{z+}} + \underset{\substack{\text{Reducing}\\ \text{agent}}}{Red} \rightarrow \underset{\text{Metal}}{Me} + \underset{\substack{\text{Oxidized form of}\\ \text{Reducing agent}}}{Ox}$$

2. Ion exchange process
   - Substrate surface has more negative standard potential
   - Electrons from exchange reaction with substrate

Oxidation:

$$Me_1 \rightarrow Me_1^{z+} + z \cdot e^-$$

Reduction:

$$Me_2^{z+} + z \cdot e^- \rightarrow Me_2$$

   - Mostly for protection of bare metals: e.g. Zn, Sn on steel; Au on brass
   - Only thin films because of self-inhibiting effect

Typical chemistry for the reduction process type

Chemistry	Meaning
Metal salt	- Provision of metal ions (e.g. sulfate based)
Complexing agent	- Prevents precipitation of metal salt
Reducing agent	- Supplies electrons for metal ion reduction (e.g. formaldehyde HCHO or hypophosphite $H_2PO_2^-$)
Activator	- Supports/activates oxidation of red. Agent (e.g. Pd)
Buffer	- pH maintenance (e.g. NaOH)
Stabilizers	- Retards homogeneous reactions (e.g. thiourea)
Accelerators	- Increase in deposition rate
Surfactants	- Wetting agent - Removal of evolved gases

Application in Damascene Technology

- Alternative method for seed layer deposition (conformal deposition)
- Deposition of barrier layers (esp. cap on Cu lines)
- Also alternative method for trench superfill

Examples for the reduction process type

- Nickel deposition
  - Deposition in alkaline or acidic solution with nickel provided from $NiSO_4$-salt
  - Complexing agents: organic acid or amine (ethylene diamine, citrate acid)
  - Reducing agent: hypophosphite (e.g. Sodium-hypophosphite: NaH_2PO_2)
  - Buffer for pH-maintenance is e.g. NaOH
  - Basic reaction steps

Oxidation of red. agent: $$H_2PO_2^- + H_2O \rightarrow H_2PO_3^- + 2 \cdot H^+ + 2 \cdot e^-$$

Reduction of Ni ions: $$Ni^{2+} + 2 \cdot e^- \rightarrow Ni$$

- Copper deposition
  - Mostly alkaline solutions with $CuSO_4$ as metal salt
  - Complexing agents
  - Reducing agents mostly formaldehyde (HCHO)
  - Reaction steps:

Oxidation of red. agent: $$HCHO + 3OH^- \rightarrow HCOO^- + 2 \cdot H_2O + 2 \cdot e^-$$

Reduction of Cu ions: $$Cu^{2+} + 2 \cdot e^- \rightarrow Cu$$

Electroless deposition of copper diffusion barriers

Background

- Conventional barrier deposition shows several drawbacks for depositions in narrow trenches (non defect free, pinches at trench top)
- Several process steps (blanket deposition, patterning)

Advantages of electroless deposition to ECD

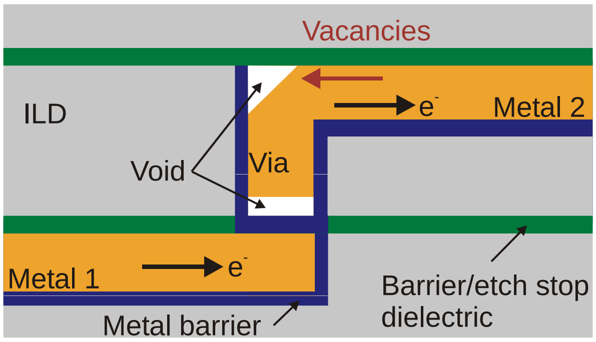
- Conformal deposition even within complex structures (narrow trenches)
- Deposition on non conductive materials
- Possibility of local selective plating - reduced process steps

Possible materials

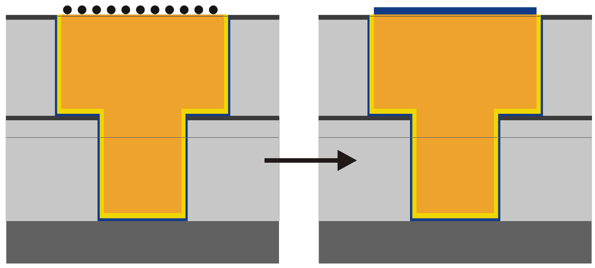
- Ni alloys (NiMoP)
- Co alloys (CoWP, CoWB)

Electroless CoWP

- Used as barrier metal and capping barrier layer
- Usually 90% Co, 2% W and 8% P
- Co forms metal-metal bonds with Cu while W and P stuff grain boundaries to inhibit Cu-diffusion
- Selective deposition onto Cu-lines after Pd-Activation (seeding) – Capping layer deposition with fewer process steps
- Copper reliability improvements through CoWP capping layers (CoWP has strong adhesion to copper and prevents Cu-diffusion/vacancy-movement and thus prevents void formation)
- Device performance improvement due to lower k_{eff} compared to previous capping layers (SiN, SiC, SiCN)



Void formation through weak Cu-barrier/etch stop layer adhesion [10]



Electroless CoWP as capping layer – Process steps

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