* BPS - Basic Process step -

-eg. Special diffusion step (pre-deposition), implantation step, special cleaning step (rinsing)

- Indivisible.
- Characterized by special parameters. physical / chemical parameters.

-Technology = Σ BPS.

* Process →
  - consists of one or more BPS
  - carried out by specific tools
  - standardized component of technology.
  - results in achievement of specific property of action

eg. doping (pre-deposition)
photolithography (deposition of resist, exposure, development)

* Process technology →
  - physical & chemical properties of action.
  - technical realization (equipment)
  - integration issues.

* Basic technology -
  - sum of processes, (or BPS) to be performed for fabrication of specific product

eg. BICMOS, SBC, SGT..

4. Basic MOS Transistor types

NMOS - enhancement type.
PMOS - enhancement type
NMOS - Depletion type
PMOS - Depletion type

3. Important trends in CMOS technology -

→ geometrical scaling
Integration degree
performance increase
increase of die size.
cost decrease per function.

5. Front end → wafer level fabrication process
Back end - packaging.

6. Basic process steps of CMOS technology.

→ ~~Photolithography~~
1. wafer processing
2. oxidation
3. Epitaxy
4. Deposition
5. Ion implantation
6. Diffusion.
7. fabrication.

4. Scaling :-

Geometrical scaling :- (const. field scaling) refers to the continued shrinking of horizontal and vertical feature ~~of~~ sizes of the chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) & reliablity values to appl^n & end customers.

Equivalent scaling :- (occours in conjuction with, and also enables, continued geometric scaling) refers to 3-Dimensional device structure (Design factors) improvements plus other non-geometrical process techniques and new materails that affect electrical performance of the chip.

ex- Cu, low-K, HKMG, electrostatic control, new channel materail, strain Engineering / stressors.

7. Gas phase deposition process

- Sputtering –
  - Interconnects for diffusion barrier, seed layer,
  - Electroplating
  - metal (Al) Alloys –

ex- Ti, TiN, ToN, Ta, metal (Al Alloys)

- CVD - Chemical vapour Deposition
  - Dielectric - SiO_2 Doped SG, Low K - dielectric SiN:H, SiCN:H, Metals, metal Nitrides. (TiN - production)

- ALD - Atomic layer deposition

High K dielectric, HfO_x, HfS_x, Si_xO_x

- Epitaxy →

P epi layer SiGe, Si on top for strain management.

Liquid phase Deposition process

- Electrochemical Deposition (ECD) - interconnect Cu; damascene (Cu)

- Electroless Deposition - Cap layer on Cu damascene Improve EM by factor 3 to 5. (CoWP)

- Spin on Deposition

Spin - coating Dielectrics spin - on glass, low k dielectrics ultra low k dielectrics, photoresists.

8. ~~What is~~ Ultra
motivation- use ultra low k dielectric ~~as~~ as insulater in on chip inter connect systems insted for SiO_2 for high performance CMOS technology?

which low k dielectrics are used? (with k value?)

→ Ultra low k dielectric used in high performance system → to reduce 'parasatic capacitence' → cross talk ↓ → signal delay↓,

~~the~~ low k dielectrics used →

SiOF → $k = 3.4 \sim 3.6$

SiCOH → $k = 2.6 \sim 3.0$

P-SiCOH → $k < 2.6$

$k = 2.0 \sim 2.6$

9. Fabrication method for porous CDO / SiCOH films (~~Types of~~

Type of process → PECVD

precursors → organosillane + porogen (TMS)

post treatment → ~~porogen~~ UV cure / UV thermal ~~assisted~~ processing ~~anneal~~ processing

→ • porogen is embedded in SiCOH matrix and evaporated during thermal or UV assisted anneal
- porogen removal & cross linking / mechanical stablity (E, H) porosity / density [optical RI].

sputtering process →

- Target materail & substrate placed in vaccum chamber
- A voltage is applied bet^n them so that target is cathode & substrate anode.
- Plasma is created by ionizing sputtering gas (Ar)
- Sputtering gas bombards target & sputters off the materail we'd like to deposit.

11. Lithography used in 32/28 nm technology nodes.

→ 193 nm immersion lithography.

feature size.

Resol^n limit → $I_{min} = K_1 \cdot \frac{\lambda}{NA}$.

immersion lithography.
λ = 193 nm,
NA - Numerical aperture

3ways to limit Imin

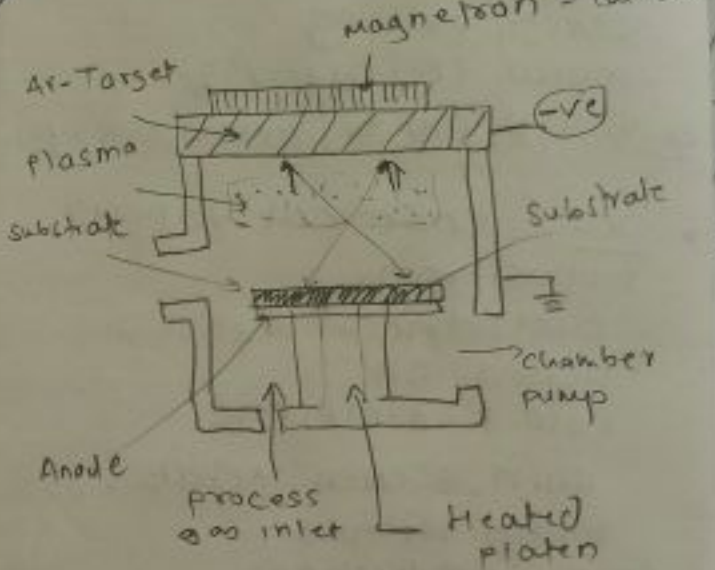
1. Reduce λ.
2. Increase NA.
3. reduce K_1

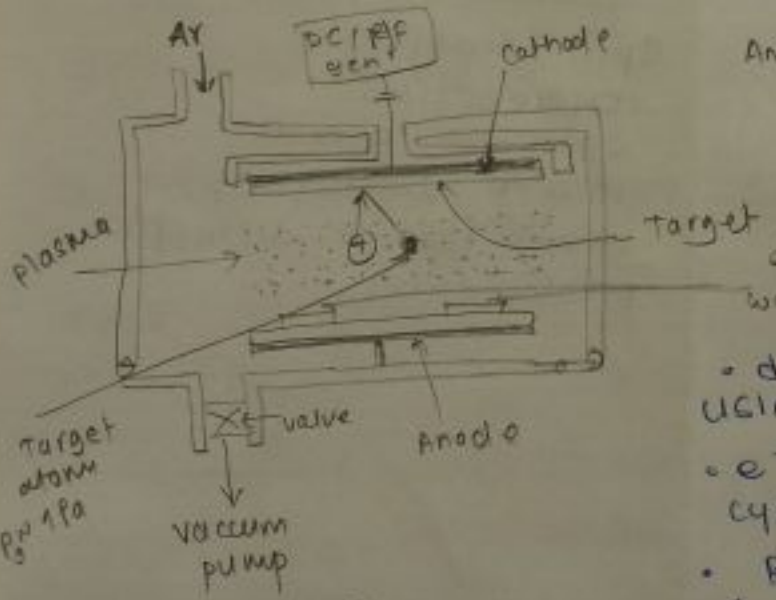
Resolution Enhancement Techniques.

1. OPC - Optical Proximity ~~Detection~~ Correction
2. OAL - Off Axis Illumination
3. PSM - Phase shift Mask
4. DE/DDL - Double Exposure
   Double Dipole Lithography

10. Basic mechanism of sputtering
- How does process work?
- Schematic cross-section of conventional sputtering chambes. (RF / DC magnetron sputtering)
- Name Modern sputtering principles to coat contact & via holes with aspect ratio (improvement of film coverage, in patterns)

Principle →
Target consist of the materail, which should be deposited on wafer.





Bias sputtering →
- Additional cathode vtg. -ve DC will be connected to substrate.
- portion of Ar^+ ions will accelerated in wafer dir^n.
→ energy of film growth increases

magnetron
- deposition rate increases using magnetic field.
- e^- will be brought on cycloids.
- By additional magnetic field trajectories of electrons elongates.
- Results in increase of ionization probablity at same pressure.

12. Methods for Dry photoresist removal.

→ 1. Plasma Stripping (in barrel reactors)
2. Downstream stripping
3. Plasma-free stripping.

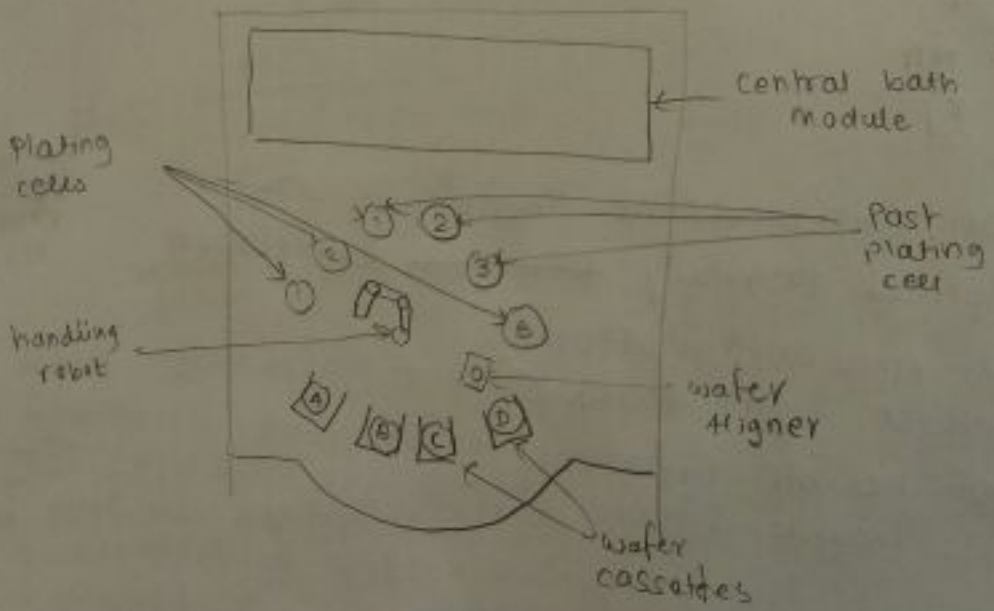
13. Advantage of using cluster tools in semiconductor processing.

- example- Integrated process flow performed in a cluster tool.
- schematic- cluster tools.

Cluster tool - Advantage → integrated processing in same environment. (vaccum)
→ saves time, → throughput defined.

eg Pre-clean TiN CVD - WCVD.

schematic



1. Process modules of conventional (Si gate, Si bulk) CMOS technology front end process flow in right sequence.

1. Shallow trench isolation (STI)
2. Twin well implants
3. Gate structure
4. Lightly doped drain implants.
5. Sidewall spacer
6. Source / Drain implants.
7. Contact formation,
8. Local interconnect.
9. Via-1 / Metal 1 formation
10. Via 2 / Metal 2 formation
11. Via 3 / Metal 3 formation
12. Via 4 / Metal 4 formation.
13. Bond Pad & metal passivation.
14. Parametric Testing.

contact formation :-

process flow.

- Removal of oxide from S/D ~~gate~~ & poly gate.

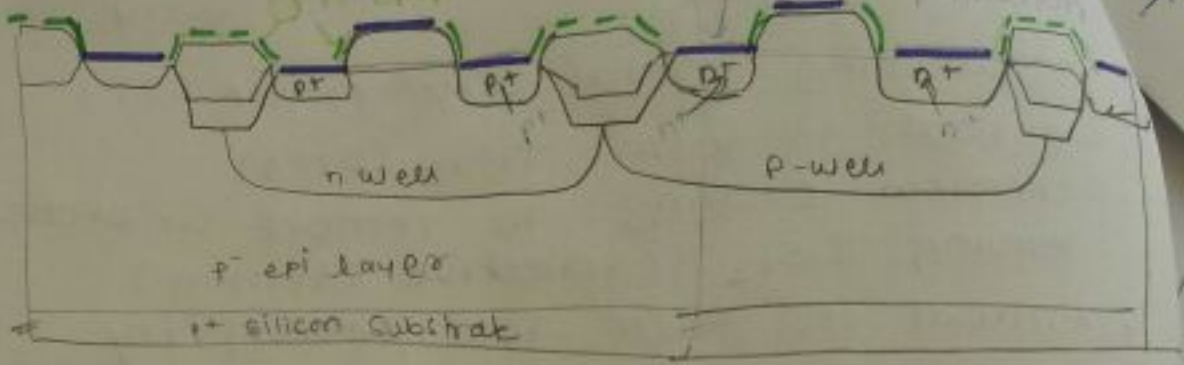
1. Sputtering metal with Argon (Ar)
2. Anneal to form $TiSi_2$ (RTP1)
3. chemical etching to remove unetched Ti, leaving $TiSi_2$ (selective etching)
4. Anneal to form low resistivity $TiSi_2$ (RTP2)

Details :- why silicides, silicidation, reaction / no-silicidation on SiO_2, RTP1 (700-750°C - C49 phase) RTP2 (800-900°C C54 phase), selective wet etch ($NH_4OH / H_2O_2 / H_2O$)

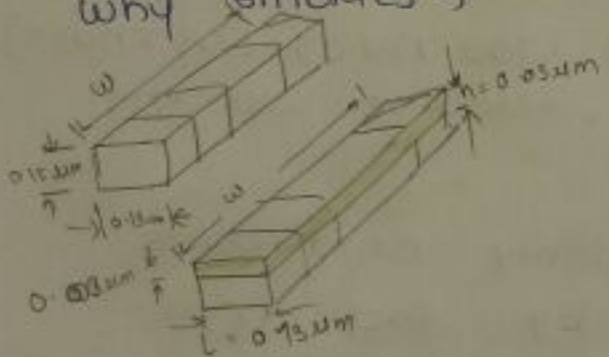
→ Metal contacts & highly conductive gate lines are formed by fact that many metals (eg Ti, Co, Pt) will no bond to SiO_2, but will easily form silicides with bare silicon. During modest heat treatment Ti/Si interface undergoes solid phase reactions forming $TiSi_2$. This contact is perfect ohmic contact with the silicon substrate.

The Ti in contact with SiO_2 doesnot stick. so a slight metal etch will remove this Ti. since Ti is already reacted & formed ~~#~~ $TiSi_2$ in the contact areas & on poly lines, This ~~omits lithography step~~ compound is impervious to Ti etchant. This omits lithography step.

- Ti is a good choice for metal contacts due to low resistivity & good adhesion.
- No mask needed, self aligned (silicide) formation



Why silicides →



Doped poly Si.

$\rho = 4500\ \mu\Omega\text{cm}$

$\rho/H = 300\ \Omega/\text{square}$.

$R = \frac{\rho}{H} \times \frac{W}{L}$.

Silicided poly-Si

$\rho = 18\ \mu\Omega\text{cm}$.

$\rho/H = 6\ \mu\Omega/\text{square}$

$R = \frac{\rho}{H} \times \frac{W}{L}$.

low resistance

↓

high conductivity

↓

to increase conductivity of contacts

15. Contact formation -

16.

Motivation to use High K metal gate

→ Enable conventional scaling of transistor as well as reduced stand by power due to reduction in gate leakage.

At device level, the performance improvement achieved by introducing HKMG is two fold.

Considering eqn in long channel approx" ①

$$I_{on} = \frac{\mu_{eff} \cdot C_{ox,inv}}{2} \frac{W}{L} (V_{gs} - V_T)^2$$

$$C_{ox,inv} = \frac{K \cdot \varepsilon_0 A}{T_{inv}}$$

A - capacitor Area ($W \times L$)
ε_0 - permittivity in vaccum.

* Drive current enhanced with HKMG with higher gate capacitance resulting from higher permitivity of high K dielectric ~~so~~ over SiO_2 along with ~~$$~~ scaling of T_{inv}. Thanks to Metal gate.

Gate First → (MIPS - Metal Inserted Poly-Si) ↗ metal electrode deposited before high temp anneal

pro: conventional process flow.
cons: Thermal budget, complex V_T tunning, mobility, reliability at thin EOT.

Gate Last → (RMG - Replacement Metal Gate) ↗ metal electrode deposited after high temp anneal

pro - thermal budget, higher strain from embedded ~~SiGe~~ SiGe S/D.

cons - complexity,
cost,
more restricted design rules.

17. ~~Describe~~

HKMG - Gate Last -

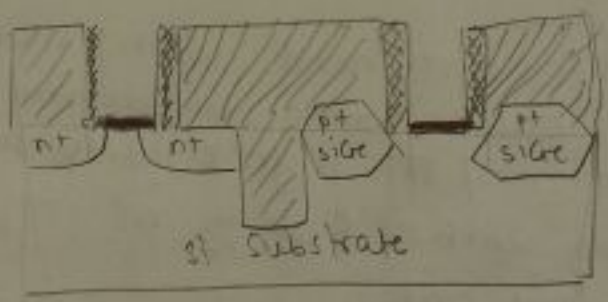
1. Poly Si Gate, High K Dielectric, NMOS, PMOS, n+, n+, p+ SiGe, p+ SiGe, Si Substrate

1. standard transistor process through source-drain formation, but including atomic layer deposition high-k dielectric.

2. spacer, NMOS, PMOS, n+, n+, p+ SiGe, p+ SiGe

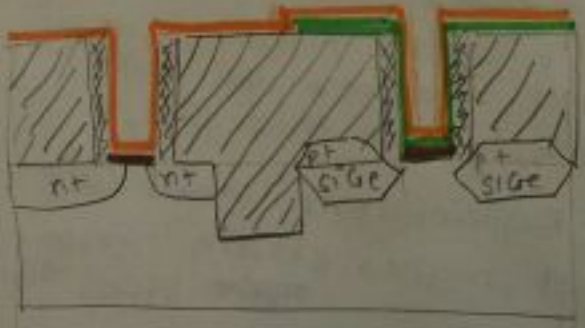
2. Deposit & planarize oxide layer

3. remove poly Si by ↓ selective etching

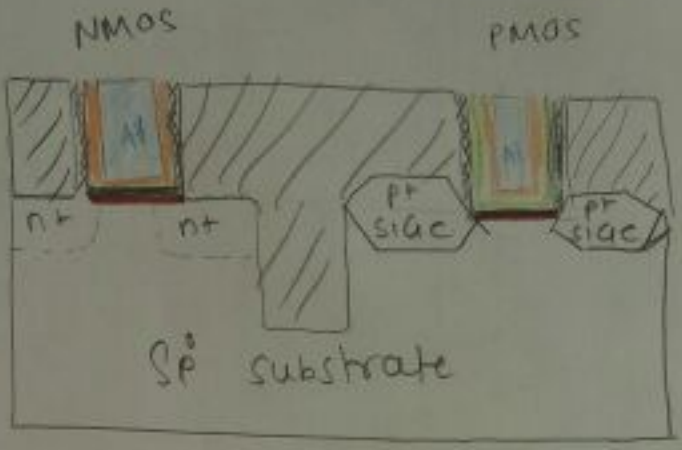


3. Etch out sacrificial poly Si gate

4.

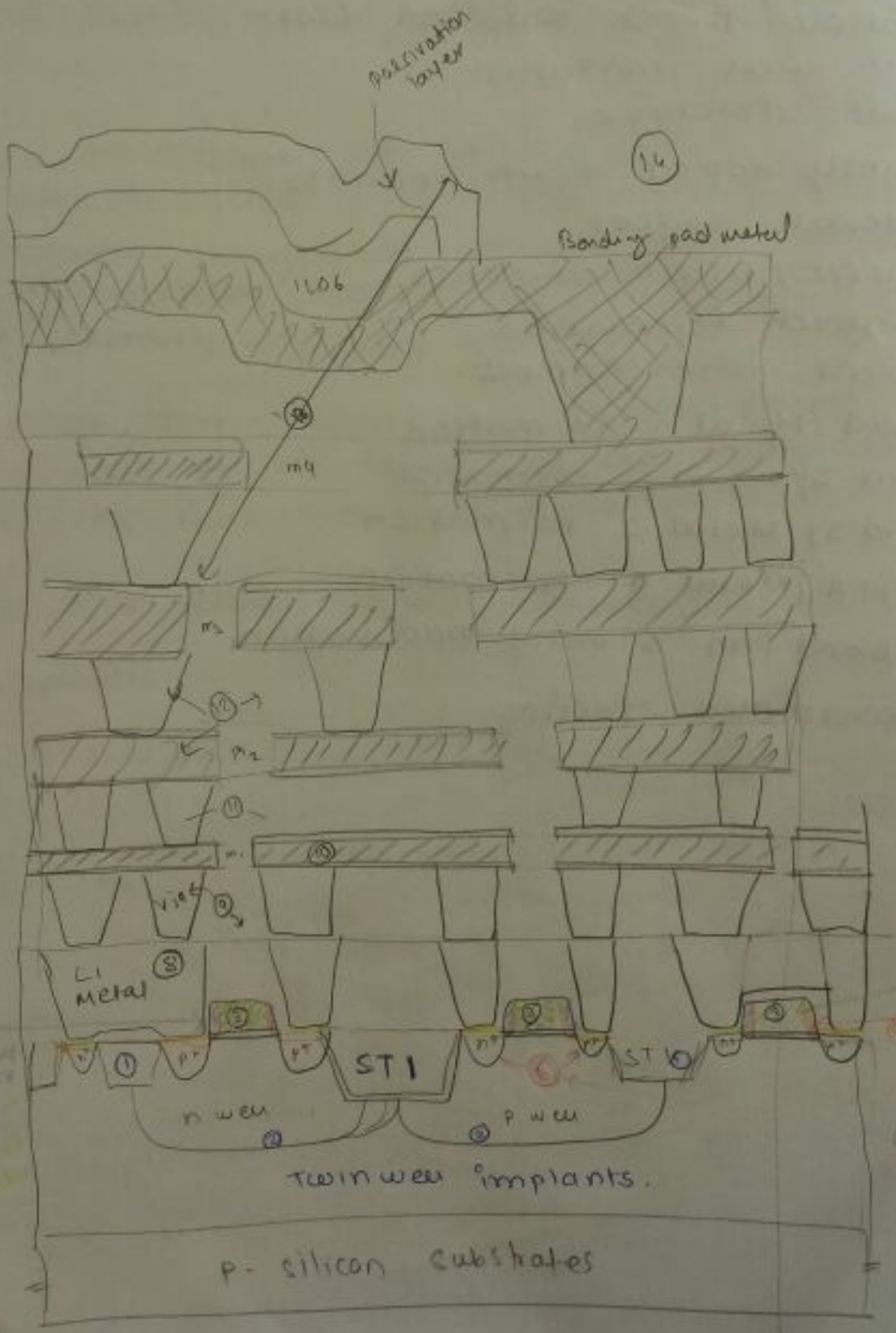


Deposit seperate NMOS & PMOS WF metal layers.



4 - Deposit Al Fill metal, planarise surface.

Completely fill gate materail.
then apply CMP- chemically mechanical polishing.


Passivation layer
14
Bonding pad metal
via6
m4
m3
m2
m1
via1
Li Metal
ST1
ST2
n well
p well
Twin well implants.
p- silicon substrates