Questions Seminar 5 part 1

1. Please explain the specifics of ALD in comparison to CVD!
2. What are the steps of an ALD cycle?
3. Please name potential applications of ALD thin films!

4. Please name the basic process steps in the process flow of lithography and patterning!
5. Please name and discuss the equation for the resolution! (How to lower critical dimension CD = min. printable feature size)
6. Please name the applied resolution enhancement techniques (RET)

7. Please define the terms “anisotropy” and “selectivity”!
8. What are potential dry etching techniques? Please name the respective etching mechanisms and the achievable anisotropy!
9. Please draw a reactor for reactive ion etching and name the different parts!

Q8 What are potential dry etching techniques? Please name the respective etching mechanisms and the achievable anisotropy!

Technique	*Mechanism - Directional behavior*
Barrel etching	Chemical - isotropic
Plasma etching Reactive ion etching	Physical & chemical – isotropic with anisotropic component ?
Physical etching (sputter etching) ion beam etching	Physical - anisotropic Physical - anisotropic

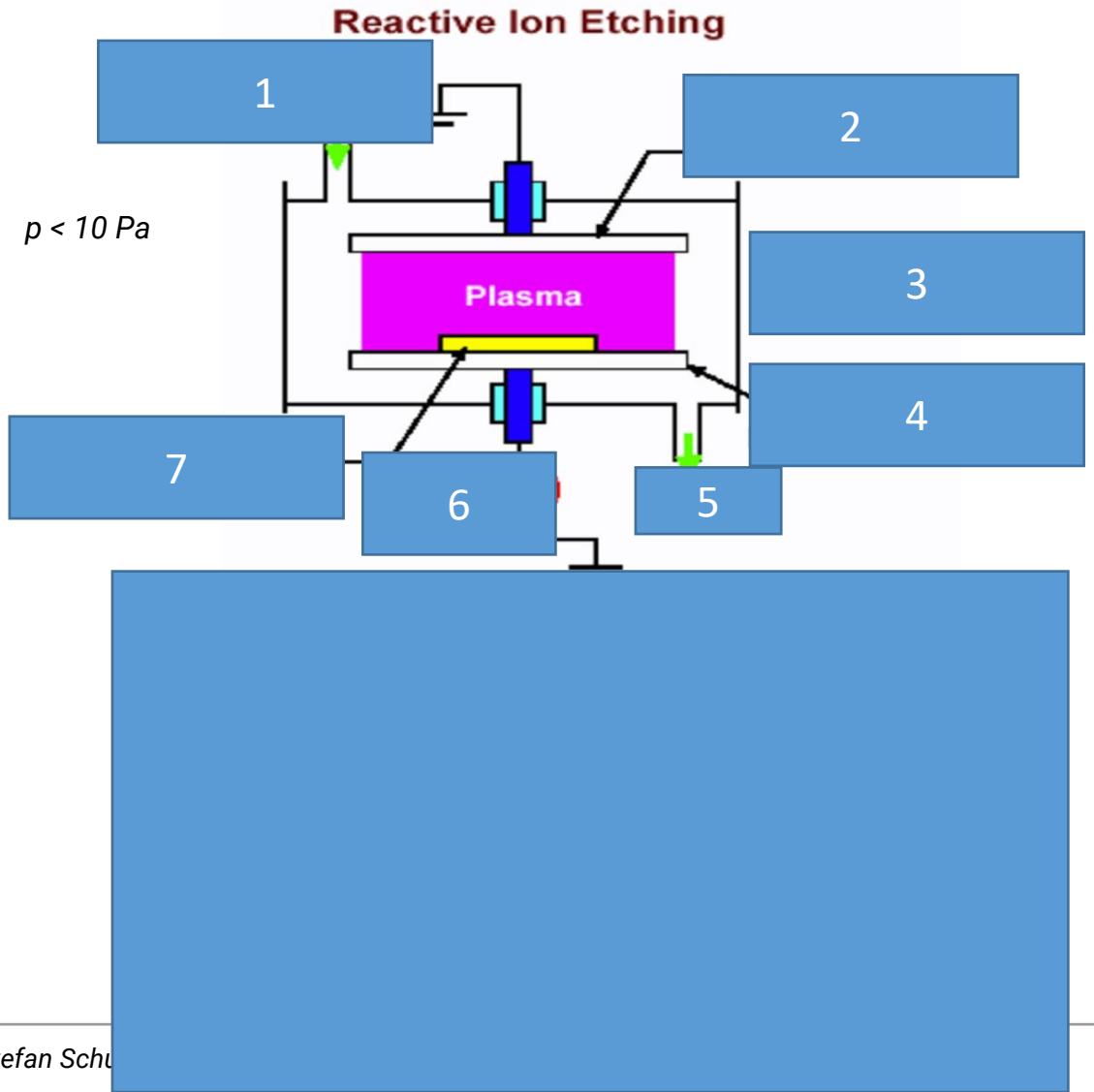
Q8 What are potential dry etching techniques? Please name the respective etching mechanisms and the achievable anisotropy!

Technique	***Mechanism***	***Directional behavior***	***Application***
Barrel Etching	*chemical*	*isotropic*	*film removal (PR)*
Plasma Etching (PE)	*phys. &* **chem.**	*isotropic with anisotropic component*	
Reactive Ion Etching	**phys.** *& chem.*	*anisotropic with isotropic component*	**film patterning**
Reactive Ion Beam Etching (RIBE)	*phys. & chem.*	*anisotropic with isotropic component*	
Sputter Etching	*physical*	*anisotropic*	*surface cleaning*
Ion Beam Etching (IBE)	*physical*	*anisotropic*	

Comparison of dry etching methods

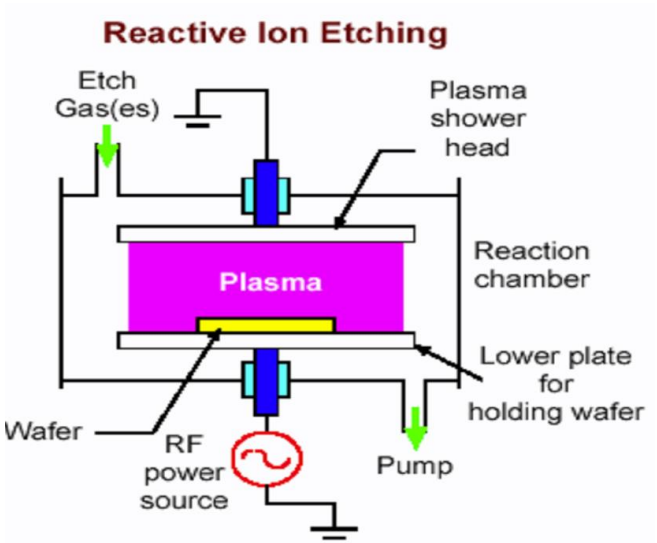
Technique	*Mechanism*	*Etching particles*	*Pressure [Pa]*	*Directional behavior*
Barrel Etching	*chemical*	*reactive radicals*	*100*	*isotropic*
Plasma Etching (PE)	*phys. & chem.*	*reactive radicals, weakly ion assisted*	*10 - 100*	*isotropic with anisotropic component*
Reactive Ion Etching (RIE)	*phys. & chem.*	*reactive radicals, strongly ion assisted*	*1 - 10*	*anisotropic with isotropic component*
Reactive Ion Beam Etching (RIBE)	*phys. & chem.*	*reactive ions*	*≤ 0.01*	*anisotropic with isotropic component*
Sputter Etching	*physical*	*inert ions*	*1 - 10*	*anisotropic*
Ion Beam Etching (IBE)	*physical*	*inert ions*	*≤ 0.01*	*anisotropic*

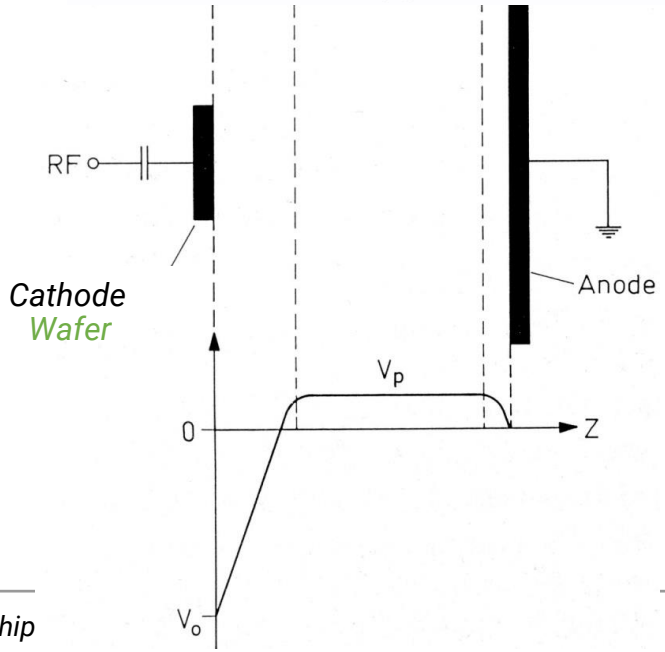
Q9 Please draw a reactor for reactive ion etching and name the different parts!



Q9 Please draw a reactor for reactive ion etching and name the different parts!

p < 10 Pa





Questions Seminar 5 part 2

1) Name the four “gas phase deposition processes” used in advanced CMOS IC technology. For each of these processes give one example for a material/thin film deposited in front end technology in production and one example for a process module, where this material/thin film is applied in production!.
2) Process module “Poly Gate Structure”: What are the basic process steps and the materials used?
3) What is the motivation to use high-k/metal gate (HKMG) structures instead of conventional SiO2/poly Si gate structures? Name the two technology approaches for HKMG applied in production! Describe the process flow of the process module “HKMG – gate last” by naming the five steps of its realization!
4) What are the benefits of silicon on insulator technology relative to conventional silicon bulk technology?
5) What is the motivation to use local stress/strain generation / strained silicon in CMOS transistors? Which type of strain do you need to enhance the NMOS and PMOS transistor, respectively? Name two approaches for local stress generation in CMOS transistors!

Q1/1: Which gas phase and liquid phase deposition processes are applied in advanced integrated circuit technology?

Gas Phase	Liquid Phase
CVD	Electrochemical Dep. (ECD)
Sputtering (PVD)	Electroless Deposition
ALD	Spin-on (deposition)
Epitaxy	

Q1/1: Which gas phase and liquid phase deposition processes are applied in advanced integrated circuit technology?

Gas Phase	Liquid Phase
PVD (Sputtering)	Electroplating / ECD
ALD	Spin on
CVD	Electroless Deposition
Epitaxy	

Q1/2: Gas phase deposition processes: which are materials to be deposited and its applications(s) in advanced integrated circuit technology?

Gas Phase	Materials	Application	Process Module
Sputtering	Metals (Cu, Al) TiN, TaN	Interconnections (Al lines, Cu seed for line/vias) Diffusion barriers, hard mask, ARC	
CVD	SiO2, low-k d. TiN Poly-Si SiN W	Interlayer dielectric Liner for W, diffusion barrier Gate electrode Etch/CMP stop layer, passivation, barrier Contact & via fill	
Epitaxy	SiGe p^- Si	Strain inducing template (increas channel mobility), raised S/D Prevent/minimize latch-up effect	
ALD	HfOx, ZrOx, mixed oxide AlOx, … TiN, W(C)N	High-k dielectric for gate dielectric High-k dielectric for capacitors Diffusion barriers, work function adjustment layers	

Q1/2: Gas phase deposition processes: which are materials to be deposited and its applications(s) in advanced integrated circuit technology?

Gas Phase	Materials	Application	Process Module
Sputtering	Al Cu Ti, Co	Interconnects (lines = horizontal interconnects) Seed layer for ECD (interconnect) S/D/G contact silicidation (SALICIDE)	Vx/Mx Vx/Mx Contact formation
CVD	TiN, WN SiO2 SiN W Poly-Si	Diffusion barrier (Cu), liner (W) Isolate transistors, ILD/IMD Passivation, CMP stop, Etch stop Vertical interconnects (via), LI Gate electrode	Vx/Mx, LI STI, Vx/Mx Bondpad/Passiv., STI, LI+Vx/Mx Vx/Mx, LI Gate formation
Epitaxy	p^- Si SiGe/Si on SiGe	Prevent latch effect Strain inducing templates, raised S/D → increase channel mobility	STI
ALD	HfOx, ZrOx, AlOx, mixed oxides TiN, W(C)N, TaN Cu Metal nitrides	High-k gate or capacitor dielectric Diffusion barrier (in Cu interconnects) Seed layer for Cu ECD Work function adjustment for high-k/metal gate	Gate formation Vx/Mx Vx/Mx Gate formation

Q1/3: Liquide phase deposition processes: which are materials to be deposited and its applications(s) in advanced integrated circuit technology?

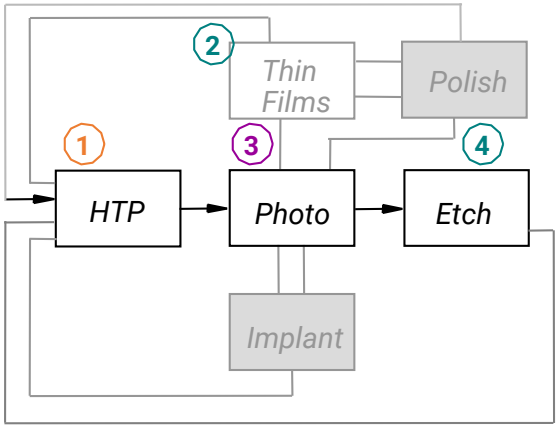
Gas Phase	Materials	Application	Process Module
ECD	Cu	SD/DD Interconnects	Vx/Mx
Electroless Dep.	CoWP	Cap layer on Cu interconnects → increase electromigration resistance/lifetime	Vx/Mx
Spin on	Photoresist	Mask material in doping (II) and patterning	Twin well, LDD, S/D Nearly all (except spacer formation and contact formation)
	Low-k/porous low-k dielectrics	ILD/IMD	Vx/Mx

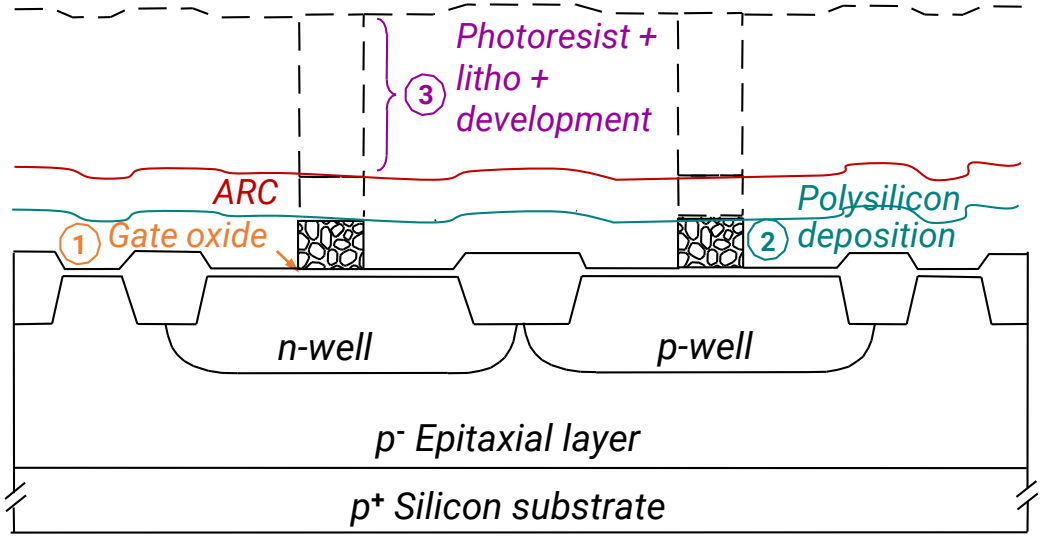
Q2 Process module “Poly Gate Structure”: What are the basic process steps and the materials used?

- *High quality gate oxide deposition (SiO2) – dry thermal oxidation*
- *PECVD of Poly-Si*
- *Deposition if the antireflective coating (ARC) layer*
- *Lithography defining the gate structure*
- *Dry etching (RIE, anistropic) to pattern ARC, Poly-Si, gate oxide*
- *Resist stripping*
- *Selective wet etching to remove the ARC*

Poly Gate Structure

- *Formation of ~2.5 nm highest quality SiO_2 (gate oxide)① by dry thermal oxidation at 1000 °C.*
- *Polysilicon (~300 nm) is then deposited on the wafer by PECVD using silane (SiH_4) ②. Since the temperature is moderate (< 500 °C) the silicon forms in poly-crystalline grains.*
- *Deposition of antireflective coating (ARC)*
- *Photoresist is applied and the most critical litho is done incl. resist developement ③ (4th mask, defines poly gates and local poly interconnects). The gate width is the smallest dimension which will be required.*

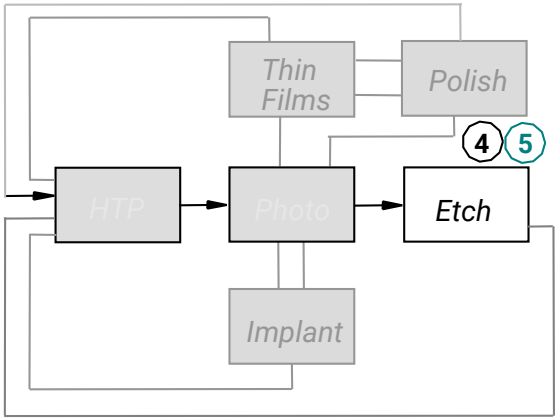


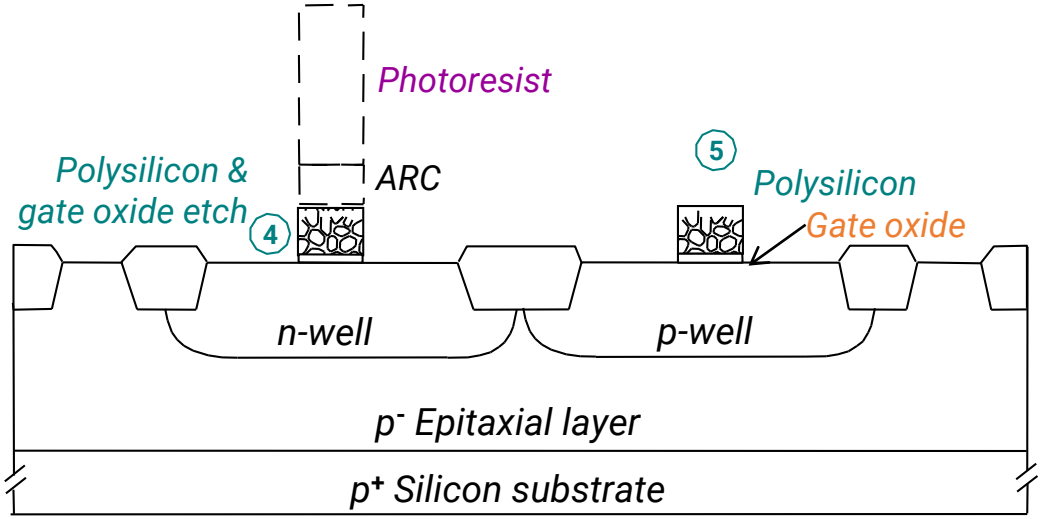


Poly Gate Structure

- *The ARC, polysilicon and the gate oxide is then dry etched (anisotropic etching) ④.*
- *Photoresist is stripped*
- *ARC is removed by selective wet etch*

⑤





Q3/1 What is the motivation to use high-k/metal gate (HKMG) structures instead of conventional SiO2/poly Si gate structures? Name the two technology approaches for HKMG applied in production!

Motivation:

- High k gate dielectrics allow for reduction of leakage currents due to tunneling
- Lower the power consumption → allow further scaling
- metal gates mitigate gate depletion effects that occur in poly-Si gates

Technology approaches:

- Gate first - MIPS
- Gate last

Q3/1 What is the motivation to use high-k/metal gate (HKMG) structures instead of conventional SiO2/poly Si gate structures? Name the two technology approaches for HKMG applied in production!

Motivation:

HKMG: performance improvement

- *HKMG technology promises to enable conventional scaling of the transistor as well as reduced stand-by power due to a reduction in gate leakage.*
- *Taking Intel's technology roadmap as a example (Fig. 5.2.1), switching to HKMG at the 45nm node enabled to resume the electrical gate dielectric scaling, while reducing the gate leakage by more than 10x.*
- *At the device level, the performance improvement achieved by introducing HKMG is two-fold. Considering the equation in the long channel approximation (1), the drive current is enhanced with HKMG through higher gate capacitance, resulting from higher permittivity of the high-k dielectric over SiO_2, along with a scaling of T_{inv} thanks to metal gate (poly depletion suppression).*

Technology approaches:

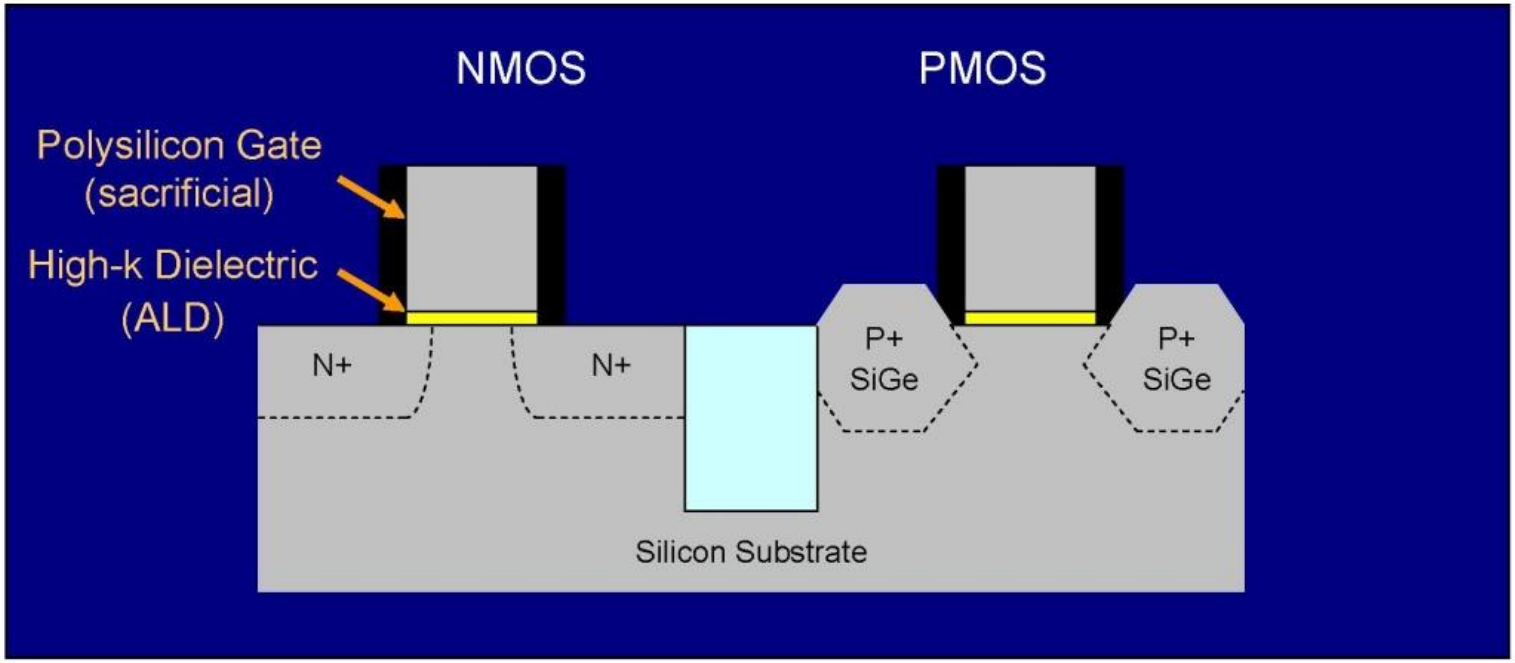
- Gate first (gate dielectric & electrode) – [MIPS = Metal Inserted Poly-Si]
- Gate last (electrode; gate dielectric can be first or last!) – [RMG = Replacement Metal Gate]

Q3/2 Describe the process flow of the process module “HKMG – gate last” by naming the five steps of its realization!

Step 1: Standard transistor formation until gate formation module, but with high-k gate dielectric (still Poly-Si as scarificial gate electrode)
Step 2: Deposit oxide (SiO2) layer and planize by using CMP
Step 3: Etch out the sacrifical Poly-Si
Step 4: Deposit NMOS and PMOS work function (WF) adjustment/metal layer seperately (→ one those needs to be patterned!)
Step 5: Deposit a low R metal layer (Al) as the gate electrode material & planarize the metal by CMP (damascene process)

HKMG: Gate Last Process Flow (1)

1

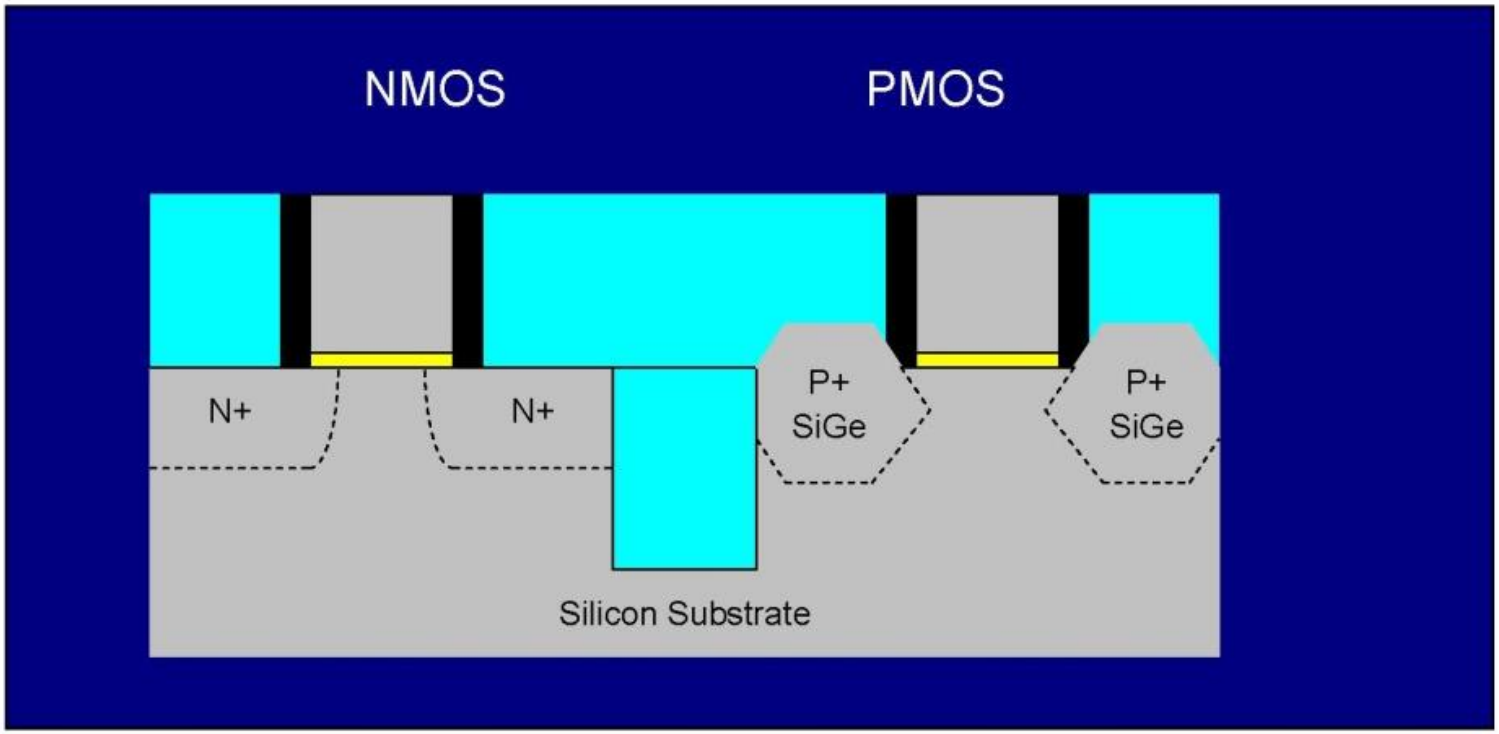


Standard transistor process through source-drain formation, but including atomic layer deposition high-k dielectric

Souce: Intel (www.intel.com/technology)

HKMG: Gate Last Process Flow (2)

2

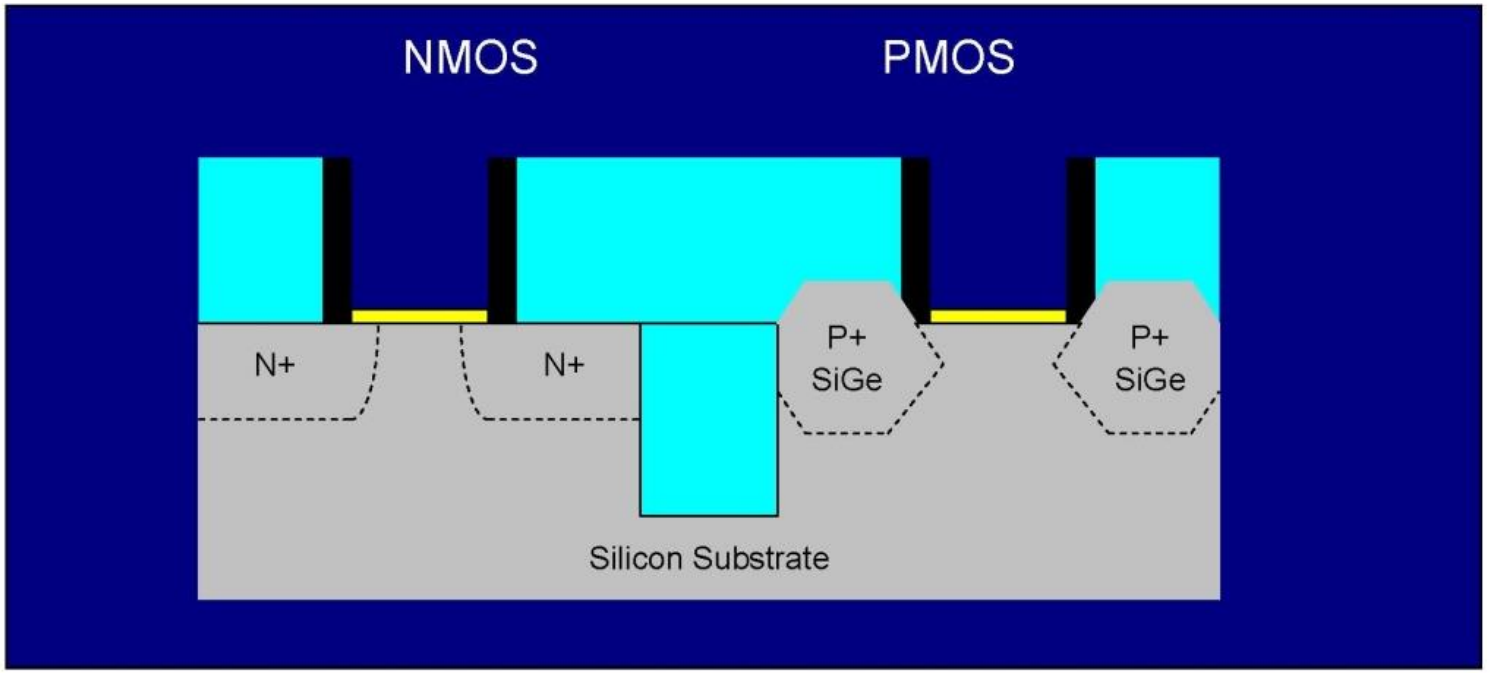


Deposit and planarize oxide layer

Souce: Intel (www.intel.com/technology)

HKMG: Gate Last Process Flow (3)

3

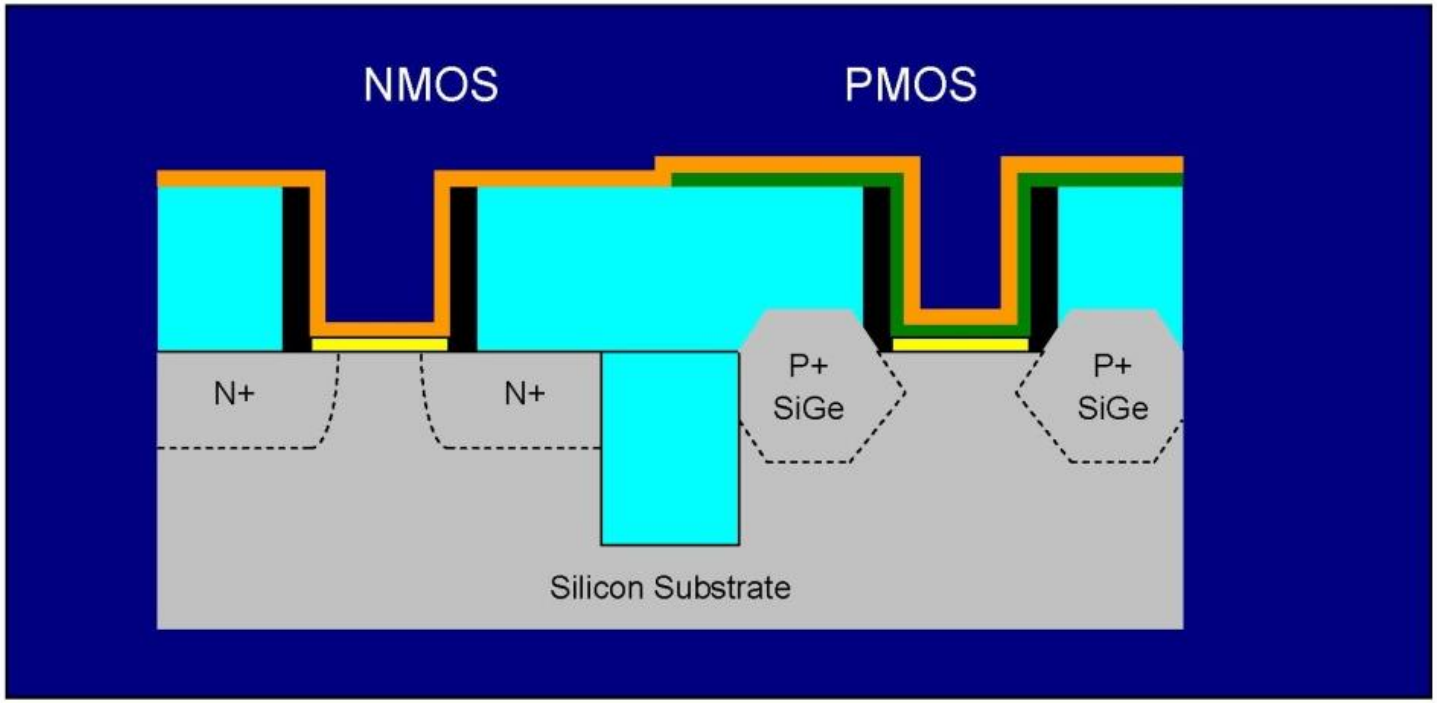


Etch out sacrificial polysilicon gate

Souce: Intel (www.intel.com/technology)

HKMG: Gate Last Process Flow (4)

4

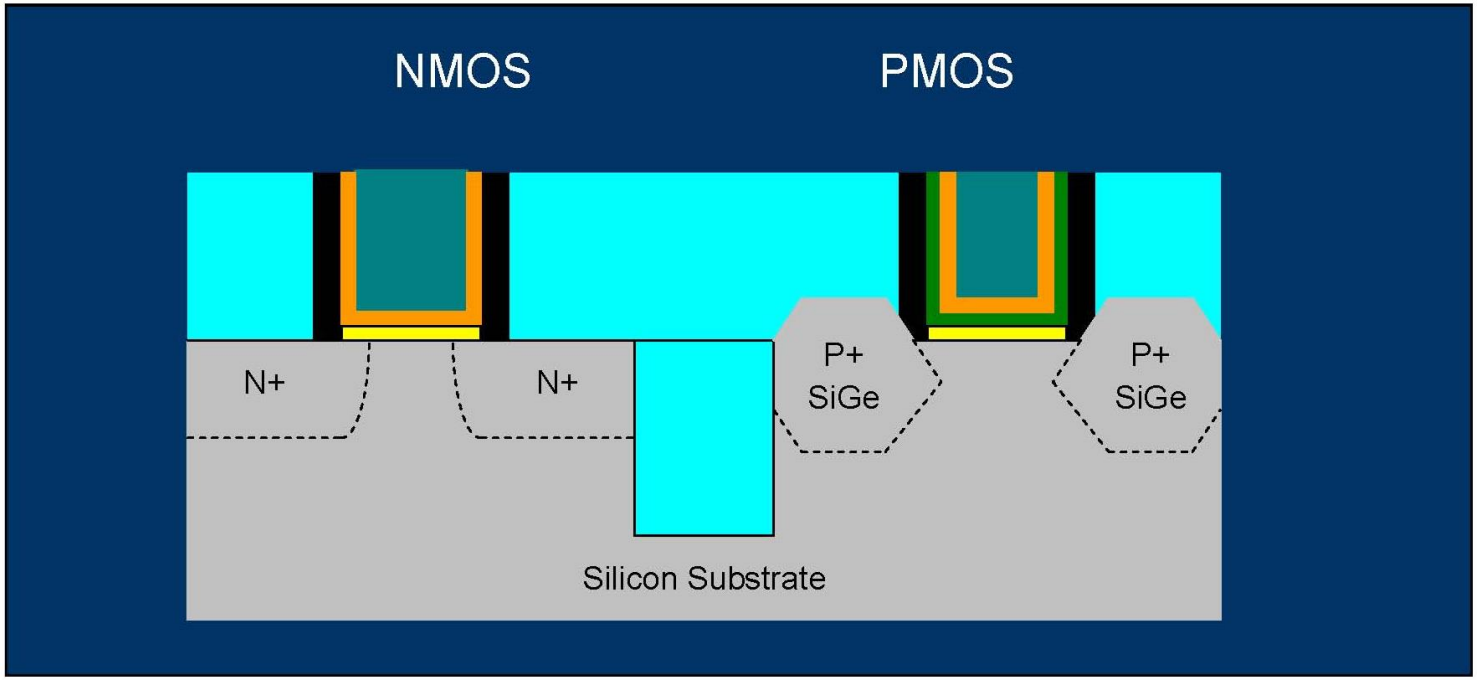


Deposit separate NMOS and PMOS WF metal layers

Souce: Intel (www.intel.com/technology)

HKMG: Gate Last Process Flow (5)

5



Deposit Al fill metal, planarize surface

Souce: Intel (www.intel.com/technology)

Q4 What are the benefits of silicon on insulator technology relative to conventional silicon bulk technology?

- Reduction of parasitic capacitances by isolating the transistor level form bulk-Si → reduction in power consumption
- Resistance to latch-up effect due to complete isolation of n and p well structures
- Combination of transistors on bulk-Si and SOI possible
- Possible: different Vt

Q4 What are the benefits of silicon on insulator technology relative to conventional silicon bulk technology?

Benefits of SOI technology relative to conventional silicon (bulk CMOS) [1]:

- *Lower parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance.*
- *Resistance to latchup due to complete isolation of the n- and p-well structures.*

Q5 What is the motivation to use local stress/strain generation / strained silicon in CMOS transistors?
Which type of strain do you need to enhance the NMOS and PMOS transistor, respectively?
Name two approaches for local stress generation in CMOS transistors!

1) Improve the charge carrier mobility in the transistor channel → improve performance (lower power consumption or to increasing switching speed)

2) NMOS: tensile strain / PMOS: compressive strain

3) SiGe/Si: strain templates; deposit stress liners on NMOS (tensile) and/or PMOS (compressive), dual stress liners (DSL) – PECVD SiN