Status: 06-2021

4 Integrated Circuit Technology

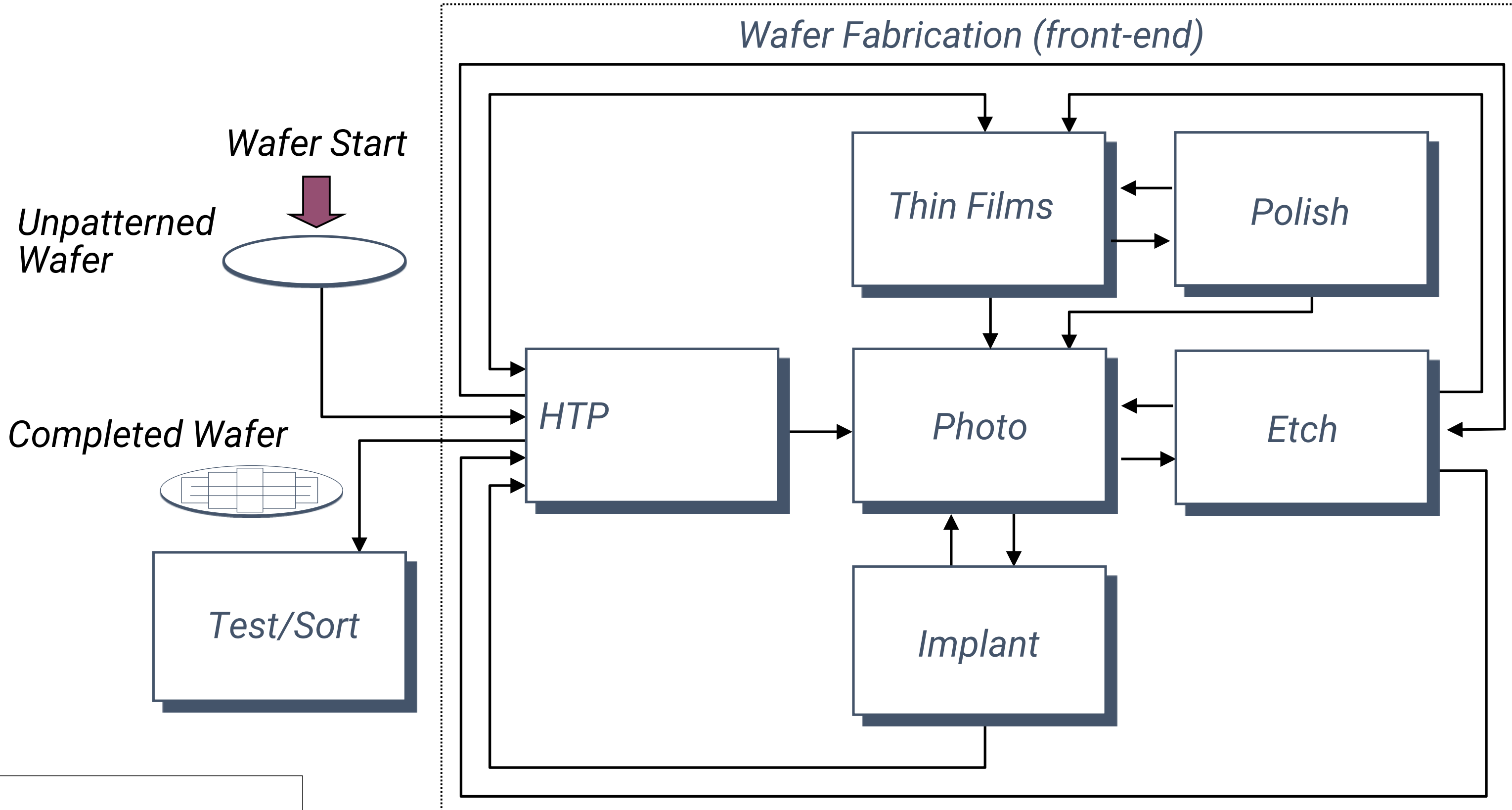
4.1 CMOS Manufacturing Process *(0.25 µm and below)*

Sources:
- *Semiconductor Manufacturing Technology, Michael Quirk, Julian Serda, Prentice Hall, 2001*
- *www.usna.edu/EE/ee452/LectureNotes/02-CMOS_Process_Steps/09_Process_Flow_Overview.ppt*
- *www.lpm.u-nancy.fr/webperso/nanomag/download/Cours%20Micro-Nano/Techno%20CMOS_Chihiwu/ch13%20rev3.ppt*

CMOS Technology

- *First proposed in the 1960s. Was not seriously considered until the severe limitations in power density and dissipation occurred in NMOS circuits*
- *Now the dominant technology in IC manufacturing*
- *Employs both pMOS and nMOS transistors to form logic elements*
- *The advantage of CMOS is that its logic elements draw significant current only during the transition from one state to another and very little current between transitions - hence power is conserved.*
- *In the case of an inverter, in either logic state one of the transistors is off. Since the transistors are in series, nearly no current flows.*

Model of Typical Wafer Flow in a Sub-Micron CMOS IC Fab



HTP:
High Temperature Processes: Diffusion, Oxidation, Anneal, Epi

6 major production areas

6 ... 8 weeks involve up to 400 process steps

CMOS Manufacturing Steps (0.25 µm and below)

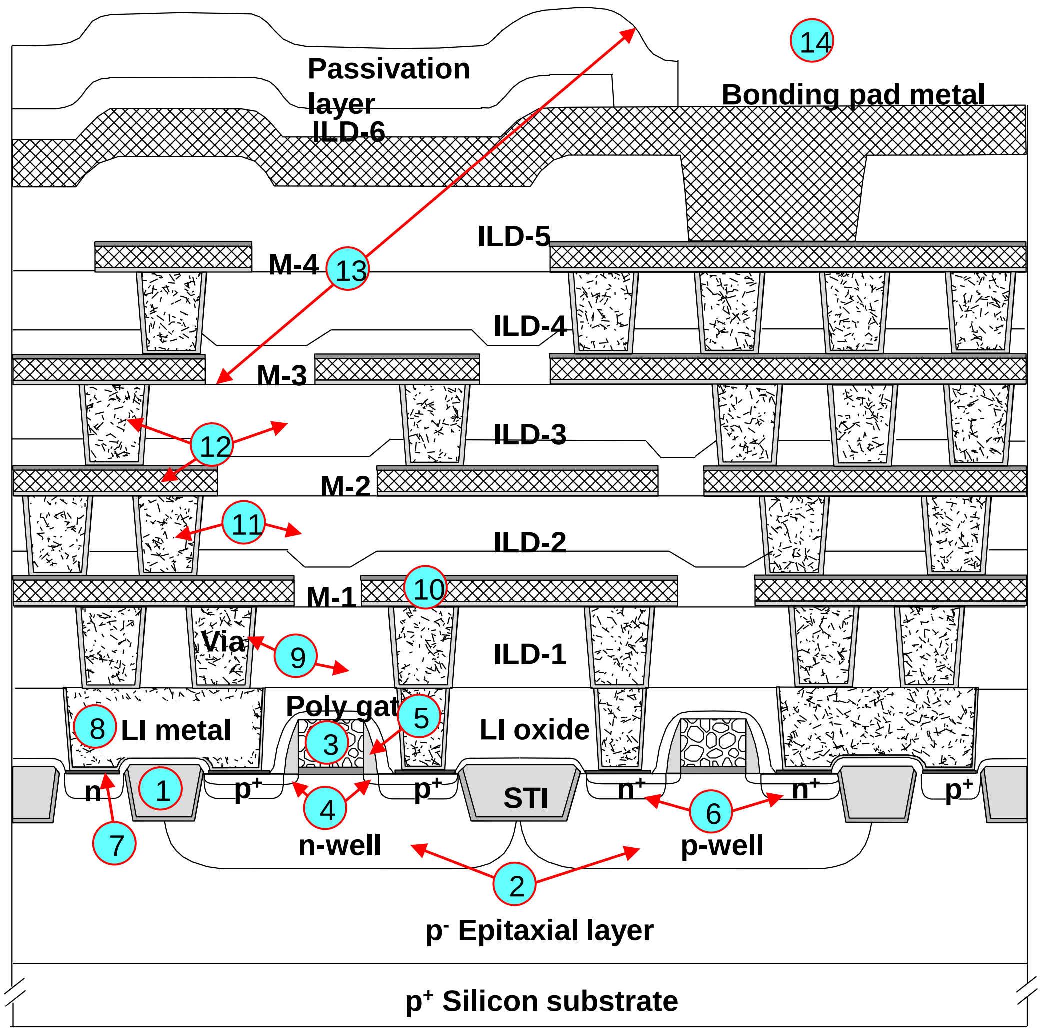
Process Modules

1. *Shallow Trench Isolation (STI)*
2. *Twin-well Implants*
3. *Gate Structure*
4. *Lightly Doped Drain Implants*
5. *Sidewall Spacer*
6. *Source/Drain Implants*
7. *Contact Formation*
8. *Local Interconnect*

FEOL

9. *Via-1 / Metal 1 Formation*
10. *Via-2 / Metal 2 Formation*
11. *Via-3 / Metal 3 Formation*
12. *Via-4 / Metal 4 Formation*
13. *Bond Pad Metal & Passivation*
14. *Parametric Testing*

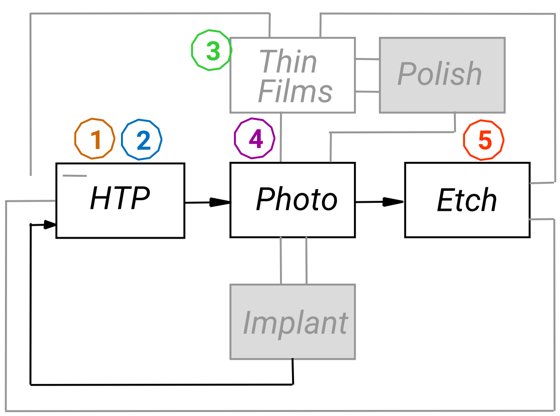
BEOL



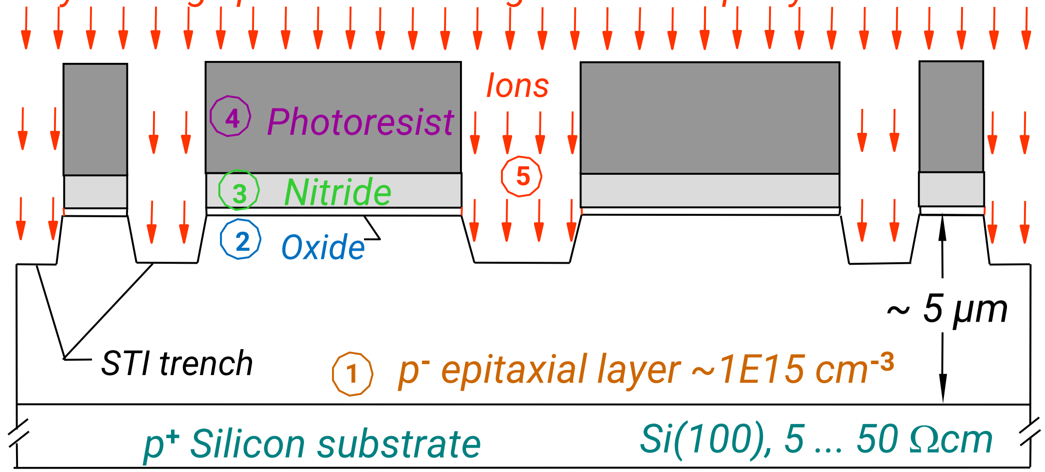
Full 0.18 µm CMOS Cross Section

STI Trench Etch

- *STI = Shallow Trench Isolation (replaces LOCOS at 0.25 µm and below, provides planar surface, no "bird's beak")*
- **Silicon substrate** *is p$^+$, in order to create a conductive ground plane which establishes the ground zero reference voltage across the chip.*
- *A thin* **p$^-$ layer** *① is epitaxially grown on top to reduce capacitance and also to prevent cross-talk latch-up.*
- *A thin* **SiO_2 layer** *(pad oxide, 15 nm) ② is thermally grown (dry O_2) to protect active areas from excessive damage during ion implantation and to control the depth distribution of dopants.*
- *Upon the SiO_2, a layer of Si_3N_4 ③ is deposited by LPCVD. Typically ammonia and dichlorosilane are introduced at medium temperature (750°C) and a layer about 150 nm is formed. Si_3N_4 is a high quality masking material in case the photoresist fails during trench etch. The trench etch step is highly energetic, and the Si_3N_4 layer protects the areas where the devices will be formed. Furthermore, the Si_3N_4 layer is used later as a CMP stop.*
- *Photoresist is deposited and patterned ④ (1st mask). Then plasma etching (5) uses high intensity RF to ionize either fluorine or chlorine based gases. The F or Cl ions react with the exposed Si_3N_4, SiO_2 and silicon, forming gaseous reaction products.*

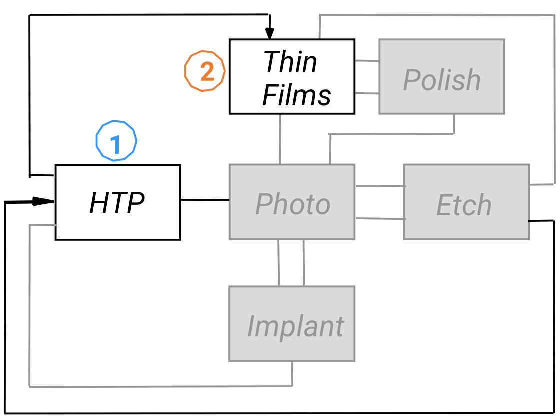


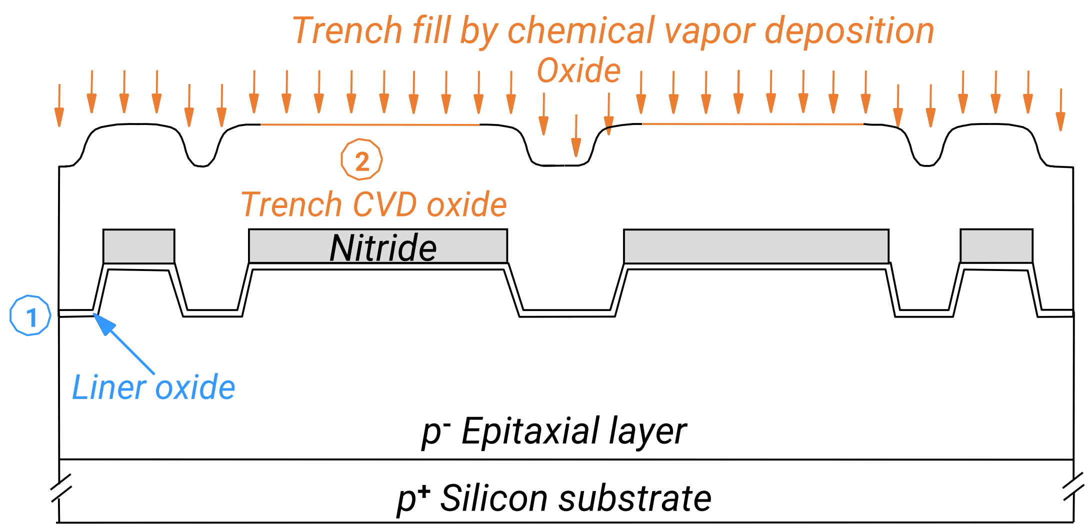
Dry etching opens isolation regions in the epi layer.



STI Oxide Fill

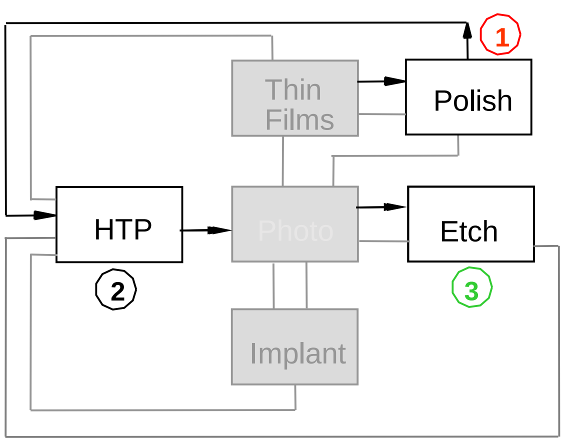
- *Formation of about 15 nm liner oxide ① in the trench by dry thermal oxidation at medium temperature (750 °C) to improve the interface between silicon and trench CVD oxide.*
- *Next a thick layer of CVD oxide, is deposited ②. This layer will act primarily as a fill to the isolation trenches and is similar to the "Field Oxide" in former LOCOS processes.*

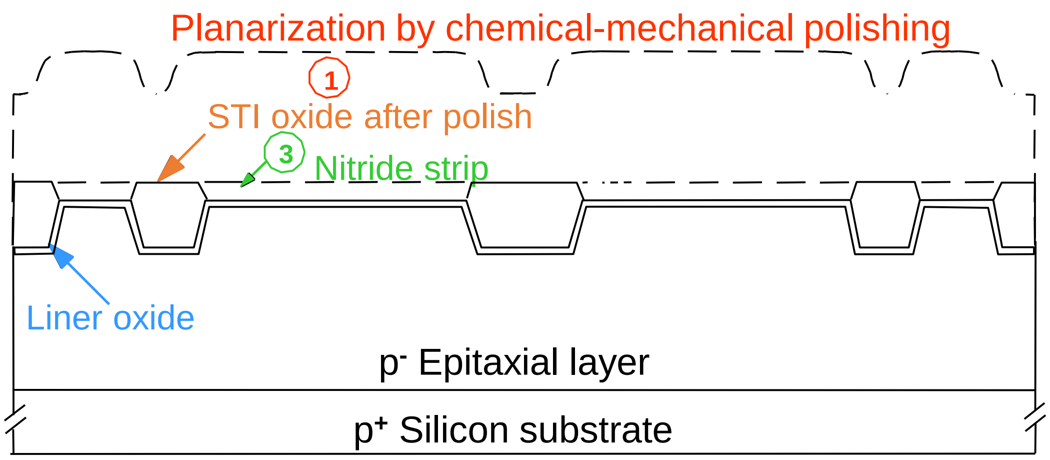




STI Formation

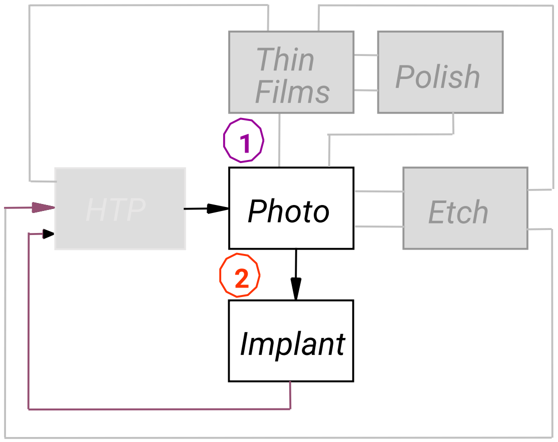
- *Trench oxide polish (CMP) ①. Nitride acts as the CMP stop layer*
- *Densification of STI oxide at 900 °C ②*
- *Nitride strip ③ in hot (150 to 200 °C) phosphoric acid (H_3PO_4) solution (high selectivity to silicon oxide)*

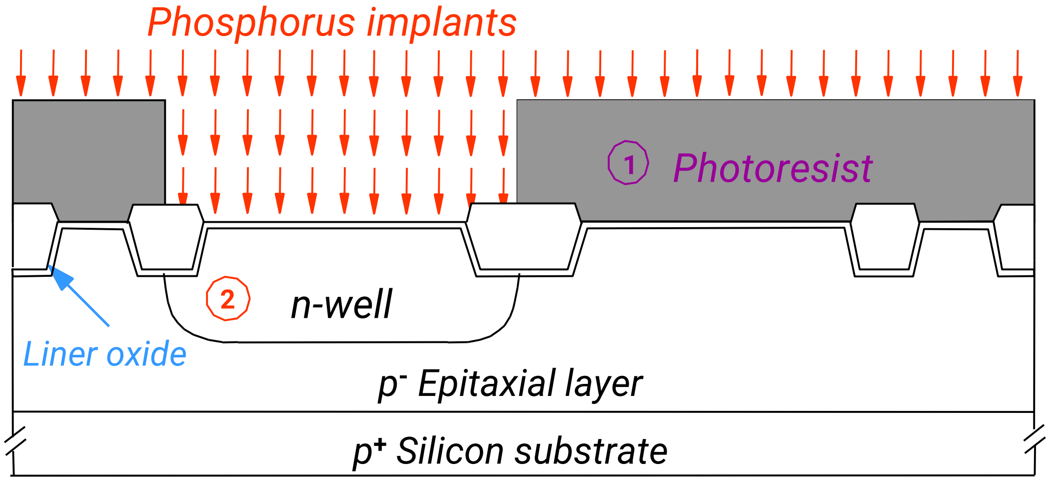




n-well Formation

- **Photoresist** ① *is used as a mask for the ion implantation (2nd mask). The ions do not have enough energy to penetrate through the photoresist. Except for the holes in the photoresist, these implanted ions stick in the photoresist. When this layer is removed the implanted ions in the photoresist are removed also.*
- *The thin layer of oxide is left over in the n-well during implantation. This is a "sacrificial oxide", usually only 15 nm thick, which prevents contamination of the region which will later-on form the gate oxide. Furthermore, the oxide acts as scattering oxide to minimize/prevent the channeling effect during ion implantation.*
- *Chained P^- implants ② :*
  - *for retrograde n-well (700 - 850 keV, ~1E13 cm^{-2})*
  - *for punch through suppression and channel stop*
  - *for V_{Tp} adjustment*
- *Resist stripping*





Threshold Voltage Adjustment

$$V_T = V_{FB} + 2\phi_F + \gamma \sqrt{2\phi_F + V_{SB}}$$

n channel MOSFET

$$\gamma = \left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\sqrt{2\varepsilon_{Si} q N}$$

$$\phi_F = \frac{kT}{q} \ln \frac{N}{n_i}$$

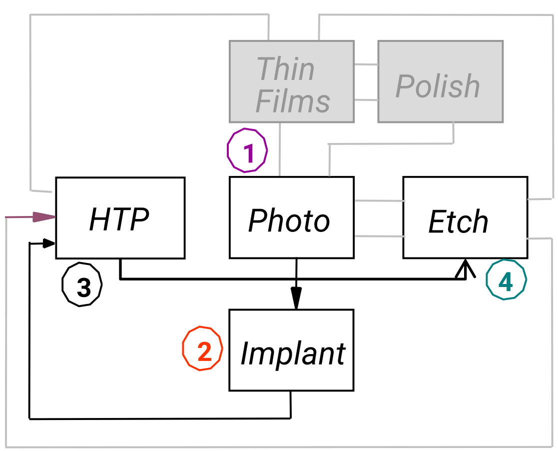
V_{SB}	*substrate bias voltage*
V_{FB}	*flat band voltage*
ϕ_F	*surface potential (diffusion potential of Si)*
γ	*body effect parameter*
N	*dopant concentration in the substrate*
t_{ox}	*oxide thickness*
ε	*dielectric constant*

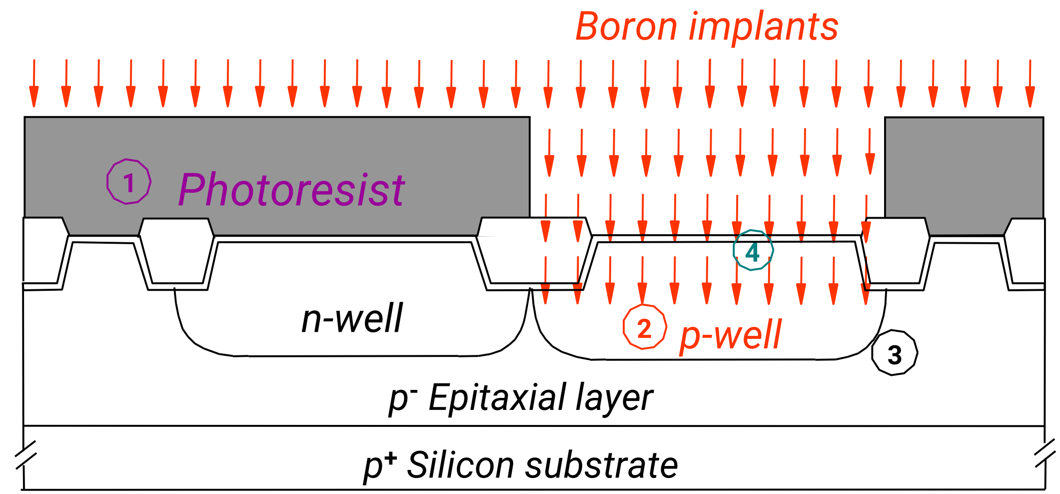
V_T depends on V_{SB} and a constant γ which depends on substrate doping N

Increasing V_{SB} causes the channel to be depleted of charge carriers and thus the threshold voltage is raised

p-well Formation

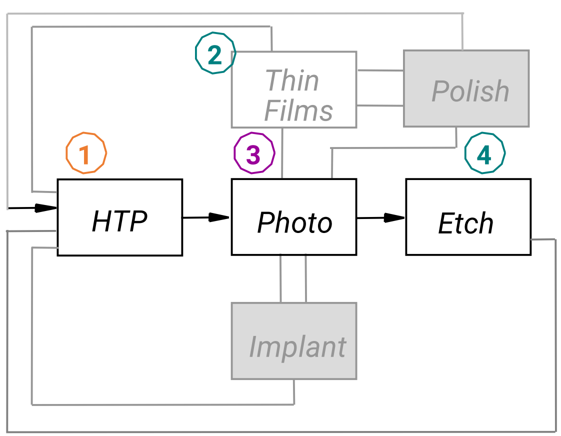
- *A new photoresist pattern ① is used for the p-well ion implantation mask (3rd mask).*
- *The thin layer of oxide is left over in the p-well during implantation.*
- *Chained B^+ implants ②:*
  - *for retrograde p-well (350 - 500 keV, ~1E13 cm^{-2})*
  - *for punch through suppression and channel stop (100 keV, ~4E12 cm^{-2})*
  - *for V_{Tn} adjustment (30 keV, ~5E12 cm^{-2})*
- *Resist stripping*
- *Annealing to repair damage and to drive the dopants deeper (900°C, 30 min or 1100°C, 30 s RTP) ③.*
- *Oxide removal ④*
- *Surface Cleaning (wet clean to remove any contaminants before gate oxide growth)*

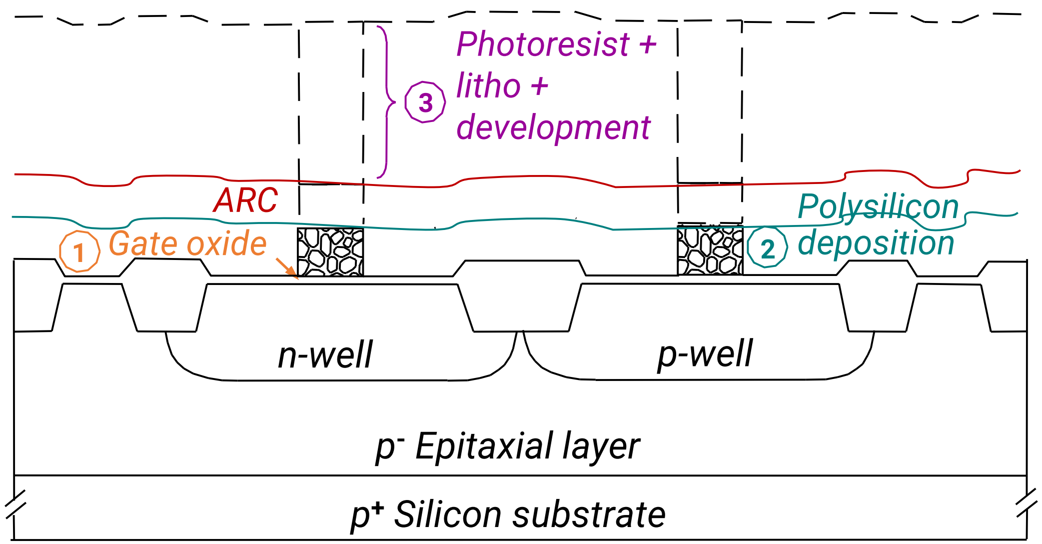




Poly Gate Structure

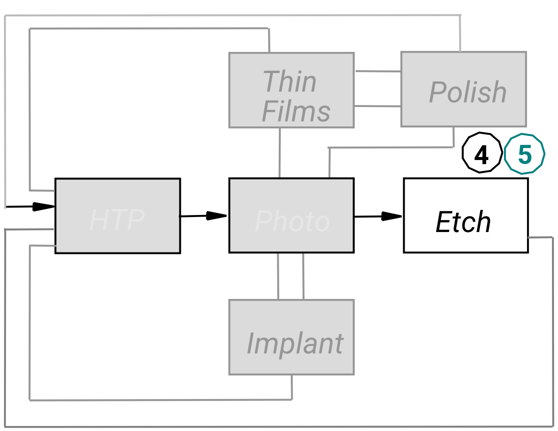
- *Formation of ~2.5 nm highest quality SiO_2 (gate oxide)① by dry thermal oxidation at 1000 °C.*
- *Polysilicon (~300 nm) is then deposited on the wafer by PECVD using silane (SiH_4) ②. Since the temperature is moderate (< 500 °C) the silicon forms in poly-crystalline grains.*
- *Deposition of antireflective coating (ARC)*
- *Photoresist is applied and the most critical litho is done incl. resist developement ③ (4th mask, defines poly gates and local poly interconnects). The gate width is the smallest dimension which will be required.*

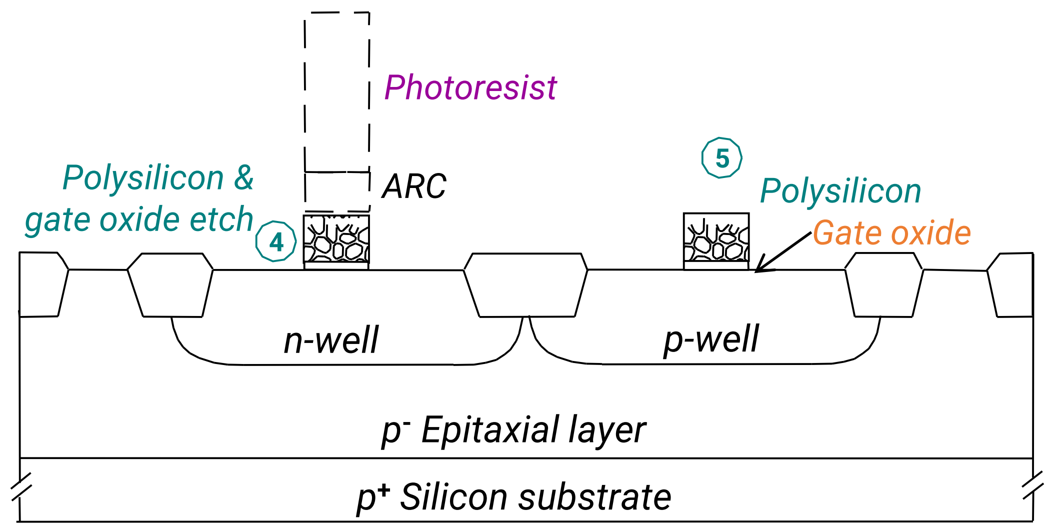




Poly Gate Structure

- *The ARC, polysilicon and the gate oxide is then dry etched (anisotropic etching) ④.*
- *Photoresist is stripped* ⑤
- *ARC is removed by selective wet etch* ⑤

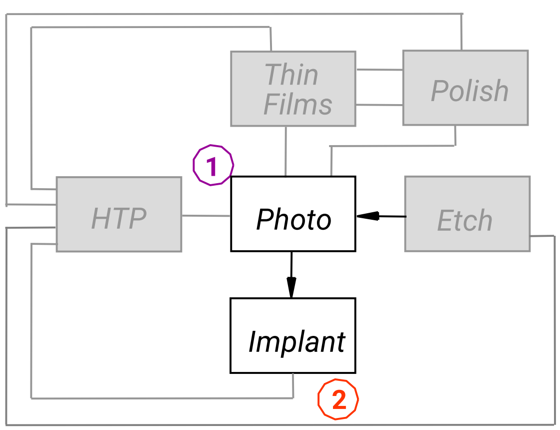


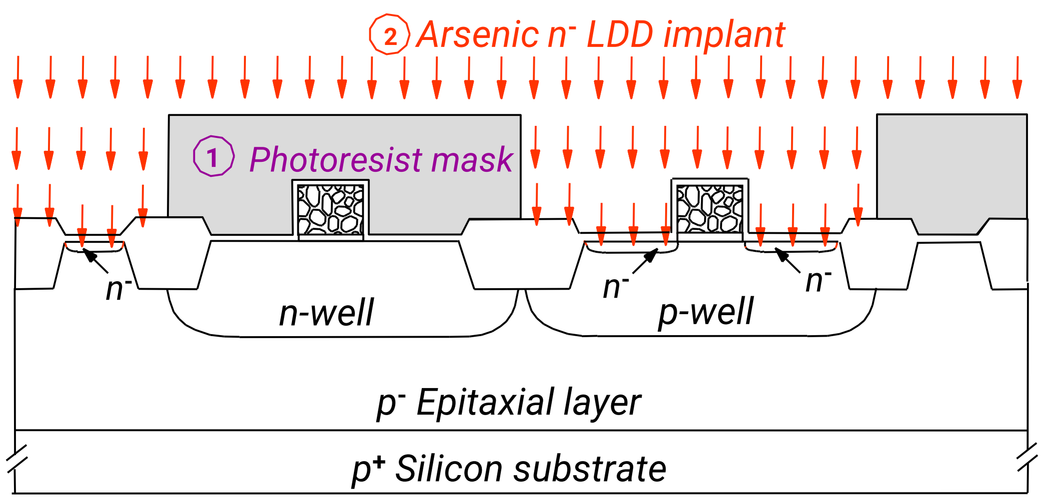


n^- LDD Implant

The concept of Lightly Doped Drain (LDD) is to prevent "punch-through". Because the gate is so narrow, the electric fields of the S/G and G/D junctions are so close that energetic thermal electrons might just jump the gap (S/D leakage). By reducing the doping of the drain (whose field controls the device current) this reduces the number of available electrons with high velocity. The source and drain contacts are typically made using an implantation of arsenic ions. Large mass implant (As instead of P) and surface amorphization helps to maintain a shallow junction. Use of Self-Aligned Gate to form Source/Drain.

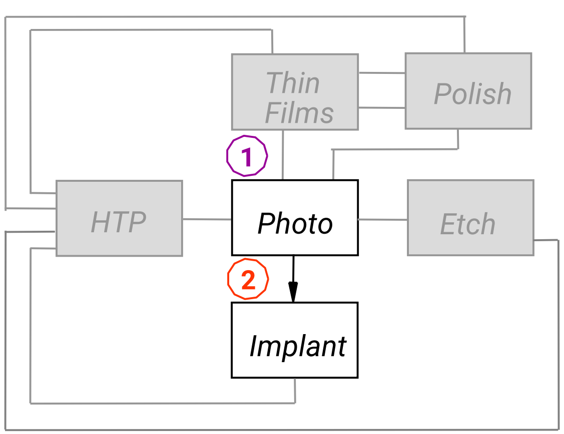
- *Screening/scattering oxide deposition (CVD)*
- *5th mask ①, almost identical to that creating the original p-well (3rd mask)*
- *As implant (3E13 - 3E14 cm^{-2}) ②*

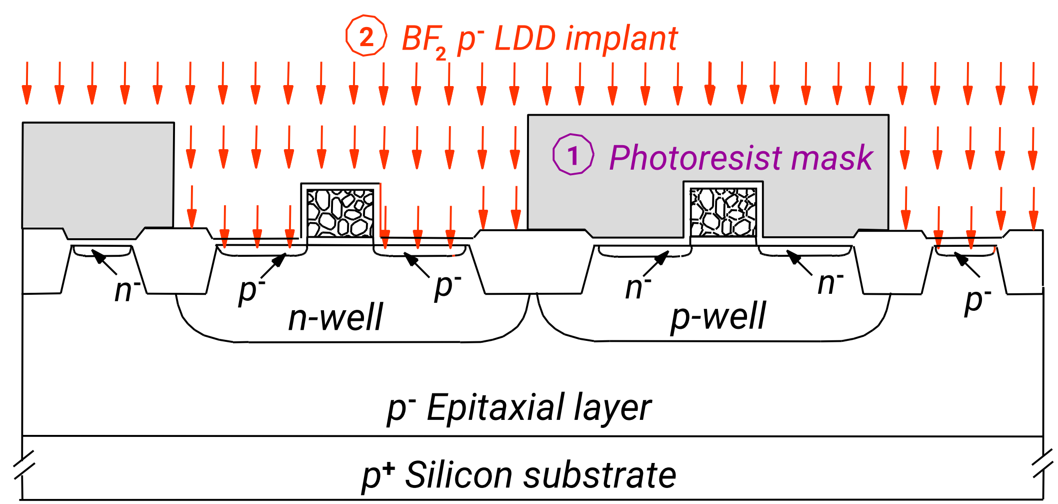




p^- LDD Implant

- Photoresist ① is deposited and patterned (6th mask).
- BF_2 is implanted ($3E13 - 3E14\ cm^{-2}$) for the Source and Drain of the pMOS cell ②. Large mass implant (BF_2 instead of B) and surface amorphization helps to to maintain a shallow junction. The implanted F will diffuse out of the wafer at the next heat treatment since silicon crystal is inhospitable to the incorporation of F atoms.

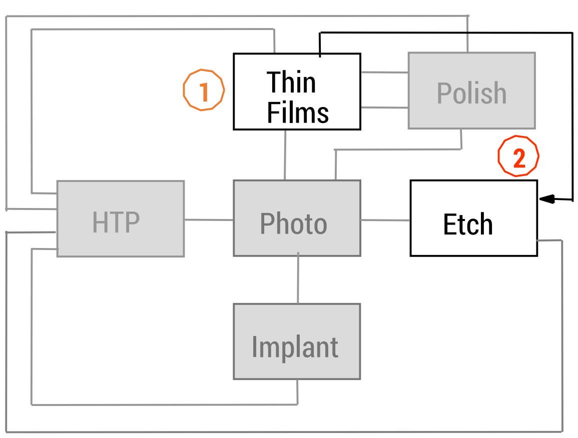


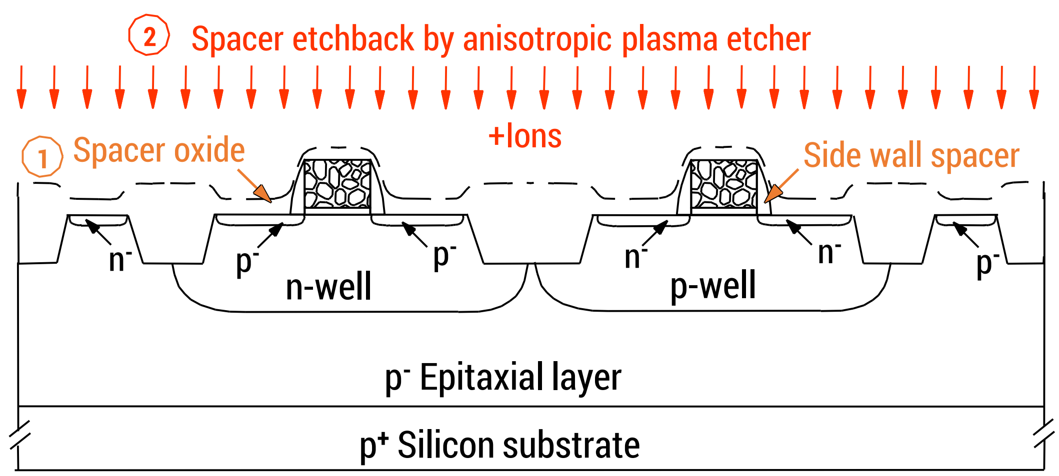


Side Wall Spacer Formation

Polysilicon will be the electrical contact for the Gate. It must be protected from the metallic contacts to the Source and Drain, so a thin "side-wall spacer oxide" (or nitride) is deposited on the side of the Gate to obtain electrical isolation. This spacer will also keep the next implantation (which completes the construction of the source and drain) away from the edge of the Gate. This will also reduce punch-through.

- *A thin SiO_2 layer ① (100 nm) is deposited using CVD. Since the CVD is conformal, the oxide will coat both horizontal and vertical surfaces equally.*
- *Without using photoresist, this oxide is immediately removed using a directional anisotropic etch ②. The etch will remove the flat (horizontal) oxide and leave the vertical SiO_2 on the sides of the Gate. This process omits a lithography step.*

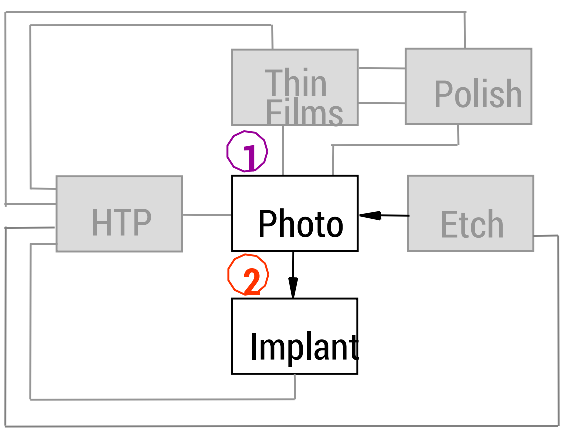


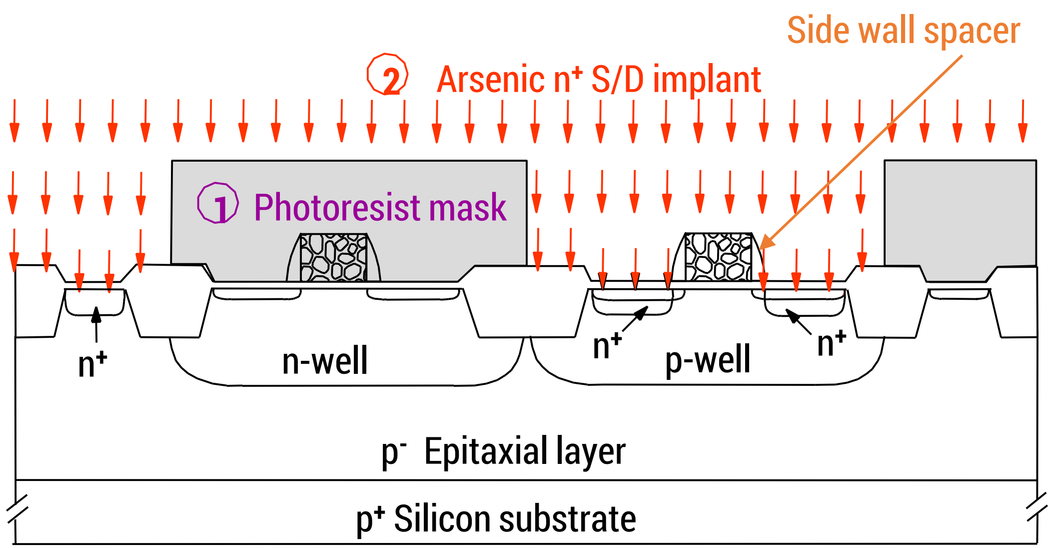


n^+ Source/Drain Implant

A second implant is made into the Source and Drain, and also into the Isolation Trench. The S/D implant is slightly narrower than the previous LDD implant because the Gate now includes the "gate side-wall spacer" which was deposited in the previous step. Hence the Source and Drain will be lightly doped next to the Gate, reducing punch-through, and more heavily doped where the metallic contacts will connect. This implant does double-duty by also forming a heavily doped junction in the isolation well, reducing any communication between this CMOS cell and the adjacent one.

- *Photoresist is deposited, exposed, and developed (7th mask) ①.*
- *A high dose arsenic implant (1 - 5E15 cm^{-2}) is made ② simultaneously doping the poly gate.*
- *Resist stripping*

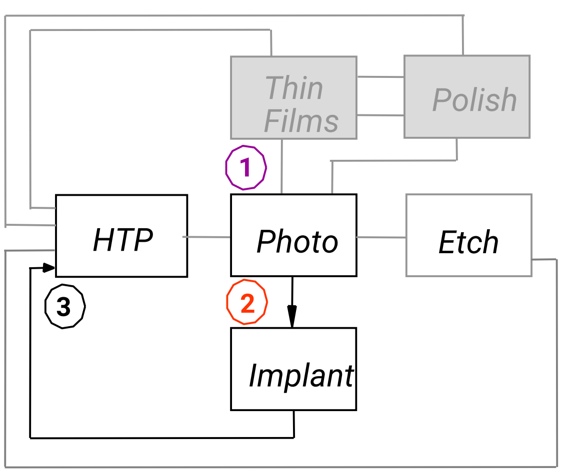


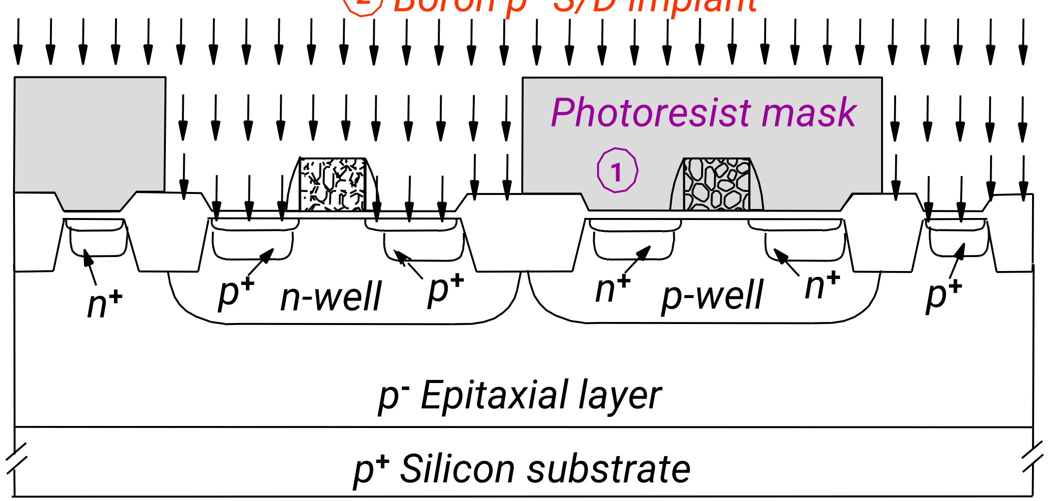


p^+ Source/Drain Implant

- *The pMOS device is patterned (8th mask) ①*
- *and implanted with boron ② (1 - 5E15 cm^{-2})*
- *Resist stripping*
- *After this step, the damage to the wafer from the series of implantation must be annealed ③. This process may be complex, with multiple stages of anneal such as 550 °C for 30 min + 750 °C for 10 min + 1000 °C for 20 min. These multiple anneals are necessary to eliminate the intermediate defect clusters that form as the silicon recrystallizes and places the dopant atoms into substitutional sites of the Si lattice.*

RTA can be used to prevent dopant spreading and to control diffusion of dopants.

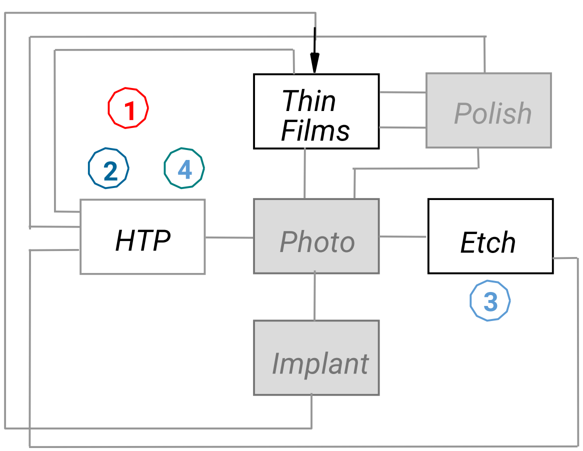


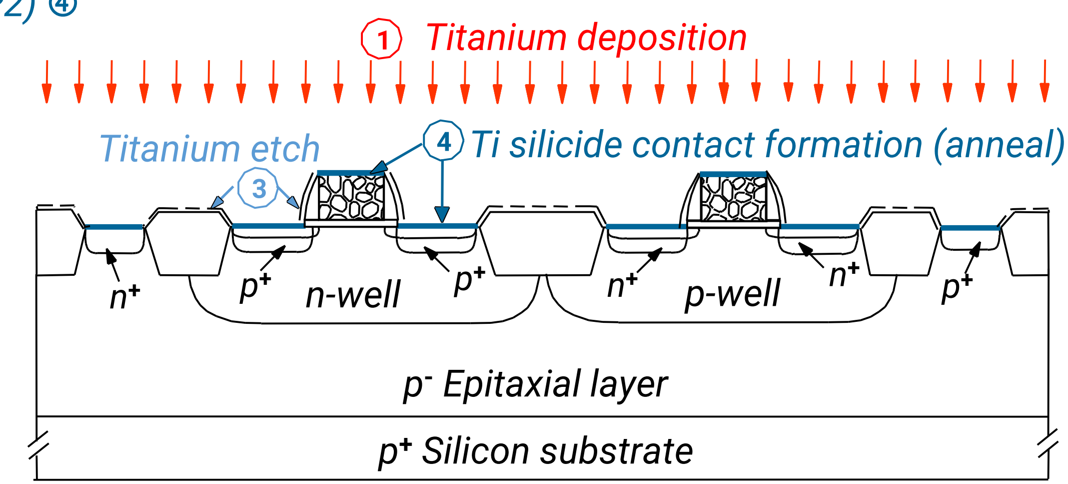


Contact Formation

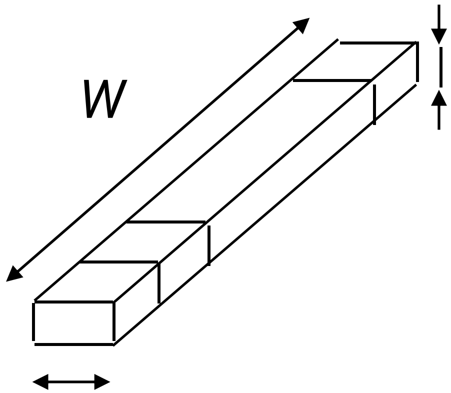
Metal contacts and highly conductive gate lines are formed by using the fact that many metals (e.g. Ti, Co, Pt) will not react with SiO_2, but will easily form silicides with bare silicon. Here Ti metal is used. During a moderate heat treatment, the Ti/Si interface undergoes solid-phase reactions forming $TiSi_2$. This contact is a perfect ohmic contact with the silicon substrate (no intrinsic fields are present). The Ti which is in contact with the SiO_2, does not react. A a selective metal wet etch will remove this Ti. The already reacted and formed $TiSi_2$ in the contact areas and on poly lines will not be etched This self-aligned silicide process omits a lithography step (self-aligned silicide (salicide) formation)

- *Removal of oxide from S/D and poly gate*
- *Sputtering of Ti metal ①*
- *Anneal to form $TiSi_2$ (RTP1) on Si areas (Single and poly crystalline, S/D/G…) ②*
- *Chemical wet etching to remove unreacted Ti from SiO_2 areas (STI, spacer), leaving $TiSi_2$ on Si areas (selective wet etching) ③*
- *Anneal to form low resistivity $TiSi_2$ (RTP2) ④*





Why do we use silicides ?

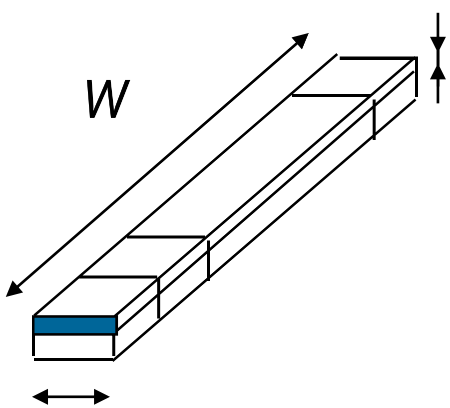


- *Doped poly-Si*

ρ = 4500 μΩcm

ρ/H = 300 Ω/square

R = ρ/H x W/L



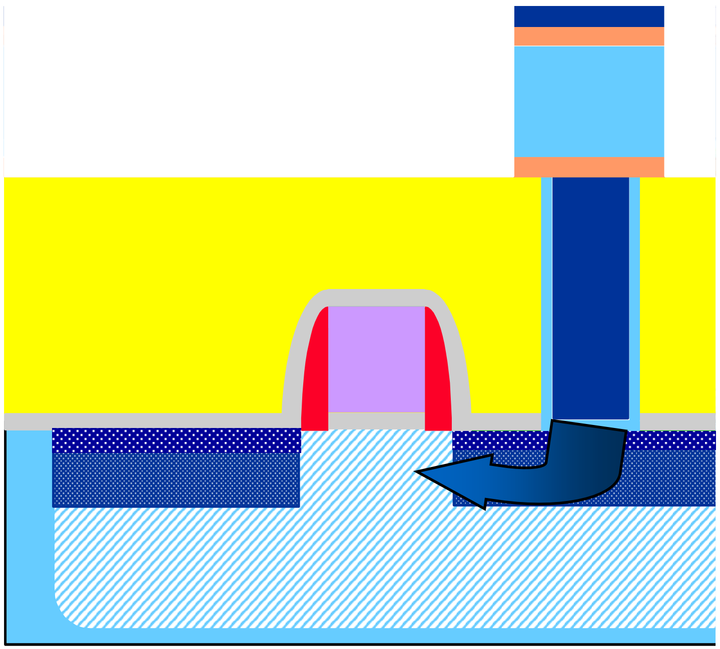
- *Silicided poly-Si*

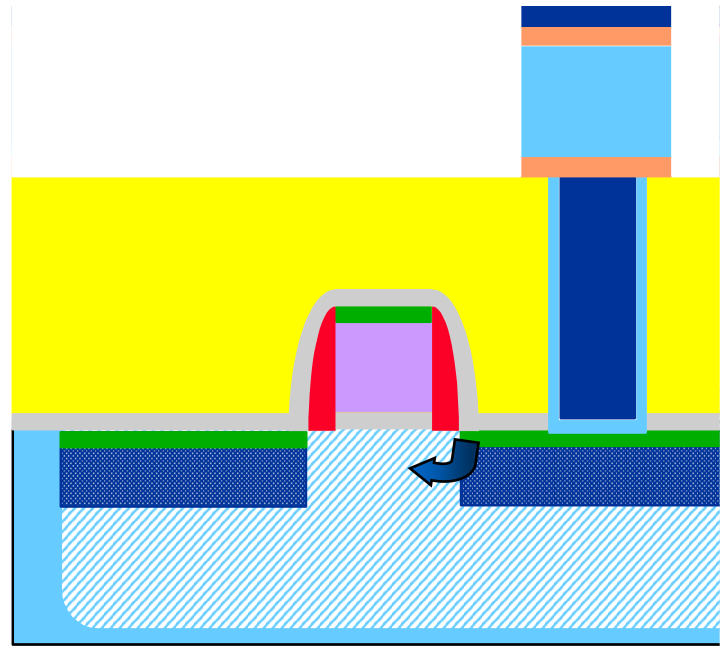
ρ = 18 μΩcm

ρ/H = 6 Ω/square

R = ρ/H x W/L

Why do we use silicides ?

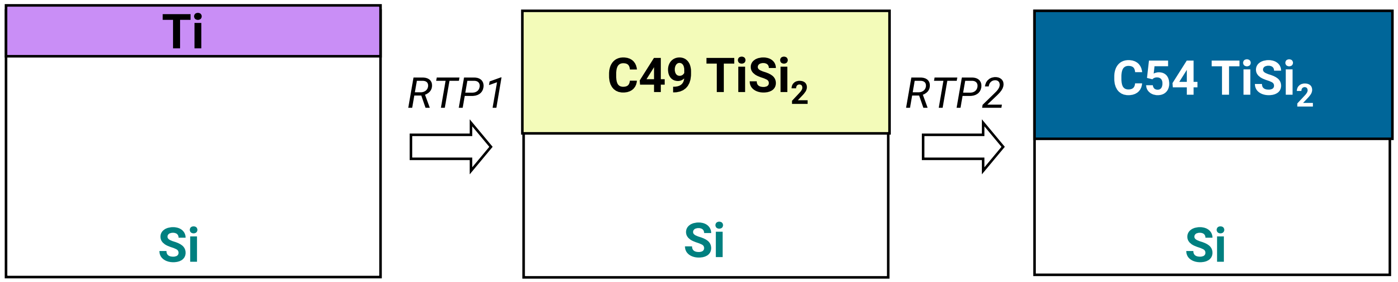




$R_{contact}$: $\rho = 10^{-5} - 10^{-6}\ \Omega\ cm^2$ | $\rho \sim 10^{-7}\ \Omega\ cm^2$

R_{series}: $R_{sheet} = 100\ \Omega$ /square | $R_{sheet} = 6\ \Omega$ /square

$TiSi_2$



Ti/Si reactions: **diffusion control (Si as diffusing species)** **nucleation control structural change**

Anneal	*Phase*	*Resistivity:*
RTP1: 700 - 750 °C	*C49 phase*	*80 - 120 $\mu\Omega$ cm*
RTP2: 800 - 900 °C	*C54 phase*	*20 $\mu\Omega$ cm*

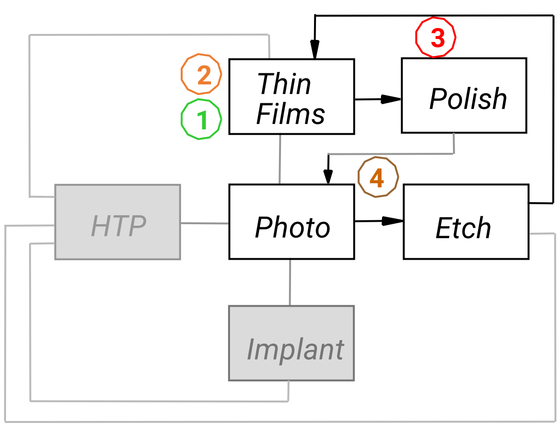
Si consumption ~ silicide thickness

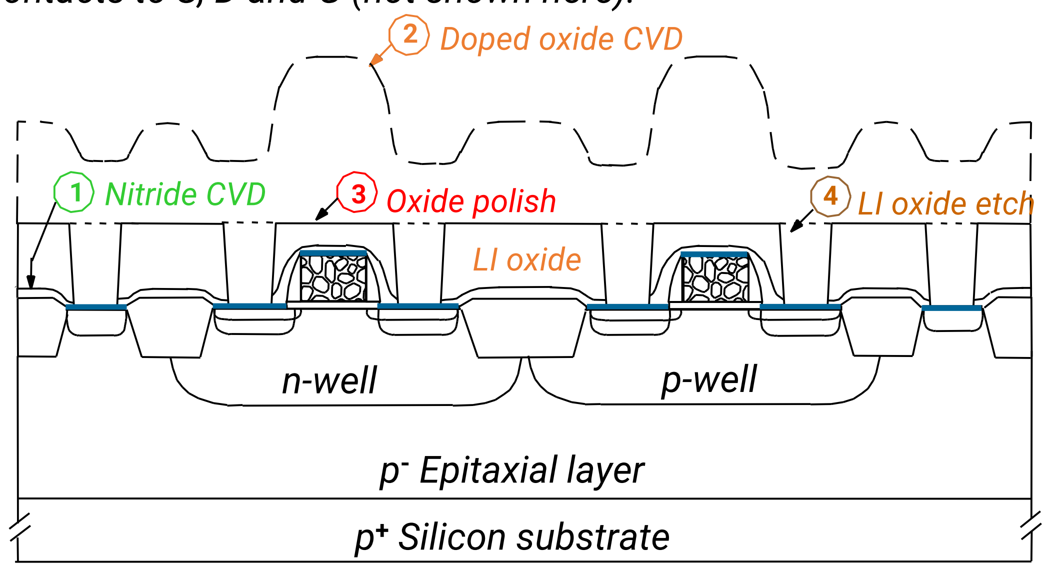
Selective wet etching: NH_4OH / H_2O_2 / H_2O

Local Interconnect (LI) Dielectric Formation

Following steps for initial oxide coating and patterning:

- *Thin layer of Si_3N_4 is deposited (CVD, 100 nm), to protect all active components from contamination and as etch stop layer for contact etch (G vs. S/D with different depth and sidewall spacer protection) ①.*
- *Thick SiO_2 is deposited (CVD, 1000 nm, ②). This oxide is usually doped with boron or phosphorus (BSG, PSG, BPSG) to obtain better dielectric qualities and passivate the Si (dangling bonds).*
- *CMP planarizes the SiO_2 layer, until it is a smooth layer of about 800 nm above silicon, ③.*
- *"Trenches/Holes" ④ are patterned into the SiO_2 /Si_3N_4 layers using lithography (9th mask) and directional plasma etching to open the contacts to S, D and G (not shown here).*

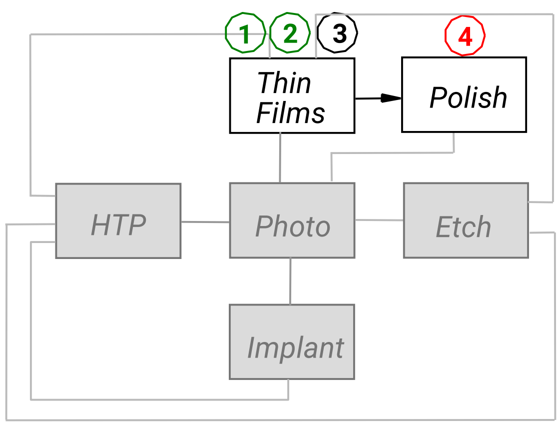


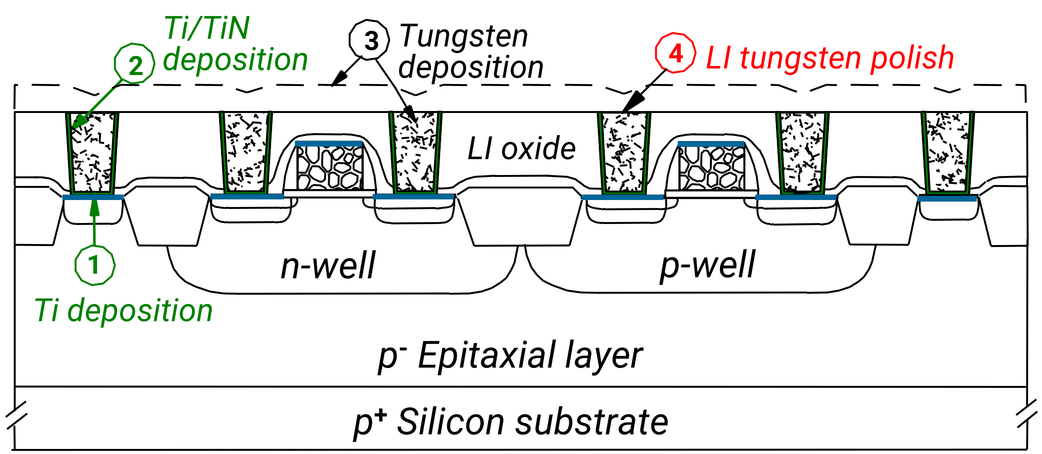


Local Interconnect (LI) Metal Formation

- *A few nm thick Ti is deposited (IPVD, CVD) ①, acting as adhesion layer and to reduce surface oxide.*
- *A thin layer of TiN is immediately applied (IPVD, CVD, ~20 nm, ②) acting as a diffusion barrier to prevent the next metal from chemically interacting with the active components. The film should be thin enough to add only little electrical resistance.*
- *Tungsten is deposited (CVD using WF_6) to fill all trenches and holes ③.*
- *A CMP polish is finally applied to remove the access metal (W/TiN/Ti) and planarize the surface ④.*
- *Thus "W plugs" were formed to connect to upper metal lines.*

This concludes the Front End of Line (FEOL) wafer processing.





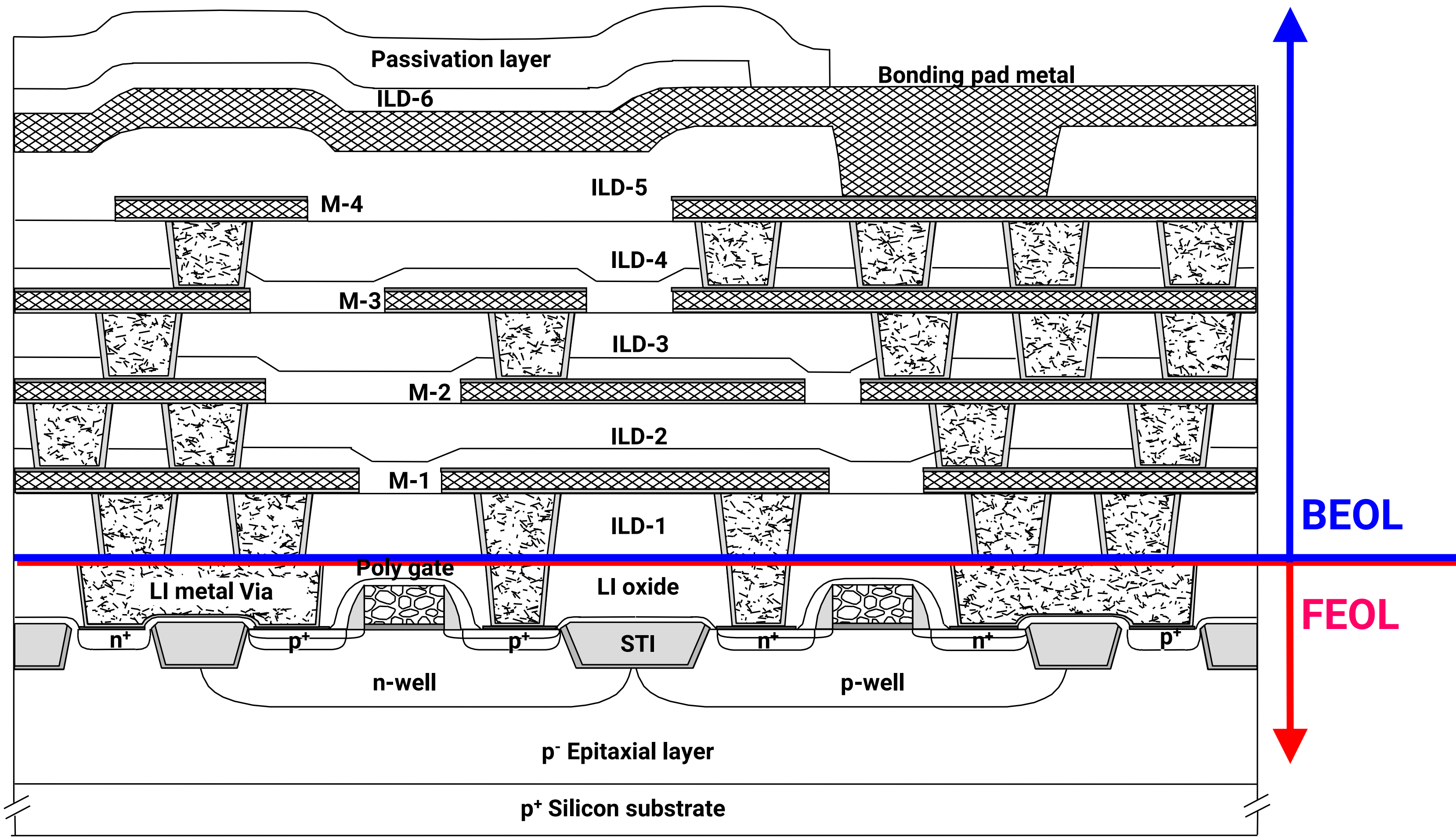
Back End of Line (BEOL)

The "Back End of Line" adds all the interconnections between modules to make the final integrated circuit.

Each layer of interconnections is separated by a dielectric layer with holes (vias) which reach down to the IC active components.

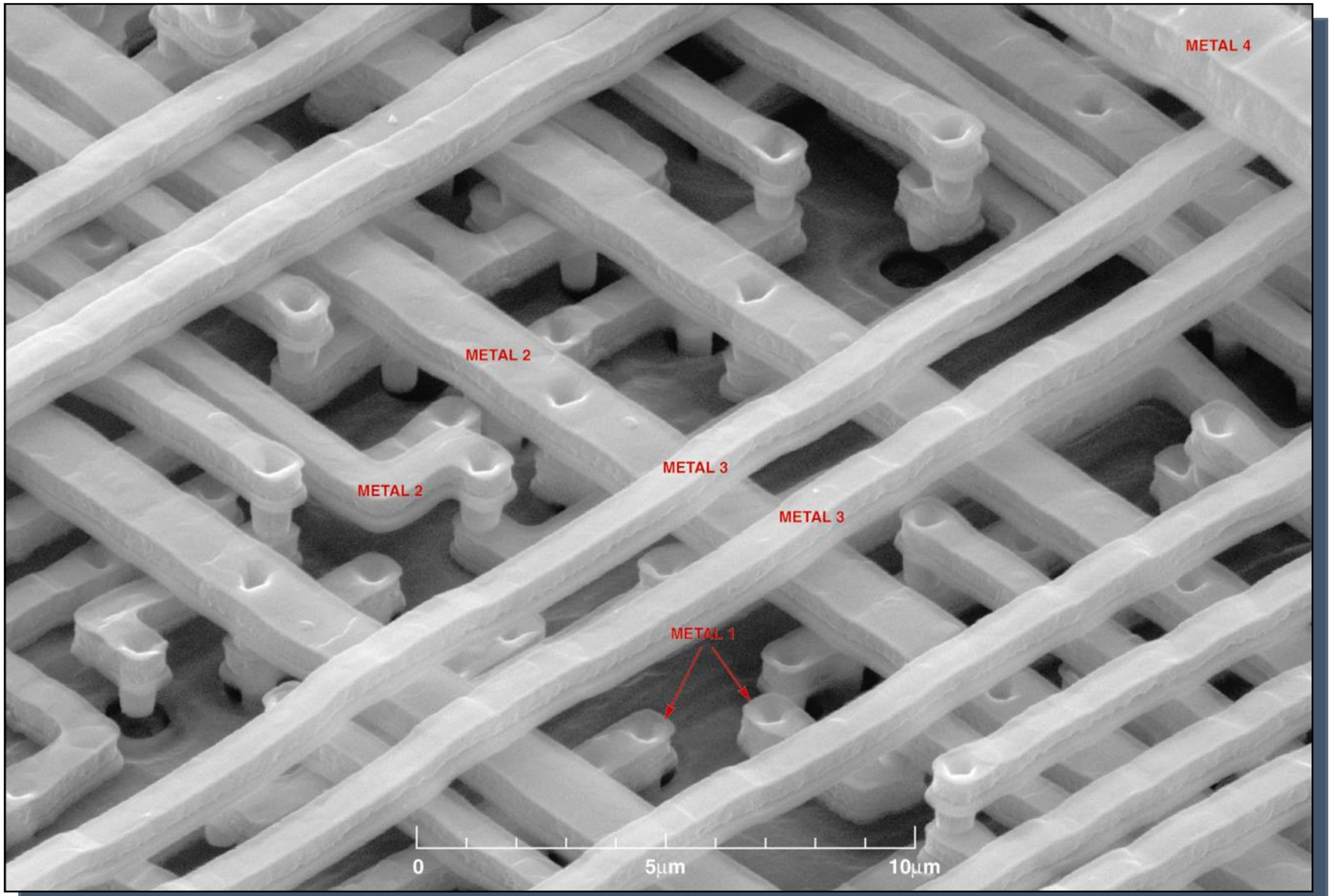
Each layer is planarized before the next the next layer is deposited.

Normally, the layers alternate with horizontal and vertical lines.



Full 0.18 mm CMOS Cross Section

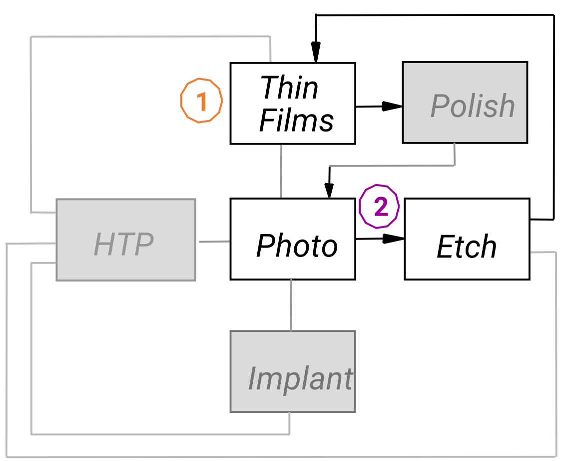
Metal Layers in a Chip

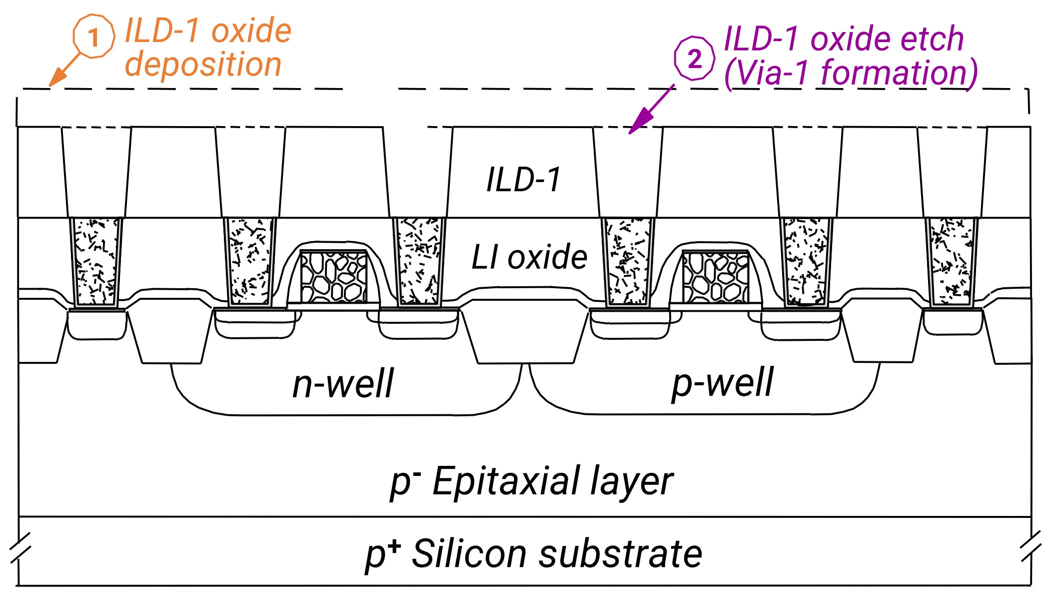


4 LM after insulator removal (Micrograph courtesy of Integrated Circuit Engineering)

Via-1 Formation (Patterning)

- PECVD of SiO_2 ①
- Lithography (10th mask)
- Reactive ion etching② to make via holes to LI (S/D and G)

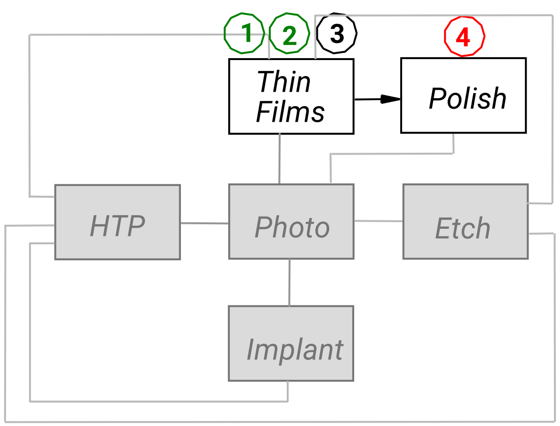


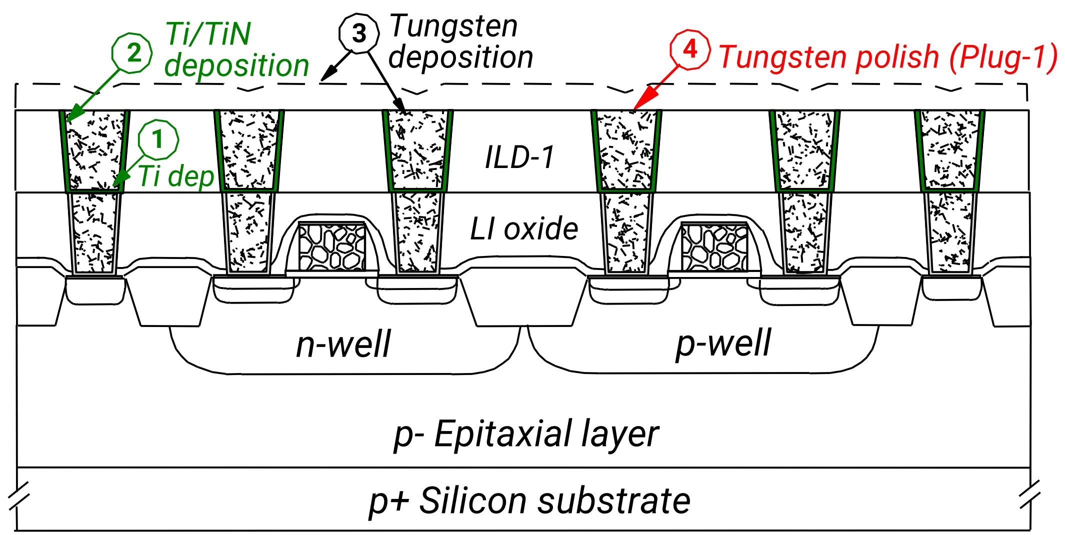


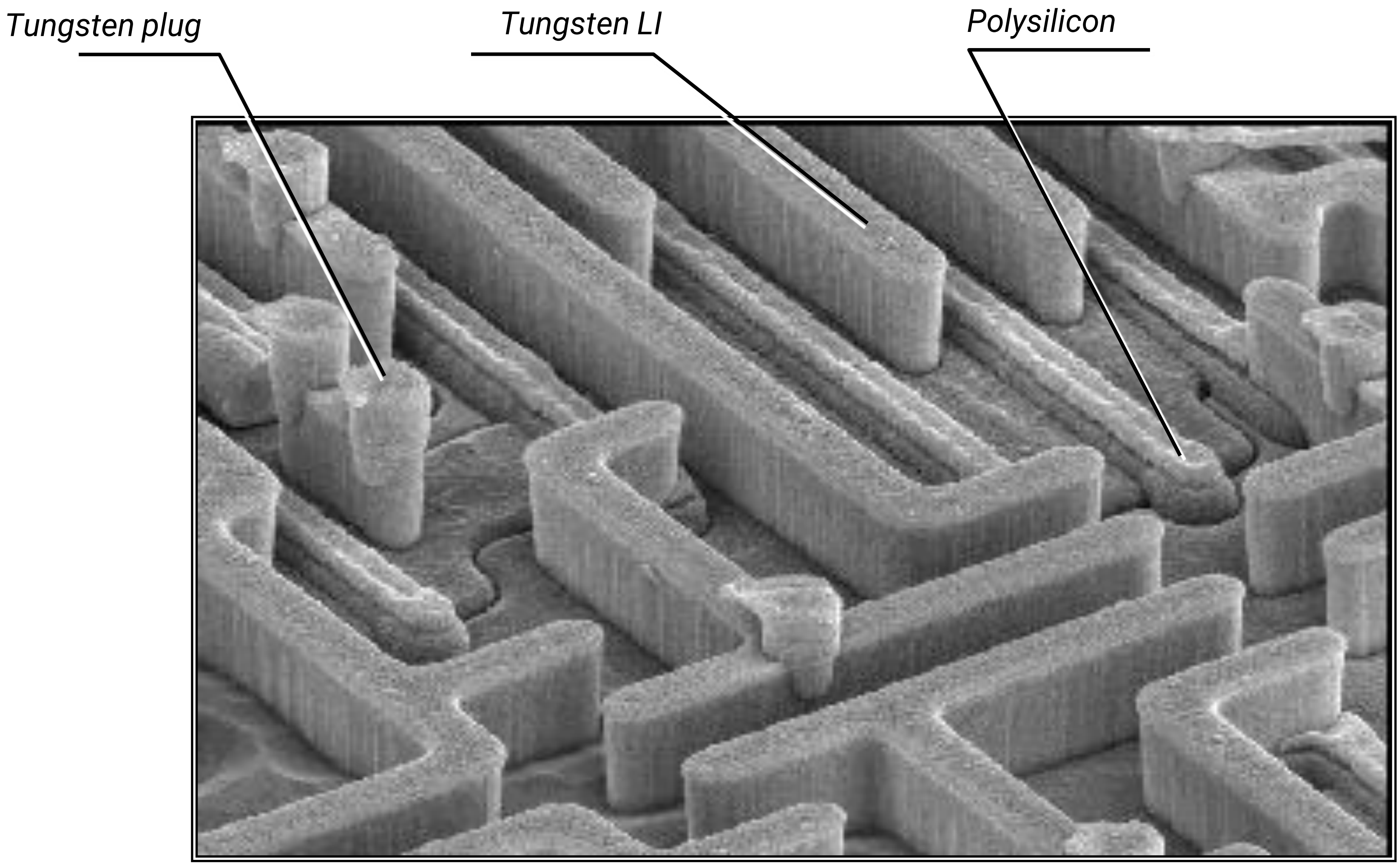
Via-1 Formation (W plug formation)

Plug = Metal core in via hole

- *Deposit thin layer of Ti (IPVD, CVD, 5 nm,①) as adhesion layer at the bottom and sides of the via holes.*
- *Deposit thin layer of TiN (IPVD, CVD, 20 nm,②) for a diffusion barrier.*
- *Deposit tungsten (CVD, 800 nm, using WF_6,③) to fill all the via openings.*
- *Use tungsten CMP process ④ to polish the tungsten and TiN/Ti down to a planarized surface of W embedded within the SiO_2.*





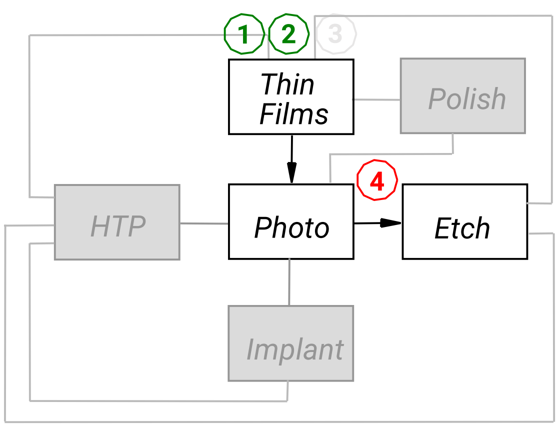


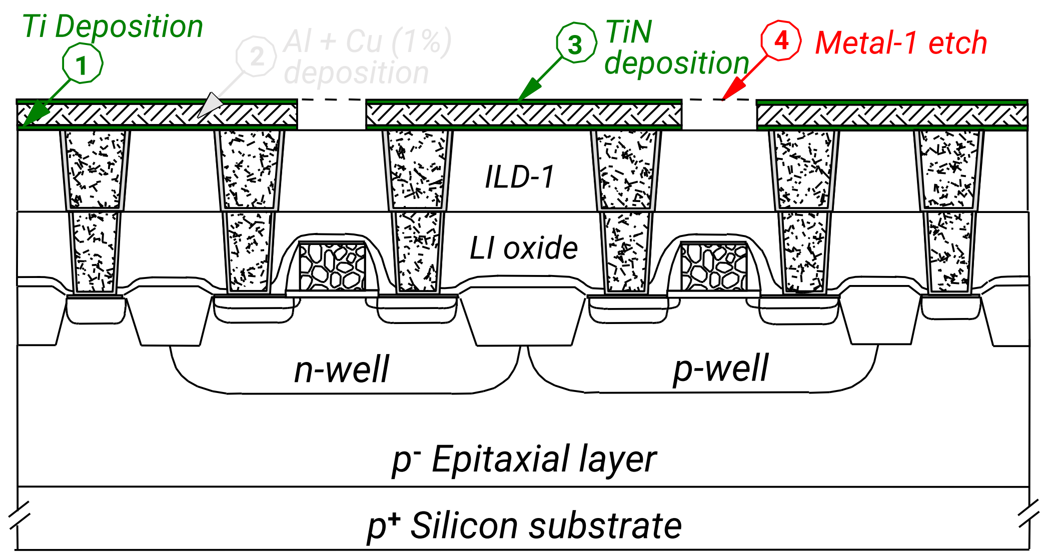
SEM photo after W plug metallization. *The oxide has been etched away, leaving only the metal. Note the very steep edges to the metallic conductors, indicating the high geometric selectivity of the Reactive Ion Etching tool. Note also the vias which are double-height structures (made of two pieces). Also shown are the polysilicon bands that tie together adjacent gates and drains for some circuit elements.*

M1 Interconnect Formation (Al subtractive)

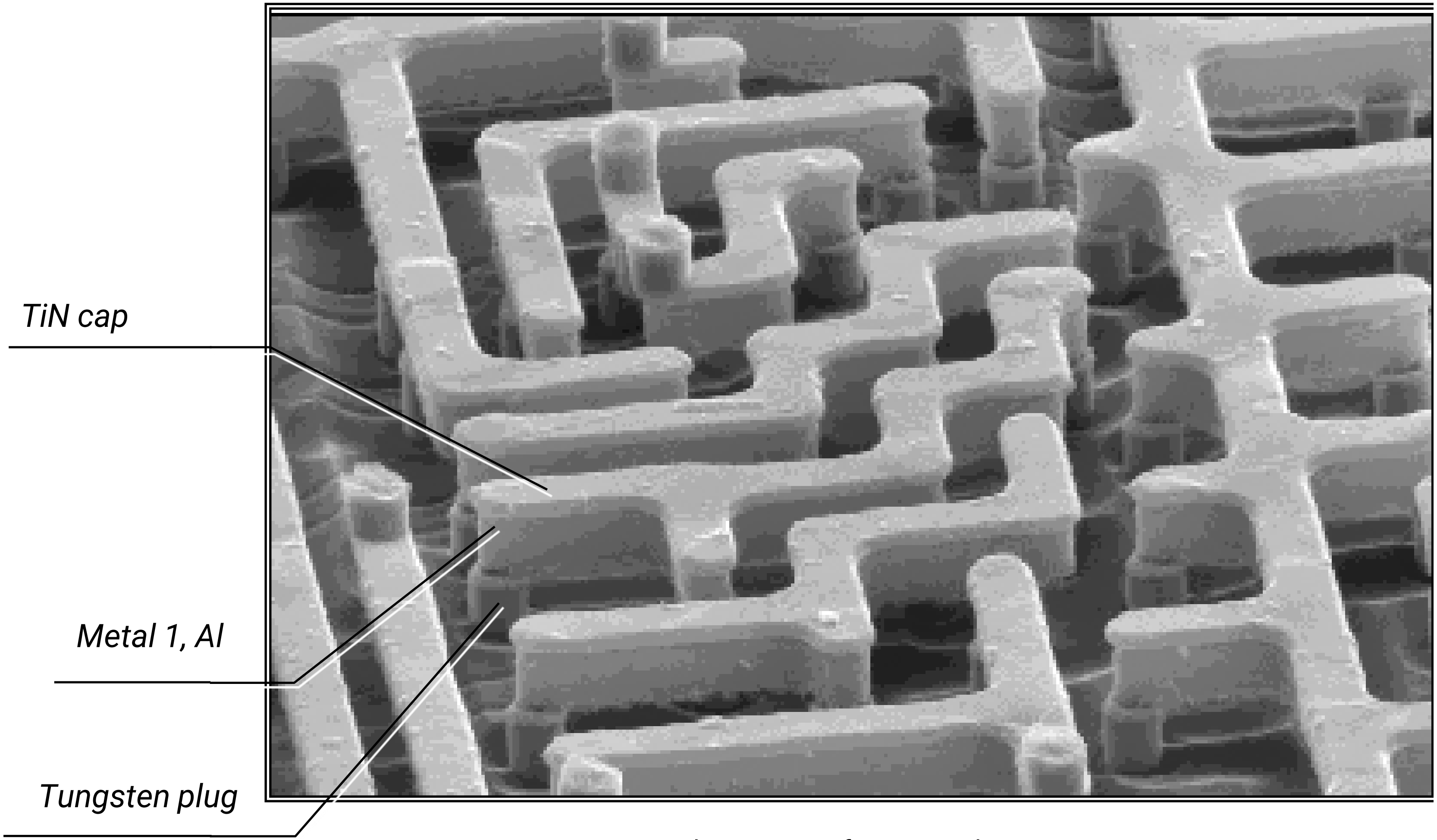
As an example of BEOL processing, an Aluminum metallization is formed. The metal stack is a fundamental block which can be reproduced for multiple interconnect layers.

- *As before, a thin layer of titanium ① is sputtered onto the wafer (which contains vias plugs and insulator) as adhesion layer (glue) between the Al wires and the underlayers.*
- *The metallization will be Al (②, 1-3% Cu, 200 nm), deposited using sputtering. The Cu is added to prevent electromigration during device operation.*
- *A thin TiN (③, 50 nm, sputtered) is deposited to act as an anti-reflective coating (ARC) over the metal. Without this, the next photoresist exposure would be non-uniform with the resist over the metal (since metal reflects light back).*
- *Photoresist is applied, exposed (11^{th} mask) and patterned, then the 3-layer metal stack (Ti/Al(Cu)/TiN) is etched using a plasma etcher ④.*





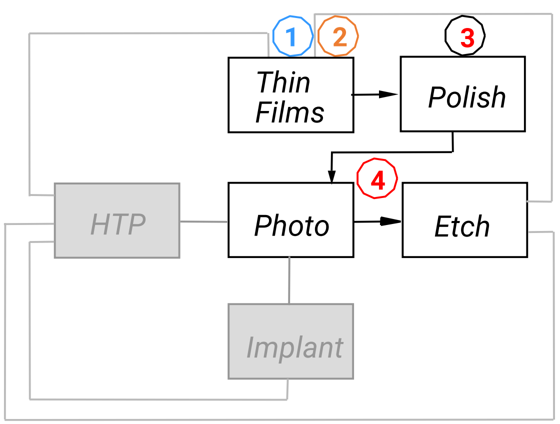
SEM Micrograph of First Metal Layer over First Set of Tungsten Vias

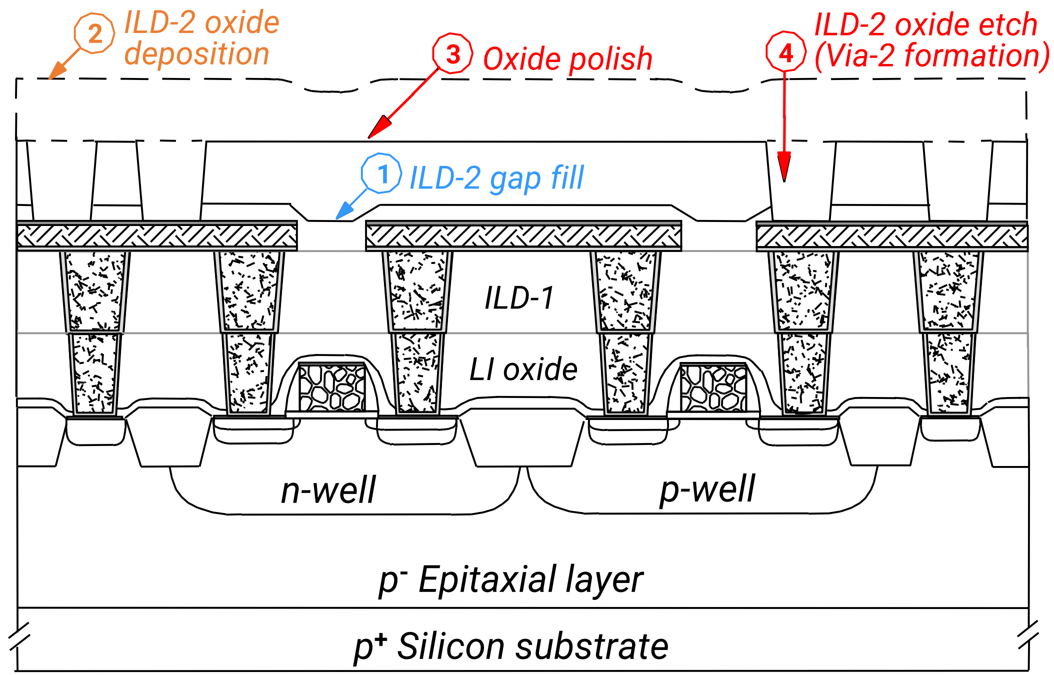


Micrograph courtesy of Integrated Circuit Engineering

Via-2 to Via-X Formation (ILD dep + Patterning)

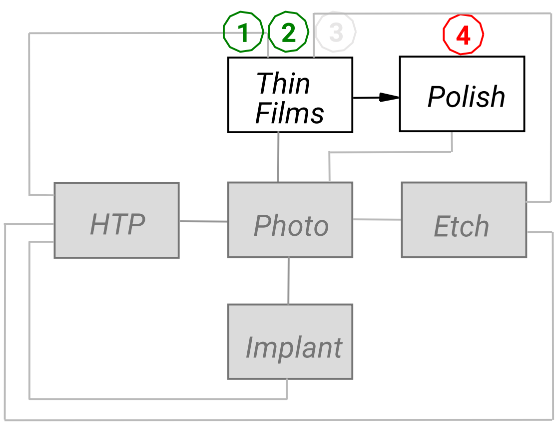
- *Deposit SiO_2 ① using HDPCVD tool (300 nm). This will void-free fill the gaps between the metal lines.*
- *Deposit thick SiO_2 ② using PECVD tool. The oxide is thick to prevent cross-talk between metal layers.*
- *Polish SiO_2 with CMP ③*
- *Apply photoresist, expose patterns for the vias (12th mask), etch via holes with plasma etcher ④.*

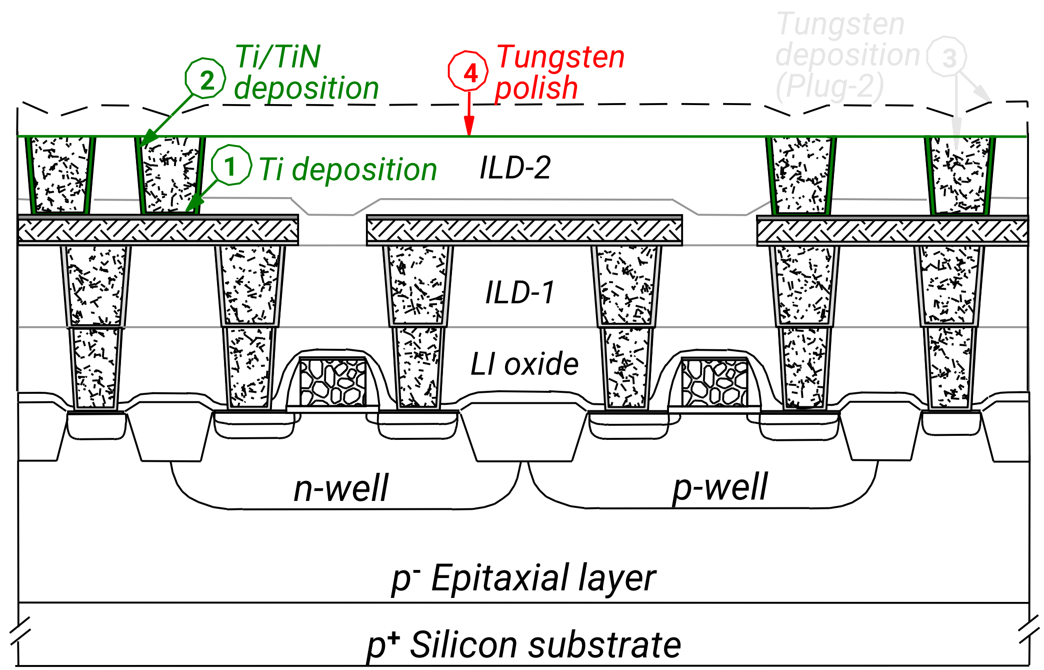




Via-2 to Via-X Formation (W plug)

- *Deposit thin titanium ① layer as glue (30 nm, sputter).*
- *Deposit thin TiN ② layer (CVD) to act as diffusion barrier between Ti and tungsten plug.*
- *Deposit thick tungsten layer (CVD using WF_6) to fill the via holes ③.*
- *Tungsten and TiN/Ti CMP ④ down to the SiO_2 surface between the metal vias.*

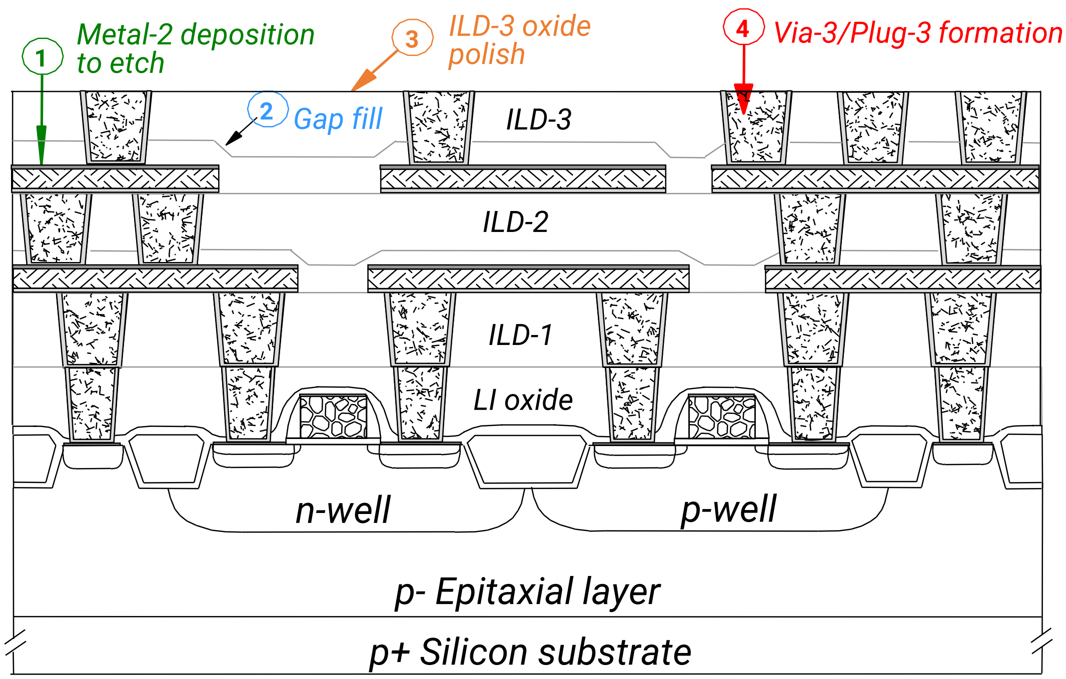




Metal-2 to Metal-X Interconnect Formation

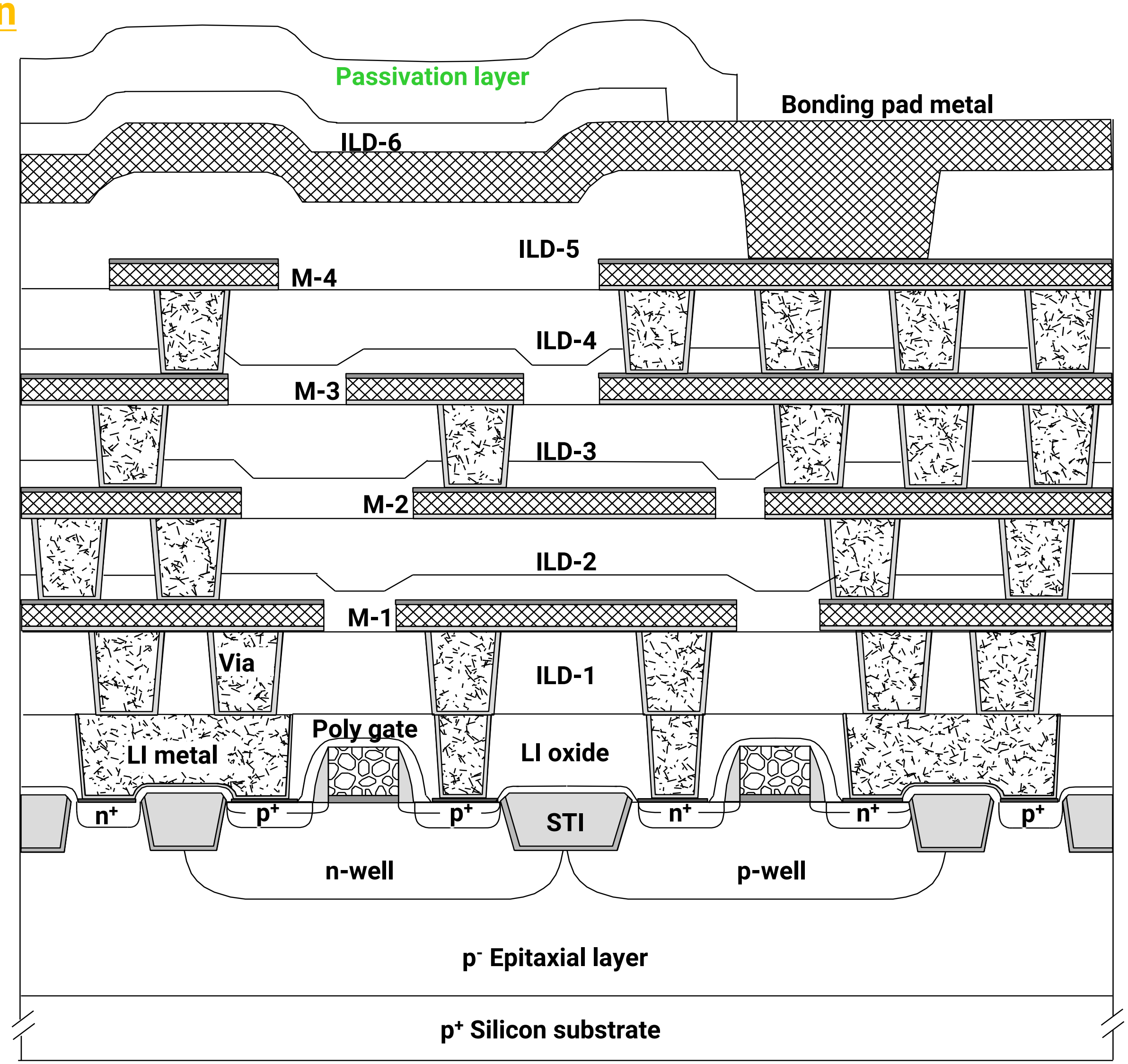
The next steps forms further interconnects between layers.
These steps are repeated for as many metallization layers as required.

- *Deposit 3-metal stack for conductors – Ti/Al(Cu)/TiN.* ①
  Pattern and use plasma etch to form lines.
- *Use high-density SiO_2 to fill metal gaps (HDPCVD tool).* ②
- *Deposit thick SiO_2 with PECVD tool to isolate the metal. Litho for vias and etch via holes.* ③
- *Coat via holes with thin Ti/TiN, then fill vias with thick tungsten layer. Polish the metals down to SiO_2.* ④

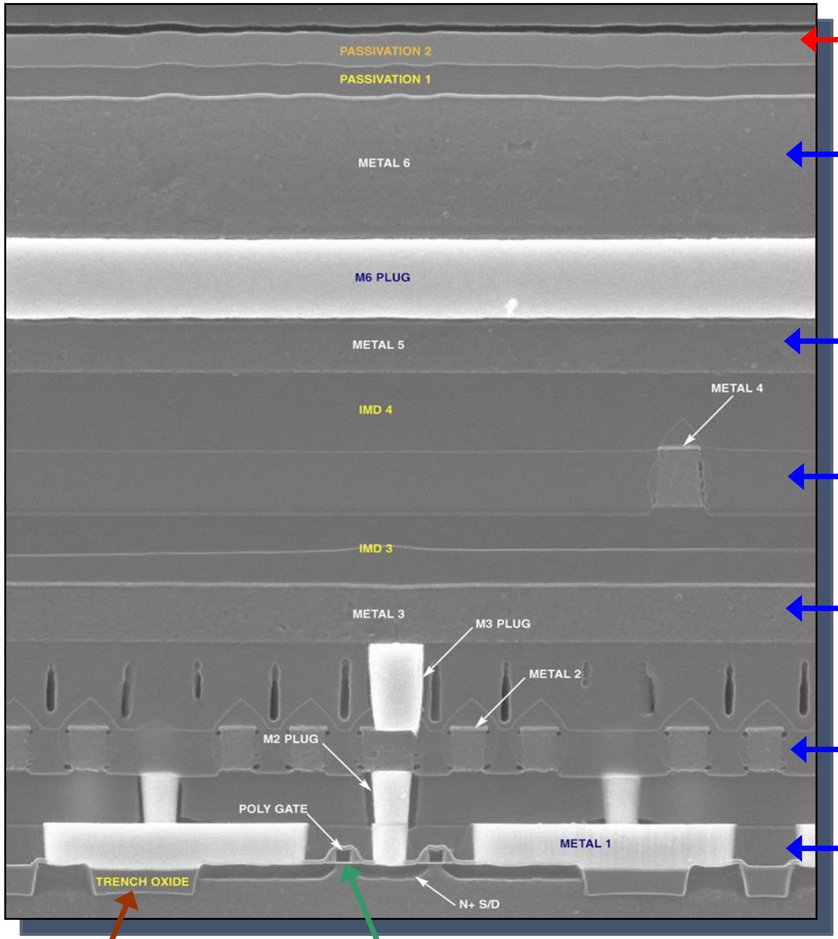


Full 0.18 mm CMOS Cross Section

- *Final layer uses wide thick metals to connect wiring to bonding pads for external connections.*
- *Passivation layer of* **Si_3N_4** *is used to protect IC from moisture, scratching, and contamination (buffer layer of SiO_2 beneath – ILD-6).*



SEM Cross-section of AMD Microprocessor



Surface Passivation Layers
SiO_2 (500nm) + Si_3N_4 (200 nm)

Metal Layer #6

Metal Layer #5

Metal Layer #4

Metal Layer #3

Metal Layer #2

Metal Layer #1

Isolation Trench

PolySi Gate Contact

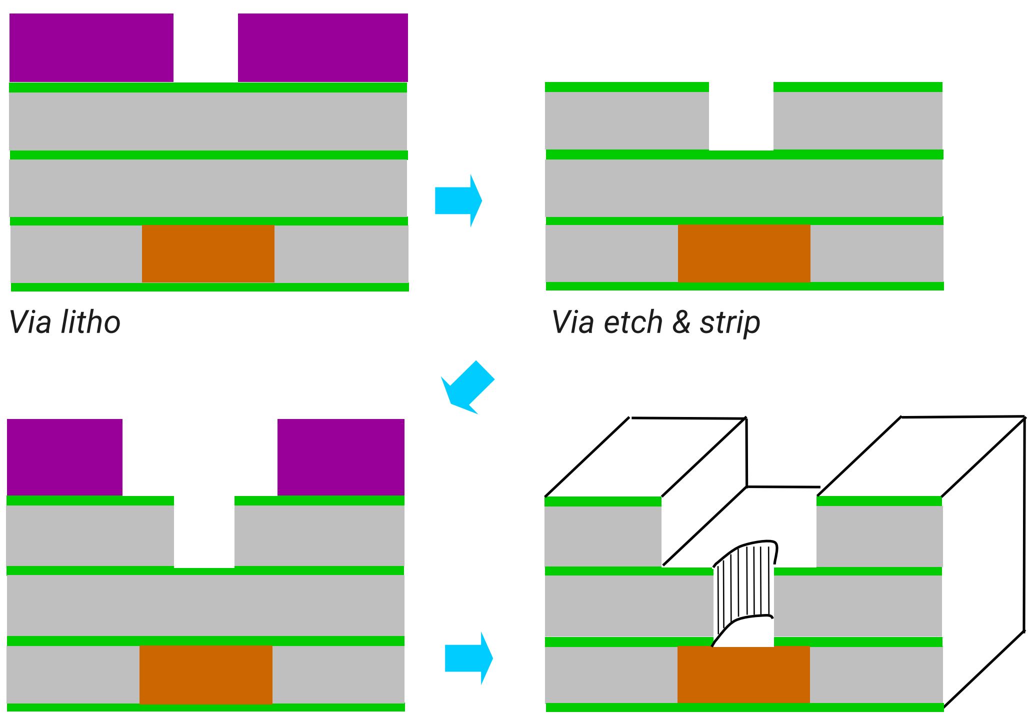
Micrograph courtesy of
Integrated Circuit Engineering

Summary of Concepts

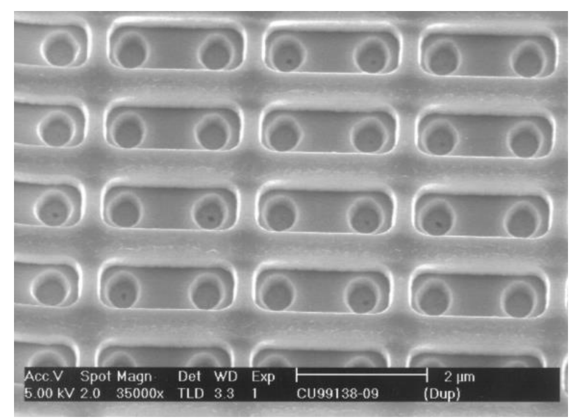
- *Damascene Process (CMP) – Process for surface planarization and provide embedded patterns (STI, W contact/local interconnect, W via, ILD planarization).*
- *Sacrificial Oxide – SiO_2 (10 nm) which protects Gate surface during prior processing.*
- *CMP & Etch Stop Layers: Si_3N_4 – Using Si_3N_4 in conjunction with appropriate high selectivity CMP and RIE processes.*
- *Anisotropic Etching – Etches "horizontal surfaces" faster than vertical surfaces. Requires highly directional (ion assisted) etch processes (RIE), along with sidewall passivation.*
- *Self-Aligned Gate – Polycrystalline Gate is used a mask for the source/drain implant. It automatically aligns these to the correct position.*
- *Gate Side-Wall Spacer – Provides insulation between the Gate and Source/Drain contacts, and also alignment of 2^{nd} high-dose S/D implant.*
- *Self-Aligned Silicide Contacts – Deposited metal reacts with silicon forming new compound (silicide). Makes ohmic contact and also allows etching of unreacted metal layer without masking (selective etching).*
- *Diffusion Barriers – TiN and Si_3N_4 can be used to encapsulate metals to prevent them from diffusing into SiO_2 and causing problems. Si_3N_4 used as passivation layer for IC protection (e.g. moisture in-diffusion).*

Alternative BEOL Concept: Cu Dual Damascene

- *It uses two dielectric etch processes, one via etch and one trench etch*
- *Metal layers are deposited into via holes and trenches.*
- *A CMP process removes copper and tantalum barrier layer*
- *Leave copper lines and plugs embedded inside the dielectric layer*



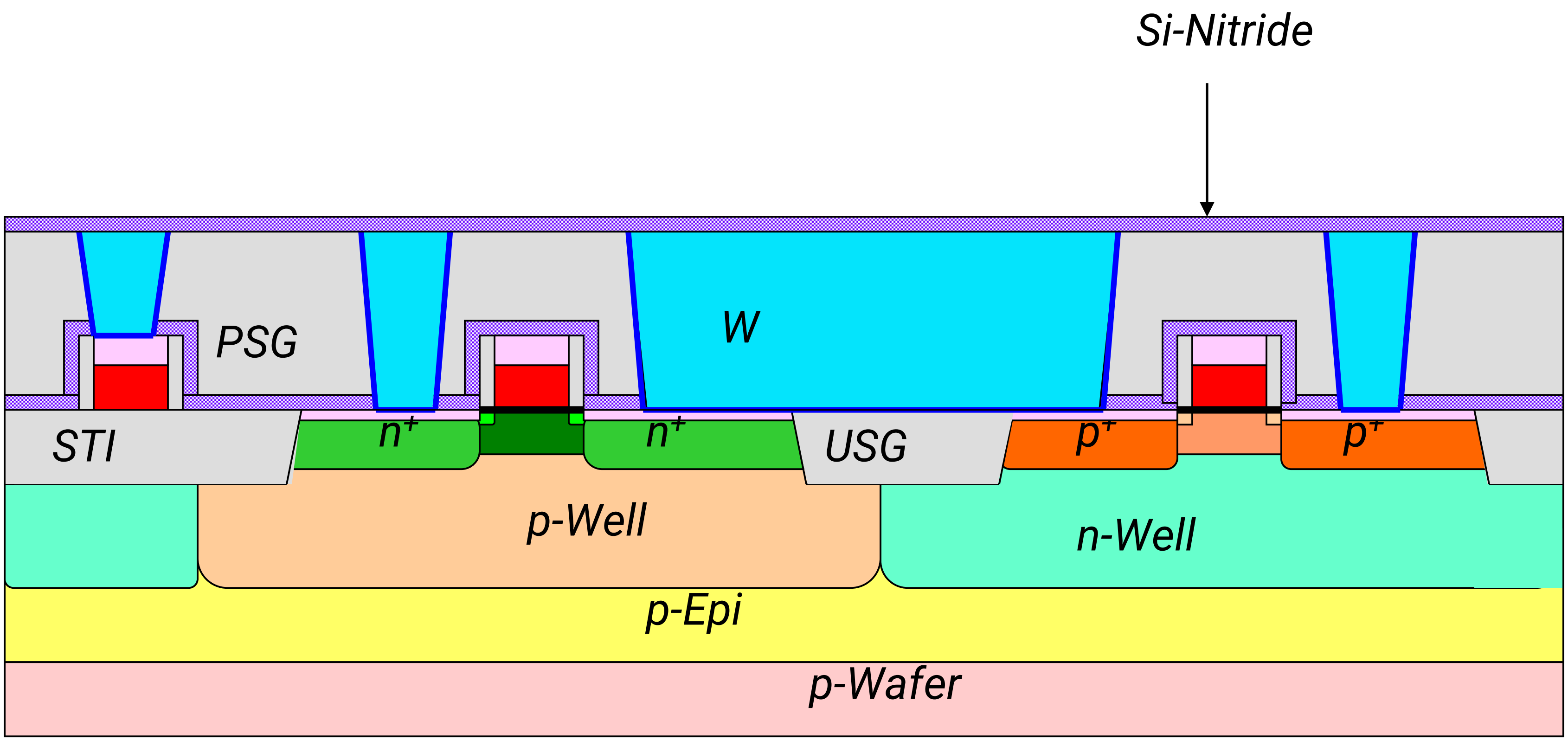
- *Resist*
- *Si_3N_4, SiC*
- *SiO_2 or Low-k*
- *Cu*



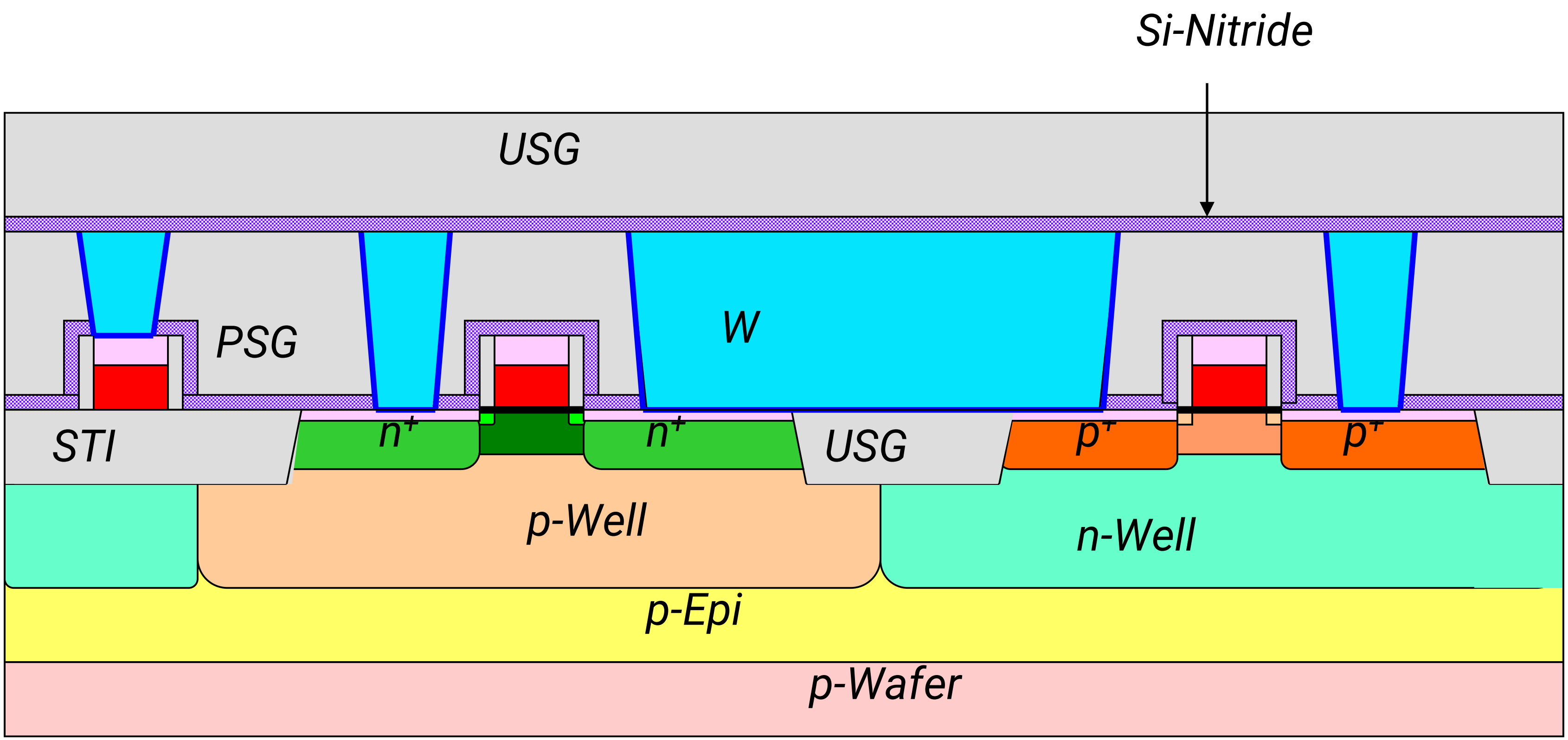
source: IMEC 2003

PECVD Nitride

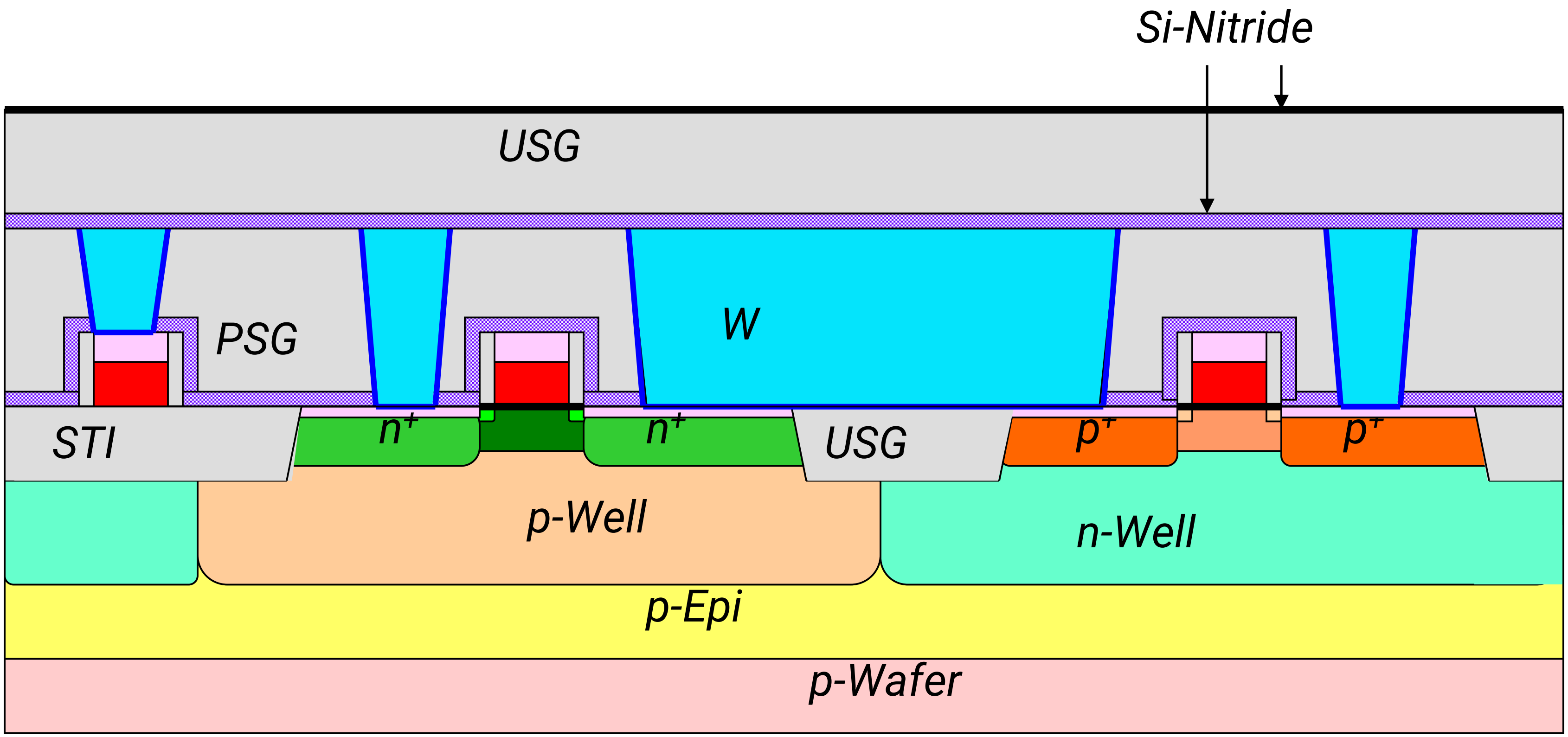
USG: undoped silicate glass (SiO_2)
PSG: Phosphorous doped silicate glass



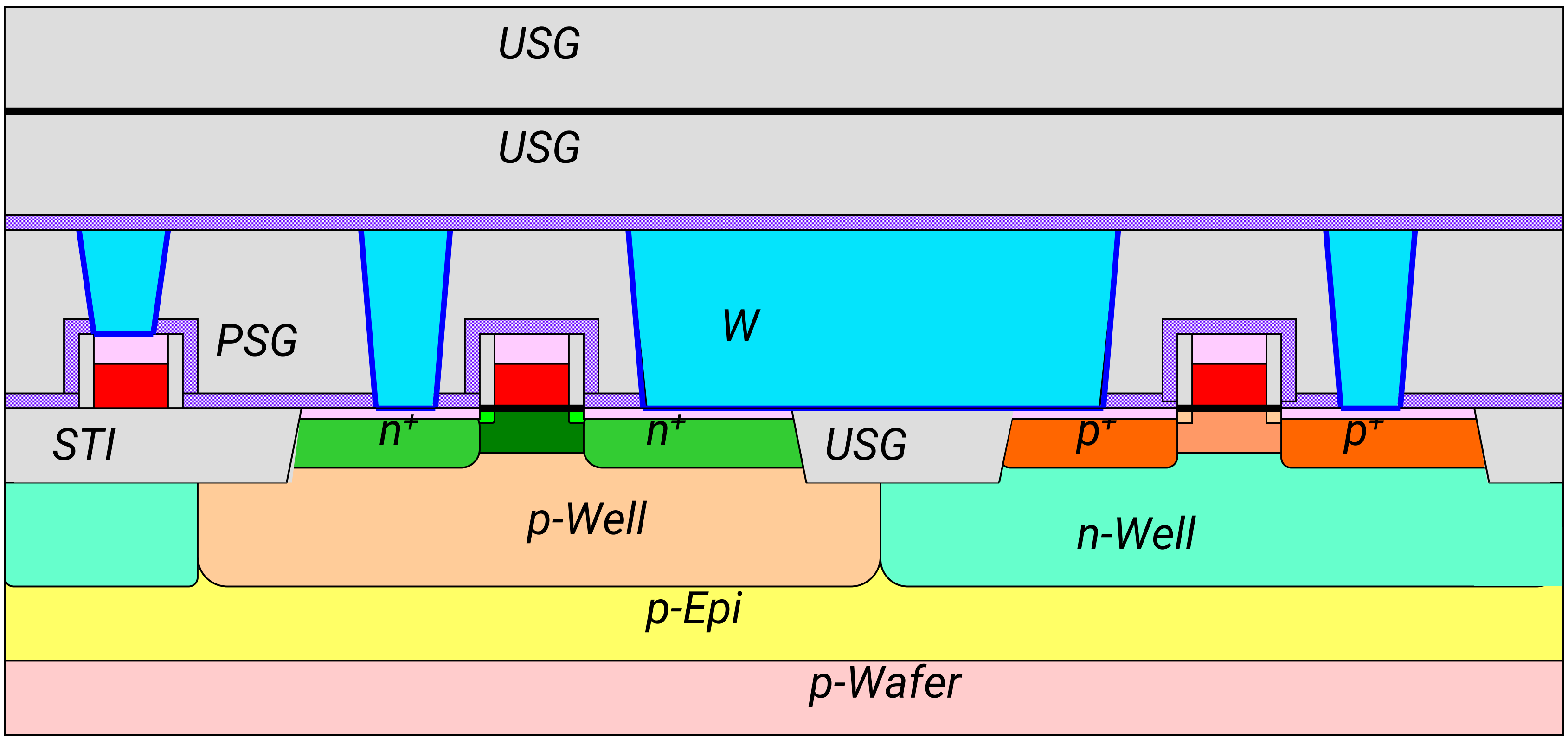
PECVD USG



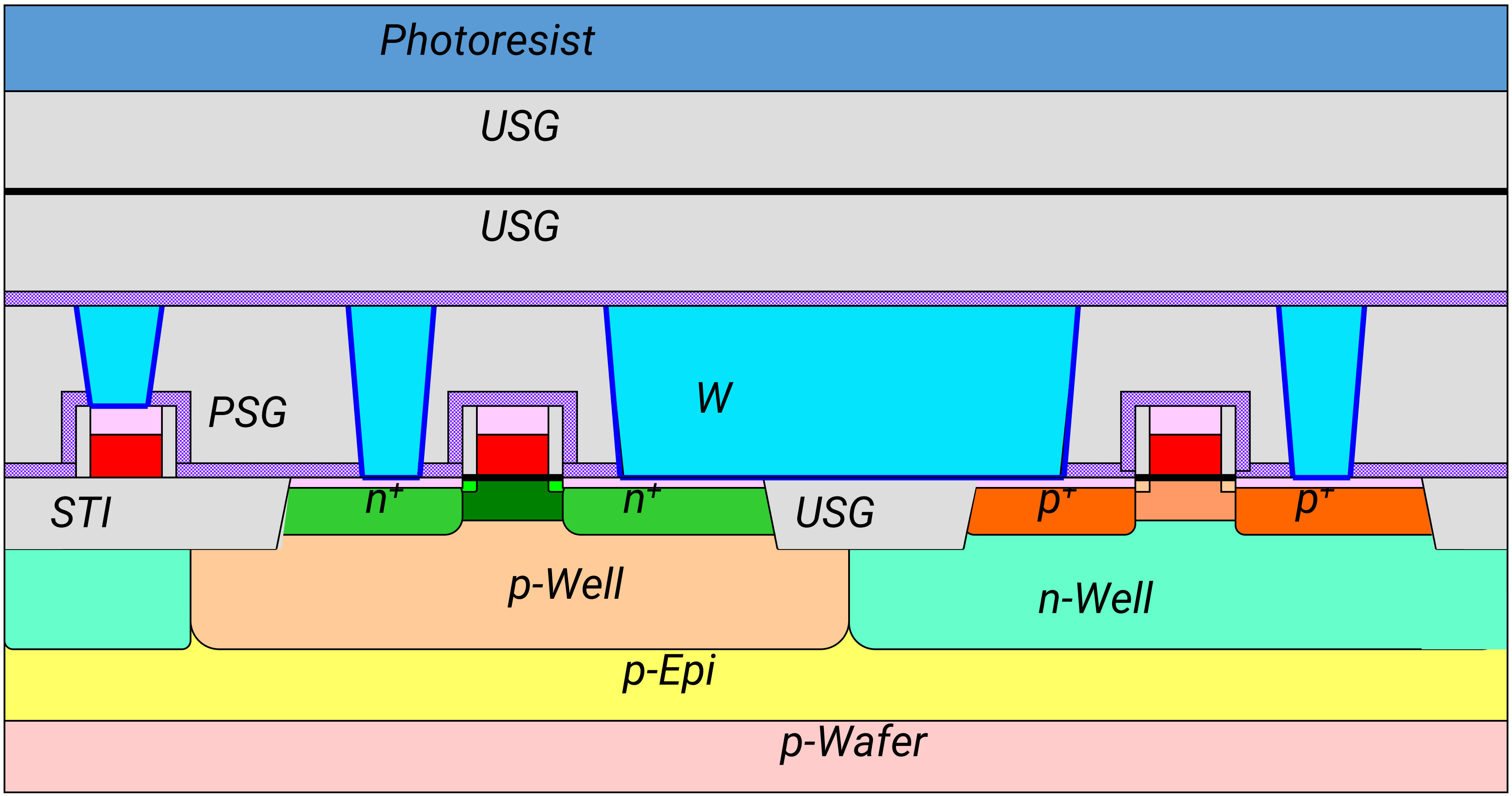
PECVD Etch Stop Nitride



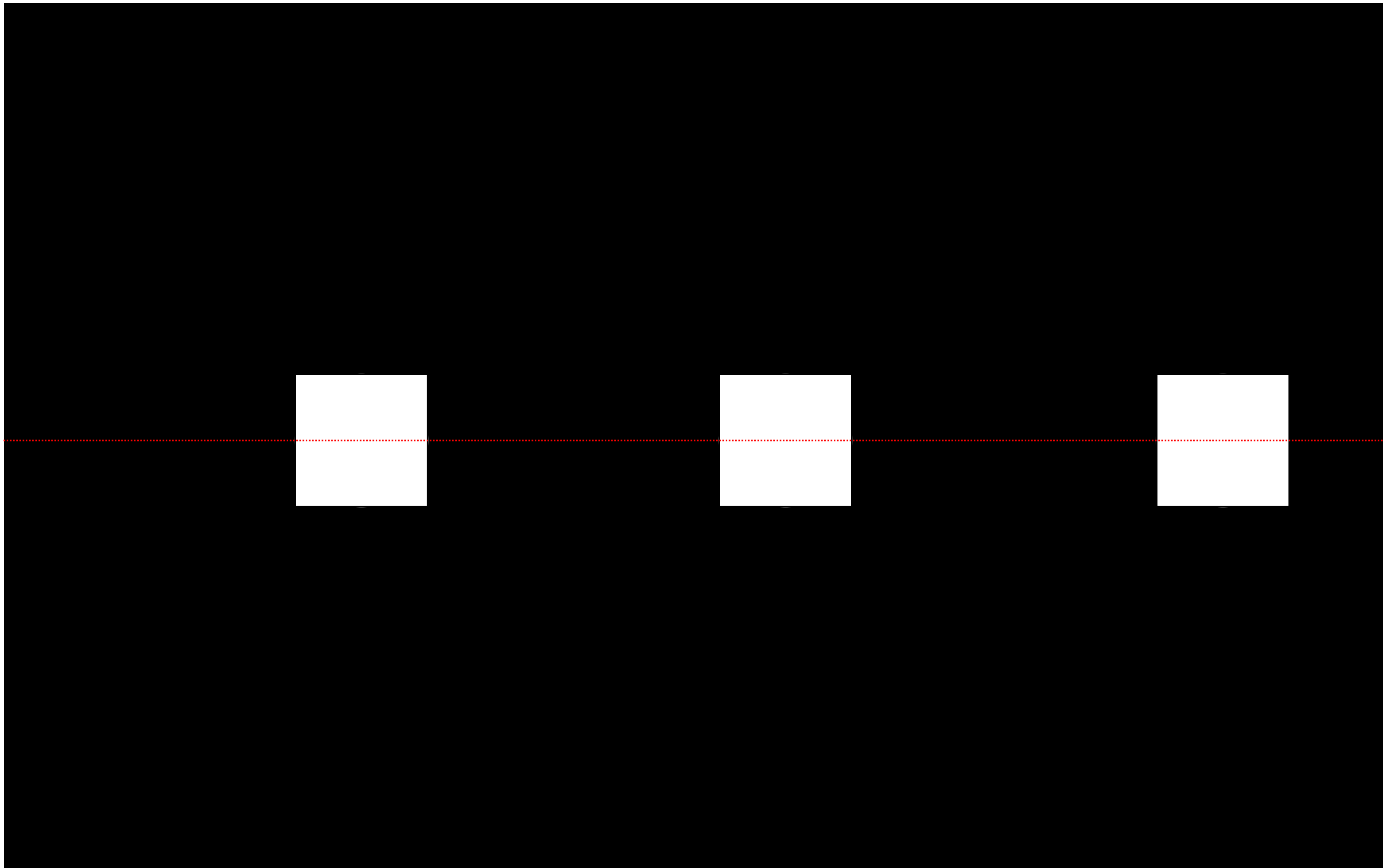
PECVD USG



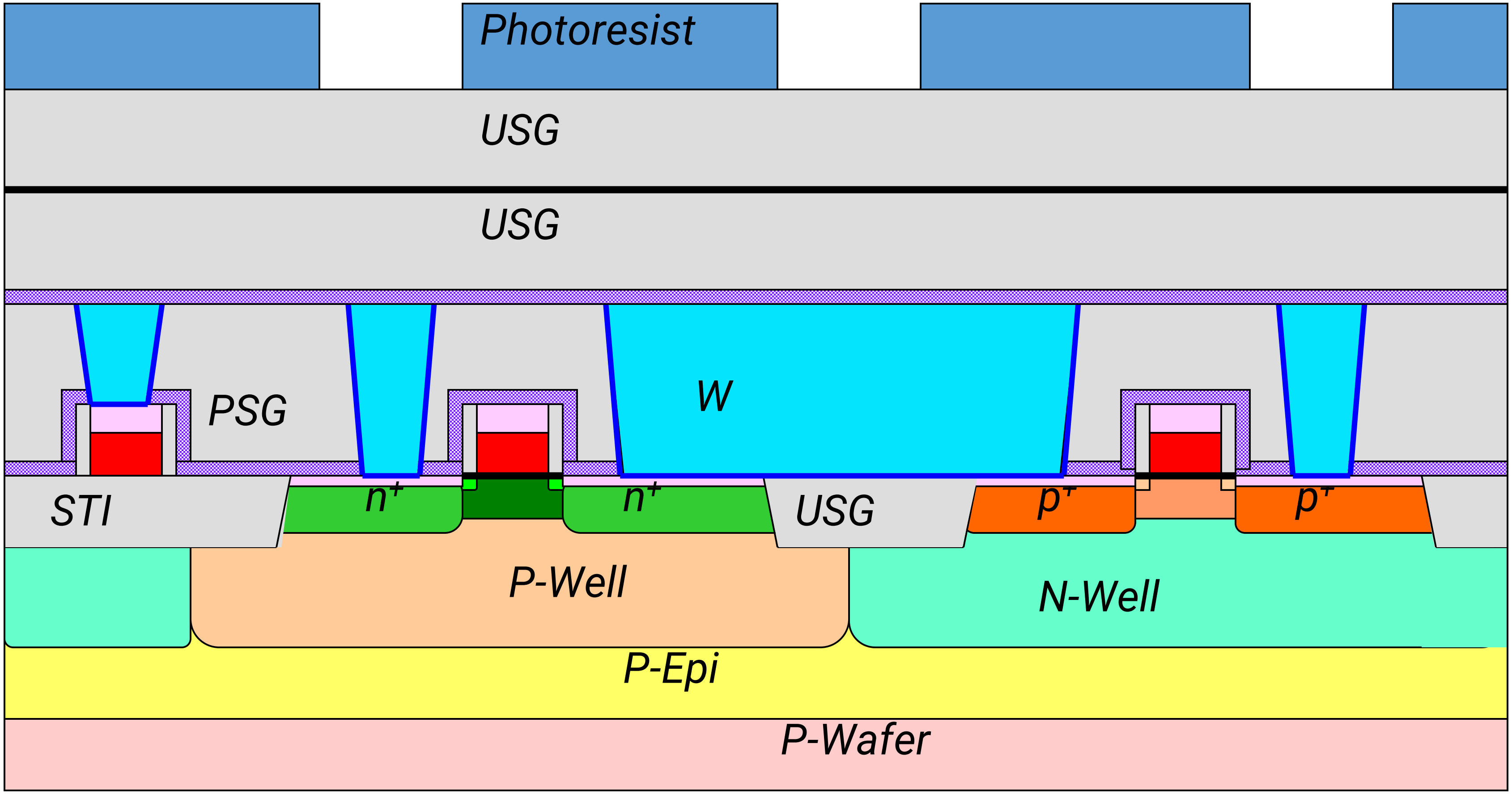
Photoresist Coating



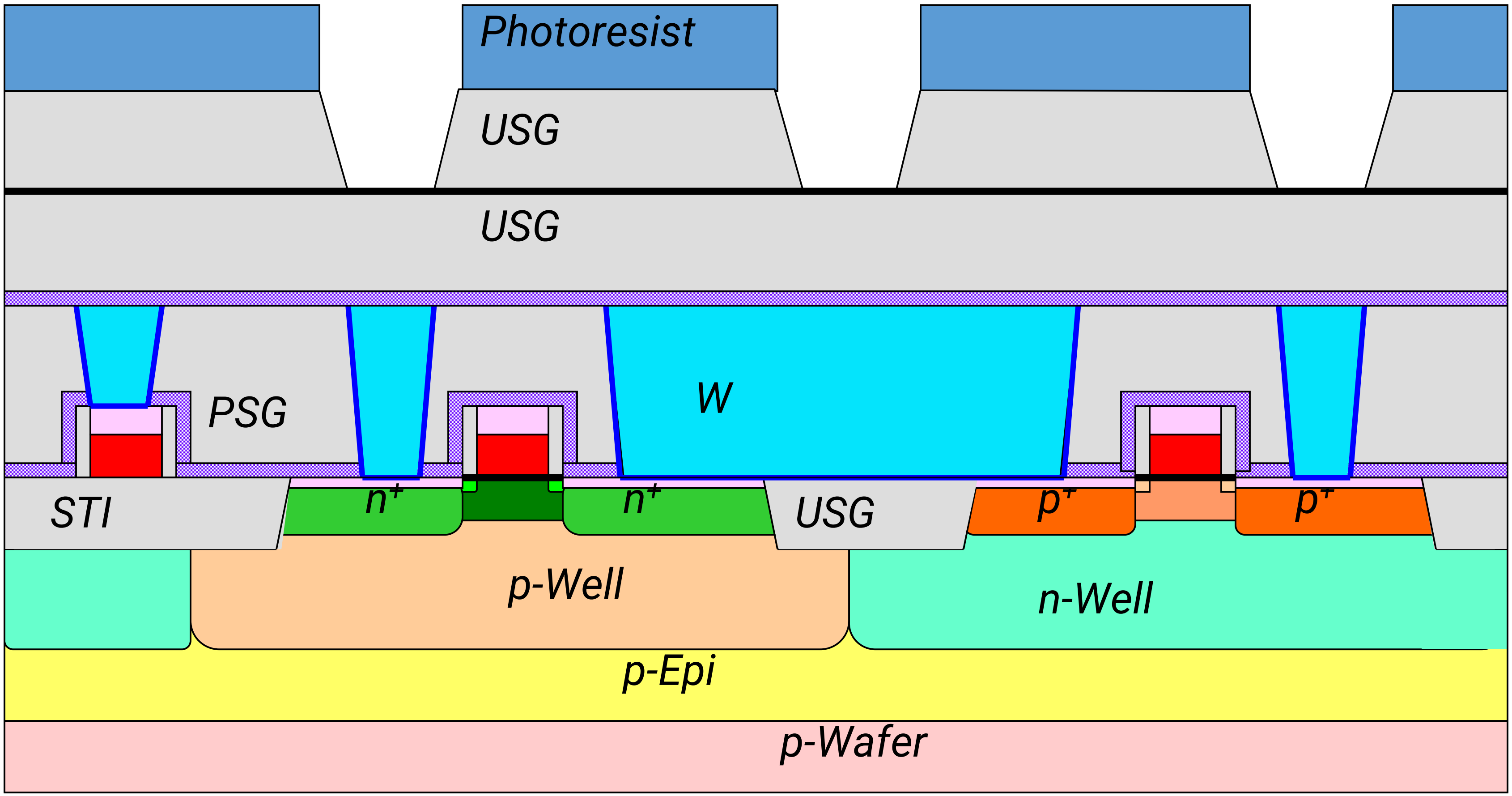
Via 1 Mask



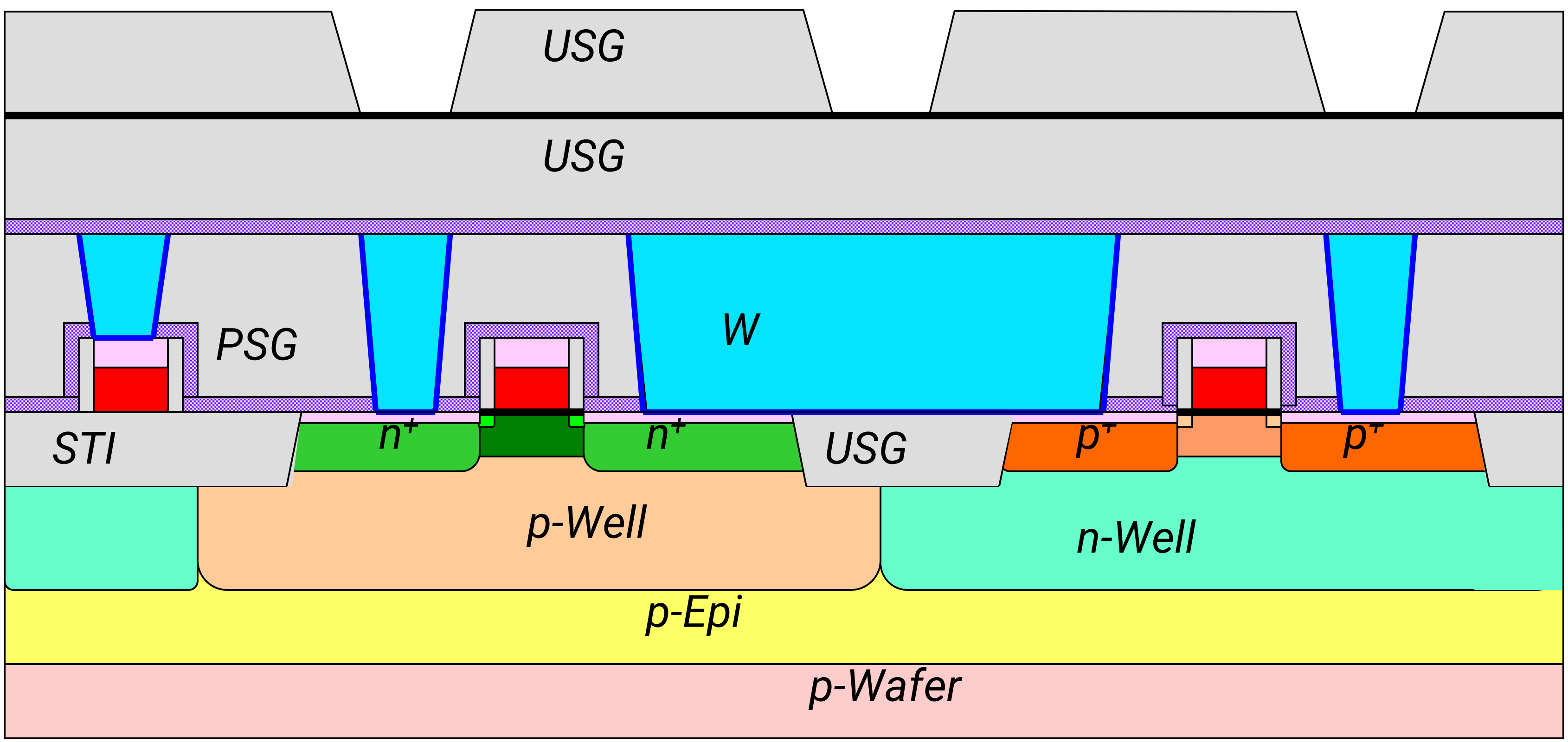
Via 1 Mask Exposure and Development



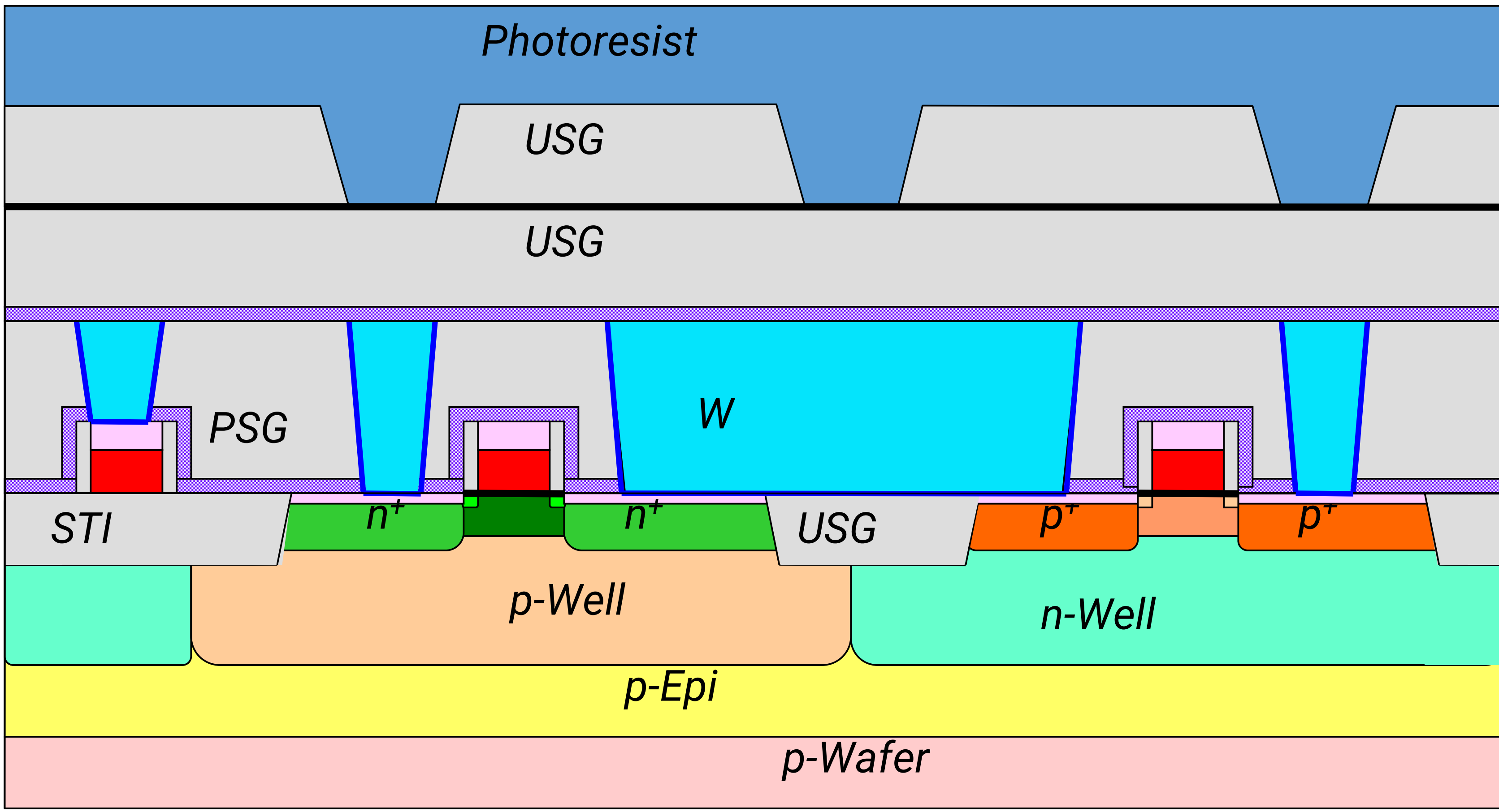
Etch USG, Stop on Nitride



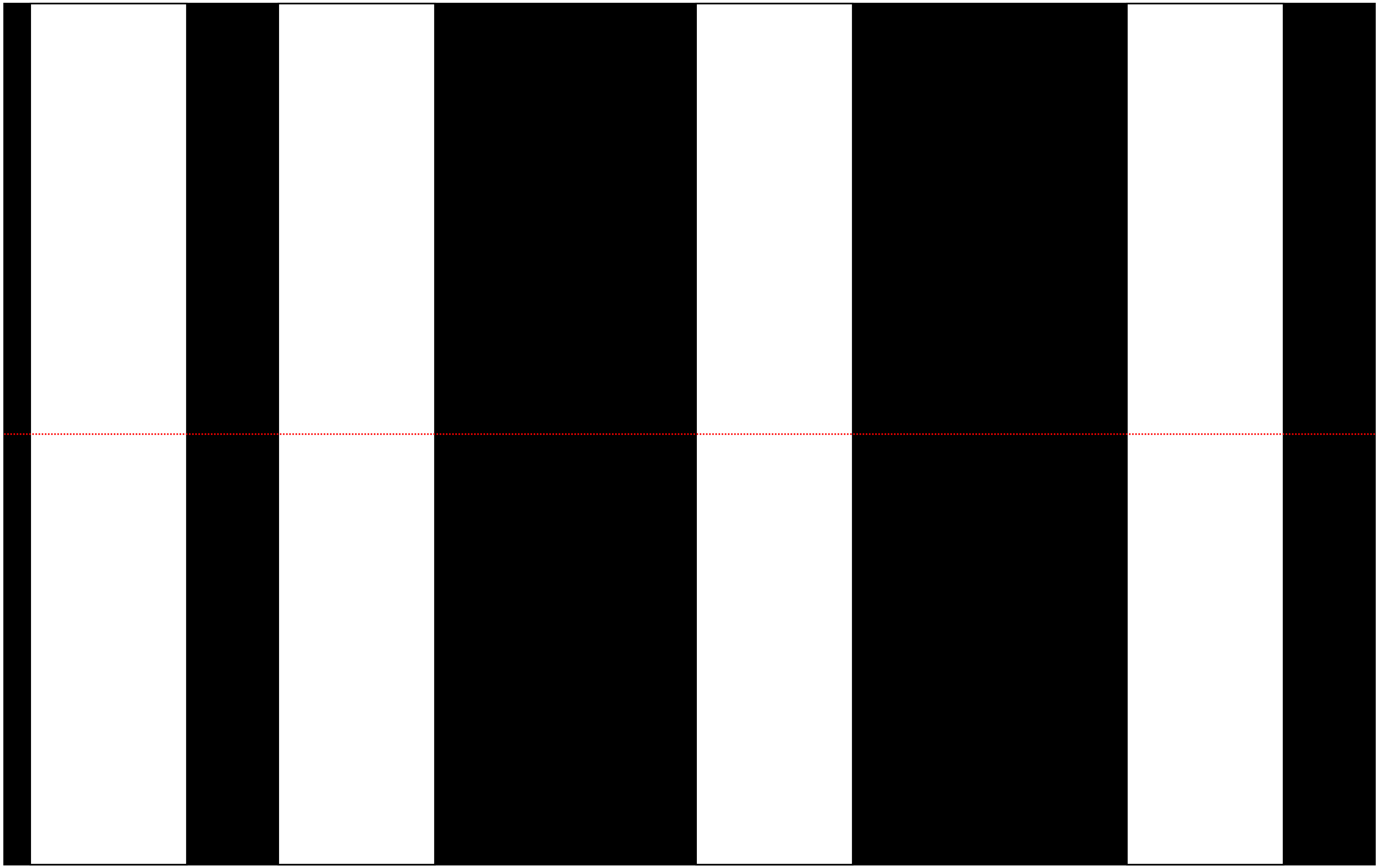
Strip Photoresist



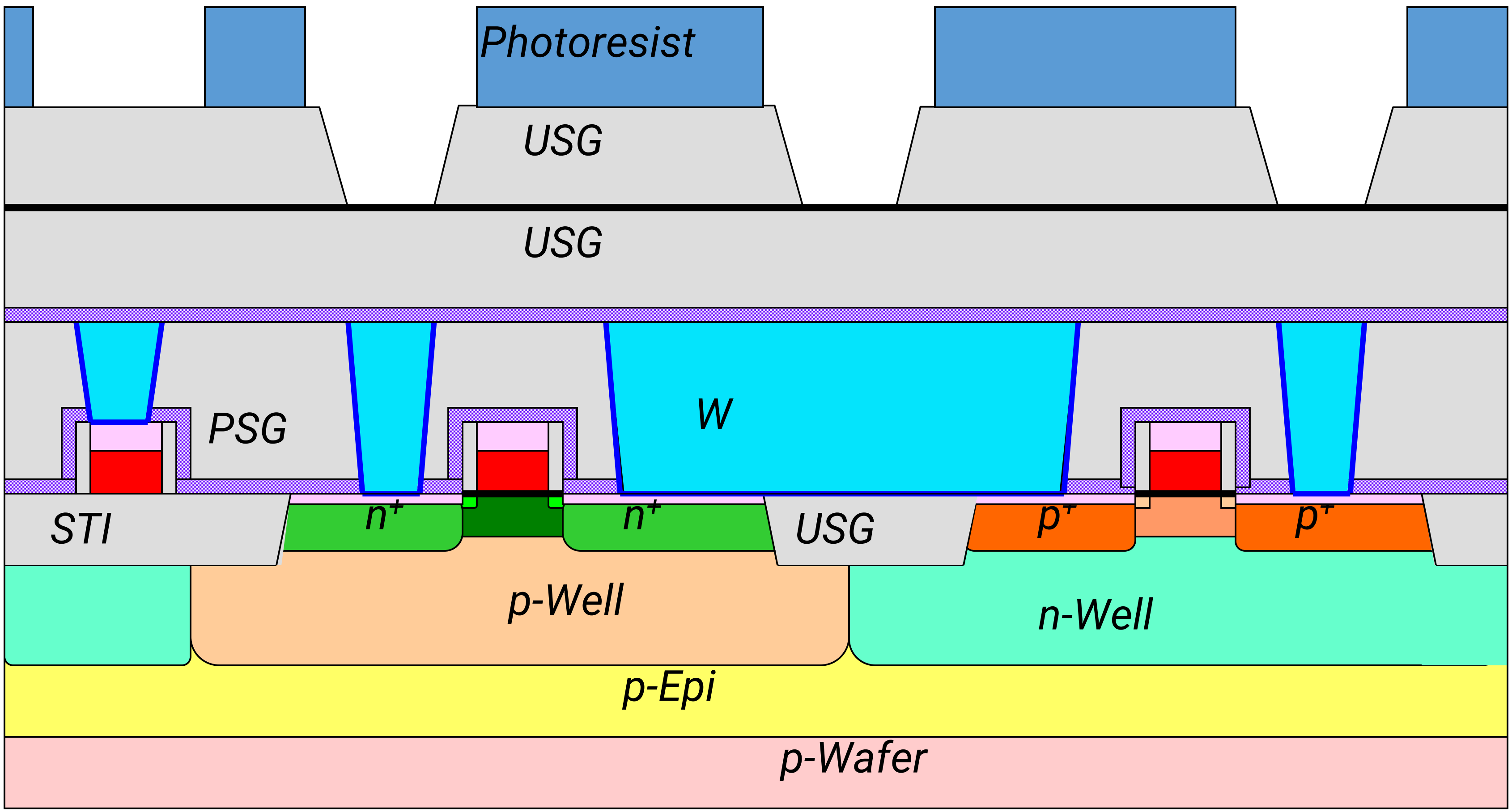
Photoresist Coating



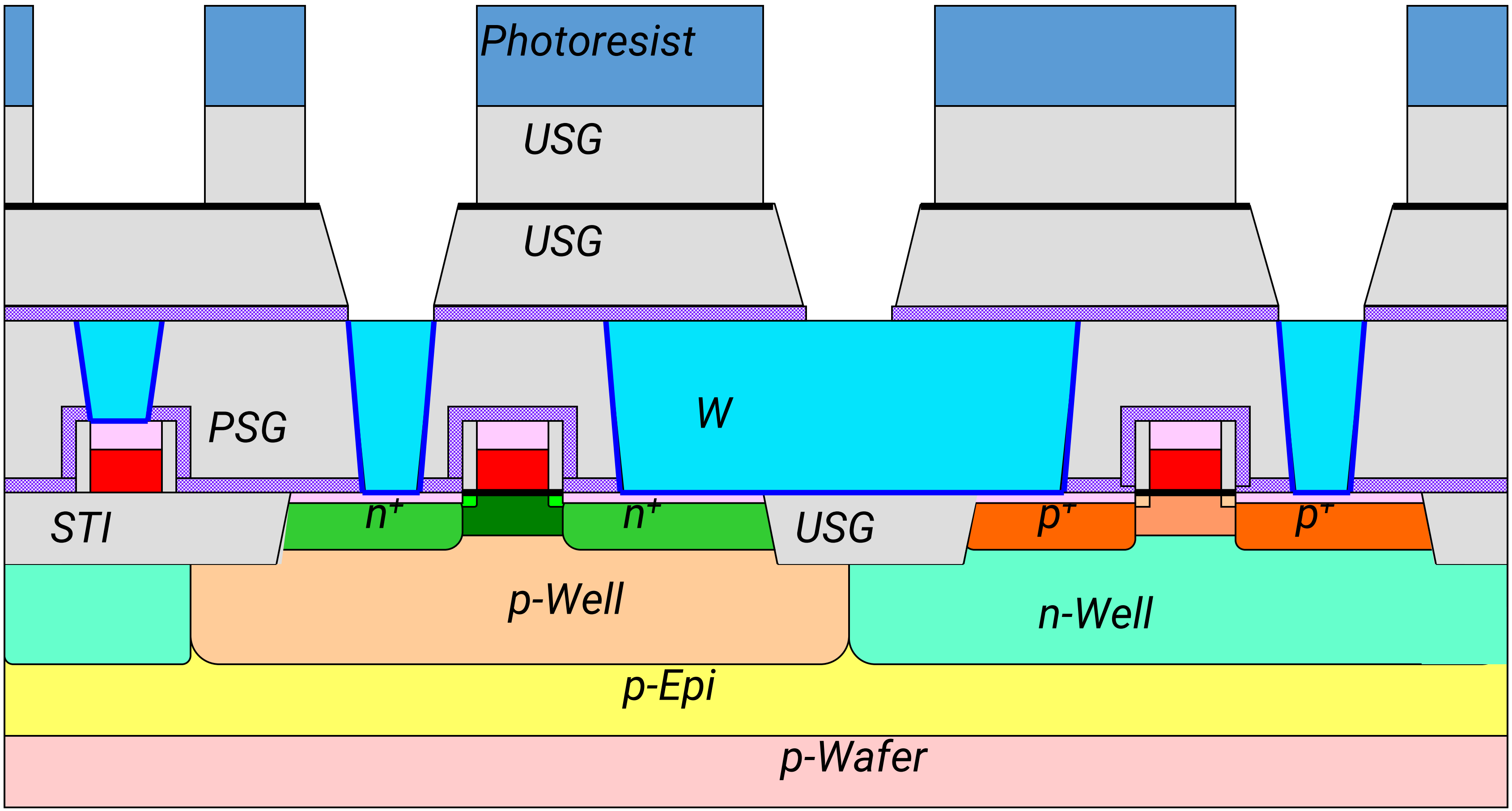
Metal 1 Mask



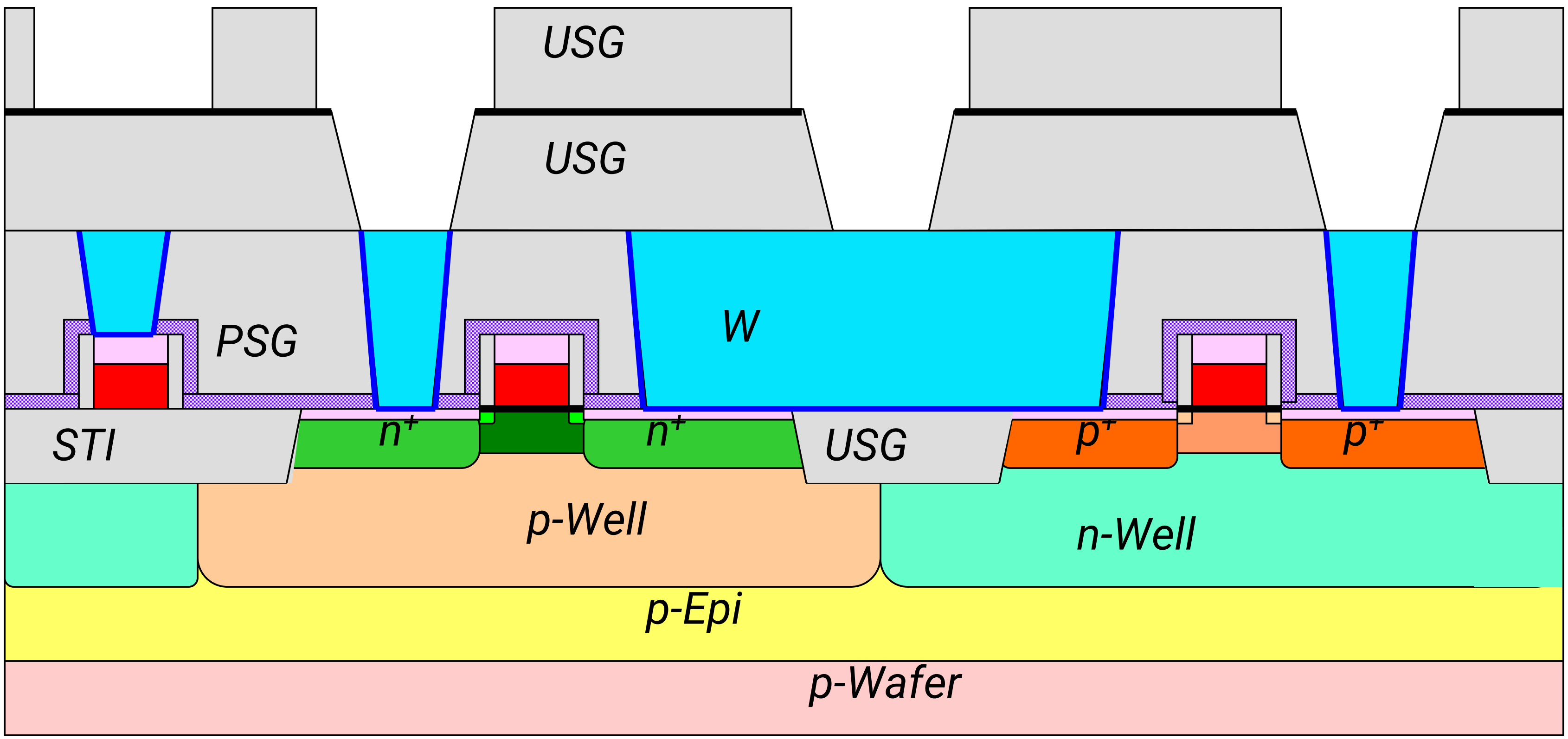
Metal 1 Mask Exposure and Development



Etch USG and Nitride



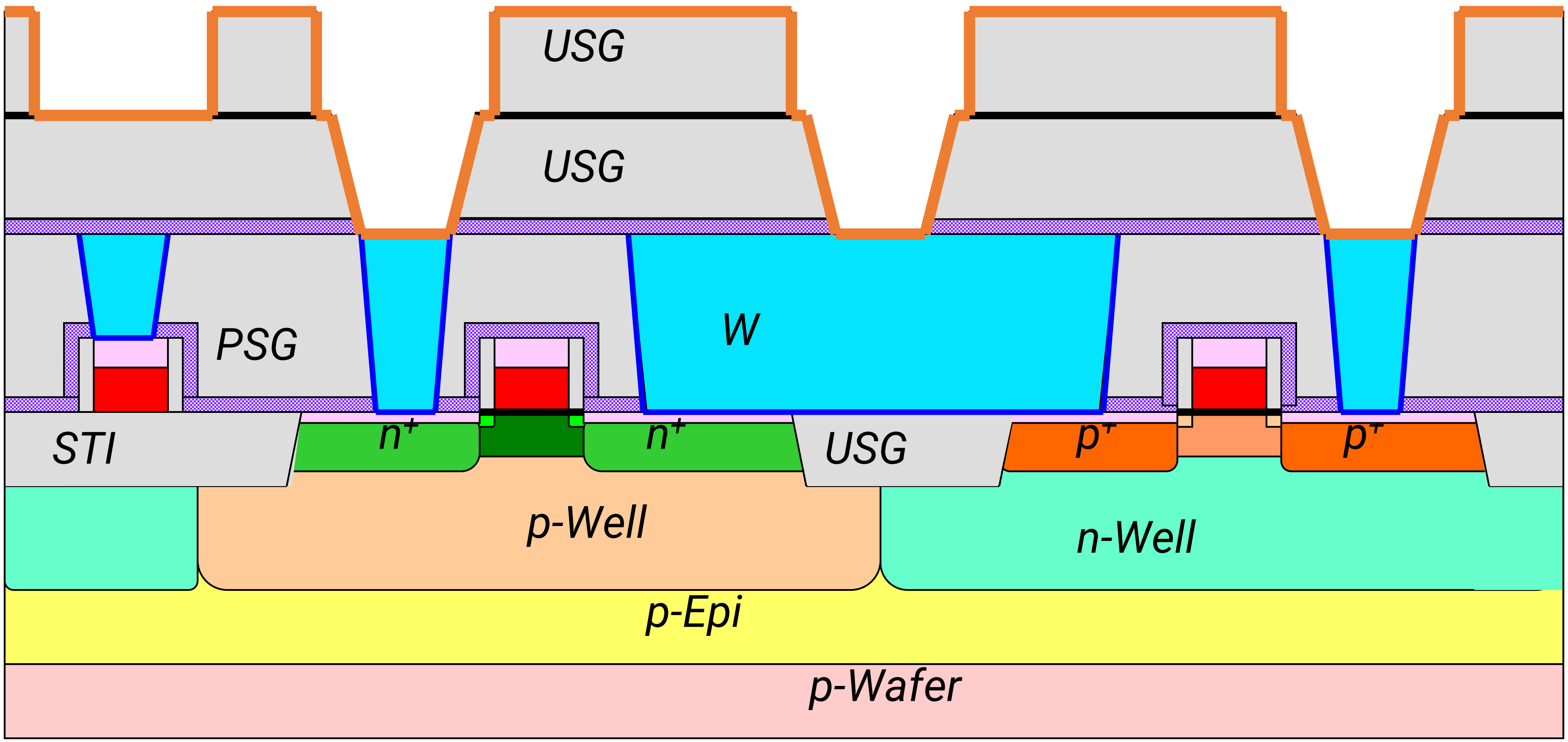
Strip Photoresist



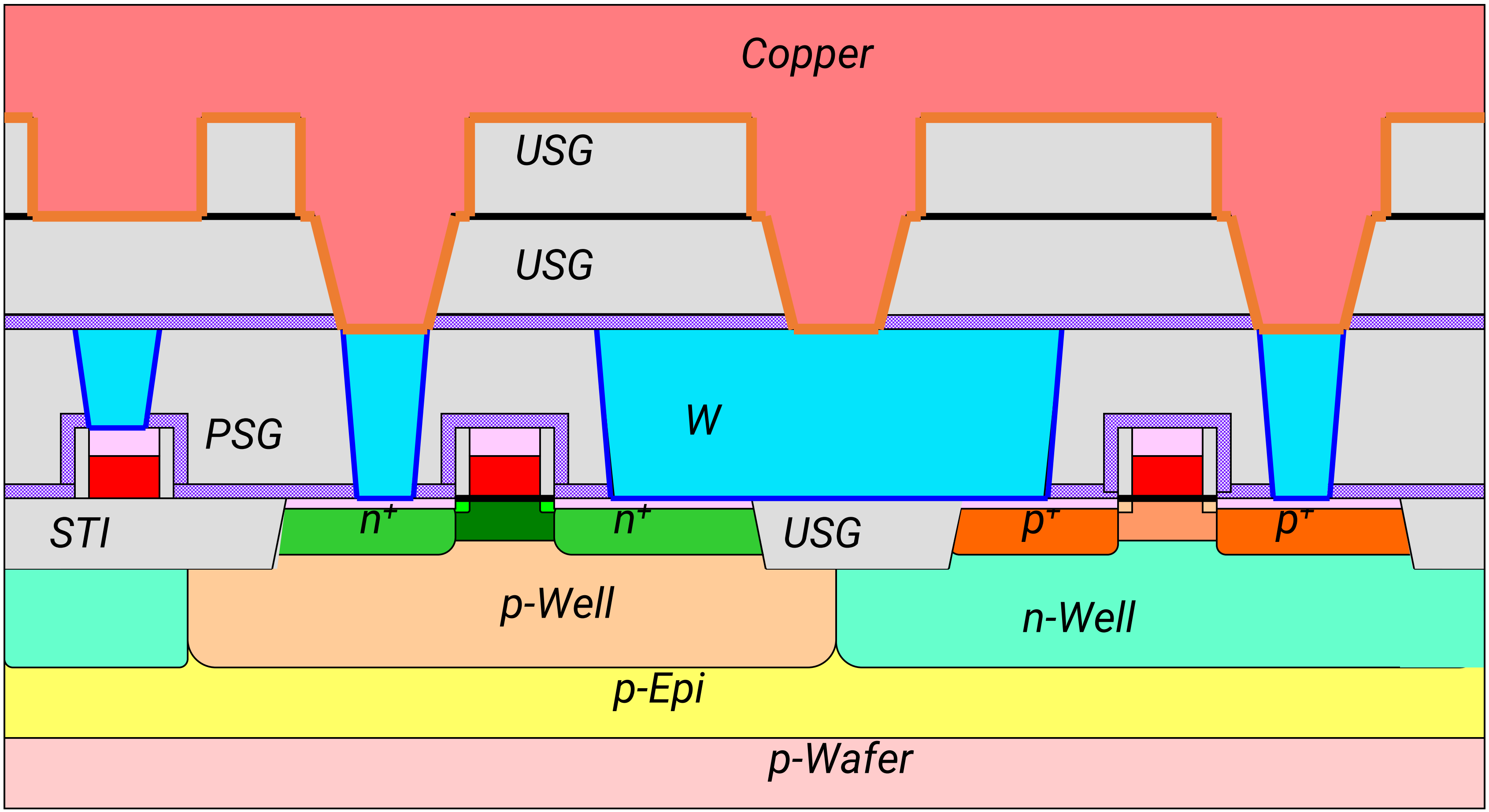
Deposit Barrier/Liner Layer(s) + Seed Layer

e.g. TaN / Ta / Cu

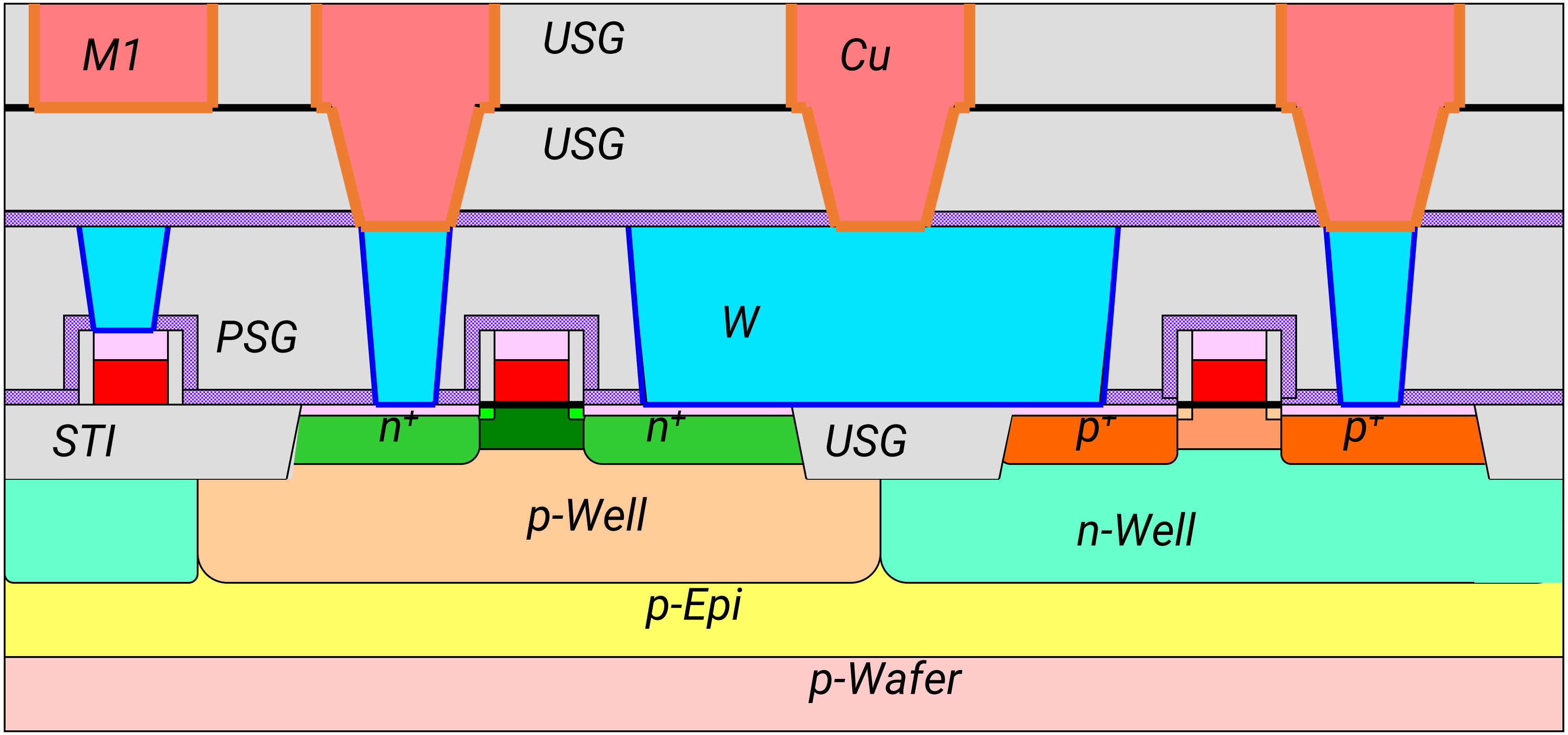
(Ionized sputtering of TaN/Ta and long throw sputtering of Cu)



Deposit Copper (ECD)



CMP Copper and Ta/TaN



PECVD Seal Nitride (SiN as dielectric diffusion barrier)