3D-integration

→ Motivation for 3D-integration?

What is 3D-integration?

3D integration implies any stacking of integrated devices (ICs, MEMS and their vertical Mechanical and Electrical connection.

• Motivation 3D-integration

① To Raise Integration Density
② To Increase performance
③ To Enhance functionality
④ To Reduce power Consumption
⑤ Minimize volume and weight
⑥ Mixed technologies: 3D SoC

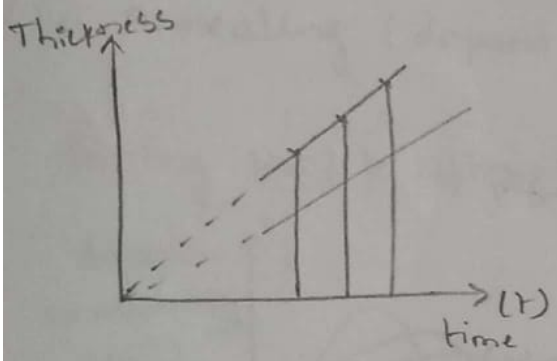
3D System integration

① Stacked Packages ② Stacked chips
③ VSI (Vertical System integration)
↳ Stacking of wafers → limits of wafer-wafer stacking technology
① Lower yield products
② Mixed technologies (different chip size)
↳ Chip-to-wafer Stacking

Fabrication of "TSV" (Through Silicon (Hole) Via)"

CVD
hemical vapour deposition)

1) Continuous process



2) Less Reactive (prevent gas Phase Rxns)

3) By time we can control thick ness (Thickness control)

4) Uniformity control:- Homogeneous temperature (T) + Gas Concentration (Partial Pressure)

5) Application in CMOS

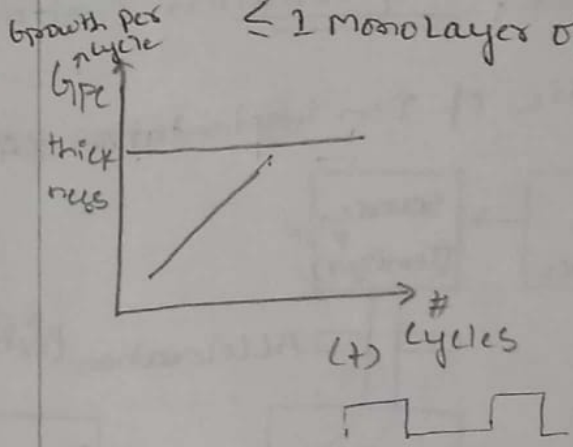
6) Interconnect System
Horizontal lines:- Cu/Al
vertical lines:- W, Cu

7) S/D/G → Silicide contact

ALD
(Atomic Layer deposition)

1) Cyclic process (4-step process)
(Atomic Layers)

Precursor - 1 Molecule
↓
Layer-1
↓
Precursor-2/ Reaction
↓
≤ 1 Monolayer of film



2) Can be Highly Reactive

3) No. of cycles controls Thickness (Thickness control)

4) Uniformity control:- Homogeneous density of adsorption site at the wafer surface (-OH groups)

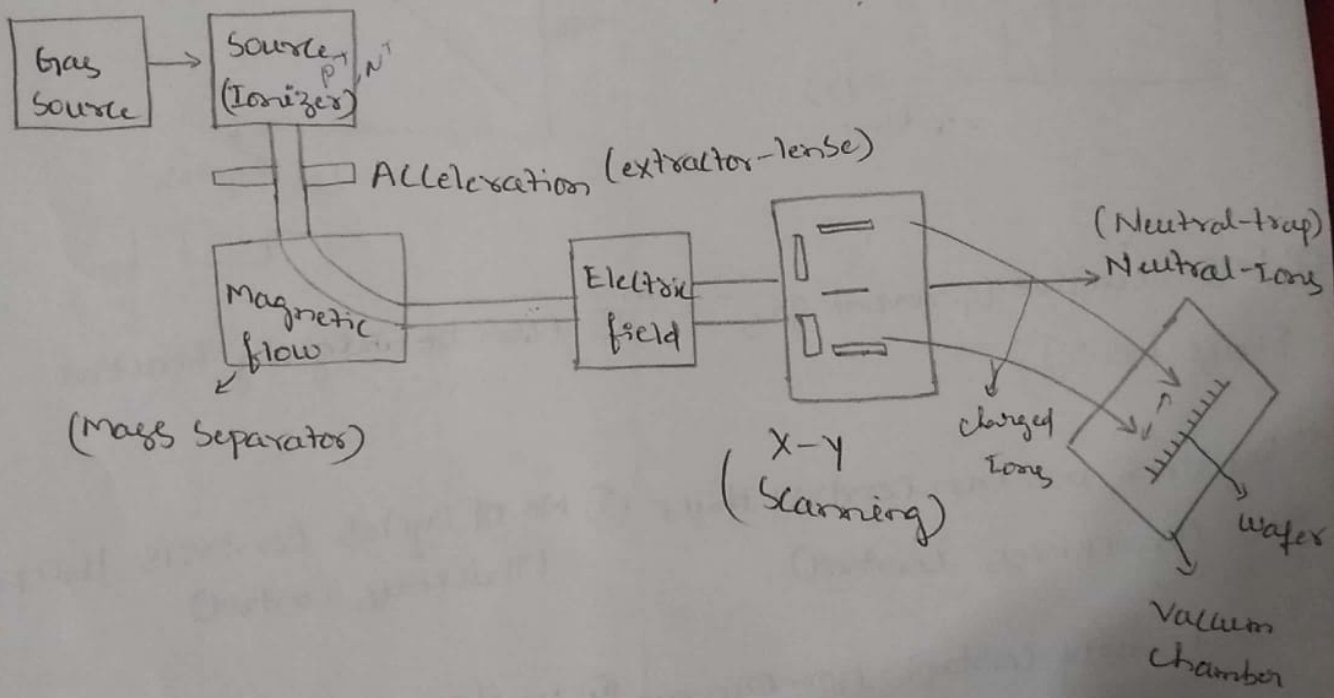
5) Application in CMOS

6) High K-dielectric (HfO_x, ZrO_x)
(Capacitor application)
(Gate oxide, Gate dielectric) 7)
↳ Capacitor dielectric $C = \epsilon_0 \epsilon_r \frac{A}{d}$

CVD	ALD
Passivation layer Si_3N_4	Conductive Diffusion-barrier → (Ti, Metal)
Gate electrode	(Copper Dual Damascene, W-Contacts)
Side wall Spacer	Seed layer - Cu (Copper) (Metals)
Shallow trench Isolation	Capacitor electrodes

Ion - Implantation

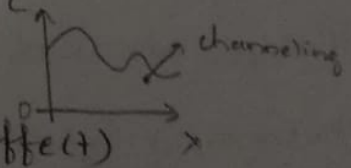
Schematic of Ion implantation equipment?



Process Steps for doping using Ion-implantation

Process Steps

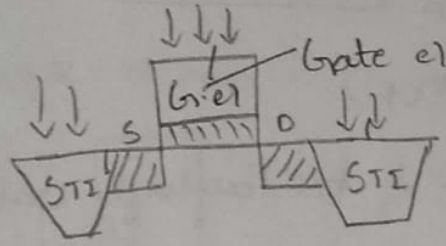
① Scattering oxide (to prevent channeling effect)



Channeling effect → Ions Hit Lattice planes of Single Crystalline Can not reach the bottom of surface)

asking Layers (SiO_2 - STI)

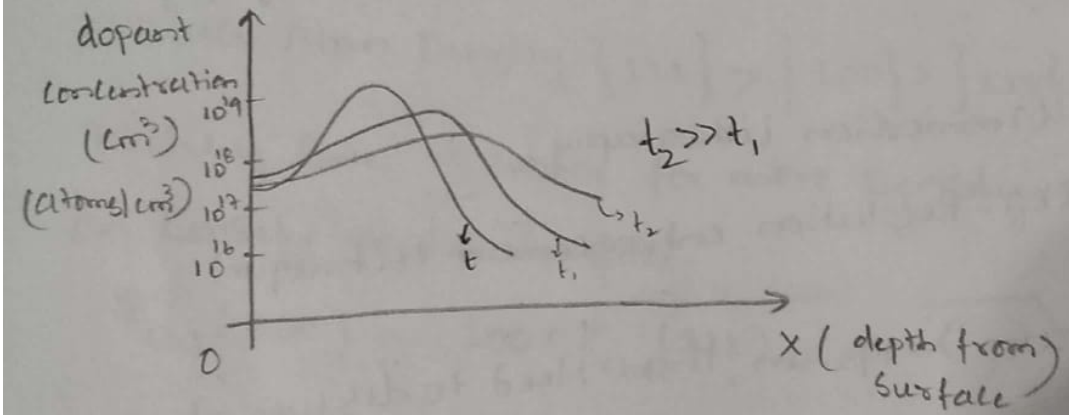
(Gate oxide + poly) . PR (Photoresist) → Masking other transistor



③ Ion Implantation

④ Annealing (dopant activation)

doping Profile after Ion implantation ?



dopant Activation Anneals ?

① furnace Anneal → (30 - 120) minutes

② Rapid thermal Annealing (RTA) → (10 - 60) Seconds

③ Flash Lamp Annealing (FLA) → (milli-Seconds) (ms)

④ Laser Annealing (μs)

Lithography

Resolution limit :- $l_{min} = K_1 \cdot \frac{\lambda}{NA}$ resolution = R

depth of focus $= Z = \pm K_2 \frac{\lambda}{(NA)^2} = (DOF)$

$K_2 - \frac{1}{2}$ for Rayleigh criterion

Discuss the option for Increased Resolution (lowering minimum exposable feature size) by using eqn for l_{min}?

$l_{min} = K_1 \cdot \frac{\lambda}{N.A}$ → $N.A = n \sin\theta$

↓

1.4 → Immersion Lithography

(a) Reduce λ

(b) Increase NA (Immersion Lithography)

(c) Reduce K_1 (RET - Resolution enhancement technique)

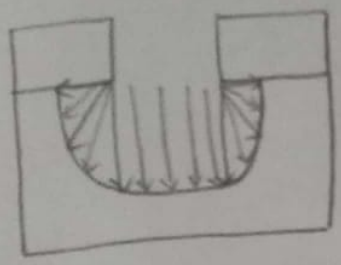
if given for certain 'λ' = 193 nm, then Need to discuss about NA, K_1

RET (Resolution enhancement technique)

1. Optical proximity correction (OPC)
2. Off Axis illumination (OAI)
3. Phase shift Mask (PSM)
4. Double exposure

Draw an Ideal Isotropic / Anisotropic etching profile?

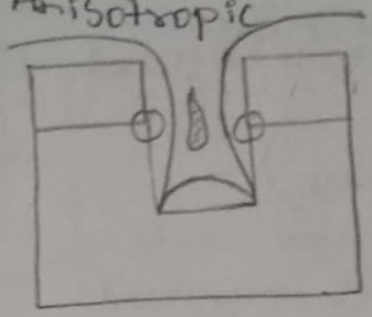
Isotropic etching



$\gamma_v = \gamma_h$

Vertical etch Rate = Horizontal etch Rate

Anisotropic



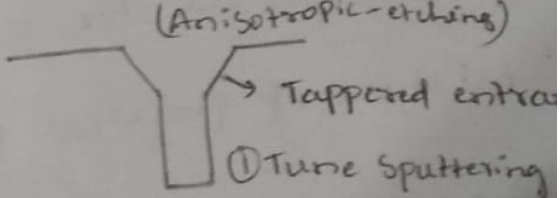
$\gamma_v >> \gamma_h$ $\quad \gamma_h \approx 0$

Vertical etch Rate >> Horizontal etch Rate

Surface Atom Density $\{111\} > \{100\} > \{110\}$

Etching Rate is lower for more Densely packed Surface than on Loosely packed Surface.

$R_{etch}(100) \sim 100 \times R_{etch}(111)$



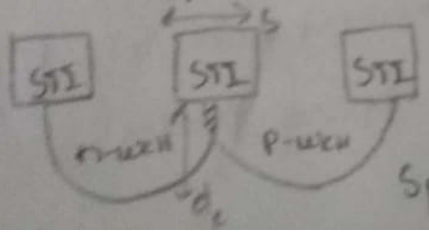
Isotropic etching → Chemical etching

but if we have different Lattice Plane then leads to different etching profile.

Aspect Ratio (AR) $= \frac{d}{w} = \frac{\gamma_{(v)}}{\gamma_{(h)}}$

Anisotropic etching best opt for CMOS application

Isotropic etching Not best for CMOS application (MEMS-best)



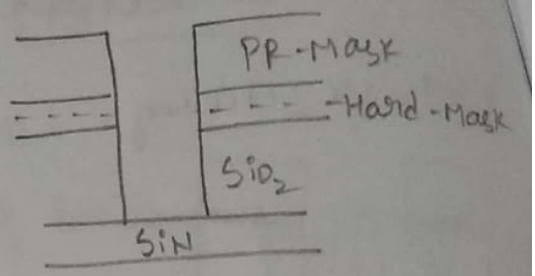
$d_e = \frac{S}{2}$

Spacing between

Definition for etch Selectivity & where it is important?

$$S_{on} = \frac{\gamma_{\text{top material}\,(\text{PR / Mask / Hard-Mask})}}{\gamma_{\text{material to be etched}}}$$

Selectivity of material



$$\left(\gamma_{mat} >> \gamma_{mask}\right)$$

Etch Selectivity is important

Etch Rate of material > Etch Rate of under layer

$$S_{\text{etch stop}} = \frac{\gamma_{\text{mat. to etched}}}{\gamma_{\text{underlayer}}} \qquad \gamma_{mat} >> \gamma_{under}$$

↑
ESL (Etch Stop - layer)

Name one process for (A) physical etching (B) chemical etching (C) mixture of physical & chemical

Physical etching :→ Ion-Beam etching (IBE) [ē-beam scan over surface

Sputter-etching [Plasma]

Anisotropic →

$$Ar \rightleftharpoons Ar^{+} + \bar{e}$$

Chemical etching :- Barrel-etching → Isotropic etching

(To Remove complete film
Stripping process

Reactive Radicals:

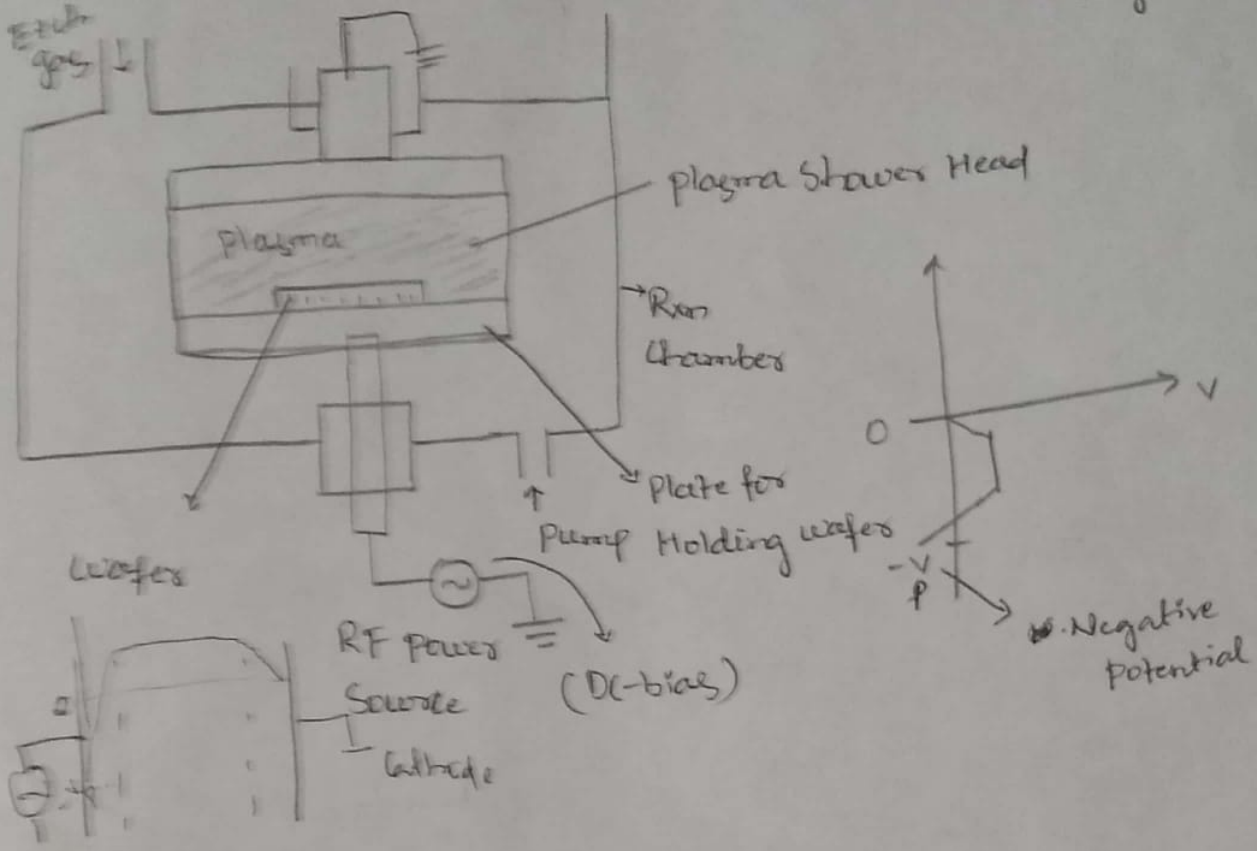
$$CF_4 \rightleftharpoons CF_3^{\circledast} + F^{\circledast}$$

Dangling

xture of physical & chemical etching

(Reactive Ion etching) - RIE

Rotating Magnetic field → To increase plasma density



→ CMP (Chemical Mechanical polishing)

Definition :

CMP :- Chemical enhanced Mechanical grinding

or

Mechanical enhanced Chemical grinding

etching

Consumables :

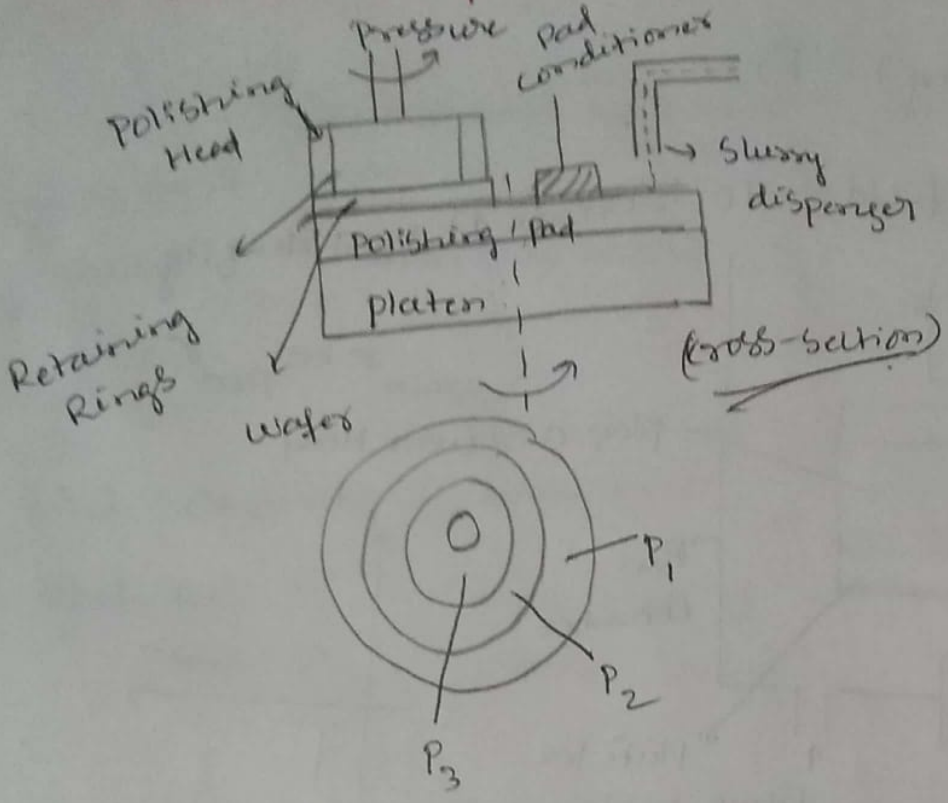
1) Slurry :- (Liquid + Solid Nano particles)

(Chemical Suspension Acidic Soln, Alkaline Solution)

2) Pads

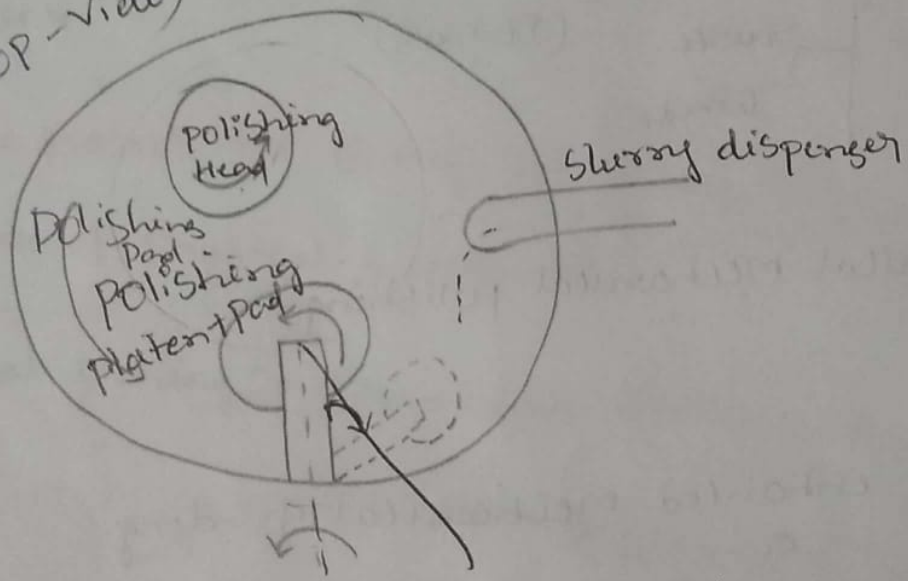
3) Pad conditioner (to get equal amount for all wafers)

Cross section and top view of CMP tool:



(Top-view of CMP tool)

(top-view)



Gas phase / vapour phase deposition process

Process	Materials	Application in CMOS	Process modules
CVD (to deposit thin films)	Metals :→ W, Cu, Al	Interconnect System Horizontal lines :→ Cu, Al Vertical lines :→ W, Cu Contacts :→ W	formation VX/
	Co, Ti	Ti → in contacts/vias W/W-adhesion + Lower contact Resistance (R_c) ↓ Co → Selective via fill in copper dual damascene	contact formation
		$TiSi_2$ → Silicides source-Drain-gate metallization	
	Poly Crystalline Silicon	Gate electrode (Local Interconnect -CI	Gate Structure
	Amorphous Silicon (a-Si)	Anti Reflective coating for doing Lithography	
	Insulators :→ SiO_2	dielectric STI (Shallow trench Isolation)	STI
		gate oxide	

Process	Materials	Application in CMOS	Process modules
CVD	Insulators:- SiO_2	PMD - pre Metal dielectric (doped)	
		Side wall Spacer	
	Low K - dielectric SiCOH	ILD, IMD - Inter level dielectric Inter Metal dielectric	
	SiC, Si_3N_4, SiCN	Isolating diffusion barrier	
		ESL (Etch Stop layer)	
		CMP Stop layer	
		Hard mask - Si_3N_4	
		Si_3N_4 - Passivation layer	
	Metal Nitrides:-		
	WN	Conductive diffusion barrier	
	TiN	Hard Mask (HM)	Vx/Mx
	TaN	Liner Material	
		Adhesion (↑) Increases and Electromigration Resistance (↑) Increases	

phase / Gas phase deposition process

Process	Materials	Application in CMOS	Process Modules
Epitaxy to make single crystalline on top	Si SiGe, GaAs, GaN	CMOS p⁻ level Optical devices	STI STI
PVD (Sputtering) (Evaporation)	Metals:- Al, W, Cu Ti, Co, Pt, Ni Metal Nitride:- WN, TiN, AlN	Al → lines Cu → Seed Layer for ECD Local interconnect Silicides of Metal on S/D/G Self aligned Silicides ↳ Contact formation Conductive diffusion barrier Liner	Contact formation Metallization
ALD 2 chemical precursor subclass of CVD	High K – dielectric:- Al_2O_3, HfO_x, ZrO_x Metal Nitrides:- TiN, WCN, TaN Metals:- Cu, Co, Ni	Gate oxide, capacitor dielectric diffusion barrier, liner Copper Seed Layer for ECD	Gate Structure √X/MX

Liquid phase deposition process :-

Process	Materials	Applications in CMOS	Process Modules
Spin-on	SiO_2 (Spin-on-Glass) Low-k-dielectric (MSQ → SiCOH) Photoresist Polymers (Carbon)	Isolation → Aluminium interconnect → Passivation Planarization → Local interconnect (Via x / Metal x) Mask Layer for pattern transfer (Etching) for selective doping (Ion-implantation) BE (Back-end) / Packaging Low k-interconnect, but High CTE	All modules LDD, S/D, Doping
ECD / ECP Electro chemical plating / deposition	Cu (Copper) Ni Au	FEOL (Front end of line) Metallization BEOL - Interconnect System Lines, Vias → Cu Dual Damascene → Cu Single Damascene	Via x / Metal - x
Electroless (EL) Plating / deposition	CO(W, P) / NiMoB ↓ not. Copper (Cu)	improvement of Electromigration Resistance of Cu-lines Copper Seed layer for ECD	