4) Define the term 3-D integration (3) what's the motivation use 3-D integration technology? (3)

→ 3-D integration implies stacking of integrated devices (ICs, moms) and their vertical mechanical and electrical connection. In order to

i) increase integration density
ii) increase performance
iii) more functionality
iv) Reduced power consumption
v) minimum volume and weight
vi) Mixed technologies : 3D SoC (14)

5) Please name the components of a copper plating bath for electro chemical deposition and their meaning / function which types of anodes can be used in electro chemical deposition?

Basic components	chemical basis	meaning
copper sulphate	metal salt	→ provision of cupric acid.
sulphuric Acid	Acid	→ Increase in conductivity

Additives:

Chlorine - Halogen - weak inhabitation of deposition necessary for operation of other additives

Carriers (suppressor) - Polyether - Inhibition of deposit, uniformity of deposite

Brighteners (Accelerator) - organic sulpher compound - Acceleration of deposition bright deposits.

leveler - organic nitrogen compound - Strong inhibition of deposition
Smooth surfaces
Strong grain refiner

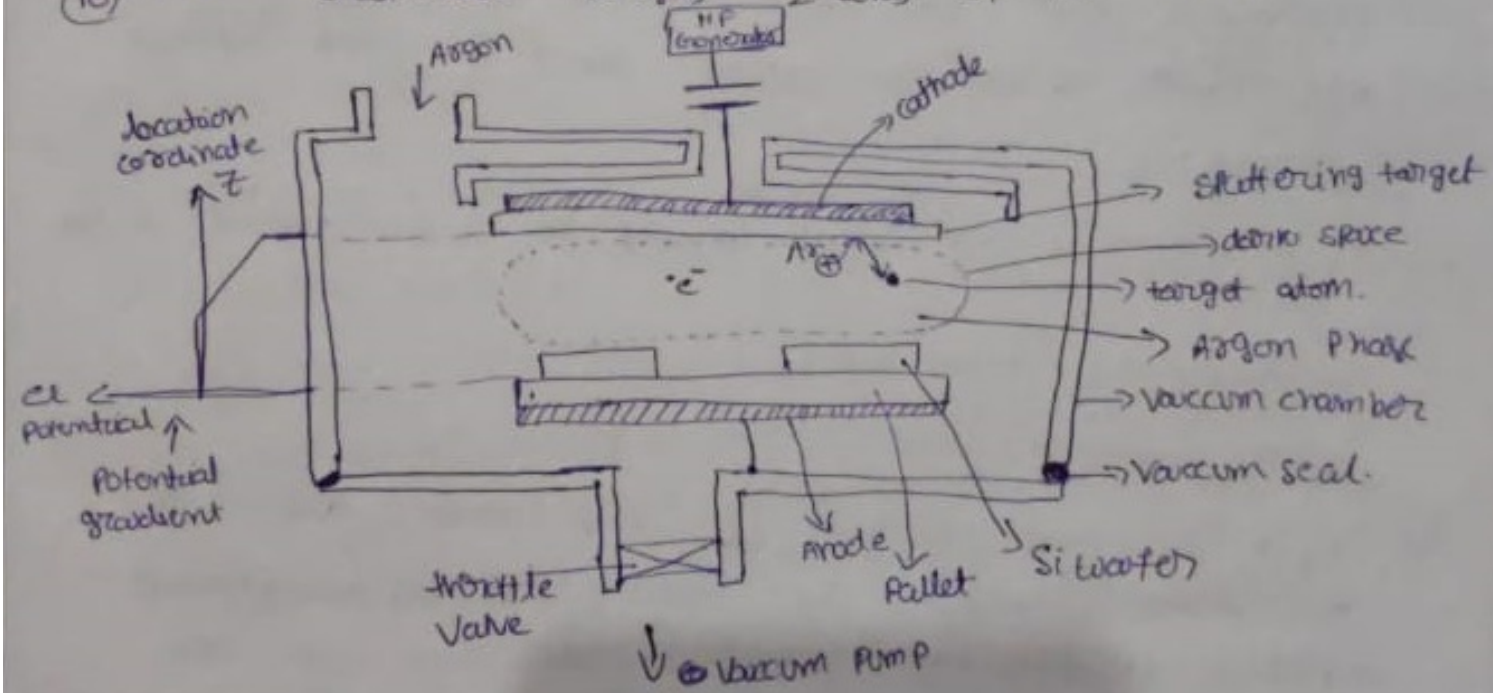
Objectives: (2)

→ High degree of dopant activation

→ Achievement of superior crystal properties

Method	process temp	process time	Boardening of ... during process time at T = 1100°C
Furnace	900-1100°C	min. hour	1 µm (1000s)
Rapid thermal Process	1000-1250°C	Seconds	0.1 µm (10s)
Flash lamp	1000 - 1300°C	milli seconds	0.01 µm (0.01s)
Laser	1100 - 1400°C	micro seconds	< 0.01 µm (0.01s)

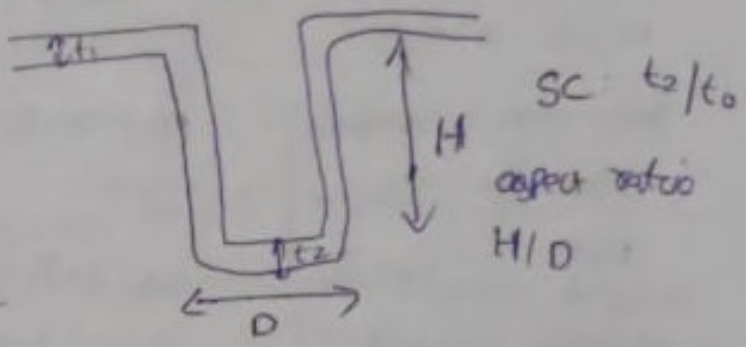
10) Draw a schematic cross-section of RF Sputtering tool name / mark the different parts. Please draw (10) the electrical Versus z-axis of the reactor.



③

11) Please define the term step coverage by a schematic and the respective equation for calculation. (6)
Please name three approaches for advanced sputtering technique to improve the step coverage of sputtering process and briefly describe, how the improvement is achived?

Step coverage: The ratio of thickness of film along the walls of a step to the thickness of the film at the bottom of a step



Advance tech:

→ ionized metal deposition
→ collimated sputtering
→ long throw sputtering

12) Please name the process steps in the technology flow of a through silicon/ Hole via fabrication and front side metallization. (5)

→ Via-1 / metal-1 formation
" 2 / " 2 "
" 3 / " 3 "
" 4 / " 4 "

→ bond pad metal & passivation
→ parametric testing

→ shallow trench isolation
→ twin well formation
→ Gate structure
→ lightly doped drain implants
→ side wall spacer
→ source / Drain implants
→ contact formation
→ local interconnect

13) which two basic metallization process sequence do exit for fabrication of interconnect system? name the conductor materials used in each of them for the and line, respectively. (6)

7) compare the deposition processes for potential conductive diffusion barriers in general (not specially for Cu) by naming their processes, their advantages/disadvantages for each processes one example of a material and its application within the respective process module?

Deposition techniques for barriers	Advantages	disadvantages
PVD Physical Vapour deposition → industrial standard: Ta and TaN for Cu metalization	→ low deposition T → good control of barrier composition	→ low step coverage
CVD chemical Vapour deposition → industrial Standard: TiN (e.g for W-CVD)	→ Good process control → high step coverage	→ partly high deposition temp → partly use of toxic reactants → risk of particle formation using NH_3
→ ALD Research focus: different material (TiN, WCN, TaN and others)	→ Potential of 100% step coverage → very thin closed layers	→ nucleation strongly depends on surface state
→ Electroless catalytic plating → use as cap layer: CoWP for better interface Cu/CoP electromigration lifetime	→ selective → self aligned → no texturing step	→ cleaning step of the Cu and ILD surface → Activation step of Cu surface to improve catalytic nature.

(14)

what are requirements for conductive diffusion barriers in Cu interconnects?

(A) i) ultra thin, but nevertheless very stable
   i) high density / no or stuffed diffusion Paths
   ii) low defect level
   iii) Thermo dynamically stable
2) Good adhesion to under ground and Cu
3) low stress
4) low resistivity
   < (1000 -- 3000) μΩ cm.

(13) which two basic metalization Process sequence do exist for the fabrication of the interconnect system? name the conductor materials used in each of them for via & the line respectively

	Via	Line
Subtractive	W	Al
Dual Damascene	Cu	Cu

14) Describe the process flow of the Process module "shallow trench isolation – STI formation" by naming the basic process steps for it's realization! Enhance this by details of the processes and materials used in these basic process steps (9P)

Draw the cross-section of the CMOS structure in three different stages of this Process module to visualize the sequence! please mark the parts and fillings accordingly

Process modules:

i) STI Trench
ii) STI oxide Fill
iii) STI Formation

Anode types: (2)

→ soluble copper anode (provides cuprac ions)

→ non soluble inter anode (ions are added from external source)

8) Please name the goals of ion implantation (3) In which process modules ion implantation is applied in the cmos technology? (3) Describe the channeling effect and give the potential measures to prevent those effect (4) (10)

Goals: → Doping

→ modification of material properties

→ Stoichiometric implantation

Process modules (3) unipolar: source/drain formation, low doped drain, channel formation, well formation, channel stopper, silicide, interconnects, doping of polysi, Bipolar: Base formation Emitter formation,

Channeling effect: ions lose considerably less energy if they travel through the crystal along low index directions

To prevent:

→ inclination of ion beam against the surface normal of the wafer.

→ Amorphous cover layers

→ pre-amorphisation

9) what are the objectives of post-annealing after ion implantation? (2) Name the methods/ processes of annealing applied in different technology nodes and sort them by the extent of broadening of dopant profiles due to diffusion starting with lowest dopant broadening? (5)

(5)

what are the benefits of silicon on insulator technology relative to conventional silicon technology)

what does full depleted SOI (FD-SOI) technology mean)

please draw a schematic cross-section of transistor with planer FD-SOI device structure)

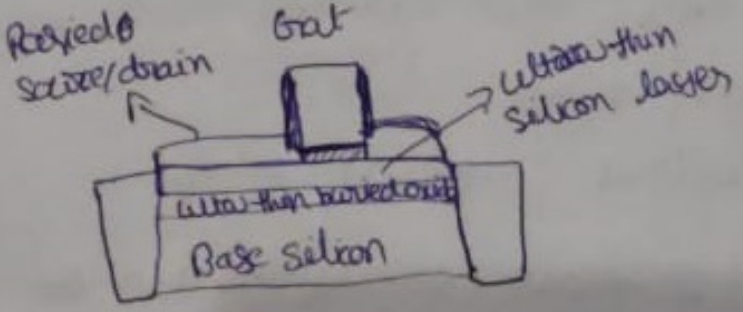
benefits:

→ lowers parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance.

→ Resistance to latchup due to complete isolation of n- and p- well structure.

SOI fully depleted Si transistors:

~~→ At 20nm~~ planer FD technology allows several methods for setting threshold voltage VT, including engineering the gate stack work function, trimming the gate length and other process engineering techniques. 28 FD SOI technology is capable of offering 3 VTs (HVT, RVT, LVT), as in traditional bulk CMOS technologies.



8) b) Unipolar technologies:

Source / drain formation.
Low doped drain
Channel formation
Well formation
Channel Stopper
Silicide
interconnects
Doping of Poly Si

Bipolar technologies.

Base formation
Emitter formation

→ At 20 nm node, short channel effect and random dopant fluctuations are major hurdles facing CMOS industry. (15)

→ An extremly alternative solution is planer, ultra thin body fully-depleted SOI transistor

→ These devices are built on an ultra-thin SOI substrate covering

→ an undoped channel. ~~material~~

→ drastically cutting short channel effects.

→ eliminate ROF issues

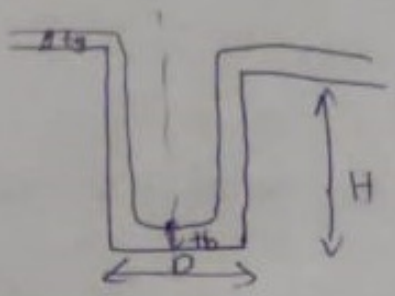
→ exhibiting excellent threshold voltage

planer FD technology allows several methods for setting threshold VT, including engineering the gate stack work function trimming the gate length and other process engineering techniques

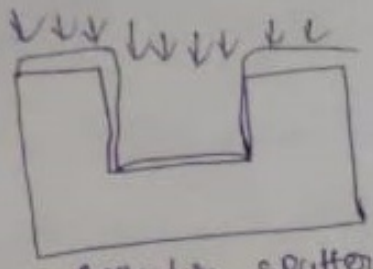
28FDSOI technology is capable of offering 3 VT's as in traditional bulk CMOS technology

e) Step coverage:

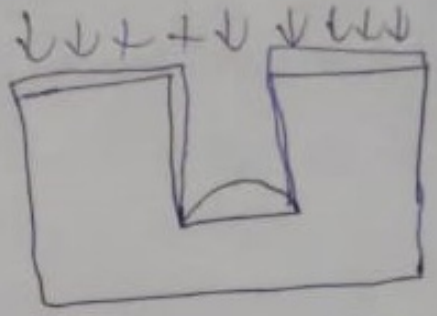
The ratio of thickness of a film along the walls of a step to the thickness of the film at the bottom of a step.



Aspect ratio : H/D
Step coverage : t_2/t_0



Regular sputtering deposition

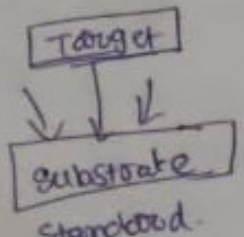


long throw sputter & collimated or ionized metal deposition

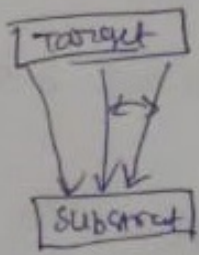
Advanced techniques:

(i) ionized metal deposition
ii) long-throw sputtering
iii) collimated sputtering

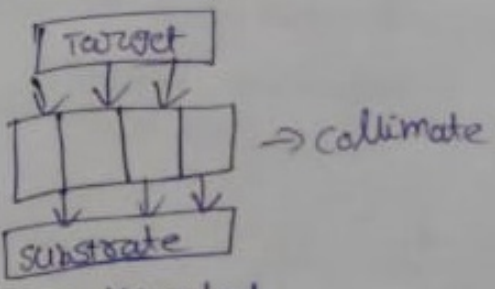
The goal is to coat high aspect ratio pattern more uniformly by more directional sputtering with narrow arrival angle distribution.



Standard



long-trough



collimated sputtering

Introduction to Microtechnologies

STI -> shallow trench isolation

-> silicon substrate is P^+, in order to create a conductive ground plane which ~~provides~~ establishes the ground zero reference voltage across the chip.

(1) A thin P^- layer (1) is epitaxially grown on top to reduce capacitance and also prevent cross-talk latch-up.

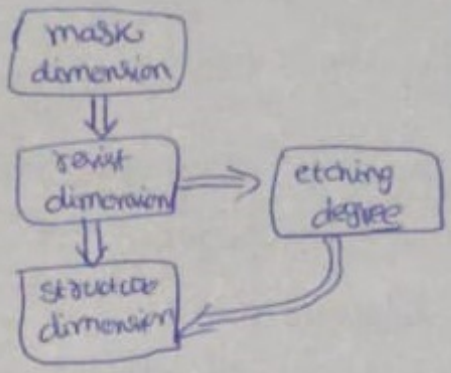
(2) A thin SiO_2 layer (Pad oxide, 15nm) is thermally grown to protect active areas from excessive damage during ion implantation and to control the depth distribution of dopants

(3) Upon the SiO_2, a layer Si_3N_4 is deposited by LPCVD typically ammonia and dichlorosilane are introduced at medium temp (750°C) and layer is about 150nm is formed. Si_3N_4 is a highly quality masking material incase of photoresist fails during trench etch. The trench etch step is highly step is highly energetic, and Si_3N_4 layer protect the areas where the devices will be formed. Further more Si_3N_4 layer used later as a CMP stop.

(4) photo resist is deposited and patterned (4) (1st mask)

(5) The plasma etching uses high intensity RF to ionize either flourine or chlorine based gases. The F or Cl ions reacts with the exposed Si_3N_4. SiO_2 and Silicon forming gaseous reaction products

Tolerance chain:



Bipolar technology:

1) insulating frame → disables parasitic currents b/w components
   pn-isolation → parasitic effects
   → capacities (voltage-dependent)
   → barrier saturation current = leakage current
   → voltage dependent stretching of RLZ
   → breakthrough

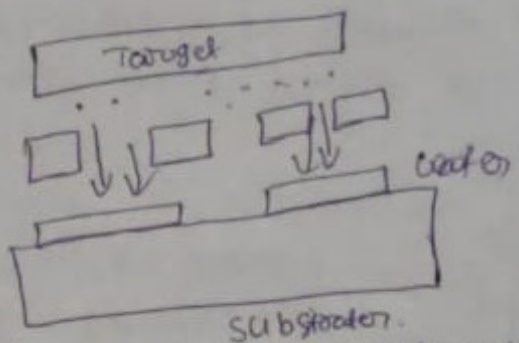
capacities at pn transitions:

→ diffusion capacity → injection of minorities → flow direction
→ depletion layer capacity → solid charge of atomic cores
→ plate capacitor model.

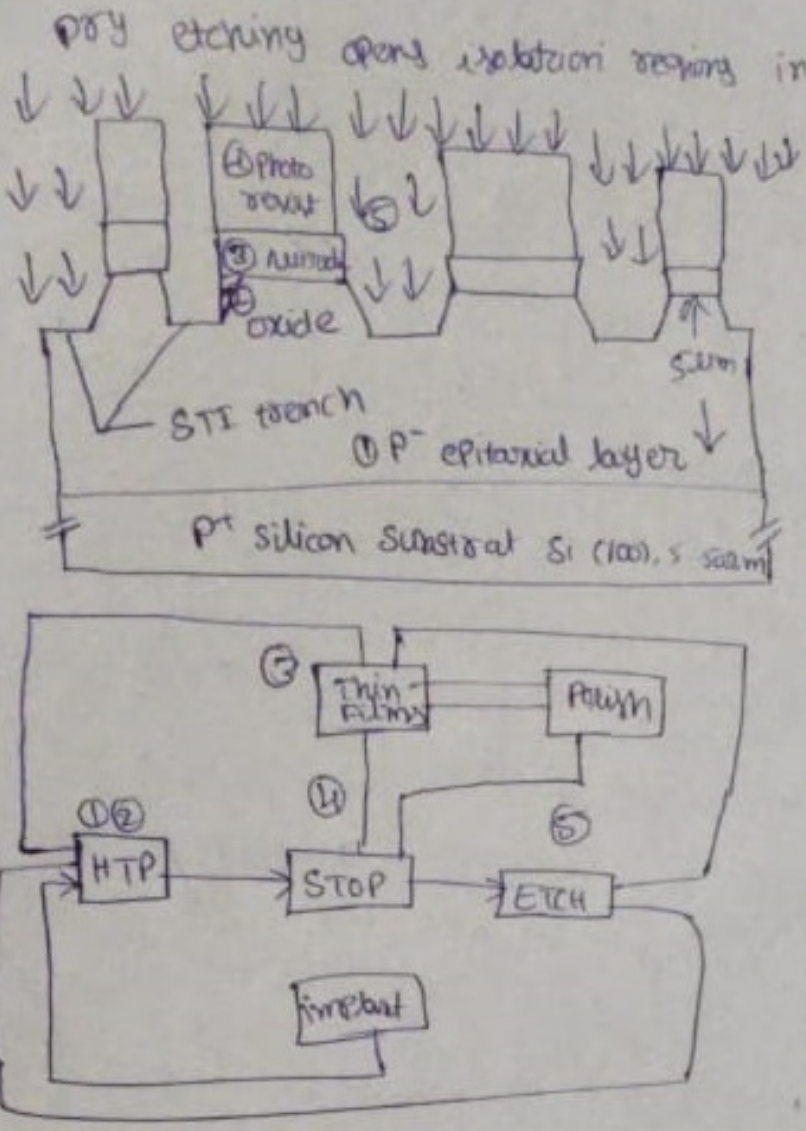
collimated sputtering:

→ insert a plate with high aspect ratio

→ sputter at low pressure, mean path is long enough that few collisions occurs b/w collimator and wafer.



→ species with velocities nearly ⊥ to wafer surface pass through the holes.
→ Reduced deposit rate continuously.

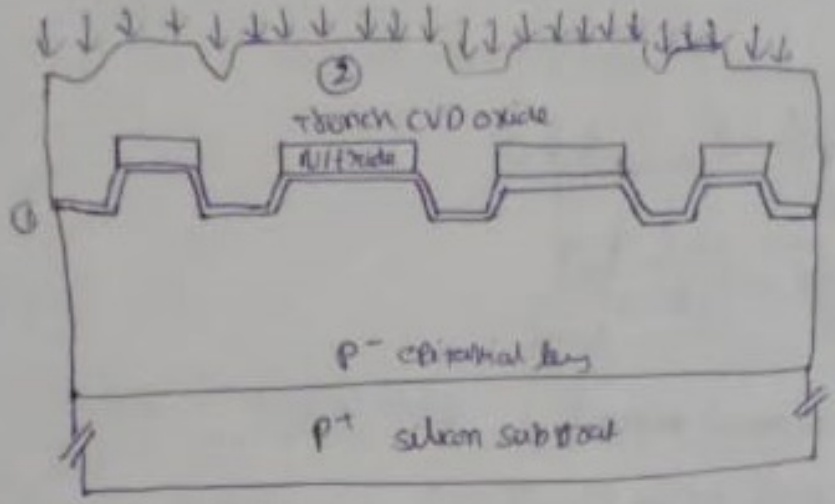


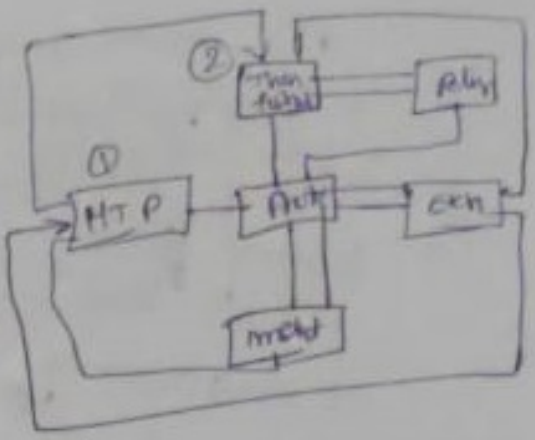
STI oxide fill:

1) Formation of about 15nm liner oxide in the trench by dry thermal oxidation at medium temperature (750°C) to improve the interface b/w silicon and trench CVD oxide

2) Next a thick layer of CVD oxide, is deposited, this layer will act primarily as a fill to the isolation trenches and similar to the "field oxide" in former LOCOS processes

Trench fill by chemical vapour deposition oxide

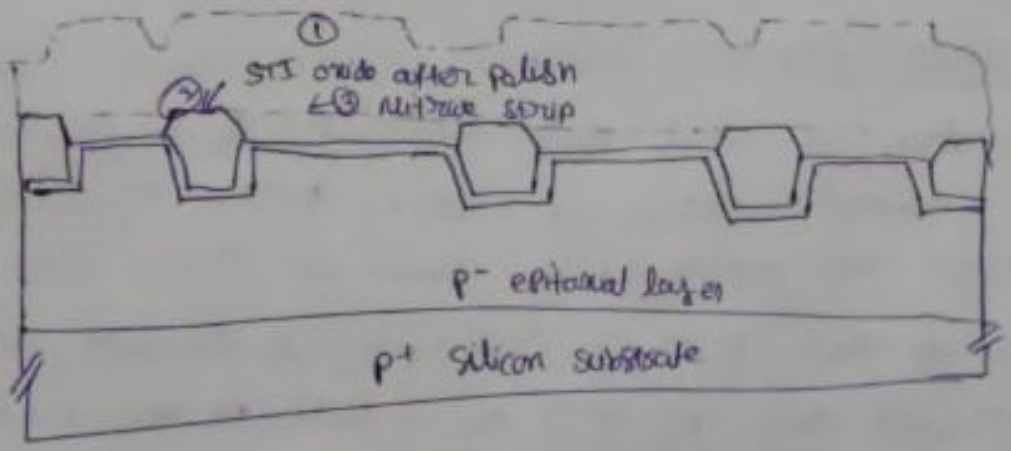


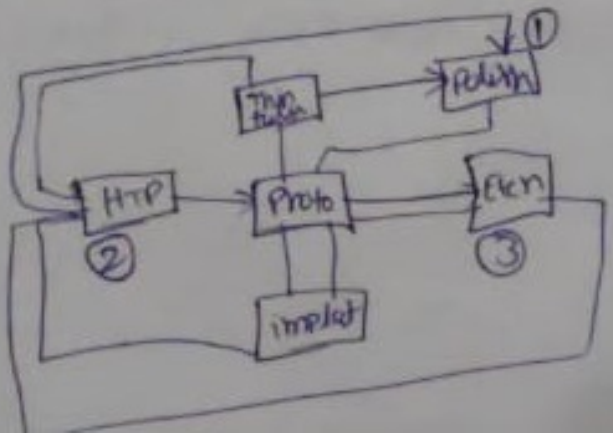


STI formation:

1) Trench oxide Polish Nitride acts as CMP stop layer.
2) Densification of STI oxide at 900°C
3) Nitride strip in hot (150 to 200°C) Phosphoric acid (H_3PO_4) Solution (high selectivity to silicon oxide)

Planarization by chemical-mechanical Polishing





ntrol of geometric dimensions

Design rule check (DRC)

→ The depiction of geometric figures of single mask levels can be achieved in different ways.

1) Bit map – depiction
   → all mask levels are scanned
   → every grid point stands for one bit.
      → geometric fig → bit is '1'
2) disassembling into rectangles:
   → addressing of corners for every geometric figure
3) Description of geometric figures as polygons
4) Description of edges

3 Topological Design rules:

→ influencial factors:

1) Depth resolution (wavelength, smallest structure dimen
2) mask transitions between transparent & opaque. (⇒ Phase Shift – mask)
3) Photoresist.
   → over and under exposure
   → diffused light.
4) development of photoresist.
5) image transfer to resist mask
6) Structuring
   → undercutting
   → under diffusion.
7) selective oxidation masking with Si_3N_4

AICT

1) Please explain term "equivalent scaling"? (2)

(A) Equivalent scaling (occurs in conjunction, with and a/o enables, continued geometrical scaling) refers to 3-D device structure ("Design factor") improvement plus other non-geometrical processes technique and new materials that effect the electrical performance of chip. Eg HKMG, ESC

2) Please name three equivalent scaling measures applied in inter connect system of IC's? (3)

A) 1) Gate stack
2) Electro Static control
3) channel material

(3)

3) Name three important trends in cmos technology?

A) i) production of many identical devices/ circuits/ chips by one process → cost

ii) characteristic quantities:

a) wafer diameter → Geometrical scaling
b) die size → degree of integration
c) no of transistor per die → performance increase
d) yield → increase of die size
→ cost reduces per function

iii) new & improved products
→ require continued increase of degree of integration
→ scaling down
→ Increases of die size