2 Microelectronics Technology

2.1 Definitions

Microelectronics

- The design, manufacture, and use of microchips and microcircuits [Oxford Dictionary].
- The technology for development and fabrication of electronic systems consisting of devices whose operation is based on the movement and storage of electrical charges.
- Comprises not only integrated semiconductor circuits, but also solid state devices having other modes of operation and their application in complex systems.

Microelectronics, Microsystems Technology (MEMS, MOEMS, …)
→ Microtechnologies

Interaction of materials, processes, equipment, technology

Scope of microelectronic products:

Memories	Processors	ASIC's	Power electronics	Microsystems

Innovations:

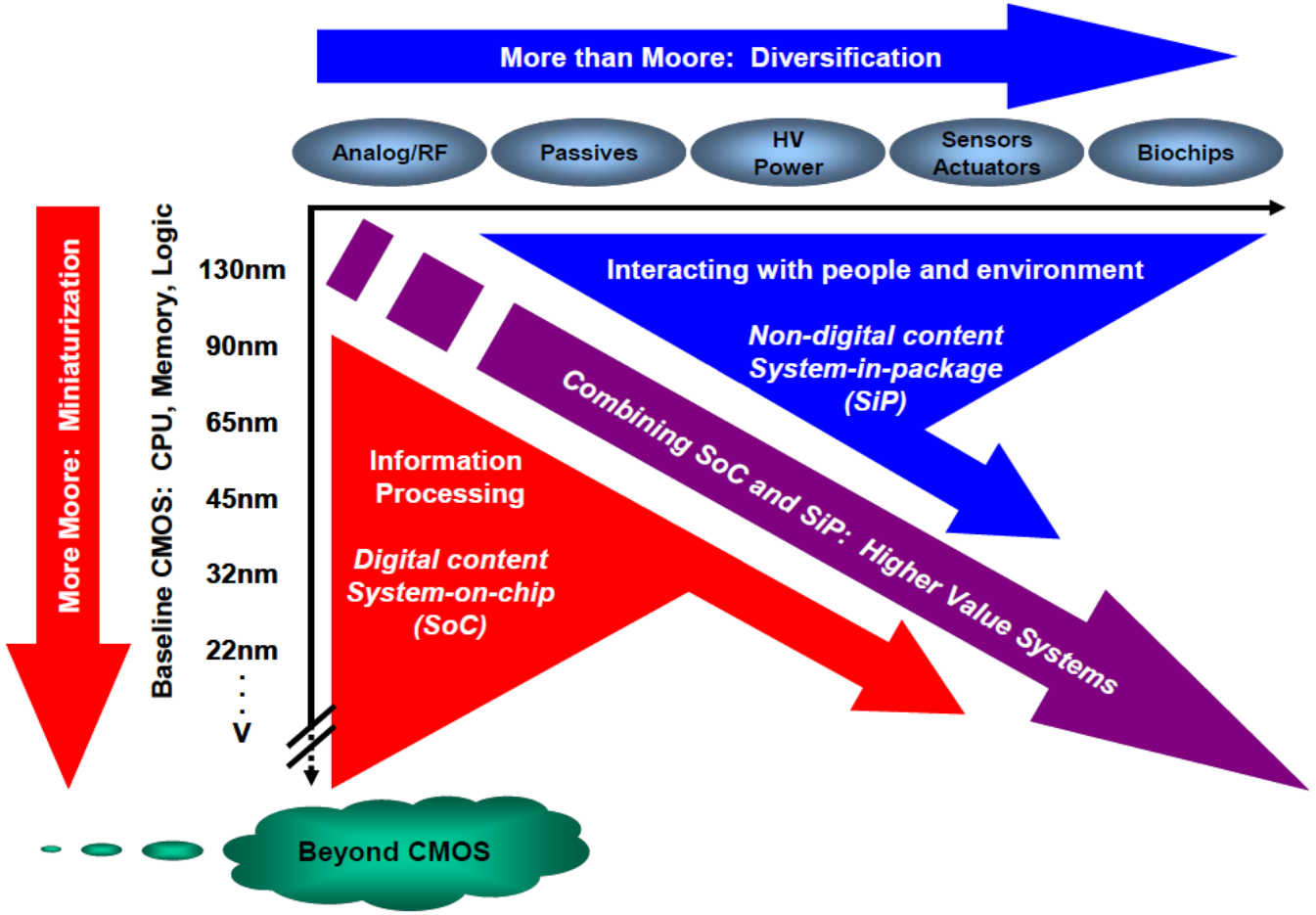
Technology driver	Architecture & design evolution	Algorithms	New technologies, Power engineering	Microtechnologies, special developments

Goals:

→ Scaling down
Decrease of all characteristic dimensions and structures
(e. g. channel length of MOS transistors)
More Moore

→ Systems (sensor, actuator) & combination with µE
(see special lecture courses)
More than Moore – Smart Systems

This lecture deals with processes and technologies which are applied in Micro and Nanoelectronics or have future application potential.



The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore").

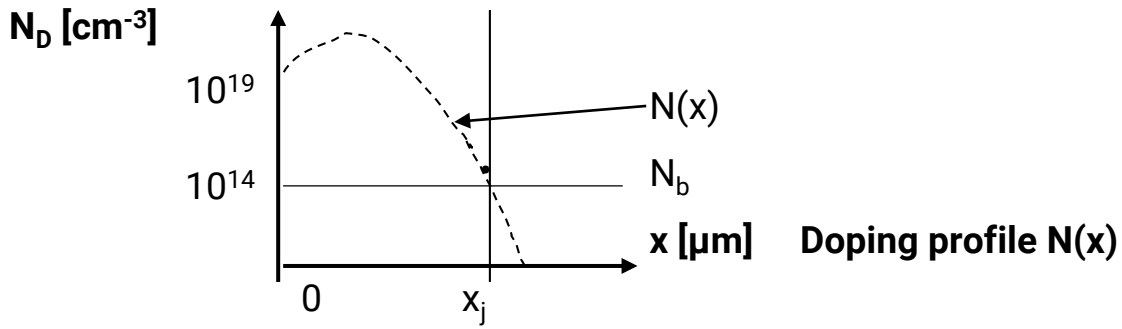
Terms

Basic process steps (BPS)

- indivisible step in the process flow
- characterized by physical / chemical parameters (temperature, pressure, gas composition...)
- e.g. special diffusion step (pre-deposition), implantation step, special cleaning step (rinsing)

Technology: ∑ **BPS**

Parameter: Special parameter determining device properties
example: Dopant concentration → resistance, depth of p-n-junction



Doping profile N(x)

Equipment: Tools for a specific process step
(e.g. implanter, PVD cluster tool, ...)

2.2 Processes / Basic Technologies

Process

- consists of one ore more BPS
- carried out by using of specific tools (equipment)
- standardized component of a technology
- results in achievement of a specific property
- e.g. doping (pre-deposition, drive in), photolithography (deposition of resist, exposure, development, ...)

Basic technology

Sum of processes (or BPS) to be performed for the fabrication of a specific product, e.g. CMOS, BICMOS, Bipolar, ...

Important:

Technology is characterized by the number of devices per chip and the critical (minimum) dimension of the device structure

Microelectronics:

- Silicon-based: Si wafer as the basic material,
  Trend: wafer diameter increases (200 mm→ 300 mm → 450 mm?)
- Other semiconductor materials (e.g. GaAs, SiC) with smaller wafer size (100, 150 mm)

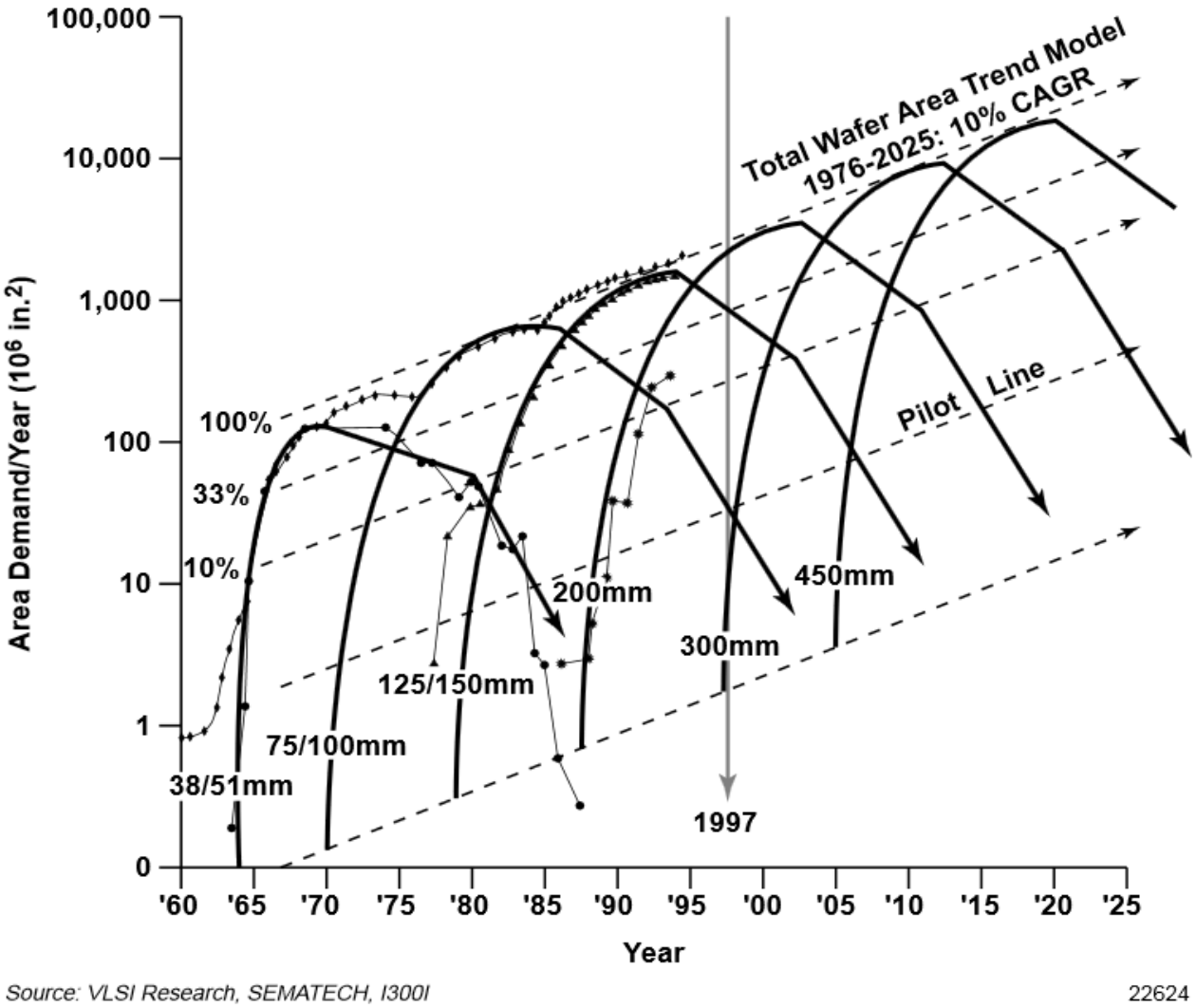


Figure 7-1. Lifecycles of Different Wafer Sizes

- History and forecast from 1997 point of view

<u>Status today (2020):</u>

- 450 mm did not enter production (yet?)
- 200 mm did not fase out as shown, but increased since ~2017/18 again

Overall Process

Phase 1: ***Preparation***

crystal pulling
mechanical treatment (diameter)
wafer fabrication: sawing, lapping, polishing

Phase 2: ***Wafer processing***
(Frontend – FE)

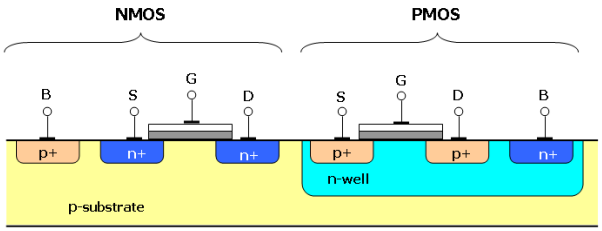
f(product,
basic technology)

∑ Basic process steps (BPS)

- BPS 1
- BPS 2
- ...incl. repetition (see lecture "Technologies for Micro and Nano Systems" and section 3.1 ... 3.9)

- BPS/processes often summarized in process modules (see chapter 5.1)

e.g. **CMOS:**



testing

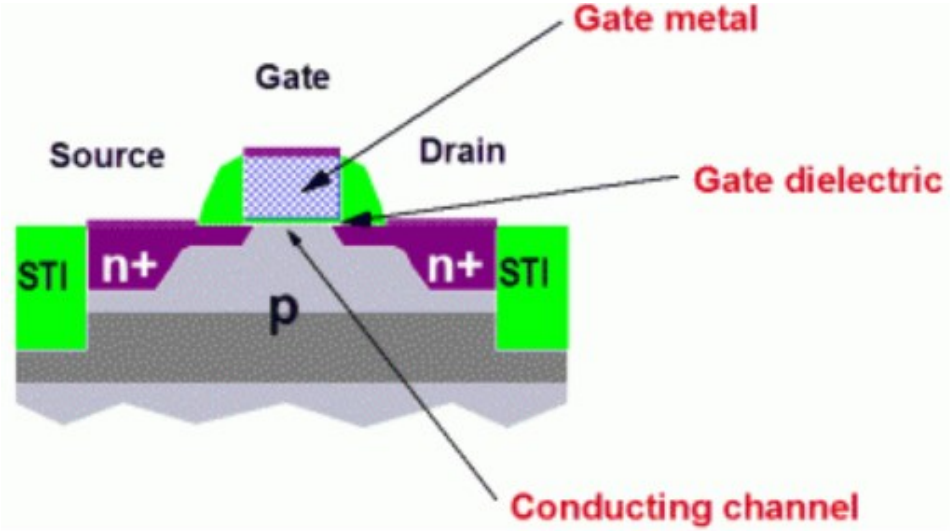
Phase 3: ***Packaging***
(Backend – BE)

die separation
mounting
bonding
encapsulation

2.3 Devices

MOS Transistor:

MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor
Basic device of MOS/CMOS Technology



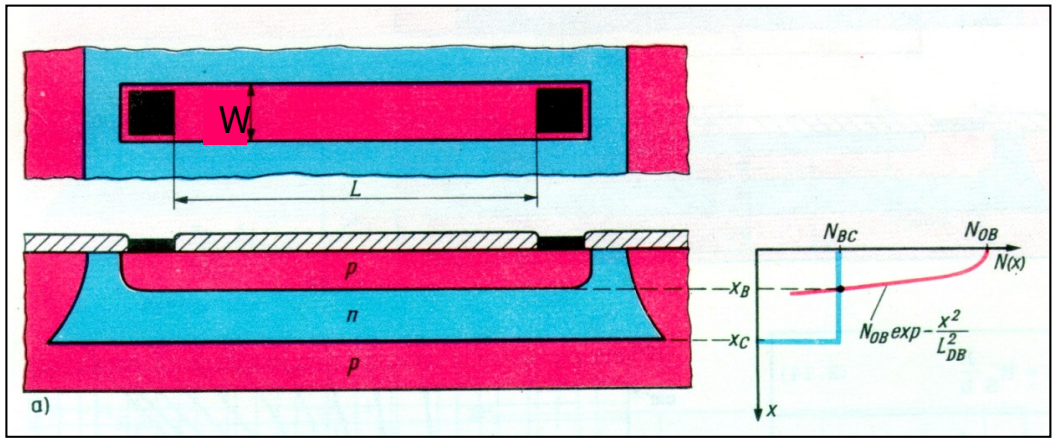
Depletion mode
→ Channel already exists at zero gate voltage. Control by depletion of majority carriers.

Enhancement mode
→ Self-blocking at zero gate voltage. Channel emerges due to enhancement of minority carriers until inversion.

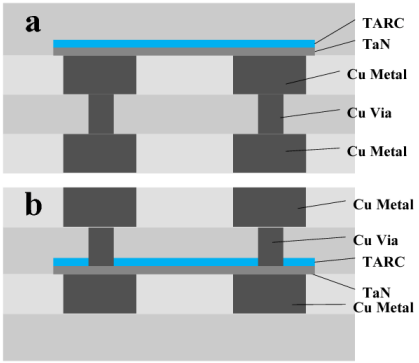
Resistor:

- Very high-resistance n-doped epitaxial layer → The low-resistance p doped layer (red) is formed by boron implantation and used as a resistor after contact formation.

$$R = \rho \cdot \frac{L}{x_j \cdot W}$$



- High resistance layers in BEOL (interconnects system), e.g. metal nitrides



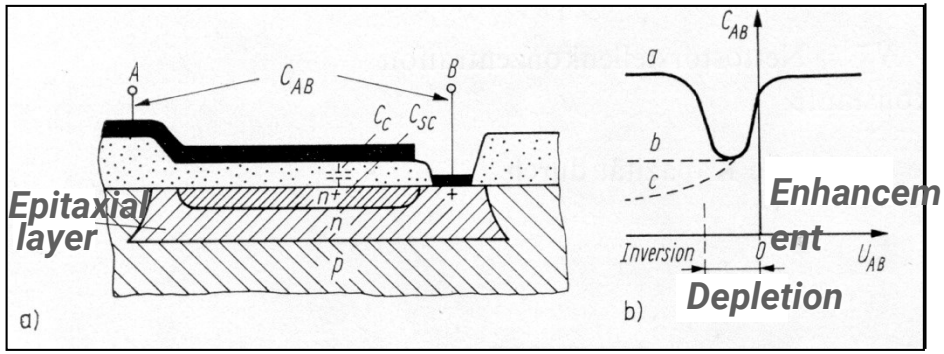
Capacitor:

$$C = \varepsilon_0 \varepsilon_r \cdot \frac{A}{d_{SiO2}} = \varepsilon_0 \varepsilon_r \cdot \frac{L \cdot W}{d_{SiO2}}$$

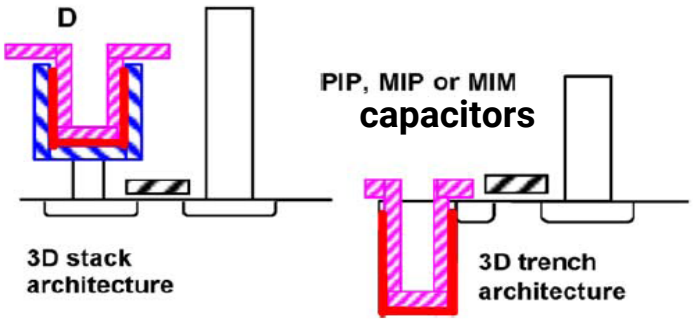
L, W = length, width of the area where the electrodes do overlap

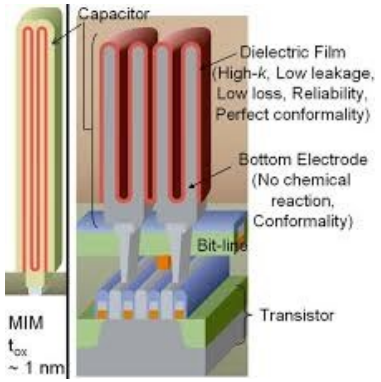
d_{SiO2} = thickness of SiO_2

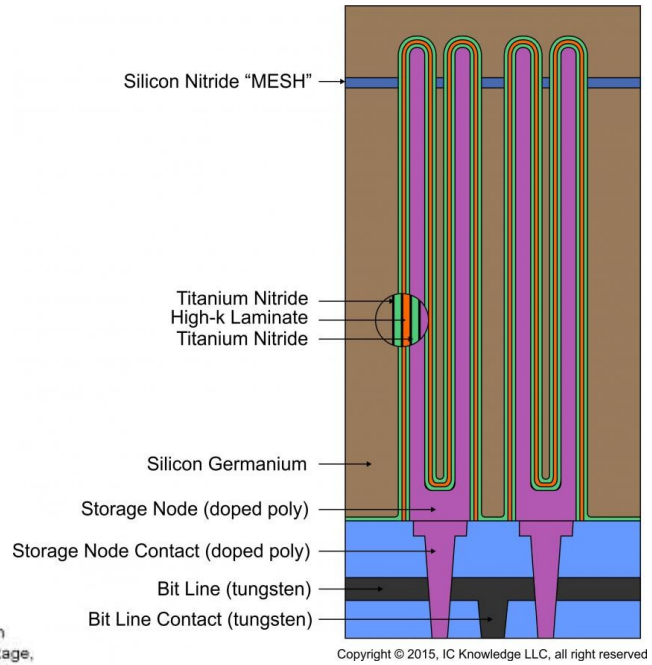
MOS capacitor



MIM (PIP, MIP) capacitor

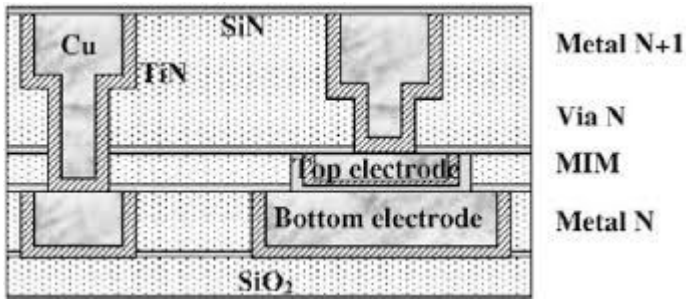


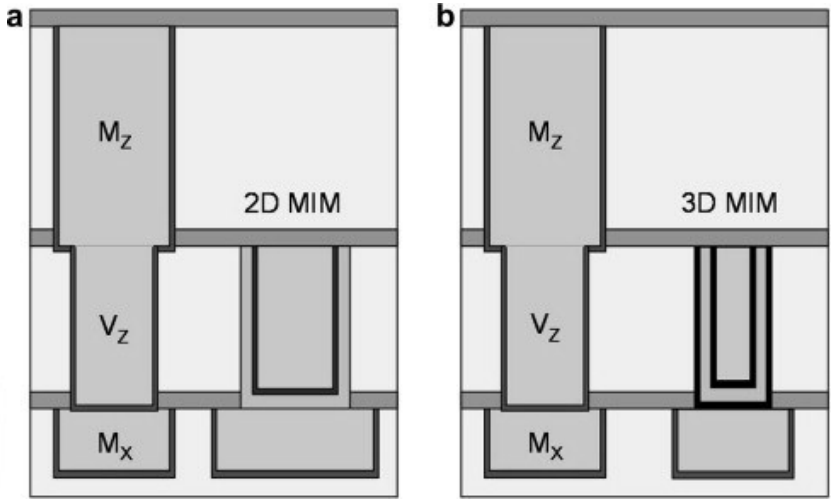




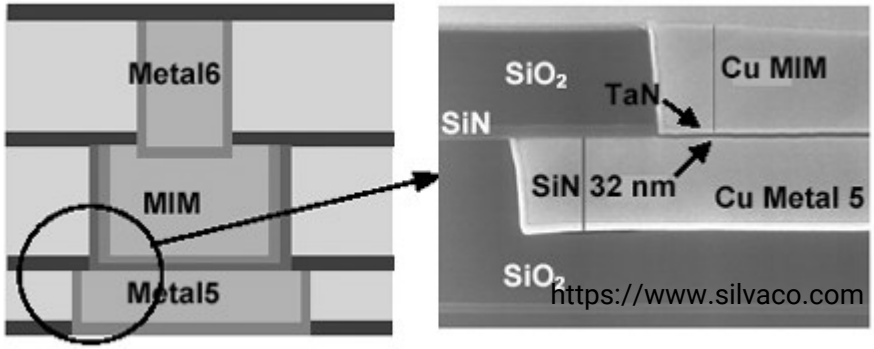
Capacitor:

BEOL integrated MIM capacitors (metal nitride electrodes & high-k dielectrics)



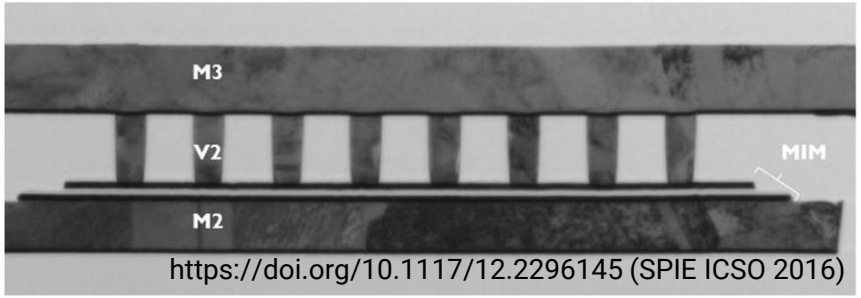


https://doi.org/10.1016/j.mee.2008.03.017



https://www.silvaco.com

MIM capacitor integrated between M2 and M3



https://doi.org/10.1117/12.2296145 (SPIE ICSO 2016)

2.4 Development Trends

- Production of many identical devices / circuits / chips by one process → cost !

- **Characteristic quantities:**
  - Wafer diameter (now: 300 mm)
  - Die size ca. 100 - 200 mm^2
  - Number of transistors per die (degree of integration)
  - Yield

- Main feature: **New and improved products (performance, reliability)**
  - Require the continued increase of degree of integration

→ scaling down (miniaturization of devices, decrease of lateral dimensions and layer thicknesses)
  - Increase of die size

Goal: equal or higher yield than in previous technology node

- **Trend:**

Year	Era	Critical dimension	Degree of integration
1968 ... 1972	MSI (Medium Scale Integration)	> 6 µm	~ 10^2
1972 ... 1981	LSI (Large Scale Integration)	2.5 ... 6 µm	~ 10^3
1981 ... 1989	VLSI (Very Large Scale Integration)	2.5 ... 1 µm	~ 10^5
since 1990	**ULSI** (Ultra Large Scale Integration)	< 1 µm	
since 2000		< 100 nm	≥ 10^8

Scaling ("More Moore")

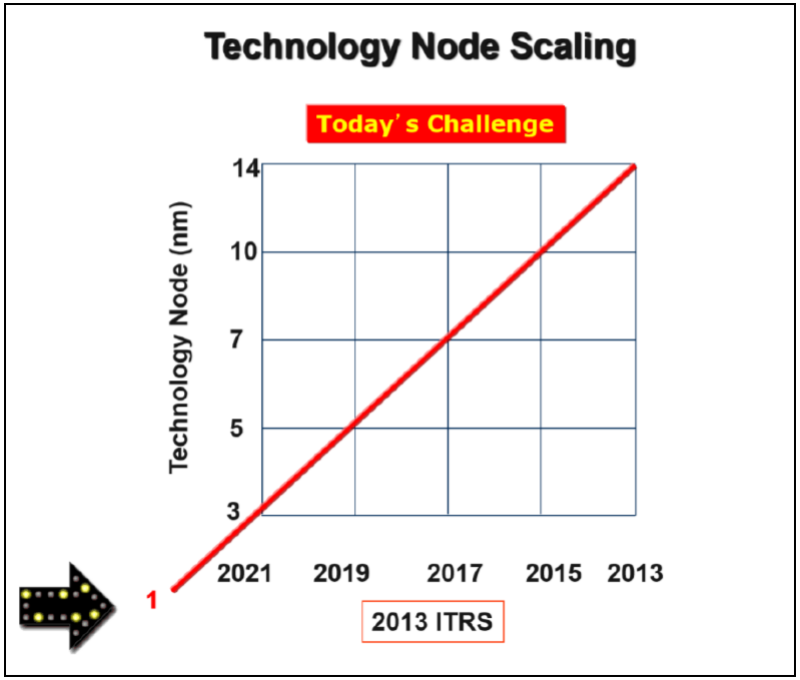
- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

- *Equivalent Scaling* (occurs in conjunction with, and also enables, continued geometrical scaling) refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

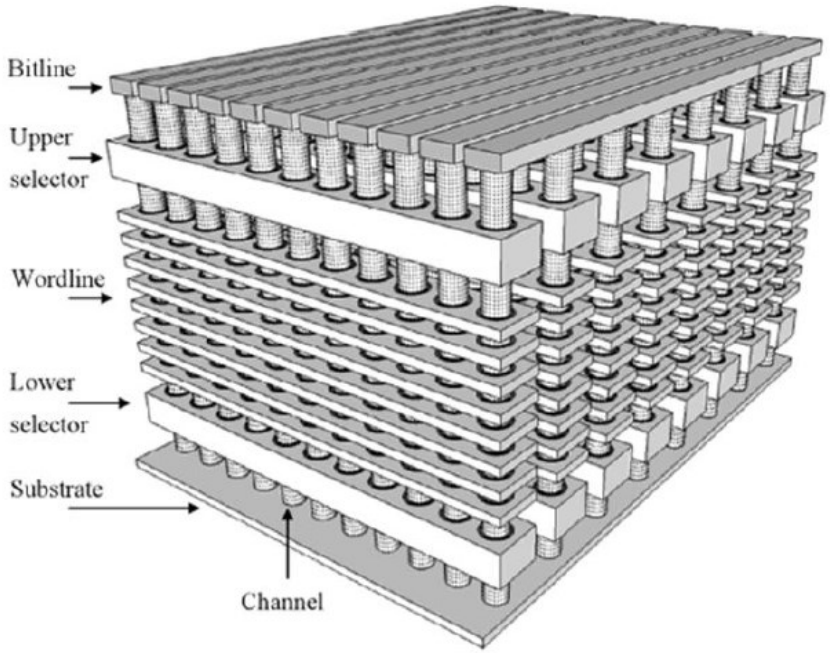
- *Design Equivalent Scaling* (occurs in conjunction with equivalent scaling and continued geometric scaling) refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.

  - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
  - Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Geometrical Scaling Limits and 3D Device Structure Improvements



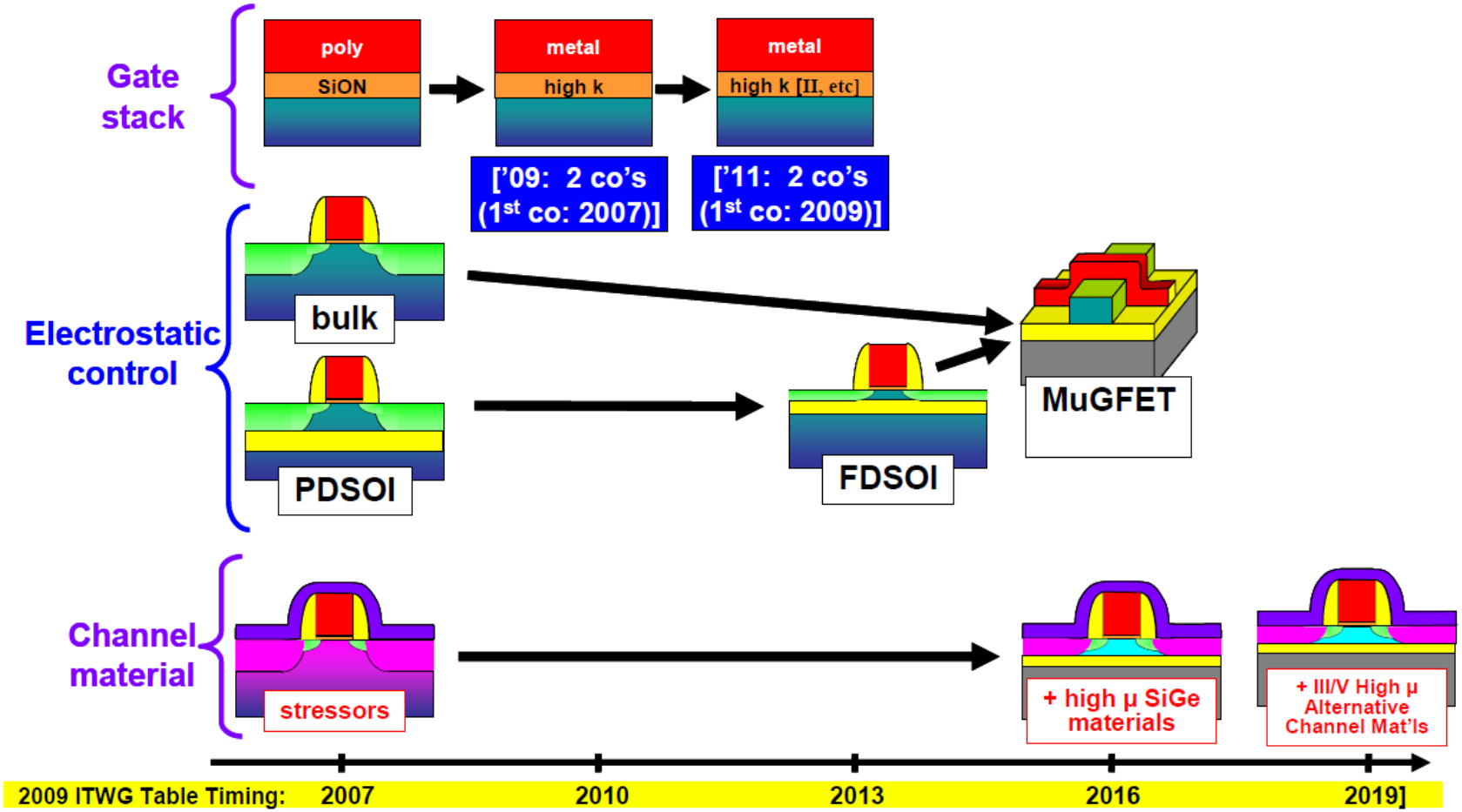
2D scaling will reach fundamental limits beyond 2020



Flash Memory Aggressively Adopts 3D Scaling in 2014

IRDS INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2017

"Equivalent Scaling" Process Technologies Timing compared to ORTC MPU/high-performance ASIC Half Pitch and Gate Length Trends and Timing (2009 ITRS)



SOI: silicon on insulator (PD: partially depleted; FD: fully depleted)
ORTC: Overall Roadmap Technology Characteristics

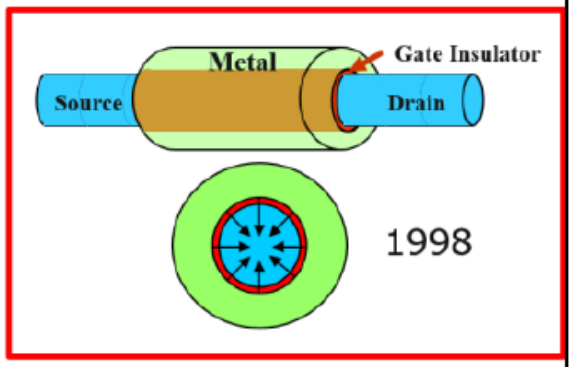
co: company
MuG: Multiple gate

Introducing Equivalent Scaling Measures

Incubation Time

$$$

	Early Invention	Focused Research	Introduction Manufacturing
Strained Silicon	1992	1998	2003
HKMG	1996	1998	2007
Raised S/D	1993	1998	2009
MultiGates	1987	2000	2011



~11 years

From Strategy to Implementation in High-volume Manufacturing in Record Time

IRDS INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2017

Trends

	Al gate PMOS	Si gate NMOS				Si gate CMOS				SGT	HKMG
	1969	1972	1975	1978	1981	1984	1987	1990	2000	2006	2009
t_{Ox} [nm]	150	120	110	70	50	40	25	20	4...7	1...2*	<1*
L_{eff} [µm]	10	6	5	3	2	1.6	1	0.8	0.15	0.06	<0.03
X_j [µm]	2	1	0.8	0.5	0.4	0.35	0.3	0.25	0.10	0.03	<0.02
Masks	5	5	6	7...10	7...10	8...12	10...15	12...18	<18	<25	~28
Diameter of Si wafer [inch]	2	2	3	4	4	5	6	6 ...	200mm	300mm	300mm

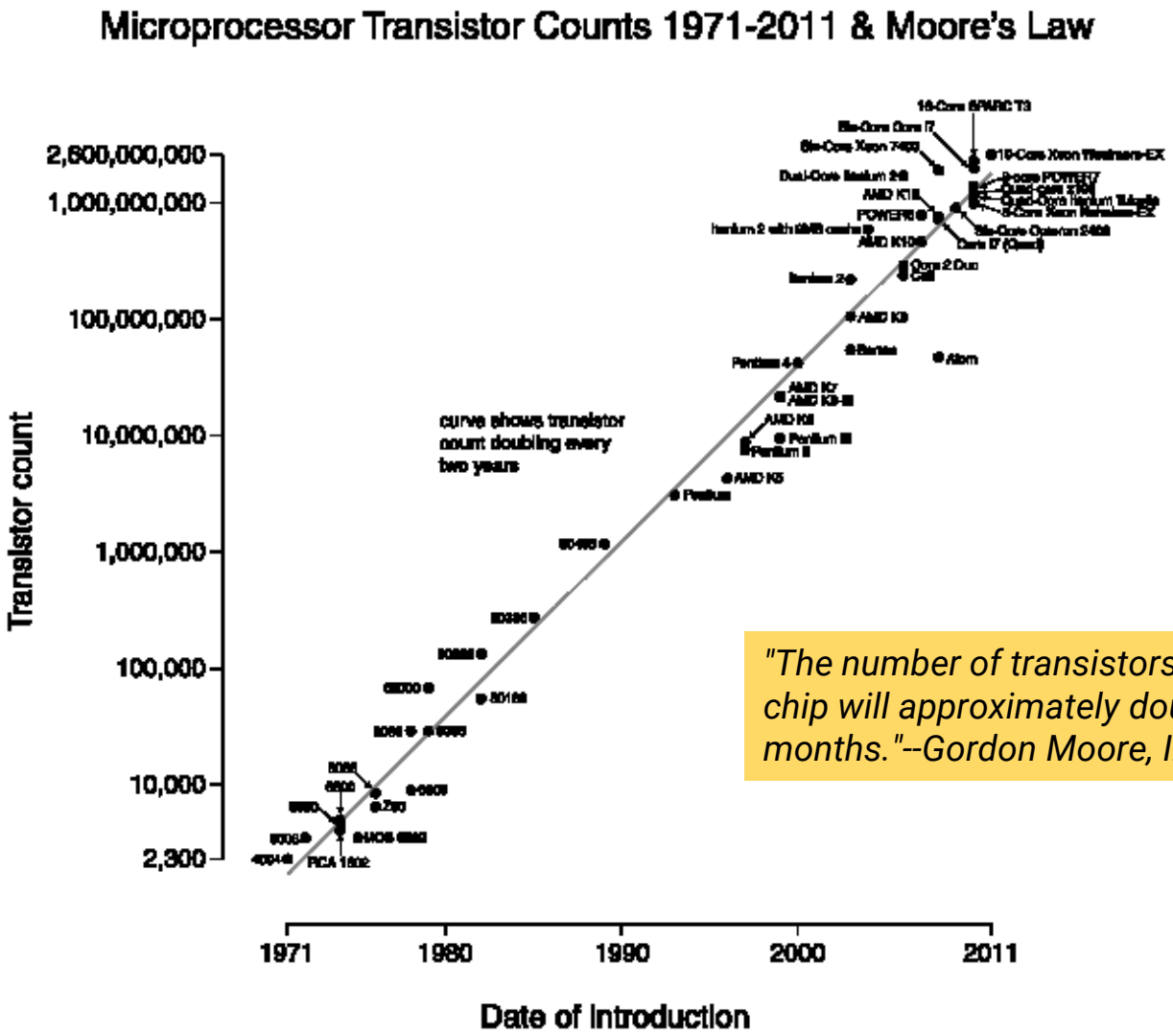
L_{eff} = effective channel (gate) length

* EOT: equivalent oxide thickness

Moore's law: **Degree of integration** $I = 10^{0.2\,(year - 1970) + 2.75}$

(I is doubled every 1.5 ... 2 years)

Murphy: **Reduction of costs per device** $K_{EE} = K_0 \cdot 10^{0.2\,(year - 1970) - 1.8}$



"The number of transistors incorporated in a chip will approximately double every 24 months."--Gordon Moore, Intel co-founder

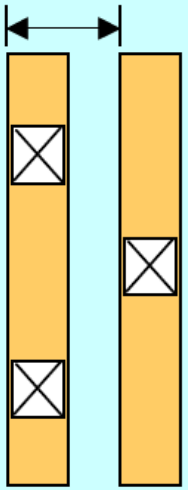
Source: http://en.wikipedia.org/wiki/File:Transistor_Count_and_Moore%27s_Law_-_2011.svg

Definition of Pitches

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

Metal

Pitch

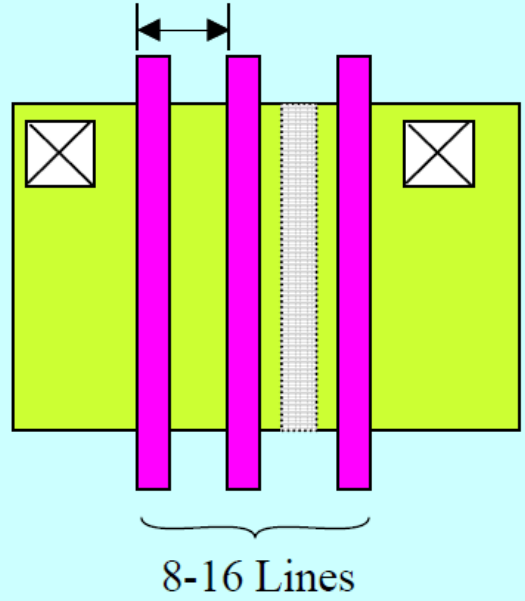


Typical DRAM/MPU/ASIC
Stagger-contacted Metal Bit Line

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2

Poly

Pitch



Typical flash
Un-contacted Poly

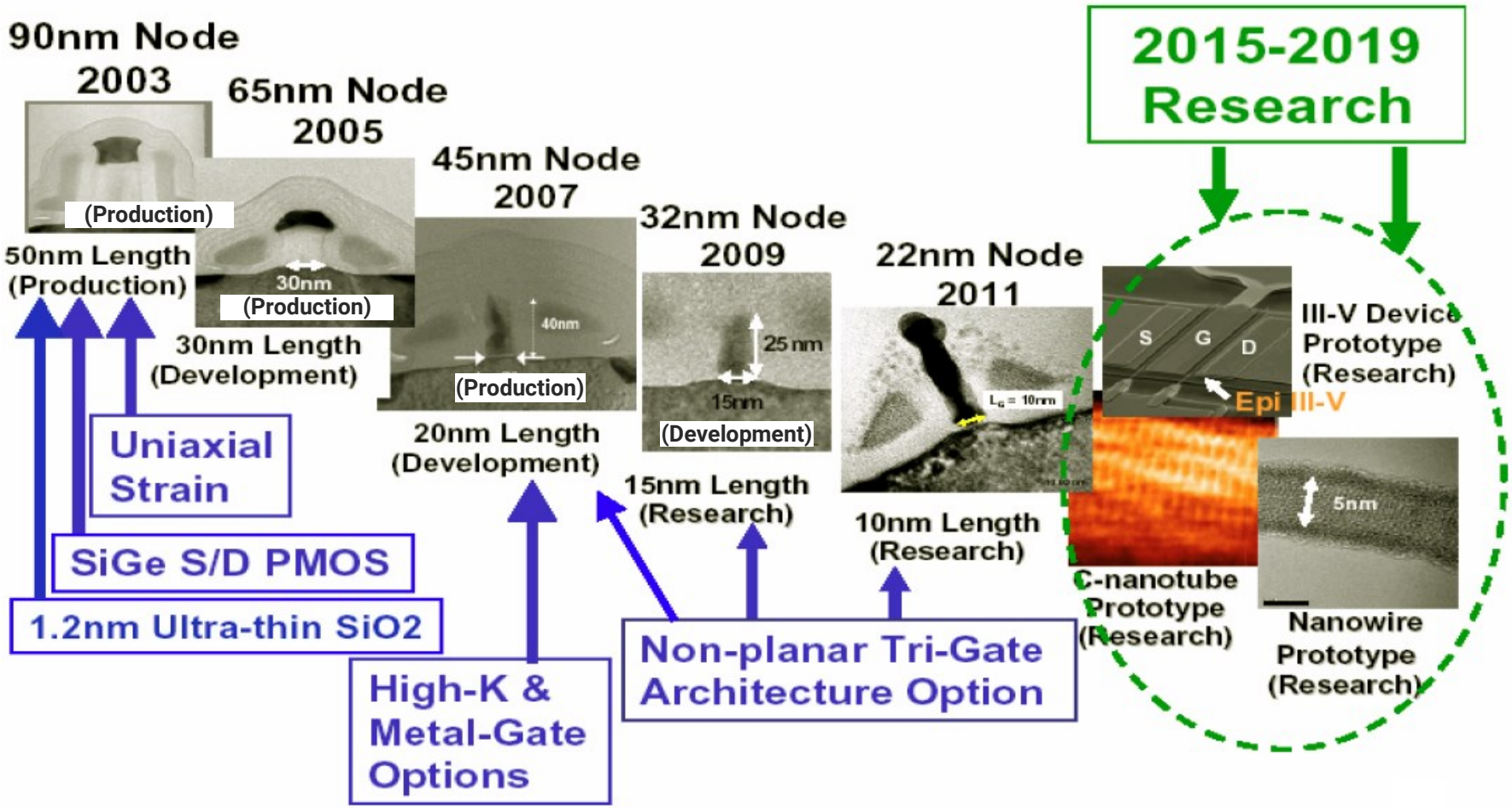
Table ES2 Overall Roadmap Technology Characteristics

2017 IRDS Executive Summary - ORTC							
YEAR OF PRODUCTION	**2017**	**2019**	**2021**	**2024**	**2027**	**2030**	**2033**
Logic device technology naming	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14 T2	P32M14 T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA, 3DVLSI	VGAA, LGAA, 3DVLSI
LOGIC CELL AND FUNCTIONAL FABRIC TARGETS							
Average cell width scaling factor	1.00	0.90	0.90	0.90	0.90	0.90	0.90
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm) [1,2]	18	14	12	10.5	7.0	7.0	7.0
Physical gate length for HP Logic (nm) [3]	20	18	16	14	12	12	12
Lateral GAA (nanosheet) Minimum Width (nm)			7.0	7.0	6.0		
Minimum Device Width (fin, nanosheet) or Diameter (nm)	8	7.0	7.0	7.0	6.0	6.0	6.0
LOGIC DEVICE Electrical							
Vdd (V)	0.75	0.70	0.65	0.65	0.65	0.60	0.55
DRAM TECHNOLOGY							
DRAM ½ Pitch (nm) [1]	18	17.5	17	14	11	8.4	7.7
DRAM cell size factor: aF^2 [11]	6	6	4	4	4	4	4
DRAM bits/1chip target	8G	8G	16G	16G	32G	32G	32G
NAND Flash							
Flash ½ Pitch (nm) (un-contacted Poly)(F) (2D) [1]	15.0	15.0	15.0	15.0	15.0	15.0	15.0
Flash Product Highest Density (independent of 2D or 3D)	512G	1T	1T	1.5T	3T	4T	4T+
Flash 3D Maximum Number of Memory Layers [6]	64	96	128	192	384	512	>512

IRDS INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2017

Nanoelectronics Road

More Moore



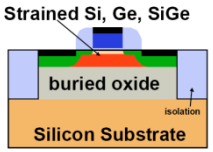
Source: A. Ionescu, European NanoDay 2007

After traditional scaling (CMOS)

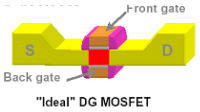
No general replacement for CMOS (yet?) !

Classical and non-classical CMOS

- high-k & metal gate
- transport enhanced



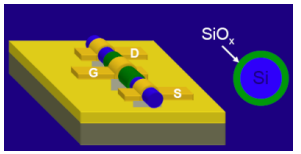
- multi-gate, UTB



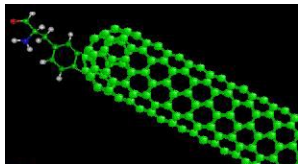
- metallic S/D
- ballistic

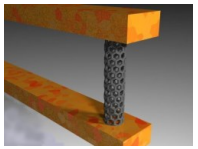
HYBRID CMOS-NANO

Nanowires (semiconductor)

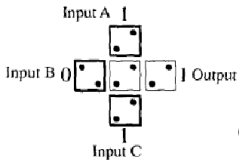


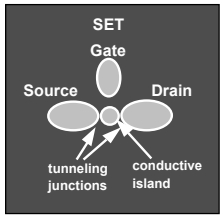
Nanotubes (CNTs)





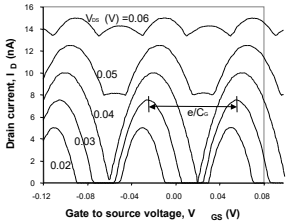
QCA

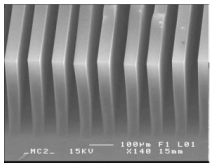




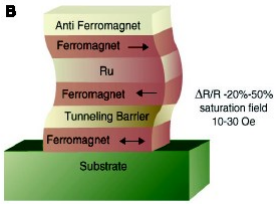
RTD RSFQ

SET



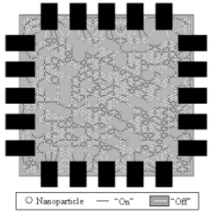


Spintronics



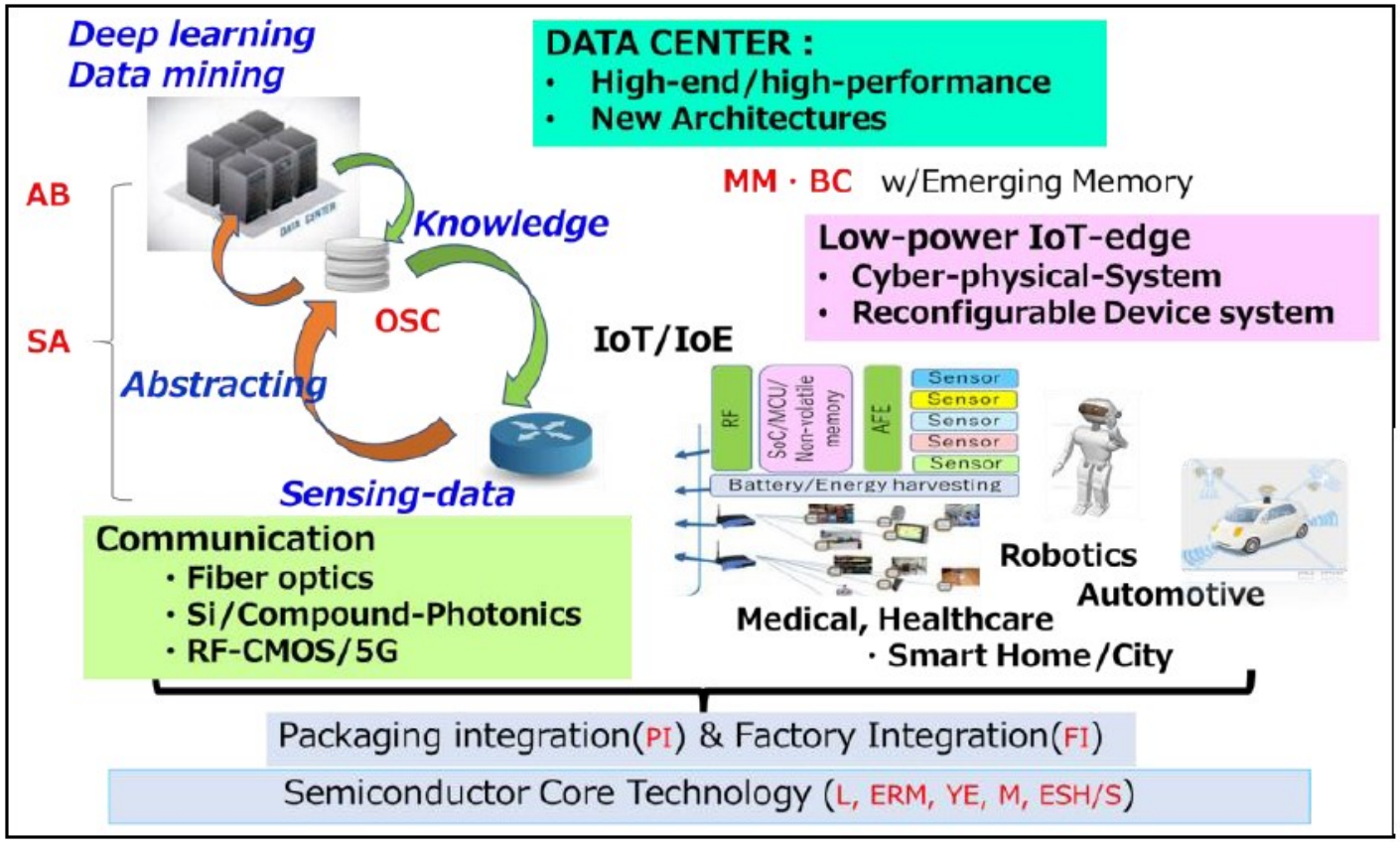
2020?

Molecular



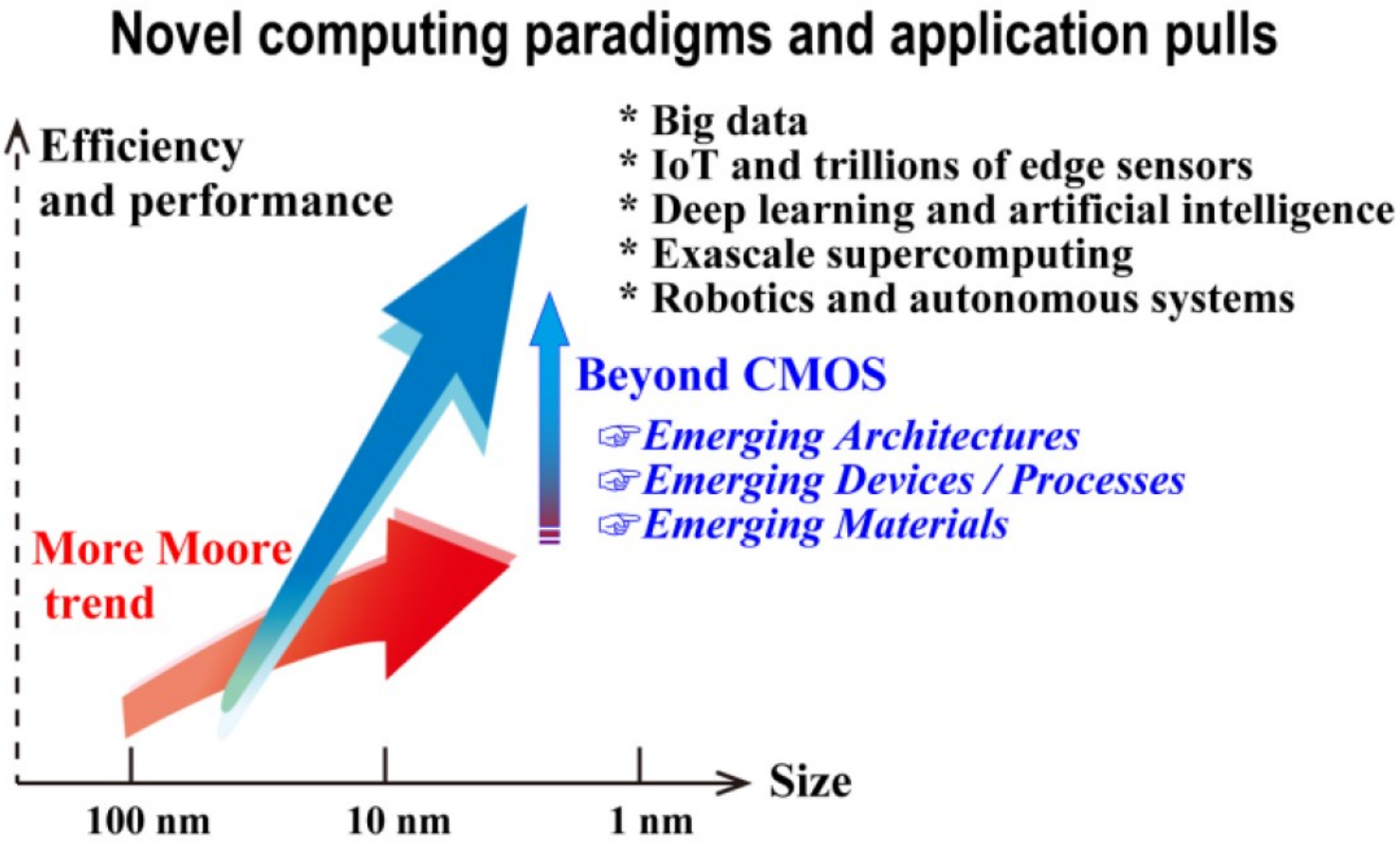
Source: A. Ionescu, European NanoDay 2007 (modified)

The New Ecosystem of the Electronics' Industry based on Semiconductor Technologies



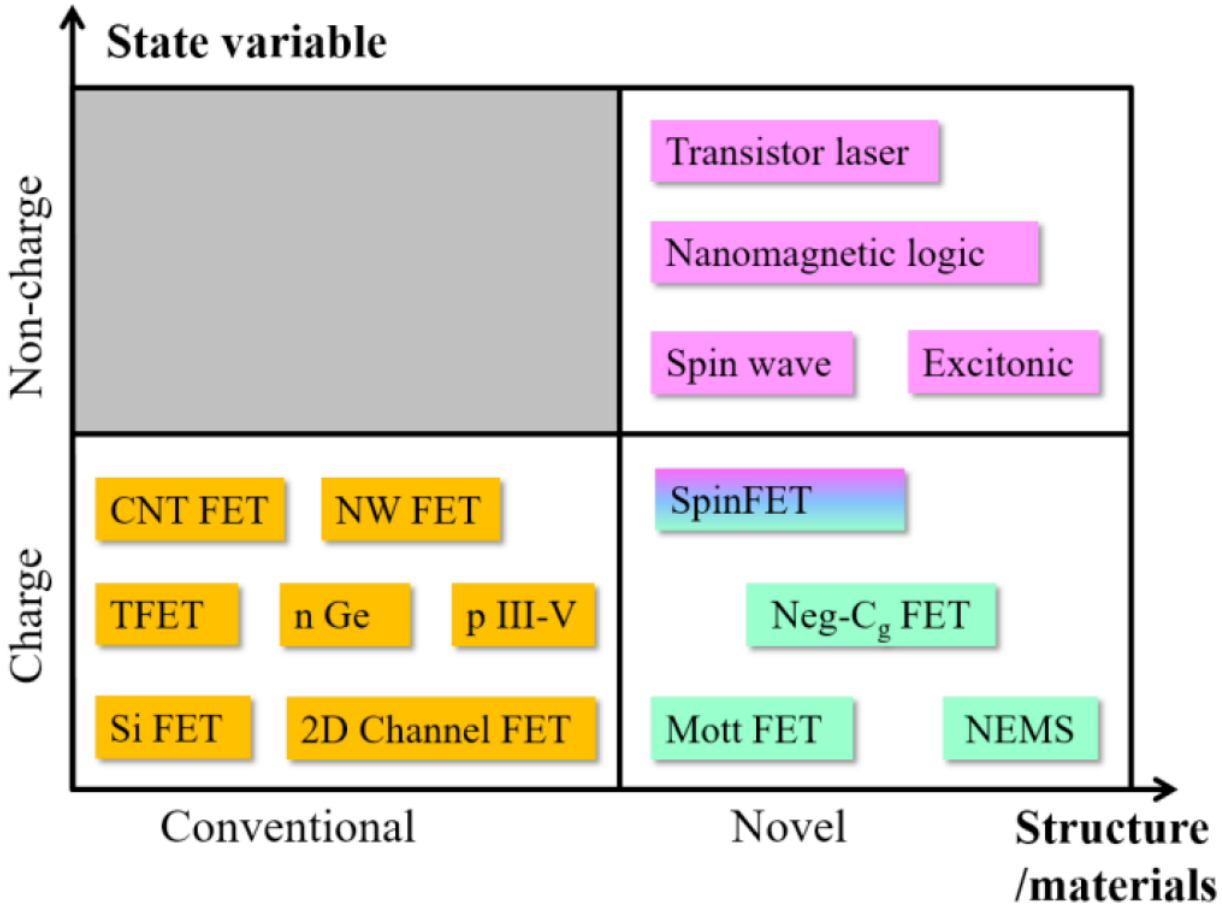
AB: Applications Benchmarking
SA: Systems & Architectures
OSC: Outside System Connectivity
MM: Moore Moore
BC: Beyond CMOS
PI: Packaging Integration
FI: Factory Integration
L: Lithography
M: Metrology
ERM: Emerging Research Materials
YE: Yield Enhancement
ESH/S: Environment, Safety & Health and Sustainability

IRDS INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2017



Relationship of More Moore, Beyond CMOS, and Novel Computing Paradigms and Applications

Taxonomy of Options for Emerging Logic Devices



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The 3 Era of Scaling Heralded by NTRS, ITRS, ITRS 2.0, and IRDS

The Different Ages of Scaling

(Different methods for different times)

1 Geometrical Scaling (1975-2002)

- Reduction of horizontal and vertical physical dimensions in conjunction with improved performance of planar transistors

2 Equivalent Scaling (2003~2024)

- Reduction of only horizontal dimensions in conjunction with introduction of new materials and new physical effects. New vertical structures replace the planar transistor

3 3D Power Scaling (2025~2040)

- Transition to complete vertical device structures. Heterogeneous integration in conjunction with reduced power consumption become the technology drivers

NTRS ITRS ITRS IRDS

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