Questions

1. Please explain the specifics of ALD in comparison to CVD!
2. What are the steps of an ALD cycle?
3. Please name potential applications of ALD thin films!

4. Please name the basic process steps in the process flow of lithography and patterning!
5. Please name and discuss the equation for the resolution! (How to lower critical dimension CD = min. printable feature size)
6. Please name the applied resolution enhancement techniques (RET)

7. Please define the terms “anisotropy” and “selectivity”!
8. What are potential dry etching techniques? Please name the respective etching mechanisms and the achievable anisotropy!
9. Please draw a reactor for reactive ion etching and name the different parts!

Seminar 4 : Deposition Processes (2) -ALD

Q1 Please explain the specifics of ALD in comparison to CVD!

A L D

- Highly reactive precursors
- precursors react separately on the substrate
- precursors must not decompose at process temperature
- Uniformity ensured by the saturation mechanism at the surface
- thickness controled by amount of cycles (growth per cycle GPC)
- Surplus precursor dosing acceptable

C V D

- Less reactive precursors
- Precursors react at the same time on the substrate
- Precursors can decompose at process temperature
- Uniformity requires uniform flux of reactants and temperature (in reaction rate limited case)
- Thickness control by precise process control and monitoring
- Precursor dosing important

Atomic Layer Deposition: Comparison of ALD and CVD

A L D

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- Precursors react separately on the substrate
- Precursors do not decompose at process temperature
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Q2 What are the steps of an ALD cycle?

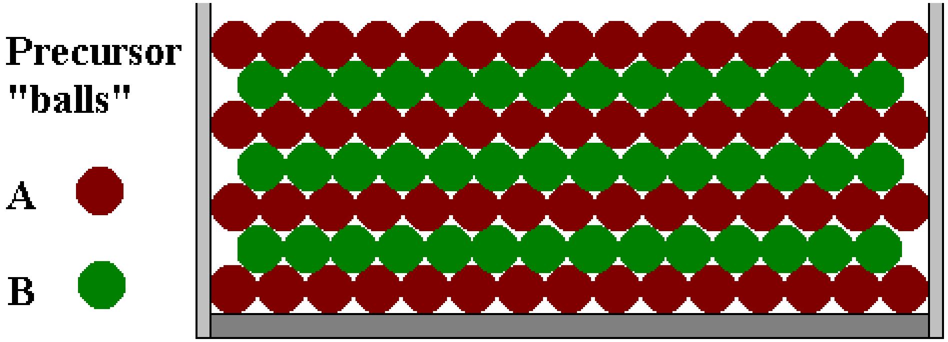
How many steps per cycle (min.)? 4 steps

Step 1: Precursor A – chemisorbs at the surface (chemical reaction, saturation of all available reaction sites)
Step 2: Purge: removal of unreacted precursor & reaction byproducts
Step 3: Precursor B – chemisorbs at the surface (chemical reaction, saturation of all available reaction sites)
Step 4: Purge: removal of unreacted precursor & reaction byproducts

How many cycles are combined for complete film deposition?

- For approx. 5 nm we may need 50 … 100 cycles (given a GPC 0.05 … 0.1 nm/cycle)

Atomic Layer-by-layer Growth

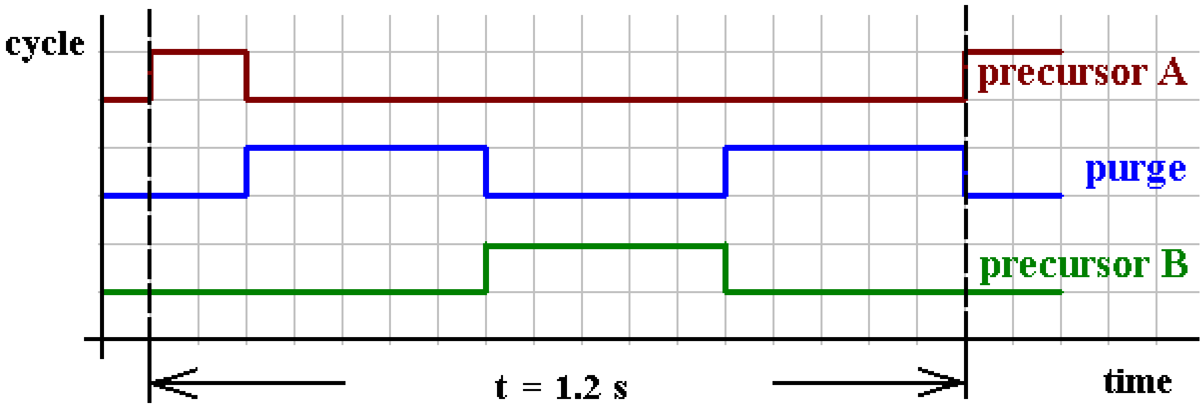


The intrinsic surface control mechanism:

Saturation of all the reaction/adsorpion sites

Purging step

ALD Cycle



Q3 Please name potential applications of ALD thin films! (in production)

Applications	Materials
1) High-k dielectrics for:	
- MOS gate insulator	HfOx, HfSixOy
- integrated capacitors (memory)	Al2O3
2) Diffusion barrier films	TiN, TaN, WCN
3) Seed layers for the electrochem. Dep. (ECD)	Cu
4) Capacitor electrodes	Ru, TiN, TaN

Atomic Layer Deposition: Processes for IC Industry

High-k gate dielectrics

- Replacement of current SiO_2/Si_3N_4 films
- Processes available for ZrO_2, HfO_2, mixed materials
- Targeted (equivalent) oxide thickness - EOT: ~ 1.0 nm

High-k capacitor dielectrics

- Replacement of current SiO_2/Si_3N_4, Ta_2O_5 films
- ALD processes for Al_2O_3, Ta_2O_5

Diffusion barriers (to avoid Cu diffusion)

- Replacement current sputtered diffusion barriers
- ALD processes for TiN, W(C)N, Ta(C)N, mixed nitrides

Conducting/Metal films

- ALD Cu seed layers for Cu electroplating
- Electrodes for high k gate and capacitor applications (metals & metal nitrides)

EOT – equivalent oxide thickness

Q4 Please name the basic process steps in the process flow of lithography and patterning!

1) pre-treatment: dehydration bake / adhesion promotor deposition
2) spin-on deposition / coating of the wafer with photoresist (PR)
3) Pre-exposure bake (drive of solvent)
4) Exposure (mask): positive resist: exposed areas will change ist properties and get resolvable
5) Post-exposure bake
6) Development of PR (patterning the PR, etching the exposed areas in a liquid solution)
7) Hard bake: making the PR more crosslinked, resistive to the etching process
8) Dry Etching – pattern the film using the PR mask (additional hard mask may be required)
9) PR stripping / removal by combination of dry/wet process
10) [cleaning]

3.6.2 Lithographic Process

Overview

Wafer Prime (HMDS)
↓
Resist Coating
↓
Soft ***B***ake, ***P***ost ***A***pply ***B***ake
↓
Exposure
↓
Post ***E***xposure ***B***ake
↓
Develop
↓
Hard ***B***ake
↓
(UV Harden)

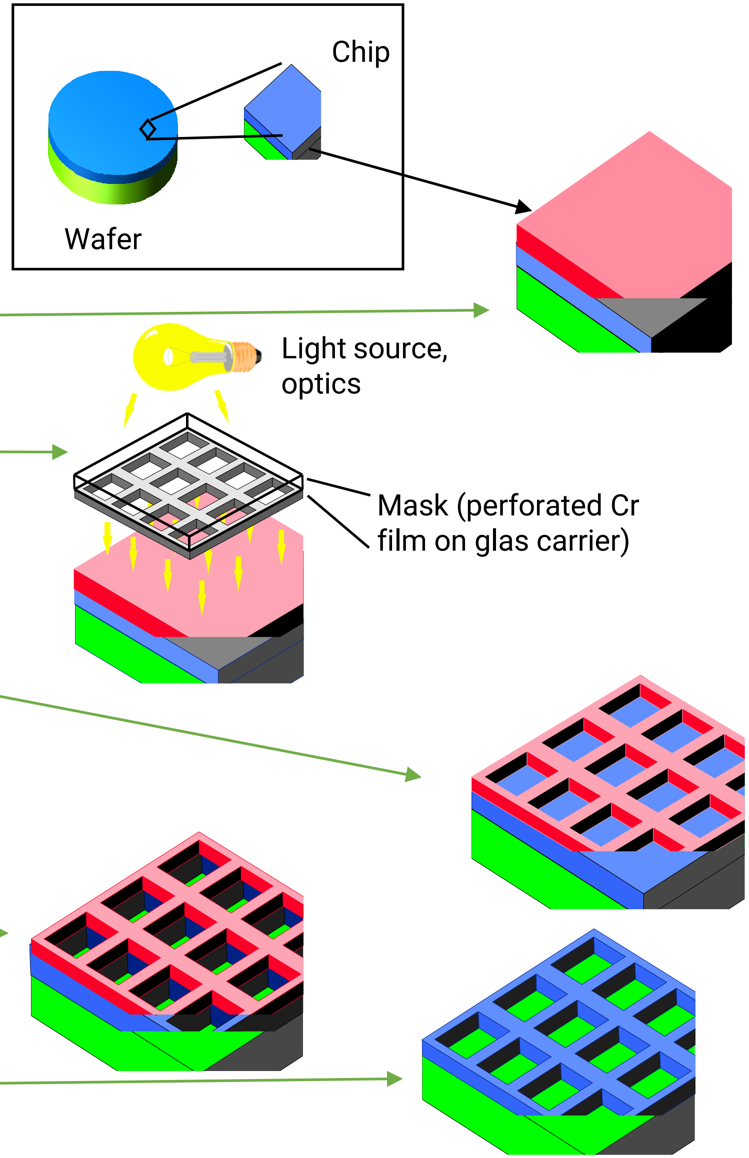
Rework → If Specifications are not met → ARC Coating, ARC Bake

↓

Pattern transfer (etching, implantation)

↓

Resist removal (stripping, dry, wet)



HMDS – Hexamethyldisilazan (Primer)
ARC - Anti-reflective coating

Q5 Please name and discuss the equation for the resolution! (How to lower critical dimension CD = min. printable feature size)

$$l_{min} = k_1 \cdot \frac{\lambda}{NA}$$

Ways to reduce l_{min}:

1) Reduce exposure wavelength (some 100 nm … DUV 248/193 nm … EUV/soft X-ray 13.5 nm)
*2) Increase the numerical aperture NA: improving optics, increase n (move from air → water = immersion litho; NA = n * sin(beta)*
3) RET – resolution enhancement techniques!

- *reduce λ (→ DUV → EUV → X-ray)*
- *increase NA (immersion litho)*
- *reduce k_1 (RET)*

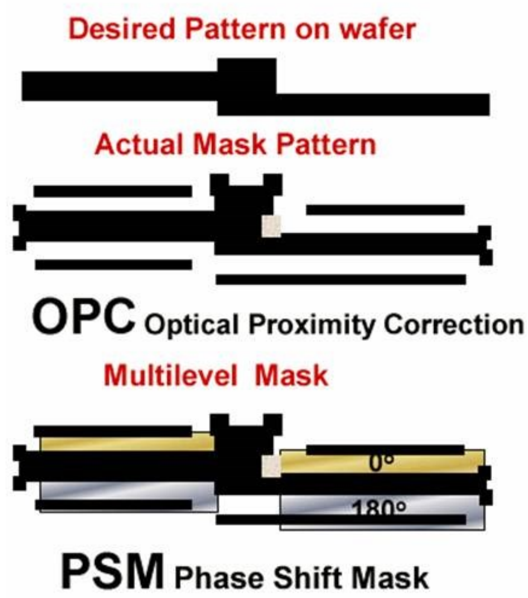
Q6 Please name the applied resolution enhancement techniques (RET)

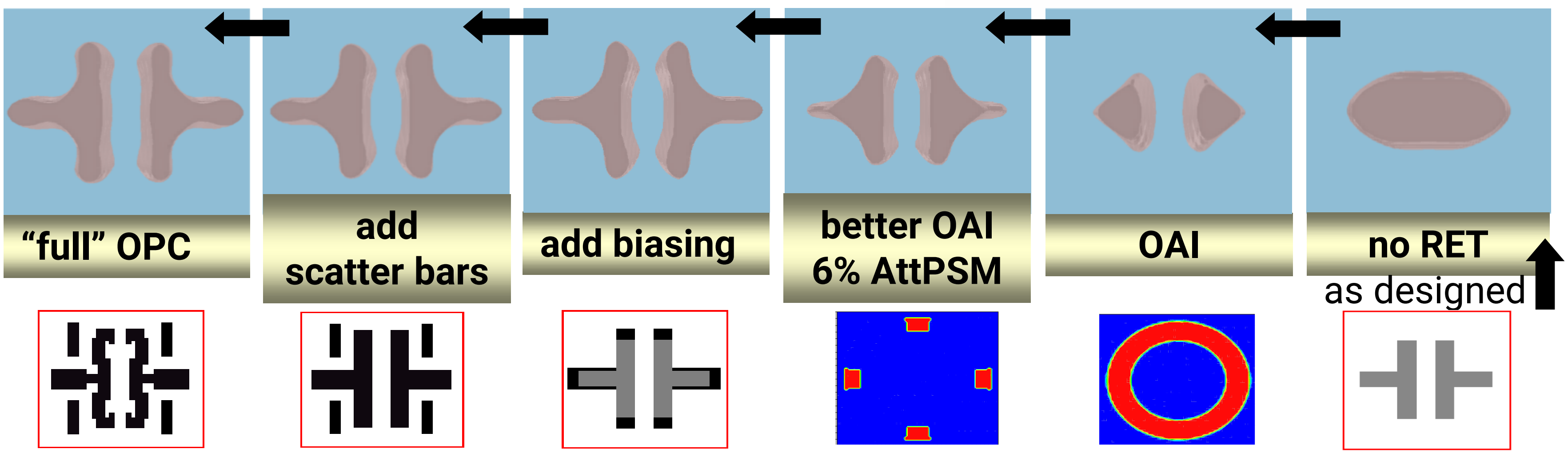
1) Optical Proximity Correction (OPC)
2) off- axis illumination (OAI)
3) Double Exposure (or even triple or more)
4) phase shift mask (PSM)
5)
6)

Combination of RET Solutions

- This is what the designer drew
- Added ‘scattering bars’ and serifs to make the polygon print more exactly
- Added additional phase features to allow printing smaller features at the same wavelength

Accurate and flexible modeling is key!



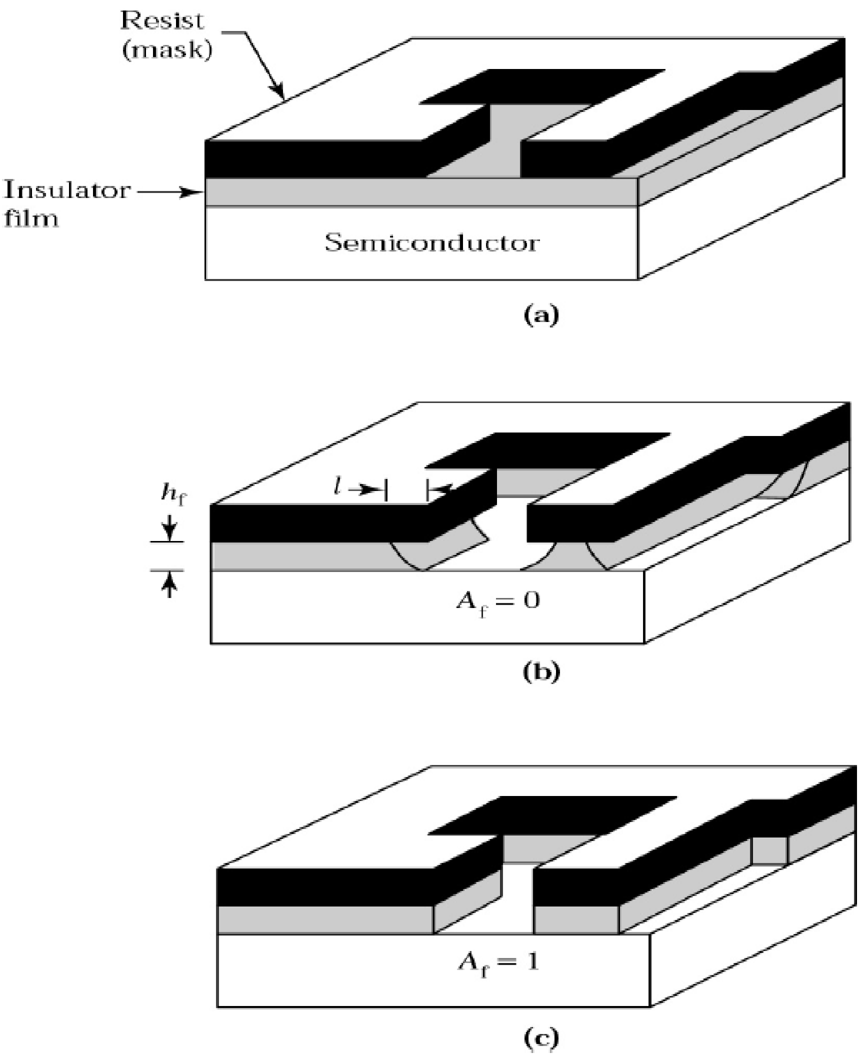


(Courtesy ASML)

Q7 Please define the terms “anisotropy” and “selectivity”!

<u>Degree of Anisotropy:</u>

$$A_f \equiv 1 - \frac{l}{h_f} = 1 - \frac{R_l t}{R_v t} = 1 - \frac{R_l}{R_v}$$



For isotropic etching: $\boldsymbol{R_l = R_v}$ ***and*** $\boldsymbol{A_f = 0}$

For completely anisotropic etching: $\boldsymbol{R_l = 0}$ ***and*** $\boldsymbol{A_f = 1}$

Selectivity: Ratio of etch rates of different materials

$S_{\text{(to) resist}} = R_{\text{etched film}} / R_{\text{resist}}$

$S_{\text{(to) underlayer}} = R_{\text{etched film}} / R_{\text{underlayer}}$