

Pros and cons for different HKMG integration options

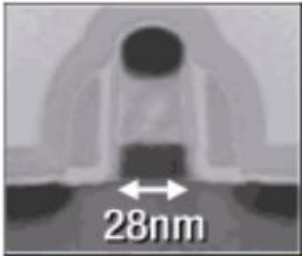

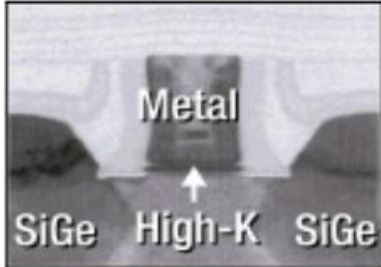
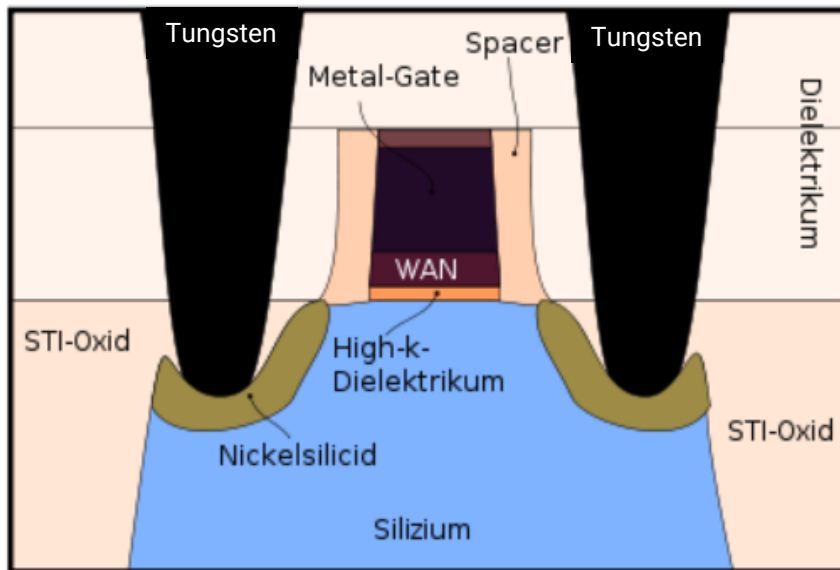
	MIPS (<u>M</u> etal <u>I</u> nserted <u>P</u> oly- <u>S</u> i)	FUSI (<u>F</u> ully <u>S</u> ilicided <u>G</u> ate)	RMG (<u>R</u> eplacement Metal Gate)
			
Dielectric	First	First	First or last
Electrode	First	Last	Last
Pros	<ul style="list-style-type: none"> • Conventional process flow 	<ul style="list-style-type: none"> • Low complexity • Thermal budget 	<ul style="list-style-type: none"> • Thermal budget • Higher strain from embedded SiGe S/D
Cons	<ul style="list-style-type: none"> • Thermal budget • Complex V_T tuning • Mobility, reliability at thin EOT 	<ul style="list-style-type: none"> • Silicide phase process window • Low V_T difficult 	<ul style="list-style-type: none"> • Complexity, cost • More restricted design rules

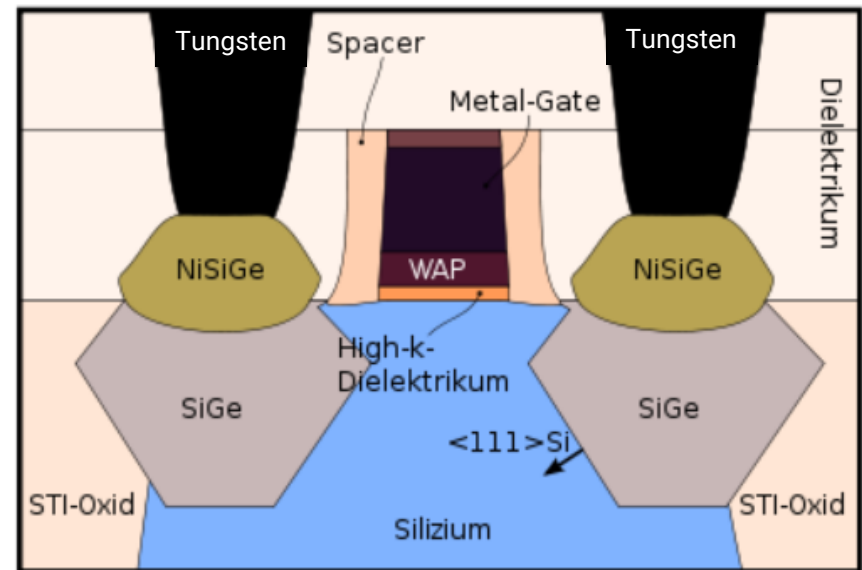
Fig. 5.2.3: Pros and cons of different HK/MG integration options. FUSI being abandoned, only gate-first (MIPS) or gate-last (RMG) are actively developed today

HKMG: Gate Last Approach

n-channel MOSFET (NMOS)



p-channel MOSFET (PMOS)



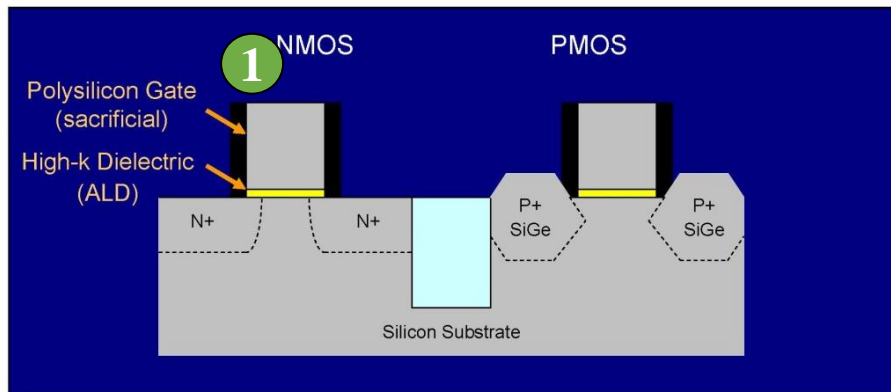
WAF = work function adjustment layer for NMOS

WAP = work function adjustment layer for PMOS

Fig. 5.2.4: Intel's HKMG Gate Last Approach (Penryn processor, 2007)

See also: http://download.intel.com/pressroom/kits/45nm/Press45nm107_FINAL.pdf

HKMG: Gate Last Process Flow (1)



Standard transistor process through source-drain formation,
but including atomic layer deposition high-k dielectric

(Fig. 1) The picture shows the standard CMOS process using ALD high-k gate dielectric.

Q1: Why STI (here light blue) is used, not LOCOS?

- a) thermal budget
- b) process costs
- c) device dimension

Q2: As high-k dielectric gate isolator material HfO_2 with a thickness of 5 nm will be used for example. The gate length and width are 45 nm and 90 nm, respectively. Which charge can be stored on this gate capacitor at a gate voltage applied of 3.3 V?

- d) 0.6 fC
- e) 0.6 pF
- f) 592 aAs

Q3: What is the maximum dopant concentration in the polygate which will be removed during this RMG process?

- g) $1\text{-}5\text{E}20 \text{ cm}^{-3}$
- h) $1\text{-}5\text{E}15 \text{ cm}^{-3}$
- i) Undoped

Q4: Which mathematical approach can be used to fit the dopant distribution?

- j) Pearson IV
- k) Gaussian
- l) Monte Carlo based algorithm

Q5: What influences the average grain size of the poly gate?

- m) doping level
- n) deposition temperature
- o) technology node

Q6: As high-k dielectric gate isolator material HfO_2 with a thickness of 5 nm will be used for example. The gate length and width are 45 nm and 90 nm, respectively. Which charge can be stored on this gate capacitor at a gate voltage applied of 3.3 V?

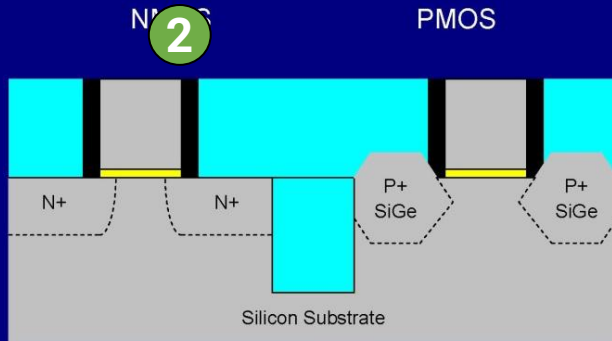
- p) 0.6 fC
- q) 0.6 pF
- r) 592 aAs

Q7: What the job of the side wall spacer is?

- s) stabilizing the gate structure
- t) optimizing the S/D doping profile
- u) protection against diffusion of gate doping

multiple selections are possible

HKMG: Gate Last Process Flow (2)



Deposit and planarize oxide layer

(Fig. 2) Deposit and planarize oxide layer

Q1: What is the thickness about of such the oxide layer?

- a) 0.1 – 1 μm
- b) 5 nm
- c) 0.020 – 0.1 μm

Q2: Can this layer be deposited by PVD?

- d) theoretically yes
- e) no!

Q3: How does the CMP process recognize its end?

- f) power consumption of the drive motor
- g) analysis of slurry composition
- h) polishing noise
- i) by using optical measurements

Q4: Which CVD precursors can be used to deposit SiO_2

- j) SiO_4
- k) O_2
- l) SiH_4

Q5: What is a difference between Epitaxy and CVD

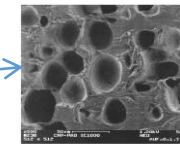
- m) process temperatur
- n) surface characteristics of wafer surface

Q6: Which materials can be deposited by CVD

- o) metals
- p) silicon
- q) isolators
- r) polycrystalline silicon

Q7: What are consumables of CMP process?

- s) brushes
- t) wafers
- u) money
- v) asperities



„hard pad“ IC1000 by Rodel
-> good planarization performance

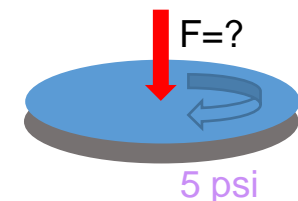


„soft pad“ Suba series by Rodel
-> low surface roughness but poor planarization performance

Q8: The CMP carrier pressure is given to 5 psi.

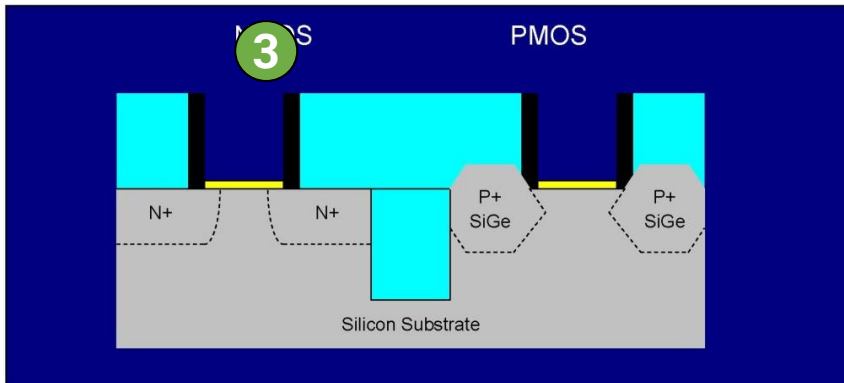
Which force must be applied on an 300 mm Wafer to get this?

- w) 25 kp
- x) 250 kp
- y) 25 N
- z) 1500 N



multiple selections are possible

HKMG: Gate Last Process Flow (3)



Etch out sacrificial polysilicon gate

(Fig. 3) Etch out sacrificial polysilicon gate

Q1: Which process can be used to remove the polysilicon gate?

- a) KOH based wet etching
- b) Barrel etching
- c) Reactive ion etching
- d) Sputter etching

Q2: This etching process is

- e) isotropic
- f) anisotropic?

Q3: This etching process is

- g) selective
- h) non selective?

Q5: Which processes in IC technology apply a plasma?

- i) ion implantation
- j) CVD
- k) Wet etching
- l) Dry etching
- m) Spin on deposition
- n) Ion beam lithography
- o) PVD
- p) ECD
- q) CMP

Q6: Where the energy for plasmas used in microelectronics technology comes from?

- r) electrostatic fields
- s) RF inductively coupled in
- t) RF capacitively coupled in

Q7: Plasma used in AICT are

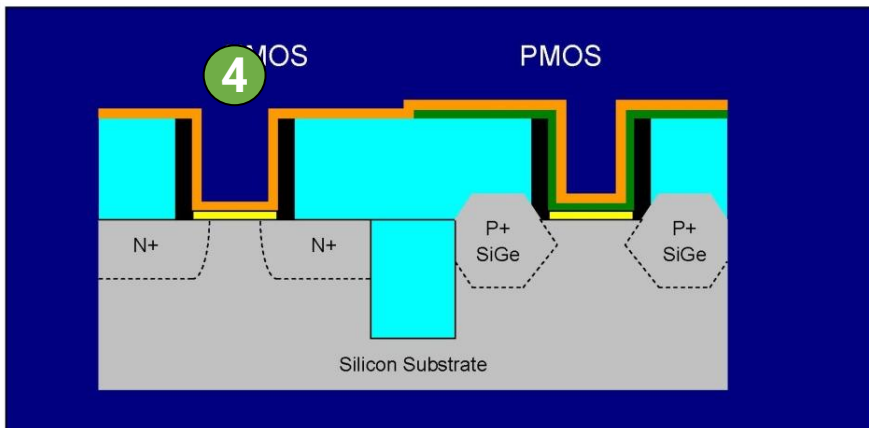
- u) "hot"
- v) "cold"
- w) "advanced" ?

Q8: Plasma used in AICT processes consists of

- x) gas atoms
- y) a low level of ions (below 1 promille)
- z) a high level of ions (5 to 10 %)
- aa) electrons
- bb) protons
- cc) radicals

multiple selections are possible

HKMG: Gate Last Process Flow (4)



Deposit separate NMOS and PMOS WF metal layers

(Fig. 4) Deposit work function layers

Q1: How many masks are required for WF layer deposition and patterning?

- a) 1
- b) 2
- c) 3

Q2: What about is the thickness of WF layers?

- d) 200 ... 400 nm
- e) below 5 nm
- f) 1 μm

Q3:

What are the Cons for the MIPS technology?

Thermal budget

- g) Complex V_T tuning
- h) Mobility, reliability at thin EOT
- i) Higher strain from embedded SiGe S/D
- j) Complexity, cost
- k) Conventional process flow
- l) More restricted design rules

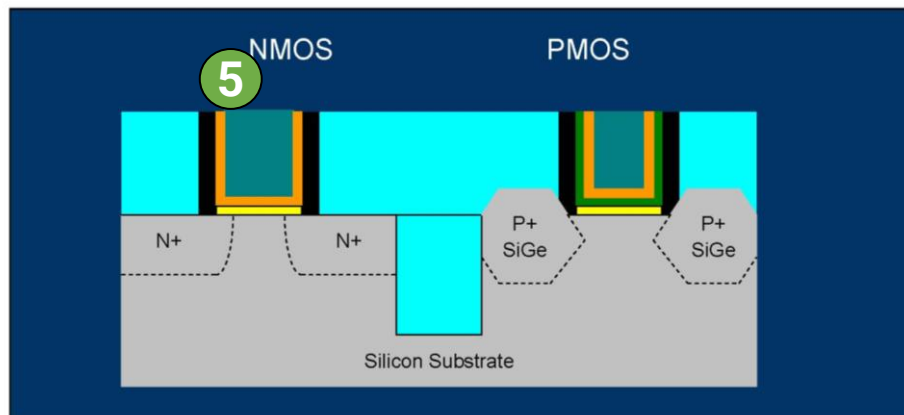
Q4:

What are the Pros for the RMG technology?

- m) Thermal budget
- n) Complex V_T tuning
- o) Mobility, reliability at thin EOT
- p) Higher strain from embedded SiGe S/D
- q) Complexity, cost
- r) Conventional process flow
- s) More restricted design rules

multiple selections are possible

HKMG: Gate Last Process Flow (5)



Deposit Al fill metal, planarize surface

(Fig. 5) Deposit Al and planarize surface

Al-PVD

Q1: An Argon ion is accelerated with the target voltage $V = 1 \text{ kV}$ and then hits the target. What is the speed of impact on target?

- a) 70 000 m/s
- b) 1000 eV
- c) 300 000 m/s

Q2: What is the speed of an electron, emitted from the target and accelerated in the same electric field?

- d) same speed as the Ar Ion
- e) 270 x faster than the Argon Ion
- f) 729 x faster than the Argon Ion

Q3: Which metals are also been used as gate electrode material in HKMG

- g) Gold
- h) Ni
- i) TiN
- j) W
- k) TaN

Q4: High-k materials are still in focus of AICT research. What are main requirements for a gate dielectric?

- l) Barrier height
- m) Permittivity
- n) Thermal stability
- o) Color
- p) Interface quality
- q) Costs
- r) UV resistance
- s) Gate electrode compatibility

Q5: HKMG technology enables

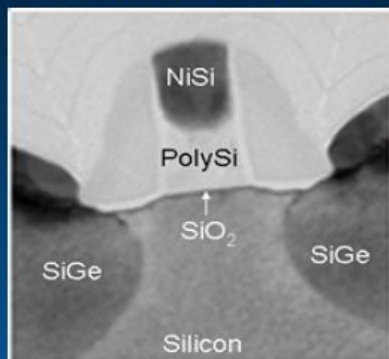
- t) higher switching speed
- u) higher switching power
- v) higher transistor density ?

multiple selections are possible

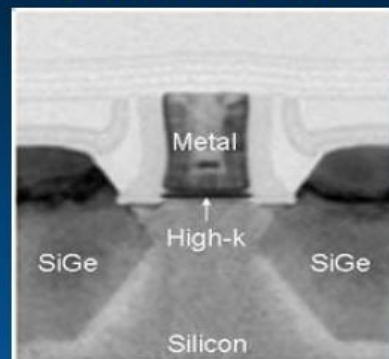
High-k + Metal Gate Transistors

Improved Transistor Density	~2x
Improved Transistor Switching Speed	>20%
Reduced Transistor Switching Power	~30%

65 nm Transistor



45 nm HK + MG



Enables New Features, Higher Performance,
Greater Energy Efficiency

