Advanced Integrated Circuit Technology – English
Some *Ü*bung Questions and Answers – 2019

1. Define Basic Process Steps (BPS), Process, Process Technology, and Basic Technology.

Basic process steps (BPS):

- Indivisible step in the process flow
- Characterized by physical / chemical parameters (Temperature, pressure, gas composition…)
  Example: Special diffusion step (pre-deposition), implantation step, special cleaning step (rinsing)

Process:

- Consists of one or more BPS
- Carried out by using specific tools (equipment)
- Standardized component of technology
- Results in achievement of a specific property
  Example: doping (pre-deposition, drive in), photolithography (deposition of resist, exposure, development, ….)

Basic Technology:

- Sum of processes (or BPS) to be performed for the fabrication of a specific product
  Example: CMOS, BICMOS, Bipolar….

Process Technology:

- Physical, chemical and other mechanism/ principle of the process
- Technical realization using specific equipment
- Process integration issues

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2. Name four basic MOS transistor types.

- NMOS Enhancement type
- NMOS Depletion type
- PMOS Enhancement type
- PMOS Depletion type

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3. Name important trends in transistor types.

- Production of many identical devices / circuits / chips by one process –> Cost decrease!
- Characteristic Quantities:
  - Wafer diameter(size) increase
  1. Die size increase
  2. Number of transistors per die (degree of integration)
  3. Yield
- Main features:
  4. New and improved products (Performance & Reliability):
  5. Continuous increase of the degree of integration
  6. Scaling down – miniaturization, decrease of lateral dimensions and layer thickness
- Goal: equal or higher yield than in previous technology node

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4.

- **Explain the terms 'Geometrical scaling', 'Equivalent scaling', and Design equivalent Scaling.**
- **Give two examples for equivalent scaling.**

Geometrical Scaling:

(Constant field) Refers to the continued shrinking of horizontal and vertical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

Equivalent scaling:

(Occurs in conjunction with, also enables, continued geometrical scaling) Refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

Design Equivalent scaling

(Occurs in conjunction with equivalent scaling and continued geometric scaling) Refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.

Examples for Equivalent scaling: low–k/Cu, HKMG, electrostatic control (SOI), new channel materials, strain engineering/ stressors.

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5. Define the terms Back-End and Front-End.

- ✓ **Front End** – Wafer level fabrication process for active devices & Interconnects
- ✓ **Back end** – Packaging

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6. The combined need for digital and non-digital function in an integrated system is translated as a dual trend in the International Technology Road Map: More Moore & More Than Moore.

- **What characterizes More and More than More?**
- **Define the meaning of Moore's law.**

More's Law:

Moore's law states that the number of transistors incorporated in a chip will approximately double every 24 months.

Things Which Characterize "More" and "More Than More":

More Moore: Decrease of all characteristic dimensions and structures (Ex: Channel length of MOS transistors)

More than Moore: Integration of various sensors and actuators with the miniaturized(micro) electronics.

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7. Name five basic process steps of CMOS Technology.

- SiO_2 oxide layer formation on the wafer surface (usually on P type Si Substrate)
- Photoresist coating on oxide layer and masking
- Etching followed by Acidic etching and then the removal of photo resist
- Implantation or diffusion to form n and p type regions.
- Removal of unwanted material
- Polysilicon deposition and metallization

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8.

- **What is the motivation to use lower–k dielectric as insulator in on–chip interconnects systems instead of SiO_2 for high performance CMOS technology?**
- **How can we achieve low–k in the dielectric materials?**
- **Which low–k dielectrics have been used so far? What are their values?**

Motivation:

Low–k dielectrics are used as insulators to decrease the parasitic RC delays such as Cross talk, Signal Delays, and power consumption.

Methods to achieve low–k in the dielectric materials:

$$\frac{\varepsilon - 1}{\varepsilon + 2} = \frac{1}{3\varepsilon_0} \Sigma N_j \alpha_j$$

N_j: Density of the material: number of atoms.

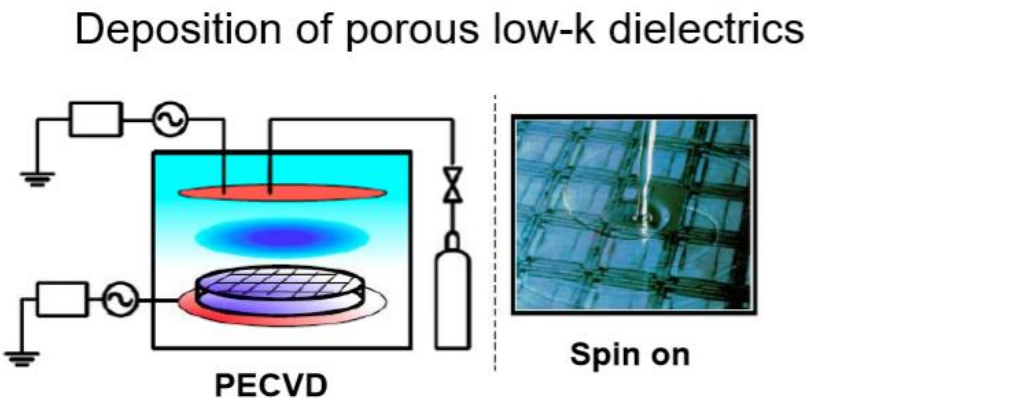
α_j: Polarizability of the combination of the material used

N_j, α_j, should be very low in order to achieve the low–k; The existed dielectric SiO_2 has a huge polarizability and density hence its k value stays between 3.9 ~4.4 which is normal k, low–k is even lower than that; Ultra low–k stands less than 2.5.

Low–k dielectrics used so far:

SiOF	3.4-3.6
Si Based (C doped)	
HSQ, MSQ	2.8-3.3
SiCOH	2.6-3.0
C based Polymers	
Non-fluoride	2.5-3.5
Fluorinated	1.9-3.0
Porous	
SiO_2 (aerogel, xerogel)	1.3-2.5
HSQ, MSQ	1.7-2.6
SiCOH	2.0-2.6

9. Process characteristics of PECVD and Spin on for low–k dielectrics.



+ Established equipment / process
+ New chemistries have been implemented
+ easier integration of the cure system into a cluster tool
- Limitations expected for materials with k < 2.2

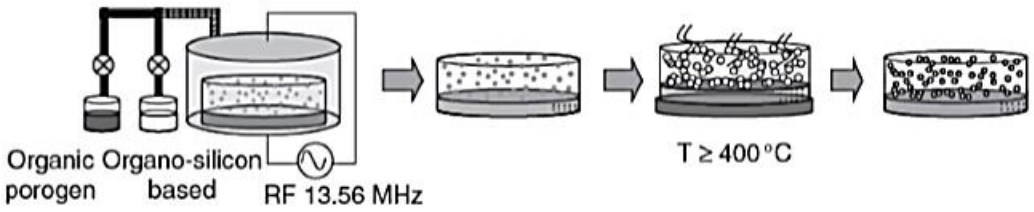
+ More simple process
+ Less expensive and easy to implement
+ Realistic solution for materials with k < 2.2
- Special equipment has to be purchased

Hybrid low-k integration (embedded low-k ILD) is expected

- Dense and porous low-k materials in dedicated levels and/or metal/via dielectric
- CVD and spin on to improve manufacturability and cost-of-ownership by eliminating process steps and allowing chipmakers to re-use their CVD equipment

10.

- **Describe the fabrication process for porous CDO/SiCOH films (type of process, precursors, post – treatment).**
- **How is the porosity in the film created?**
- **What is the role of the post-treatment & Which film properties are affected?**



Type of process used:

PECVD (Plasma Enhanced Chemical Vapor Deposition) porogen approach, deposition from the decomposition of (at least) two precursors in the plasma.

Currently used in high-volume manufacturing for 32 and 28nm technology.

Precursors:

- Pure organic molecule (porogen)
- Organo-Silicon (Matrix Precursor) (Molecule with Silicon atoms and Organic radicals)

Process Flow:

1. **Formation of a hybrid film** composed of ***Organo-Silicate-based matrix*** enclosing organo inclusions.
2. **Post-deposition treatment (curing)** for porogen removal **&** Cross Linking
   Example: Thermal annealing, removal of the organic phase consisting mostly porogen molecule fragments

   ➔ Film becomes Porous + Ultra Low–k

Film Properties affected:

- Mechanical stability (E, H)
- Porosity / density (optical – R.I)

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11.

- **Basic mechanism of sputtering process – How does the film deposition process work?**
- **Schematic cross section of conventional sputtering chamber (RF or DC magnetron).**

– **Name the modern sputtering principles to coat Contact & Via Holes with high aspect ratio.**

Sputtering is a process to deposit thin film on a substrate where the atoms are ejected from a solid target (Material to be deposited on the wafer) material by the bombardment of the target by energetic particles.

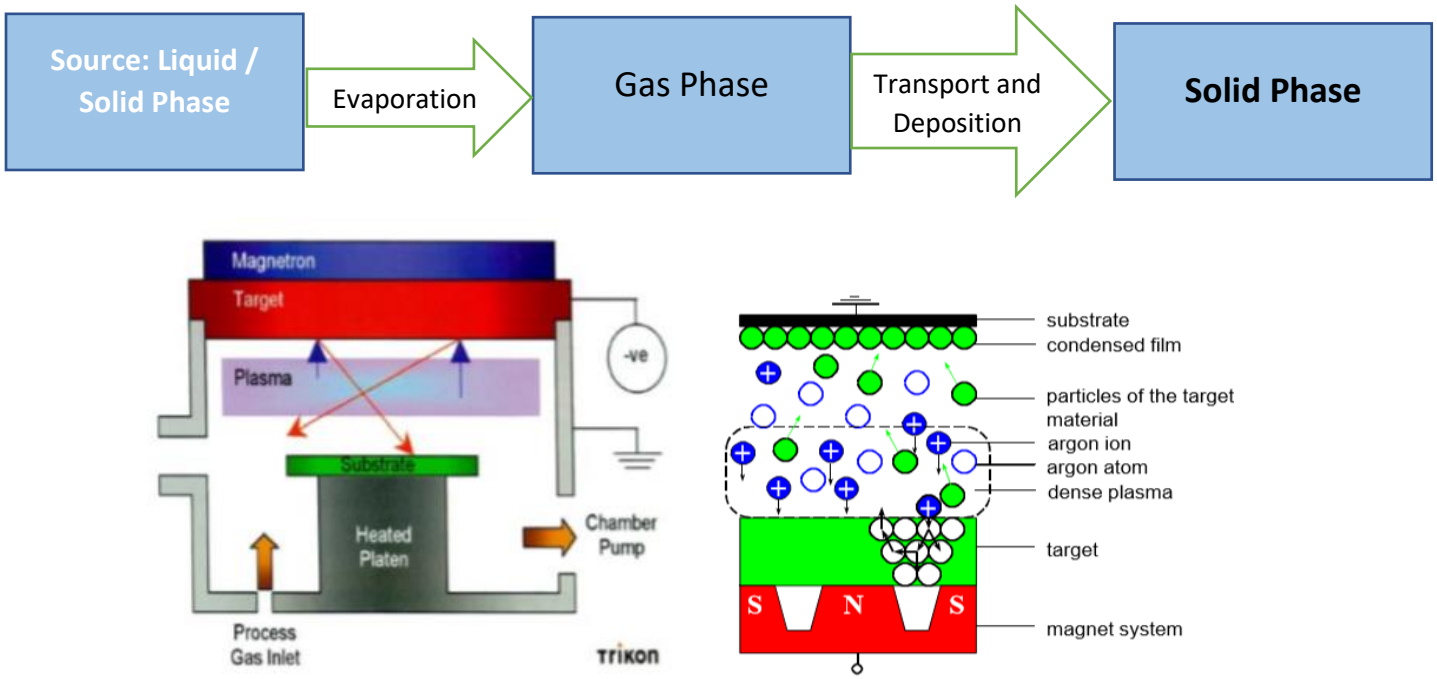

Figure 1 DC Magnetron Sputtering

Steps involved in Sputtering:

- Ions are generated & Directed at a target
- Ions sputter the target atoms
- The ejected atoms are transported to the substrate
- Atoms condense & form a thin film

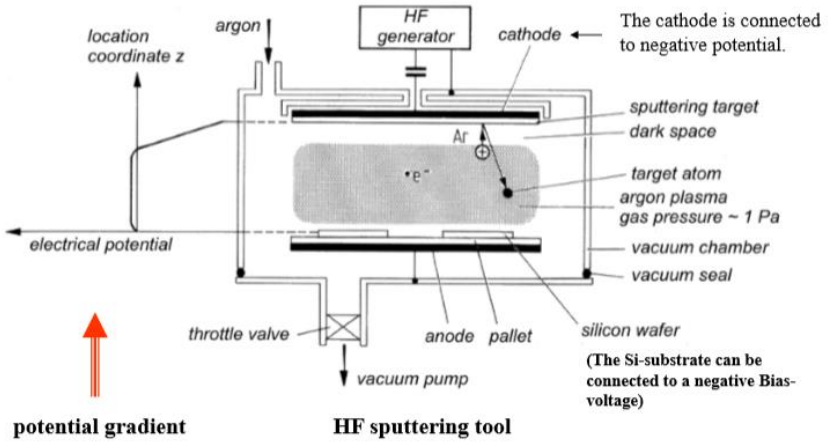

Figure 2 RF Sputtering

Modern Principles:

a. Ionized metal deposition
b. Collimated sputtering
c. Long throw sputtering

12.

- **Which kind of lithography is used in 32/38 nm technology nodes? Using the equation for minimum printable feature size l_{min}.**
- **Discuss how l_{min} can be reduced and thus even sub exposure wavelength feature sizes can be achieved. Name three resolution enhancement techniques.**

- *193nm immersion lithography* is used in 32/28nm technology nodes.
- $I_{min} = \frac{K_1 \times \lambda}{NA}$ K_1 – Rayleigh limit; $\lambda - Wavelength;$ NA: Numerical Aperture.
- **3 Ways to increase l_{min}:**
  - **I.** Reduce λ
  - **II.** Increase NA (Immersion-Litho)
  - **III.** Reduce K_1(RET)
- **3 resolution enhancement techniques:**
  - **I.** Optical proximity correction (OPC)
  - **II.** Off-axis illumination (OAI)
  - **III.** Phase shift masks (PSM)
  - **IV.** Double exposure / double patterning (DA)

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13. Name at least two processes for dry photo resist removal.

- Plasma Stripping (in barrel reactors)
- Downstream stripping
- Plasma free (ozone & UV) Stripping

14.

- **Name the process modules of conventional (Si-gate, Si bulk CMOS Technology Front End Process flow in the Right Sequence.**
- **Mark the borderline between FEOL and BEOL in the sequence.**

Process Modules (0.25 µm and below):

1. Shallow Trench Isolation (STI)
2. Twin-Well Implants
3. Gate Structure
4. Lightly doped drain implants
5. Sidewall Spacer
6. Source/Drain Implants
7. Contact Formation

FEOL (FRONT END OF LINE)

8. Local Interconnect
9. Via-1 / Metal 1 Formation
10. Via-2 / Metal 2 Formation
11. Via-3 / Metal 3 Formation
12. Via-4 / Metal 4 Formation
13. Bond Pad Metal & Passivation
14. Parametric Testing

BEOL (BACK END OF LINE)

15.

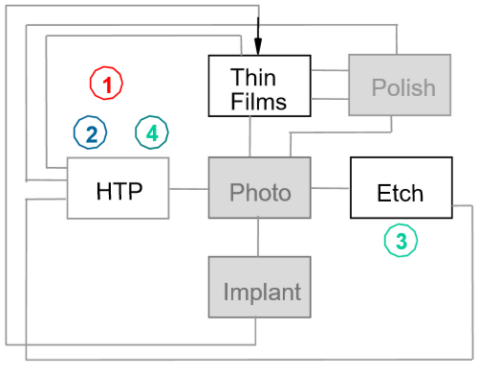
- **Describe the process flow of the process module "contact formation" by naming the basic process steps for its realization.**
- **Enhance this by detailing process parameters and additional explanations for these basic process steps, if presented in the lecture.**
- **Draw the cross – section of CMOS structure in the different stages of this process module to visualize the sequence.**
- **Why do we need to use Silicide for S/D and gate contact?**

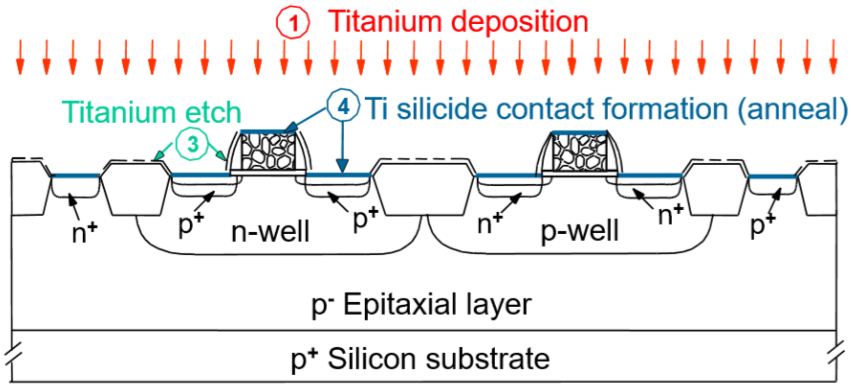
Remark ①: - You may group two or more basic process steps in one picture as far as they are clearly identified.

Remark ②: - Once you have drawn the detail CMOS base structure cross-section in 1st figure, you may use a simplified base structures in your drawings for the next steps.

Process Flow for Contact Formation:

- Removal of oxide from S/D and Poly Gate.
- Sputtering metal with Argon ①
- Anneal to form $TiSi_2$(RTP1) ②
- Chemical Wet etching to remove unreacted Ti, Leaving $TiSi_2$(Selective Etching) ③
- Anneal to form low resistivity TiSi2 (RTP2) ④





Need for using Silicides:

Channel length directly influences the increase of gate resistance. Hence to minimize this kind of parasitic resistances.

This silicide is used for:

- Polycide gate (silicide on polysilicon)
- SAlicide (self-aligned silicide) on source-drain
- Local interconnection between devices, e.g., between source/drain diffusion of one device to gate of another in a SRAM cell.

Why particularly this silicide:

- Low resistance
- Little or no electro migration
- Easy to dry etch
- Good contacts to other materials
- Good process compatibility with Silicon

16.

- **What is the motivation to use high–k / metal gate (HKMG) structures instead of conventional SiO_2/Poly-Si gate structures?**
- **Name the two technology approaches for HKMG and discuss advantages & drawbacks of each one.**

- **Motivation to use High–k metal gate:**
  - In conventional SiO_2/Poly-Si gate further miniaturization of device i.e., below 2nm would not be possible because of the tunneling currents / leakage currents.
  - Standby, power consumption or reliability of the device is not that great in conventional gate dielectric materials because of leakage currents.
  - Hence this HKMG makes sure there is no leakage currents through higher gate capacitances.

- **Two Integration Techniques for HKMG:**

1. **Gate first MIPS: Metal Inserted Poly Silicon**

Pros	Cons
○ Conventional Process Flow	○ Thermal budget ○ Complex V_T Tuning ○ Mobility, Reliability at thin EOT

2. **Gage Last RMG: Replacement Metal Gate**

Pros	Cons
○ Thermal Budget ○ Higher strain from embedded SiGe S/D	○ Complexity, Cost ○ More Restricted design rules

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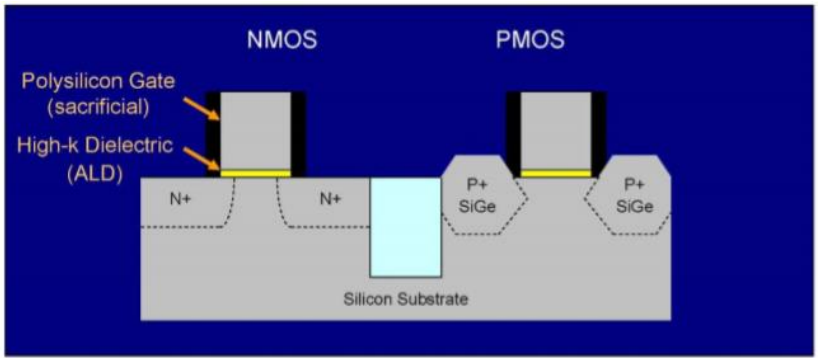
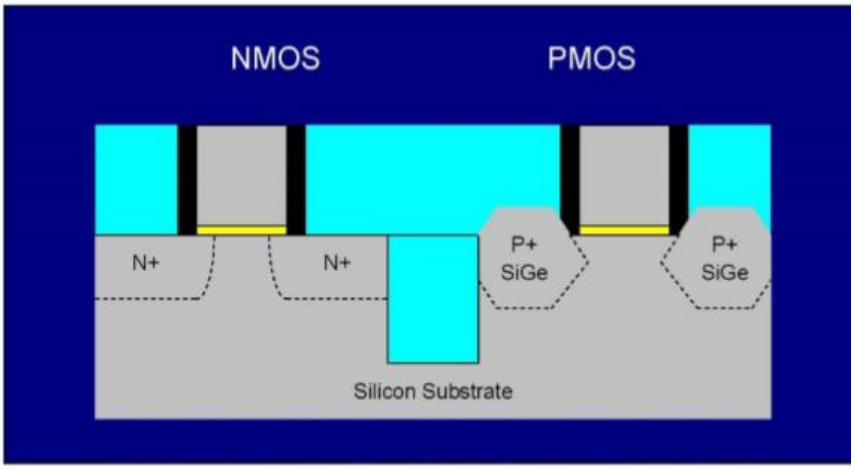
17.

- **Describe the process flow of the process module "HKMG Gate Last Approach" by naming & briefly describing the five steps of its realization.**
- **Draw the schematic cross sections of the gate structures in different stages of this process module to visualize the sequence.**

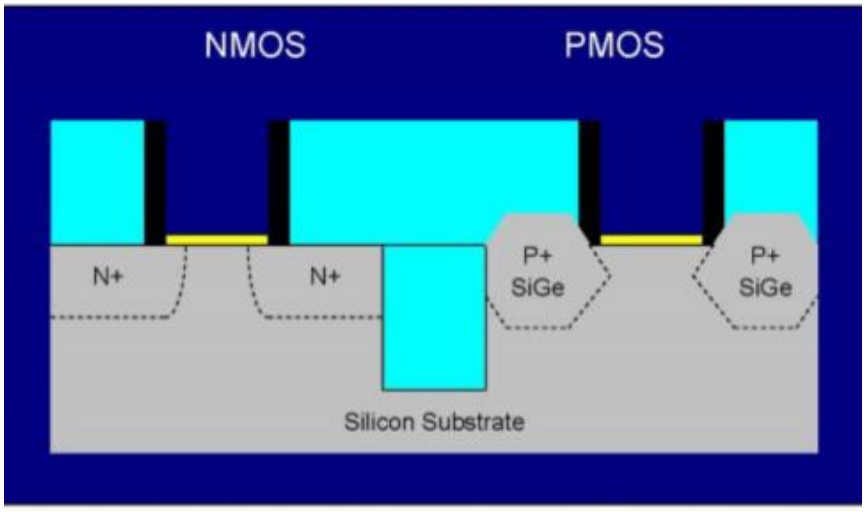
① Standard transistor process through source–drain formation but including atomic layer deposition high–K dielectric.



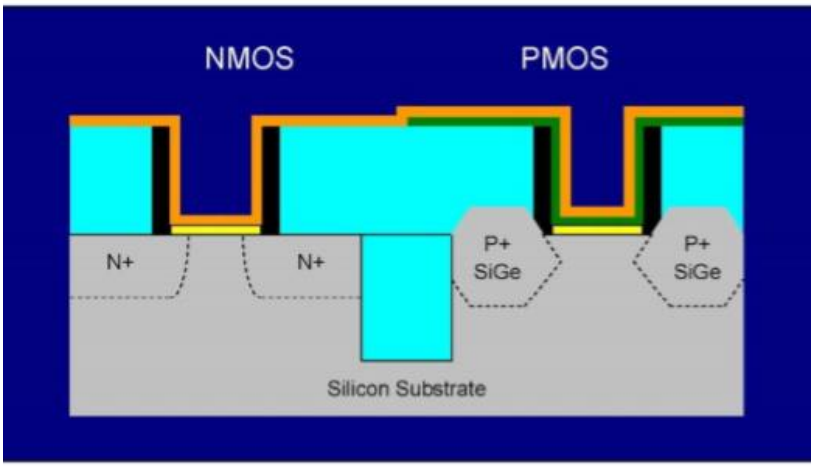
② Deposit and Planarize oxide layer



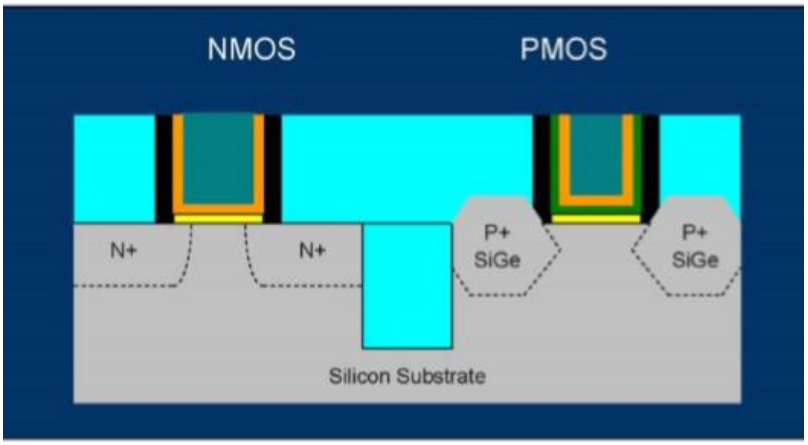
③ Etchout sacrificial polysilicon gate



④ Deposit Sperate NMOS and PMOS WF Metal layers



⑤ Deposite Al fill metal, planarize surface



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18.

- **CVD of silicon nitride is widely used in CMOS Technology.**
- **Name four applications of silicon nitride thin films including the specific function of the Si Nitride.**
- **Provide the respective process module in which this application is implemented.**

Applications & Their Process Modules:

Applications	Process Modules
○ CMP–Stop layer in shallow trench isolation	STP
○ Etch–Stop layer in damascene structures	Vias / Metals
○ As stressor film(s) over n- and p-MOS transistors	NMOS / PMOS layouts
○ Side wall spacer to form LDD Structure & to serve as sidewall passivation during SAlicide process	Side wall Spacer
○ A mask for the selective oxidation of silicon	LPCVD
○ As final passivation and mechanical protective layers for IC encapsulated plastic packages	Passivation

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19.

- **Name three resolution enhancement techniques.**
- **Explain one in detail, if necessary, use a schematic.**

I. Optical Proximity Correction (OPC)
II. Off-Axis Illumination (OAI)
III. Phase Shift Masks (PSM)
IV. Double Exposure (DE)

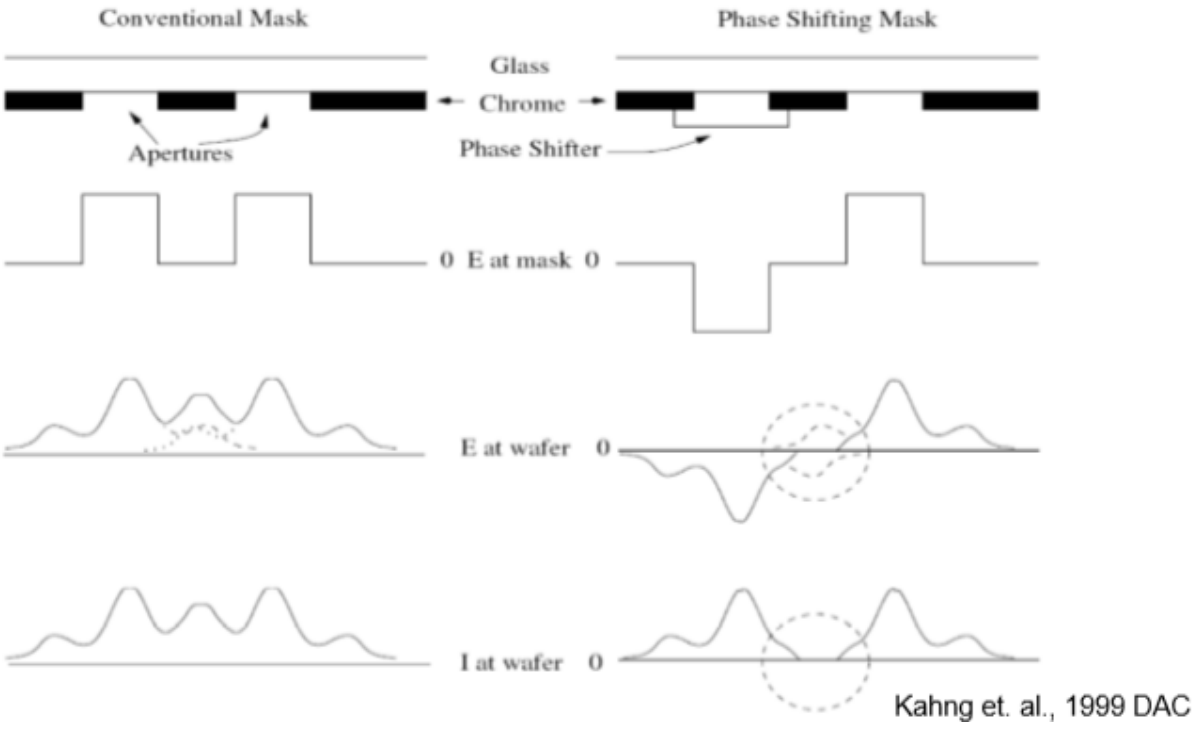
Phase Shift Masks (PSM):

Purpose:

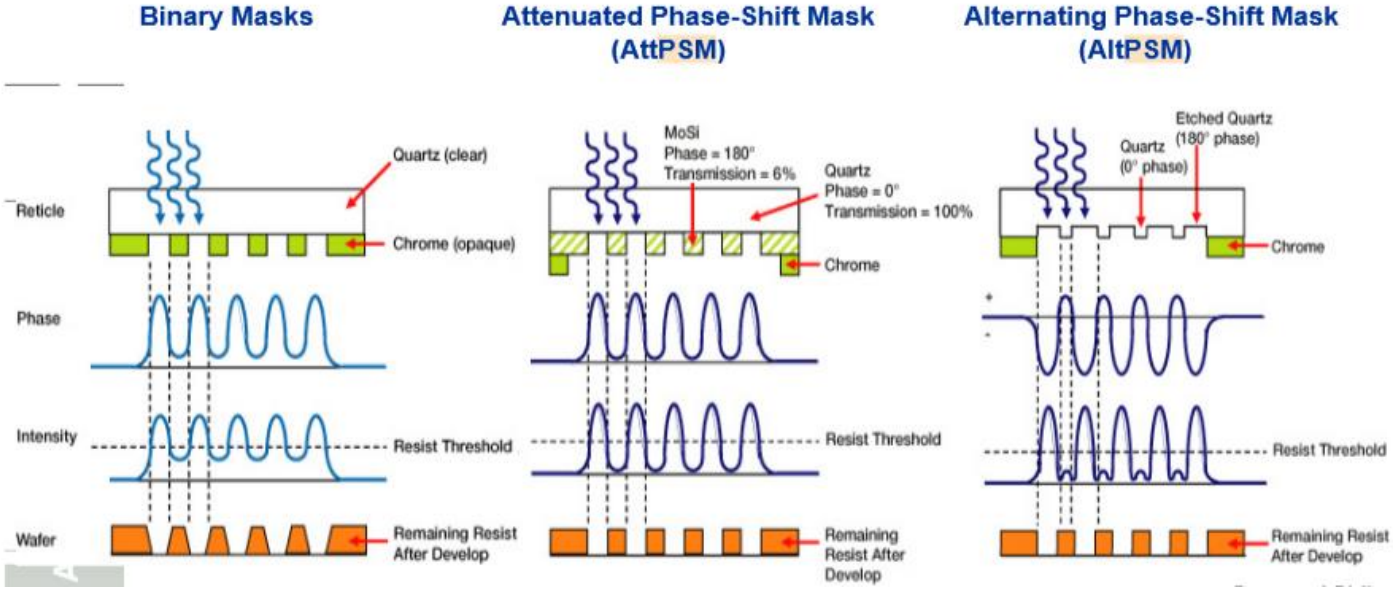
Enhanced contrast –> Enhanced Resolution –> Improvement of process window

Basic Principle:

Introduction of a phase difference of 180^0 on specific parts of the mask structure.



Kahng et. al., 1999 DAC



- The Phase Shifter reverses the sign of the electric field.
- The light diffracted into the nominally dark region will interface destructively.

- So PSM can help in resolving the features which may be violating the minimum spacing design rule by assigning opposite phases to the conflicting features.

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20. In ion implantation process the so called "channeling effect" can be observed under certain conditions. Please name two measures to prevent the appearances of the effect in practical applications.

- Inclination of the ion beam against the surface normal of the wafer (minimum channeling at 7^{o}–10^{o})
- Amorphous cover layers (Scattering Oxide)
- Pre-amorphization (e.g. Si^{+} in Si)

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21. Which two basic metallization process sequences do exist for fabrication of the interconnect system? Name the conductor materials used in each of them for the via & the line respectively.

	Via	**Line**
Subtractive	W	Al
Dual Damascene	Cu	Cu

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22.

- **What is the motivation to use local stress/strain generator strained silicon in CMOS transistors?**
- **Which type of strain do you need to enhance the NMOS & PMOS transistors respectively?**
- **Name two approaches for local stress generation in CMOS transistors.**

Motivation to use strained Silicon:

- Used as the transistor channel in CMOS
- Increases the mobility of charge carriers
- Electron mobility of charge in strained silicon is two times that of relaxed silicon
- Peak mobility gain occurs at standard operating temperatures
- Increases the circuit speed, reduces power consumption
- Based on existing infrastructure

Which Type:

- P-Type (PMOS) – Comprehensive (SiGe on Source and Drain)
- N–Type (NMOS) –Tensile (Silicon nitride capping film)

Approaches to generate local stress generation:

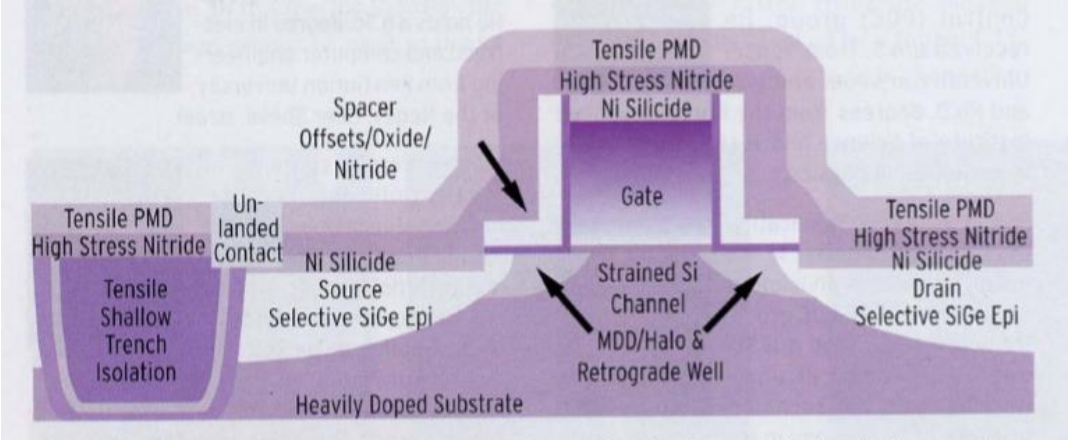

Figure 1. CMOS transistor schematic showing key methods of generating local stress, such as

- Tensile/Compressive SiN Layer
- PMD layer
- STI Liner and recessed SiGe S/D

Stress from these layers induces uniaxial strain in the channel, leads to higher mobility and higher drive current.

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23. Please name two future transistor options which allow further IC Performance improvements or going beyond MOSFET.

- Multi-gate FIN Transistors
- Tunnel Transistors
- Advanced channel materials (Ge Transistors)

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24.

- **What is the motivation to use short duration annealing process?**
- **Please name two of these short annealing processes & provide the approximate process time (order of magnitude) & broadening of dopant concentration profiles at 1100°C due to diffusion for the above-mentioned process times.**

Motivation to use Annealing:

- ✓ High degree of **dopant activation**
  (depends on temperature, about 900°C are necessary for Si)
- ✓ Achievement of superior **Crystal Properties** (mobility μ, Minority life time ƈ)

Methods of Annealing:

Annealing Method	**Process temperatures**	**Process Time**	**Broadening of profiles during process time at T = 1100°C.**
Furnace (Ex: in N_2, H_2)	900-1100	Min, h	1 μm (1000 s)
Rapid thermal processing (RTP)	1000-1250	S	01μm(10s)
Flash Lamp	1000-1300	ms	0.01 μm (0.01s)
Laser	1100-1400	μs	<0.01μm(001s)

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25.

- **Describe the process flow of copper dual damascene process.**
- **Explain the challenges in doing Dual Damascene Process.**

Process flow for Dual Copper Damascene Process:

- ✓ Very much like Single Damascene process except using two di-electric etch process steps
  - Creates Vias and Lines by etching holes and trenches in the dielectric, and then depositing copper in both features.
  - One Via creation by etching a hole & One Trench creation by etching a trench
- ✓ The above are two steps of etch processes, can be performed in any order *(Trench first then Via / Via first then Trench).*
- ✓ Then these etch gaps are filled with required metals.
- ✓ Excess metal is removed using CMP.
- ✓ If required, the Di-electric is redeposited.

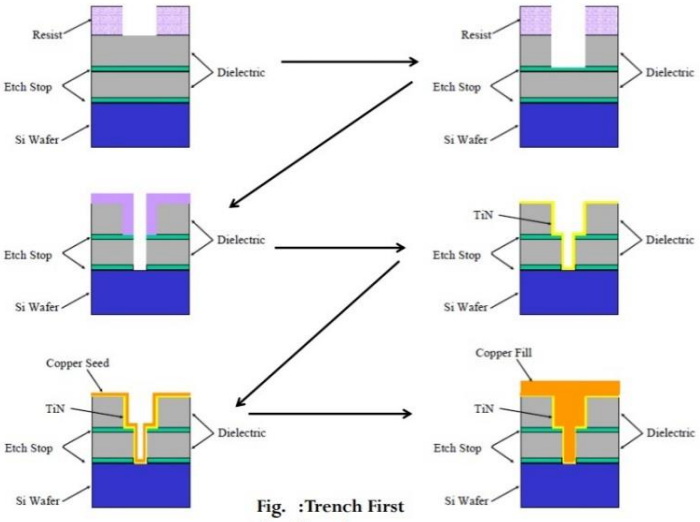

Fig. :Trench First then Trench

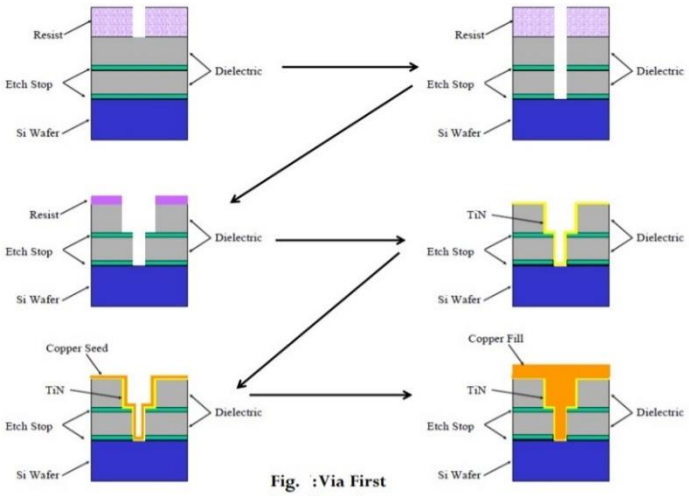

Fig. :Via First then Trench

Challenges in doing Dual Damascene Process:

➔ **Via First then Trench Approach:**

Residual photoresist remains in the bottom of the via during the trench etch, it is absorbed and alters the K value of dielectric.

➔ **Trench first then Via approach:**

Photoresist also pools in the open trench structure prior to via patterning

➔ **Most Low–k dielectric films are hydrophilic**

It is critical that surface hard mask (photoresist) shield the dielectric from moisture as well as protect dielectric from aggressive cleans.

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26.

- **Name the four "gas deposition processes" used in advanced CMOS IC Technology.**
- **For each of these processes give one example for a material/thin film deposited in front end technology in *production* as well as one example for a process module, where this process is applied in *production*! (If necessary, use a table)**

1. Chemical Vapor Deposition (CVD)
2. Epitaxy
3. Atomic Layer Deposition (ALD)
4. Sputtering/Physical Vapor Deposition

Process	Materials	Application in CMOS	Process Modules
CVD **(to deposit this films)**	I. Poly Silicon	Gate	Gate Structure
	II. W, Cu, AL	Inter Connect system	Vias / Trenches
Epitaxy **(to make single crystalline on top)**	Si	CMOS P^- Level	STI
ALD **(to have more chemical precursors while depositing thin films)**	HFOx	HKMG	Gate Structure
Sputtering (PVD) **(Sputtering / evaporation)**	TaN, Ta	Cu Dual Damascene	Vias / Trenches

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27.

- **What is the definition for "Chemical Mechanical planarization (CMP)"?**
- **which capabilities does the CPM process have?**
- **Provide three examples for application of CMP in IC Technology.**
- **Please name the consumables used in CMP Process.**
- **Draw a schematic of the 1. CMP equipment configuration, 2. Polishing Pad and Pad Conditioner, 3. Polishing Head.**

Chemical Mechanical Planarization (CMP):

Chemical Mechanical Planarization (CMP) is mechanically enhanced chemical etching or chemically enhanced mechanical grinding to planarize surfaces by removing unwantedly present material after some other process steps.

Capabilities of CMP:

- Can planarize surfaces by removal of materials such that topography is eliminated, or material is left at defined areas.
- CMP provides local and global planarity
- CMP enables indirect patterning due to an adjustable polish selectivity between different materials.

Example Applications:

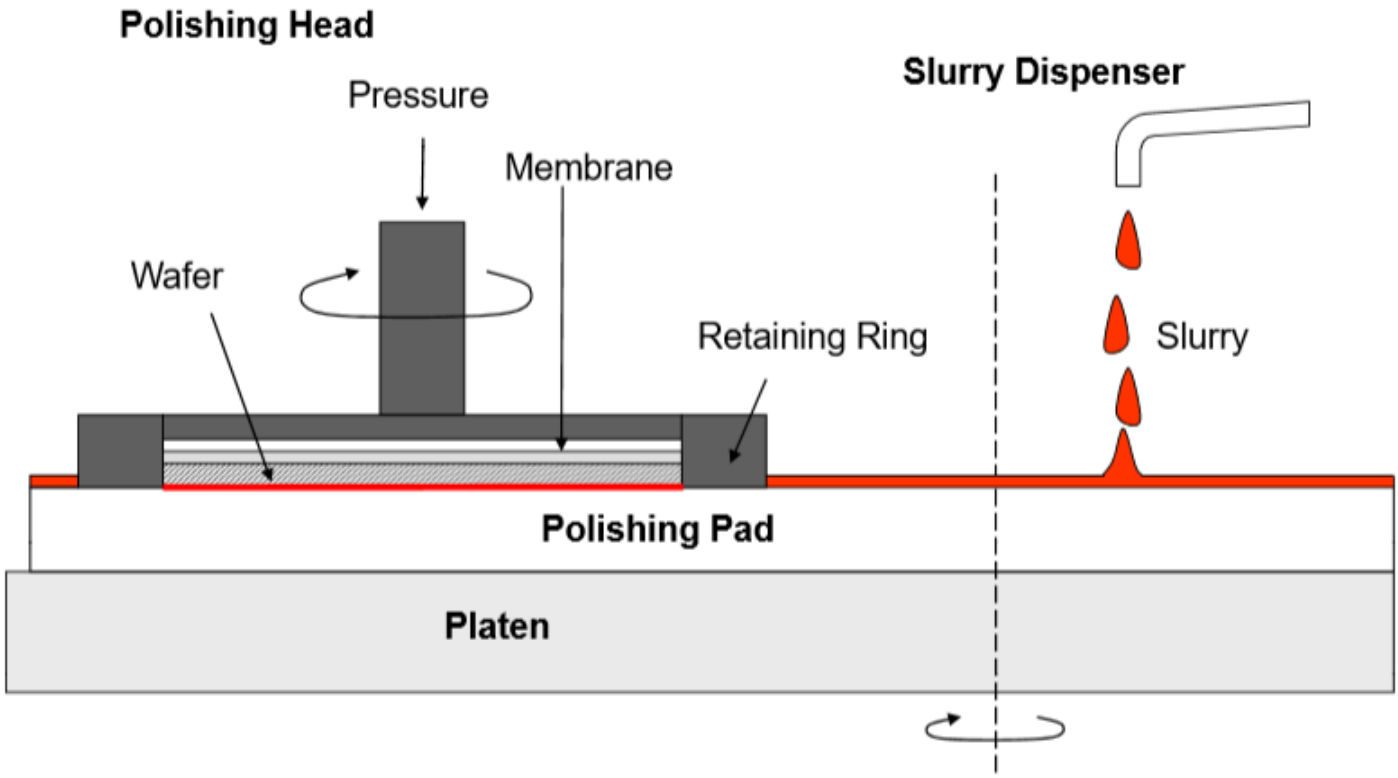
- STI Formation
- Tungsten plug formation
- Deep trench capacitor
- Cu dual damascene

Consumables in CMP:

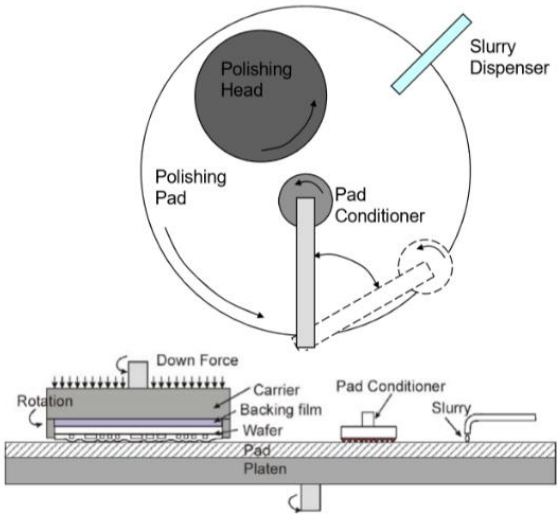
I. Slurries
II. Pads
III. Brushes and Conditioner

Schematics –

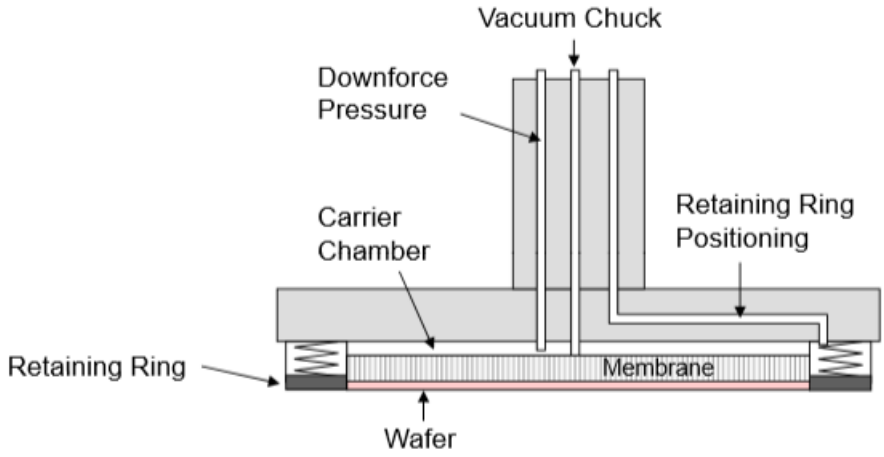
1. **CMP Equipment Configuration:**



2. **Polishing pad and Pad conditioner of CMP**



3. Polishing Head:

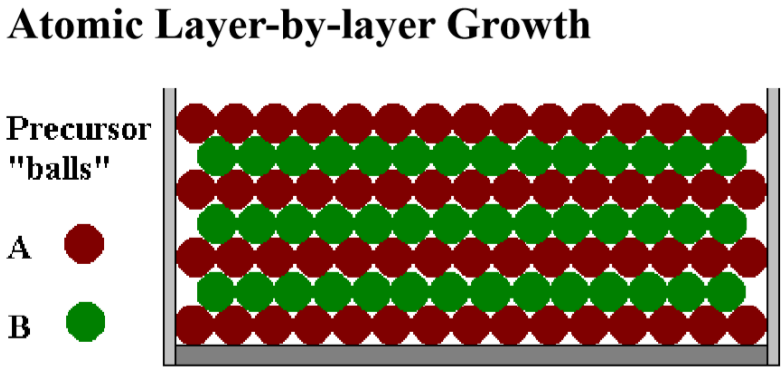


28.

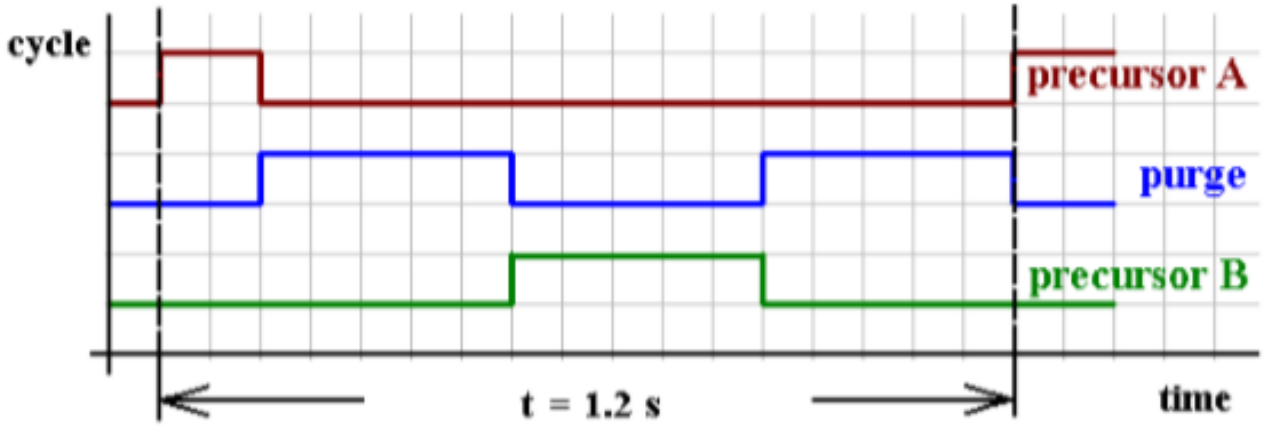
- **What is ALD?**
- **Draw the diagram of the gas flow sequence of one Atomic Layer Deposition (ALD) cycle(s).**
- **Name three applications of ALD processes currently used or to be potentially used in future in production of advanced integrated circuit technology / Give some applications of ALD.**

Atomic Layer Deposition (ALD):

Atomic layer deposition (ALD) is a thin-film deposition technique based on the sequential use of a gas phase chemical process; it is a subclass of chemical vapor deposition. The majority of ALD reactions use two chemicals called precursors.



Gas flow diagram/sequence of ALD Cycle(s):



Applications of ALD:

1. ALD of high–k dielectrics
2. ALD of diffusion barriers
3. Copper ALD for seed layers in Cu damascene

29.

- **In which process module is Tungsten(W) CVD applied in current IC Production?**
- **Give the chemical reaction of a tungsten CVD process using tungsten hexafluoride precursor and hydrogen reduction gas indicating either solid(S), liquid(L) or gaseous(G) state of the reactants and reaction products.**

Process used the Tungsten(W) CVD:

Metal layers or Interconnect lines/wires/systems use this Tungsten(W).

Chemical Reactions involved in Tungsten(W) CVD:

I. **Hydrogen reduction of WF_6 –> blanket W deposition for contact and Via fill**

$$WF_6 + 3H_2 \rightarrow W\downarrow + 6HF\uparrow$$

II. **Silane reduction of WF_6 –>** **nucleation step for blanket W CVD**
Selective deposition for contact / Via fill

$$2\,WF_6 + 3\,SiH_4 \rightarrow 2\,W\downarrow + 3\,SiF_4\uparrow + 6\,H_2\uparrow$$

$$WF_6 + 2\,SiH_4 \rightarrow W\downarrow + 3\,SiHF_3\uparrow + 3\,H_2\uparrow$$

III. **Silicon reduction of WF_6: parasitic reaction during contact fill on Si**

$$2\,WF_6 + 3\,Si \rightarrow 2\,W\downarrow + 3\,SiF_4\uparrow \; < 400^oC$$

$$WF_6 + 3\,Si \rightarrow W\downarrow + 3\,SiF_2\uparrow \; > 500^oC$$

IV. **Aluminum reduction of WF_6: parasitic reaction during via fill**

$$WF_6 + 2\,Al \rightarrow W\downarrow + 2AlF_3\uparrow$$

30.

- **What is the advantage of using cluster tools in semiconductor process?**
- **Give an example for an integrated process flow performed in a cluster tool and draw a schematic of this cluster remote components like pumps, heat exchanges etc...**

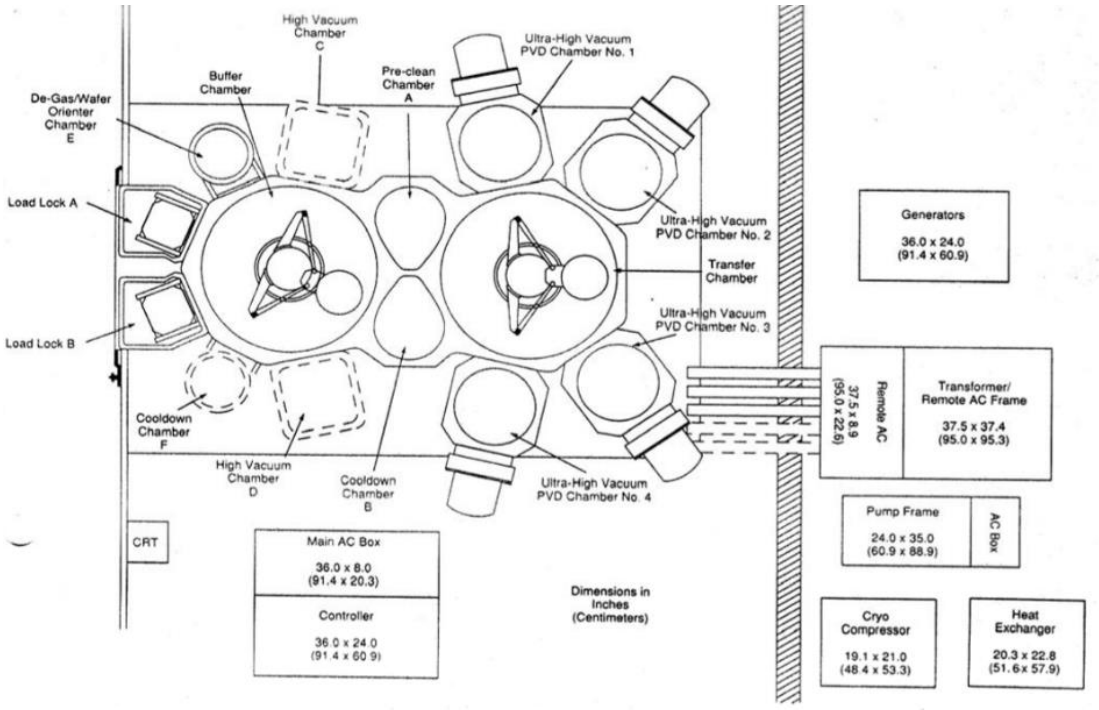
Advantages of Cluster Tool:

- Short Cycle times
- Fast process development
- Higher yield efficiency
- Less risk of contamination.

Example of Integrated process:

Pre-Clean —> TiN CVD —> WCVD

Schematic of cluster tool:



Endura 5500: cluster tool. Applied Materials, USA

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31. Gas V/S Liquid phase deposition. (Comparison in terms of type process, materials used, application in CMOS, and Process Modules)

32.

- **Which types of CVD processes do you know?**
- **Which types of chemical reactions are mainly involved?**

33.

- **Diffusion barriers**
- **Requirements for diffusion barriers**
- **CVD of TiN (Process)**
- **Precursors**
- **Characteristics of the process**
- **Definition of the Step Coverage**

!!For the answers of 31, 32, 33 please refer the Übung (Seminar SS2019) notes!!