3.1.4 Low-k dielectrics

Authors: S.E. Schulz, N. Ahner

(A) Overview and application requirements

- **Challenge: Shrinking sizes - RC delay**
- **Solution: Change dielectric material and metal**
- **Dense, porous or air gaps: low *k* materials concepts**
- **Application requirements**

(B) Depositon of porous low-k dielectrics

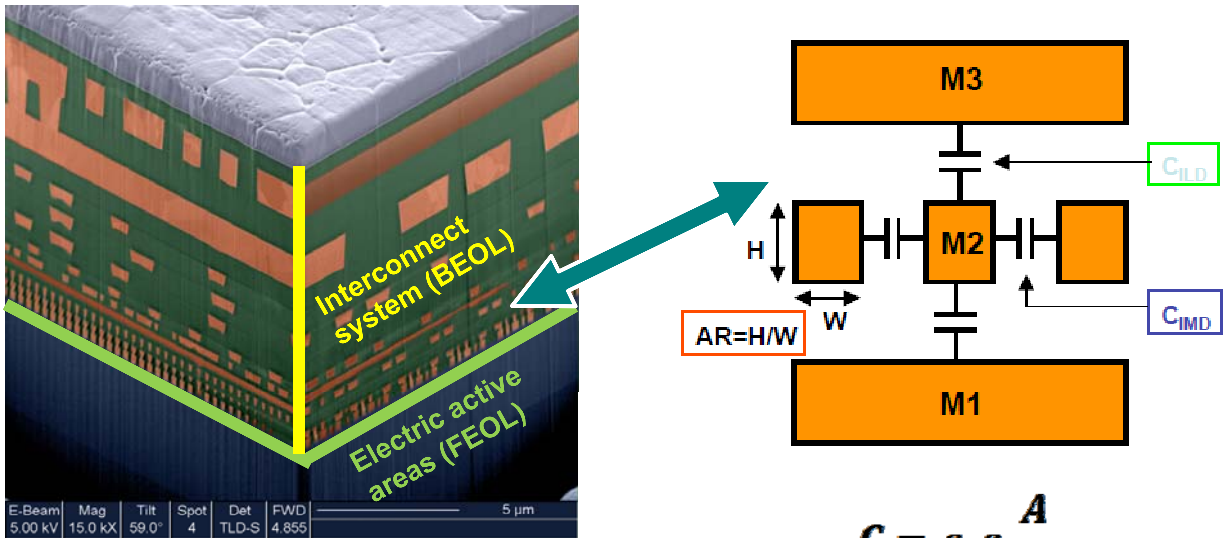
- **PECVD vs. Spin coating**
- **Porous SiCOH by PECVD and UV assisted curing**

(C) Future of low-k dielectrics

- **ITRS predictions on ILD k-values**
- **New developments and emerging materials**

Status: 30.04.2014

Interconnect Challenges – Shrinking feature sizes



$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

Integration of dielectric materials with lower permittivity (k-value)

RC-Delay

$$\tau \propto RC_{inttot}$$

Power

$$P = \alpha C_{inttot} V^2 f \propto C_{inttot}$$

Crosstalk

$$X_{talk} \propto \frac{C_{IMD}}{C_{inttot}} = \frac{1}{1 + \frac{\left(\varepsilon_{ILD} / \varepsilon_{IMD}\right)}{AR^2}}$$

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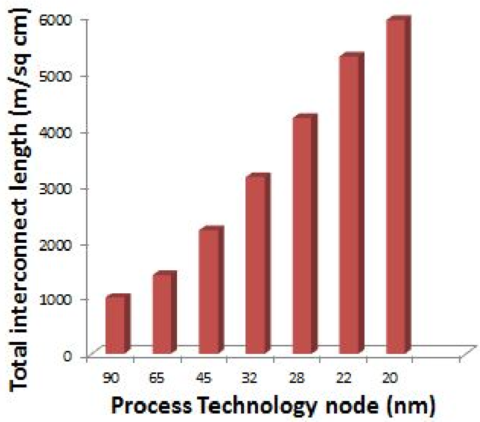
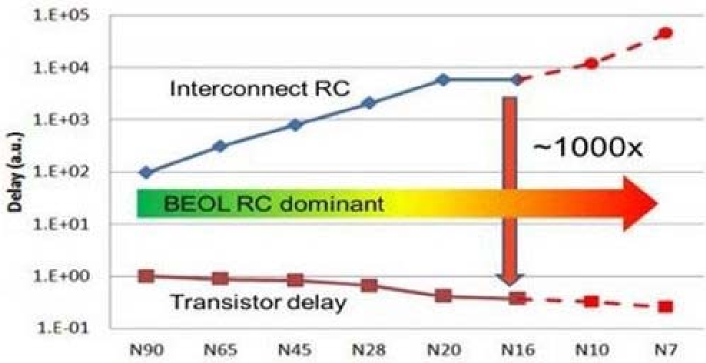
Interconnect Challenges – RC delay dominance



Source : Data Derived from ITRS Interconnect Tables



Source: EET Asia

With further downscaling the next IC generations become „interconnect heavy", more than 50 per cent of their cost is due to the back-end-of-line (BEOL) wiring levels, and designs are dominated by interconnect delay.

Source: http://www.eetasia.com/ART_8800696620_590626_NT_d54bc924.HTM, March 28th 2014

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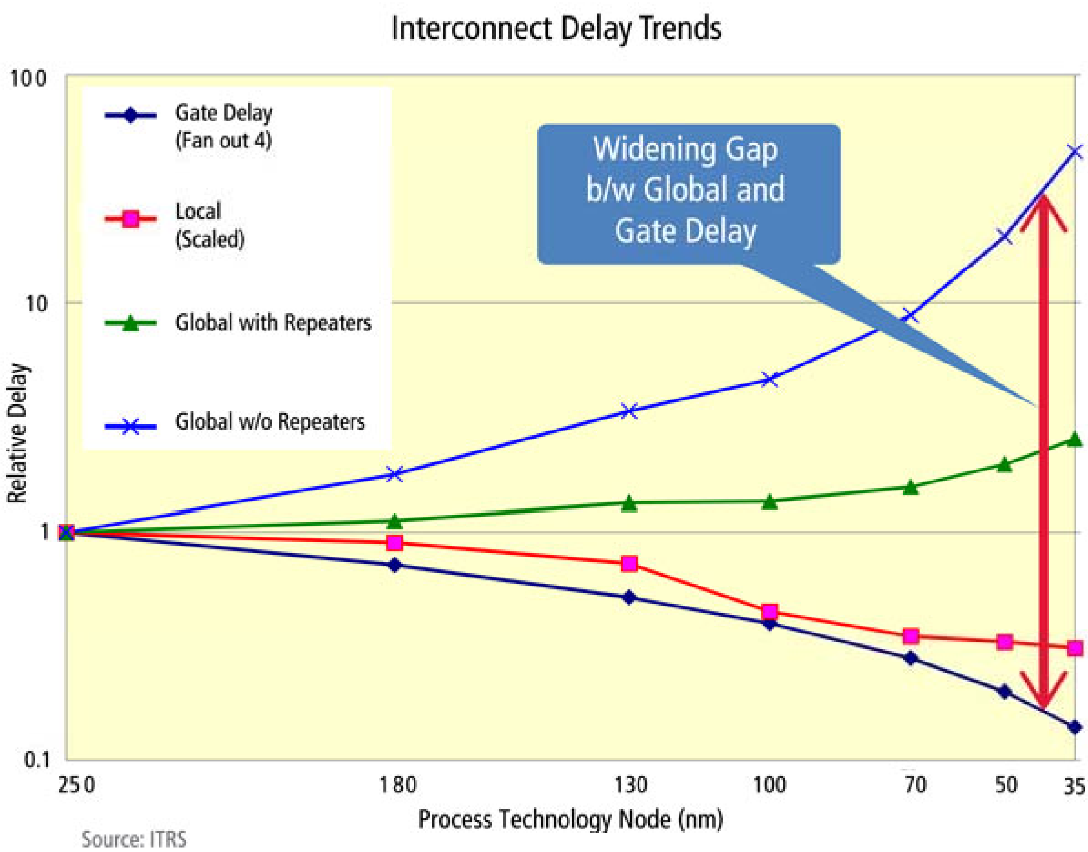
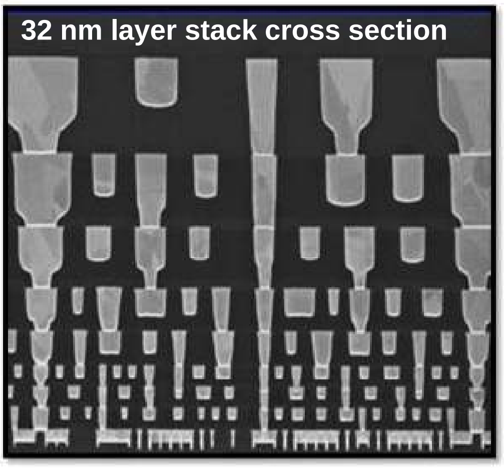
Interconnect Challenges – RC delay evolution

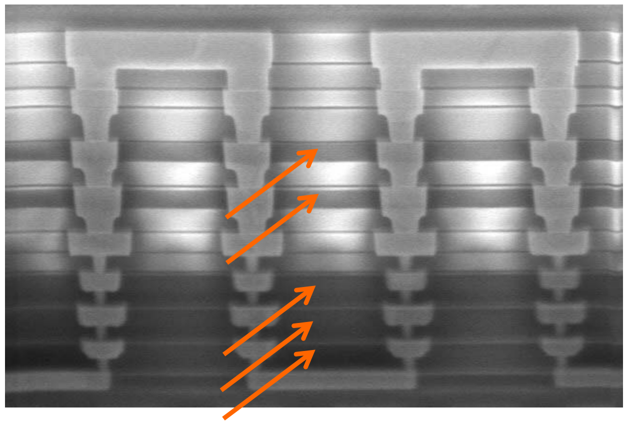


Source: ITRS

How to fight RC delay – Design, Architecture, Technology



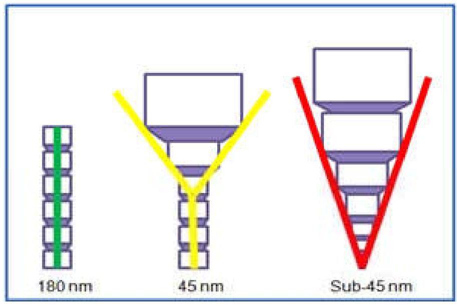
Source : Intel



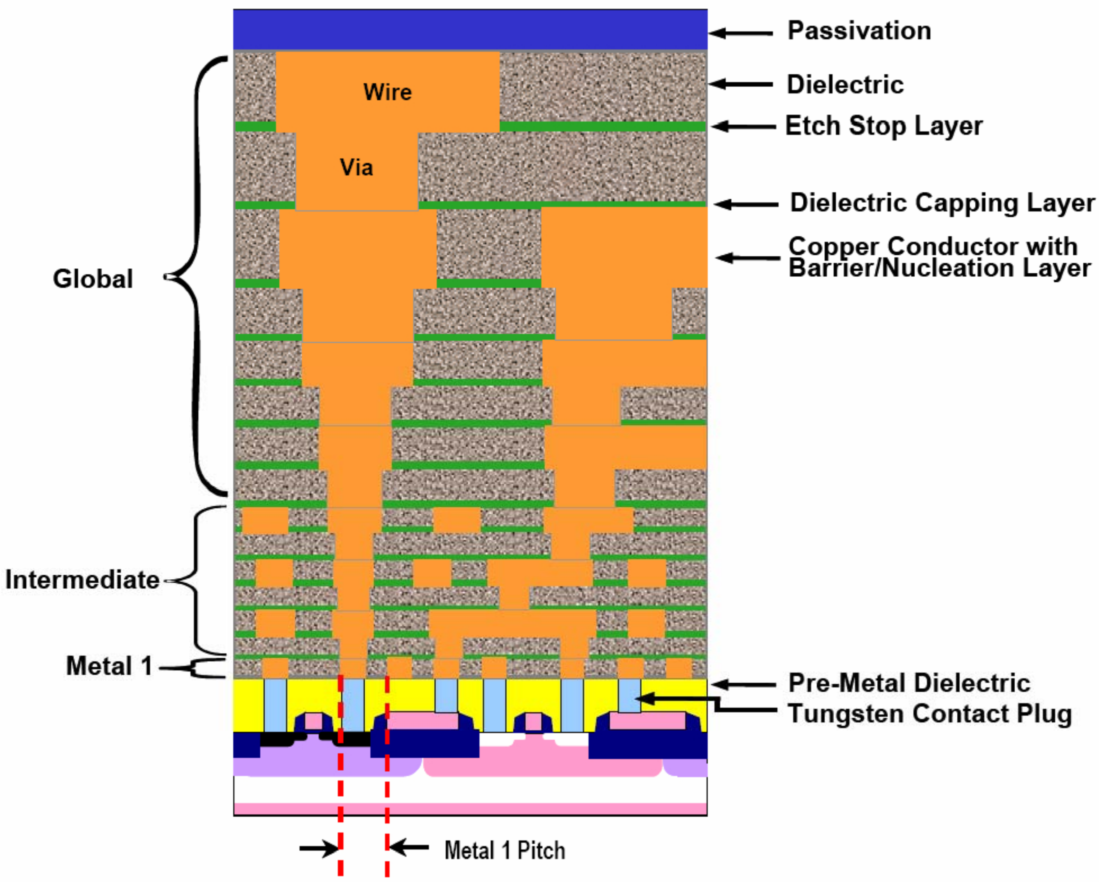
FIB cross-section of a 9 metal layer test structure with Cu/low-k (OSG) interconnect stack (Source: Fraunhofer IZFP)

Hierarchical wiring (reverse scaling)

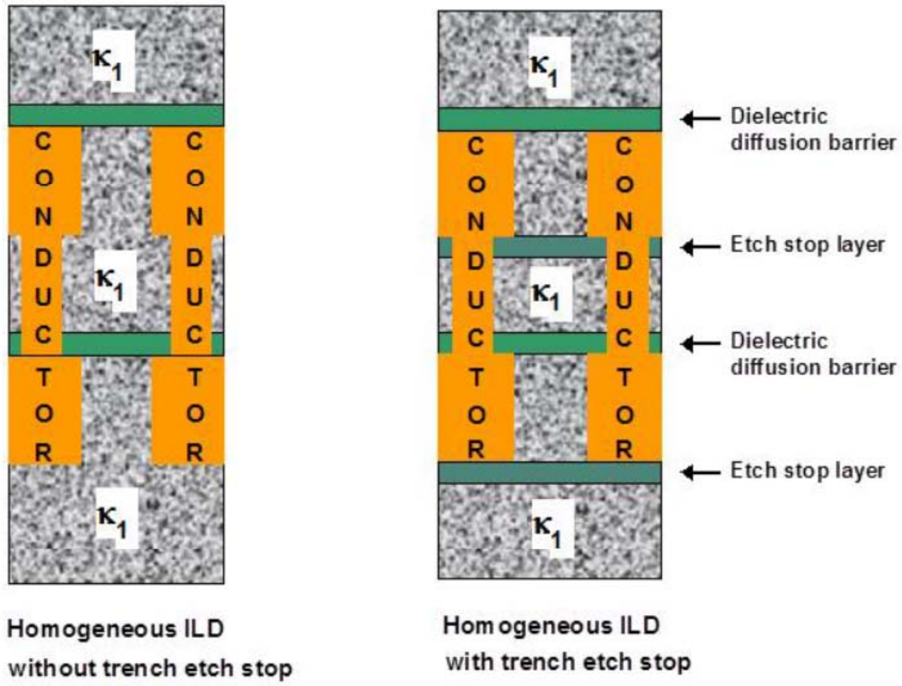
Metal layer stack variation across process nodes



Multilevel Metallization: Hierarchical Architecture



Typical ILD Architechtures



ITRS 2011

Fighting RC delay increase – materials approach

Solution

Dielectric material → Reduction of permittivity:

Substitution of low-k materials for SiO_2

⇒ reduction of permittivity up to about 60 %
but:
- huge variety of proposed low-*k* materials
- many challenges to process compatibility

Metal → Reduction of metal resistivity:

Substitution of Cu for Al

⇒ reduction of resistivity about 35 %

Dielectric	Permittivity
SiO_2	3.9 ... 4.1
Low *k*	1.5 ... 3.5

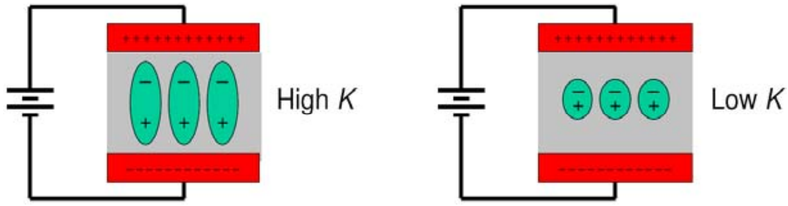
Metal	Resistivity [µOhm cm]
Al alloy	~ 3.0 ... 3.3
Cu	~ 1.9

How to achieve a low dielectric constant k?

k: physical measure of the electronic polarizability of a material

- Electronic polarizability: tendency of a material to allow an externally applied electric field to induce electric dipoles (separated positive and negative charges)

$$\frac{\varepsilon - 1}{\varepsilon + 2} = \frac{1}{3\varepsilon_o} \sum N_j \alpha_j \downarrow$$



N_j = total number of the atoms or molecules
α_j = polarizability of that particular atoms or molecules

A low-k dielectric is an insulating material that exhibits weak polarization when subjected to an externally applied electric field.

→ low-k: k is lower than that of SiO_2 (3.9 to ~4.4)
→ ultra low-k: k < 2.5

How to build a low dielectric constant material?

1. Minimize polarizability

- Choose a nonpolar dielectric system: polarity is weak in materials with few polar chemical groups and with symmetry to cancel the dipoles of chemical bonds between dissimilar atoms

- Introduce elements with smaller electronic polarizability, e.g. C, F

Bond	C–C	C–F	C–O	C–H	O–H	C=O	C=C	C≡C	C≡N
Polarizability (Å)	0.53	0.56	0.58	0.65	0.71	1.02	1.64	2.04	2.24

(Source: K.J. Miller et al., Macromolecules, 23, 3855 (1990))

- Minimize the moisture content of the dielectric / design a dielectric with minimum hydrophilicity ($k_{water} \approx 80$ → only small traces of water need to be absorbed before the low-k dielectric loses its permittivity advantage)

How to build a low dielectric constant k material?

2. Increase the free volume → reduce N_j

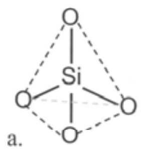
Microscopic level:

→ increase bonding length, bonding orientation, e.g. partially substitute Si-O (1.5097 Å) by Si-CH_3 (1.857 Å)

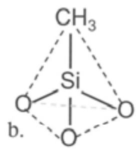
→ discontinue the network by inserting single bond atoms or groups in the backbone structure: adding F or CH_3 into SiO_2 network

Macroscopic level:

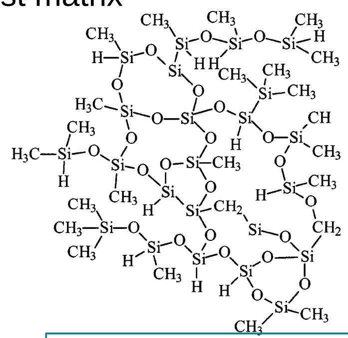
→ Add porosity (k_{air} = 1): incorporation of a thermally degradable material (porogen) within a host matrix



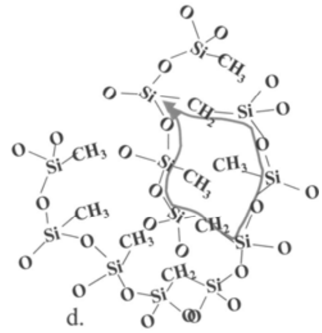
SiO_2
k ≈ 4.0



C-doped oxide
k ≈ 3.0



Dense SiCOH
(Precursor TMCTS)
k min. 2,6



Porous SiCOH
(Precursor TMCTS + Porogen)
k ≈ 2,1 – 2,5

Low-k dielectric materials: Ultra low-k materials concepts

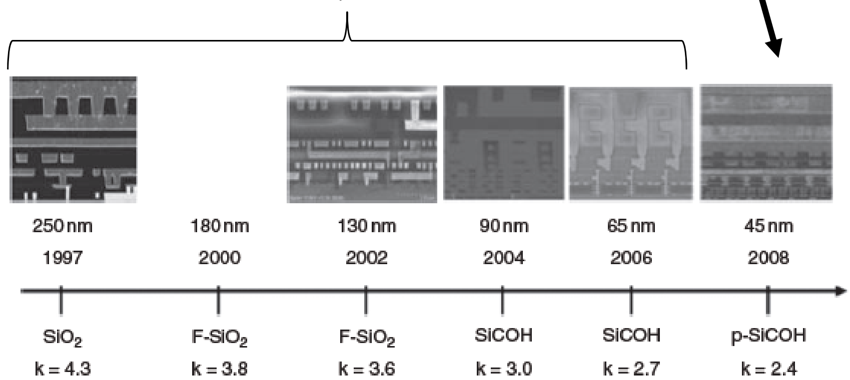
Dense films

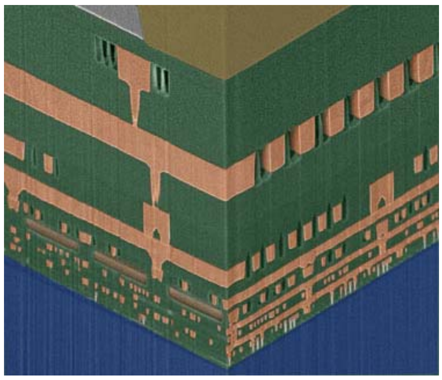
- Minimum bulk k > 1.9 (CF polymer)
  Practicable: k > 2.2 (thermal stability, but CTE mismatch → reliability issues)
  → SiCOH materials k > 2.7

Porous films

Air gaps

- Potential of k_{eff} < 2.0
- Design adaptions needed





Source: IBM

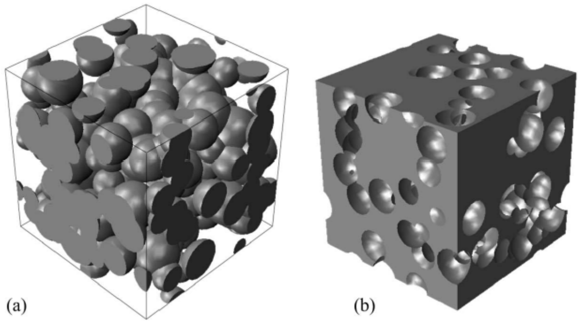
Timeline for IBM volume manufacturing of CMOS microprocessors from 1997 to 2008

CTE: coefficient of thermal expansion

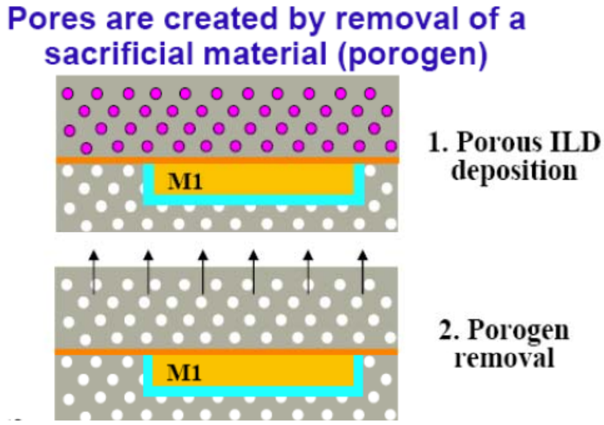
Porous ultra low-k materials

Inherent porosity or porosity introduced by porogens

- Shape of pores, interconnectivity
- Pore size distribution (micro < 2nm, meso < 50 nm, nano > 50 nm)



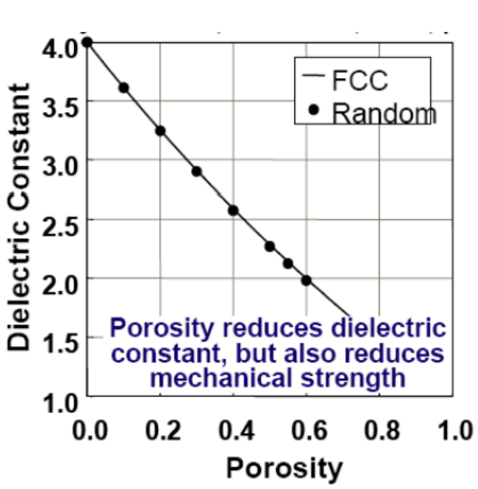
a) Random overlapping spherical solids
b) Random overlapping spherical pores

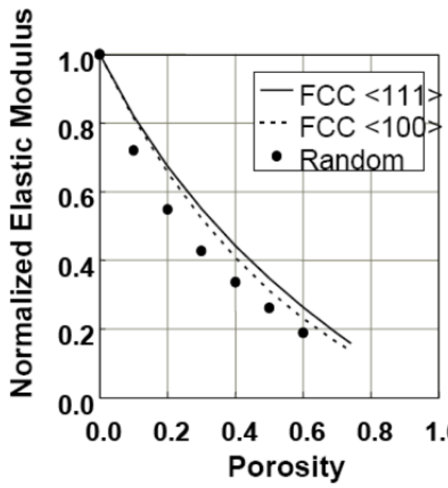


Source: Fraunhofer IZFP

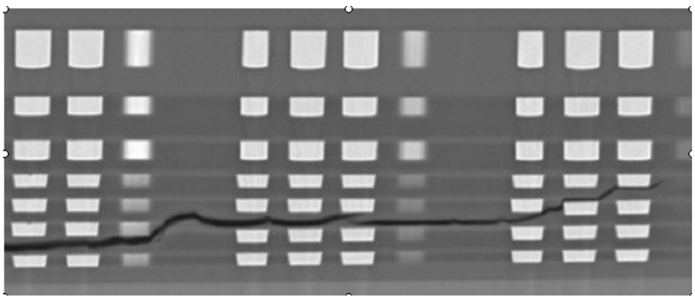
Porous ultra low-k materials – Porosity vs. Elastic Modulus

How much porosity is needed? How much porosity can be controlled ?



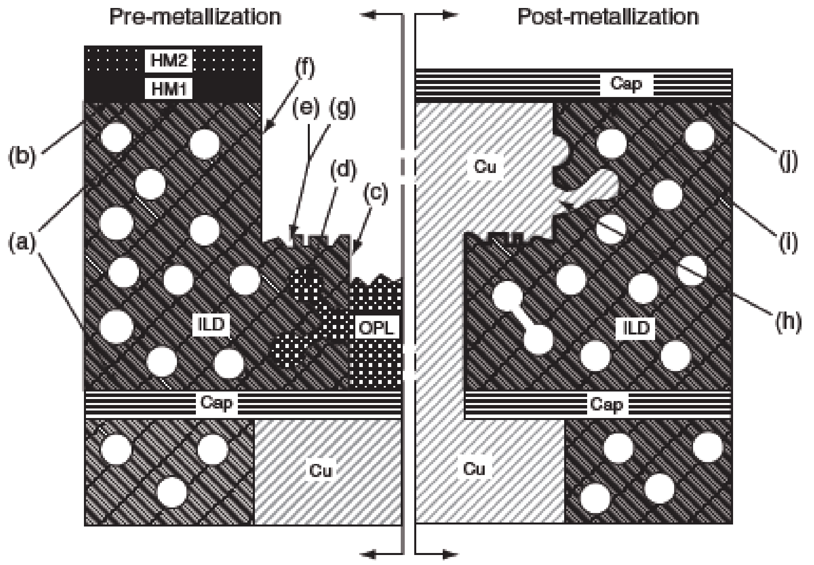


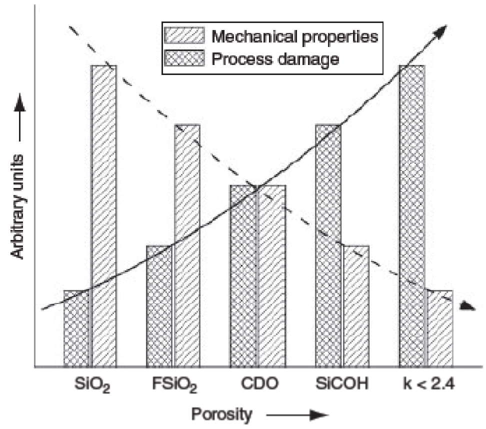
Reduced mechanical properties of porous low-k dielectrics can lead to critical reliability issues, e.g. crack formation during processes which induce high forces to the stack, e.g. CMP, packaging



Source: J. Gambino, IRPS Short Course 2006; R. Huang, Impact of Chip-Package Interaction on Reliability of Copper/Low k Interconnects and Beyond, iMechanica

Porous ultra low-k materials – Process induced damage





a) Adhesion failure;
b) ILD plasma damage
c) Sidewall ILD damage from via-etch and PR strip
d) OPL (organic planarization layer) penetration during via-fill
e) LBR (line bottom roughness) and pitting from uneven etch front
f) Sidewall ILD damage from line etch and PR strip
g) Exacerbated LBR and pitting due to cap-open
h) Discontinuous barrier layer due to large, interconnected pores
i) ILD damage from CMP
j) Cu pre-clean/cap deposition plasma damage

Low-k and ultra low-k Dielectrics - Material Groups

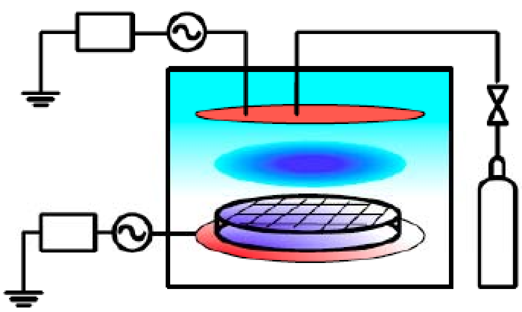
Material (group)	Deposition process	k-value
SiOF / FSG	CVD	3.4 … 3.6
Si based (C-doped)		
HSQ, MSQ	spin on	2.8 … 3.3
C / CH_3-doped SiO_2 (SiCOH)	CVD	2.6 … 3.0
C based polymers		
nonfluorinated	spin on	2.5 … 3.5
fluorinated	spin on	1.9 … 3.0
a:CF	CVD	2.1 … 2.6
porous		
SiO_2 (aerogel, xerogel)	spin on	1.3 … 2.5
HSQ, MSQ	spin on	1.7…2.6
surfactant templated silica	spin on	1.8…2.5
C / CH_3-doped SiO_2 (SiCOH)	**CVD**	**2.0…2.6**
carbon based polymers	spin on	1.8…2.5
air gaps	[CVD/spin on]	1.1 … 2.8

Required properties of low-k materials

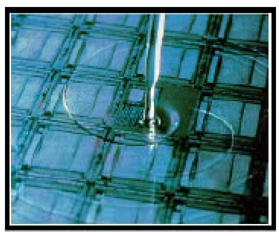
Electrical	Chemical	Mechanical	Thermal
Isotropic k-value	No material change when exposed to acids and bases	Thickness uniformity on wafer and wafer to wafer	T_g > 400 °C
Low dissipation	Etch rate and selectivity better than oxide	Good adhesion to metal and other dielectrics	Low coefficient of thermal expansion
Low leakage current	Low moisture absorption	Low residual stress	Low thermal shrinkage
Low charge trapping	Low solubility in H_2O	High hardness	Low weight loss
High electric field strength	Low gas permeability	Low shrinkage	High thermal conductivity
High reliability	High purity	Crack resistance	
High dielectric breakdown voltage	No metal corrosion	High tensile modulus	
	Long shelf life	High elongation at break	
	Low cost of ownership	Compatible with CMP	
	Commercially available		
	Environmentally safe		

Michael E. Clarke, Introducing low-k dielectrics into semiconductor processing: Application Notes, www.mykrolis.com

Deposition of porous low-k dielectrics



PECVD



Spin on

+ Established equipment / process
+ New chemistries have been implemented
+ easier integration of the cure system into a cluster tool
- Limitations expected for materials with k < 2.2

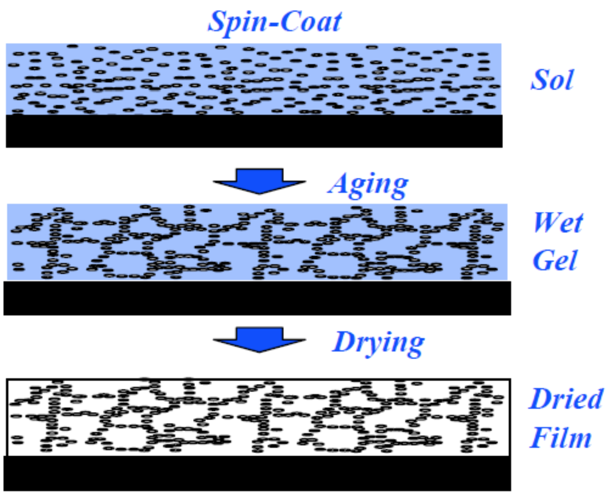
+ More simple process
+ Less expensive and easy to implement
+ Realistic solution for materials with k < 2.2
- Special equipment has to be purchased

Hybrid low-k integration (embedded low-k ILD) is expected

- Dense and porous low-k materials in dedicated levels and/or metal/via dielectric
- CVD and spin on to improve manufacturability and cost-of-ownership by eliminating process steps and allowing chipmakers to re-use their CVD equipment

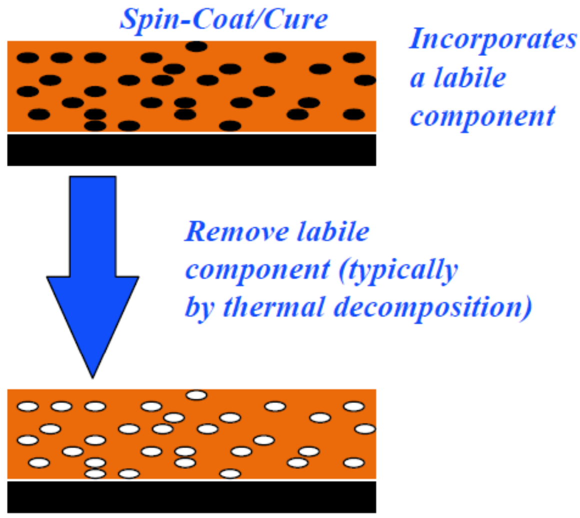
Deposition of porous low-k dielectrics by spin coating

Sol-Gel Process



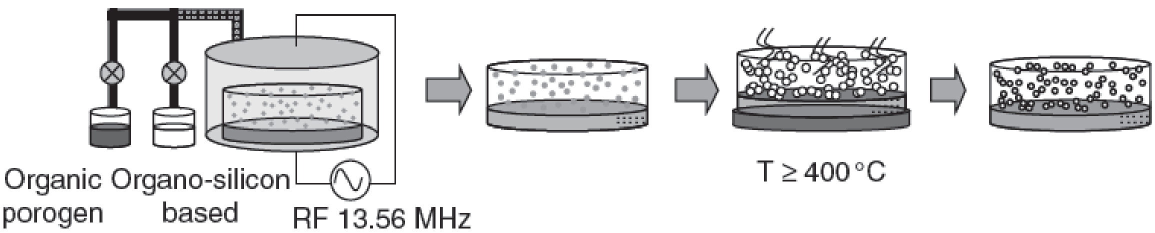
Aerogels, Xerogels

Templating Process



HSQ / MSQ with porogenes, surfactant templated materials

Deposition of porous low-k dielectrics by PECVD



PECVD porogen approach: subtractive process, currently performed in high-volume manufacturing for 32 and 28 nm technology nodes and beyond

- Deposition from the decomposition of (at least) two precursors in the plasma
  - Pure organic molecule (porogen)
  - Molecule consisting of silicon atoms and organic radicals (matrix percursor)

1. Formation of a „hybrid“ film composed of organosilicate-based matrix enclosing organic inclusions
2. Post-deposition treatment (curing), e.g. thermal annealing, removal of the organic phase, mostly consisting of porogen molecule fragments

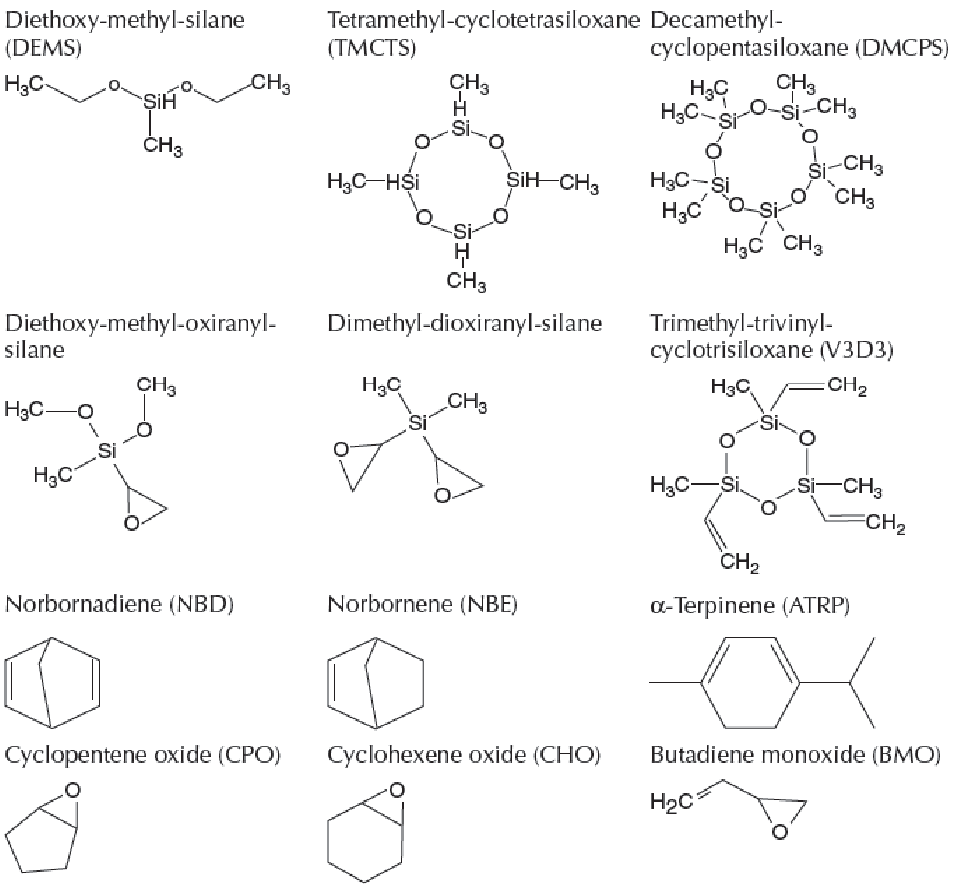
   → Film becomes porous and has ultra low-k properties

Source: Advanced Interconnects for ULSI Technology, 2012 John Wiley & Sons, Ltd

Matrix precursors and porogenes

Matrix

Porogen

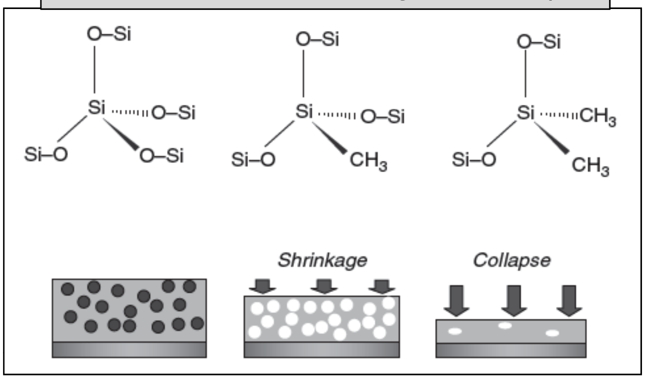


Source: Advanced Interconnects for ULSI Technology, 2012 John Wiley & Sons, Ltd

Precursor choice and process conditions

- Matrix and porogen precursors should be chemically compatible
- Optimized plasma conditions:
  - Prevent excessive dissociation of the skeleton precursor
  - Ability to produce a SiCOH film with k close to 3
  - Ensure the dissociation of the porogen precursor
- Precursor choice:
  - highly reactive porogen, e.g. by epoxy ring
  - close dissociation energy threshold between matrix and porogen precursor
- Ensure mechanical properties of the film
  - Matrix must be strong enough to avoid collapse after porogen removal
  - Minimized bonding to the porogen species to avoid the formation of dangling bonds or other defect sites
- Ensure efficient porogen incorporation by optimizing the porogen/matrix precursor flow rates

Different -Si-O- configurations and the difference between shrinkage and collapse



Source: Advanced Interconnects for ULSI Technology, 2012 John Wiley & Sons, Ltd

Porogen removal by UV assisted curing

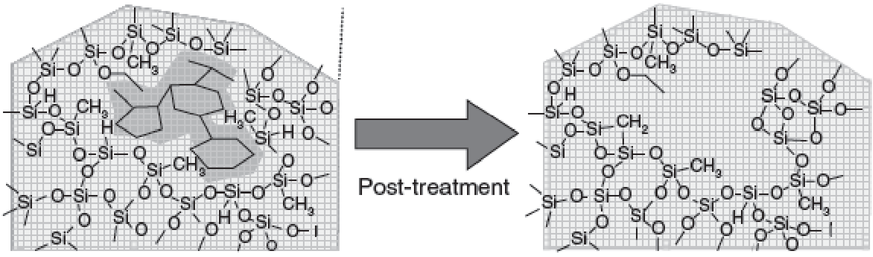
Curing methods: thermal annealing, curing assisted by electron beam, UV radiation, H_2 plasma and supercritical CO_2

→ Thermal annealing alone:

- no sufficient enhancement volumic concentration of Si-O-Si bonds → poor mechanical properties
- long duration (up to 12h) and high temperature load (up to 450°C)

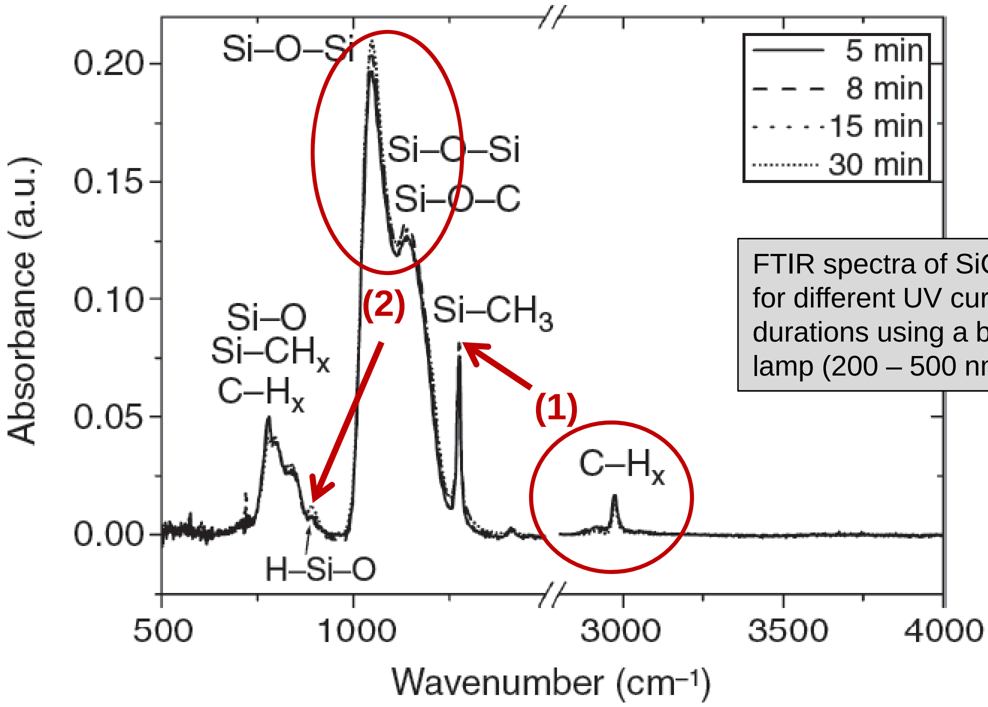
→ **Thermal annealing assisted by UV radiation:**

- processing at 400°C for short durations (a few minutes)
- enhanced mechanical properties of the film due to increased Si-O-Si crosslinking



Source: Advanced Interconnects for ULSI Technology, 2012 John Wiley & Sons, Ltd

UV curing mechanisms



FTIR spectra of SiCOH cured for different UV curing durations using a broadband lamp (200 – 500 nm)

Indicators of porogen removal and mechanical properties enhancement:

(1) Decrease of carbon content (2900-3100 cm^{-1} porogen; 1275 cm^{-1} carbon linked to matrix)

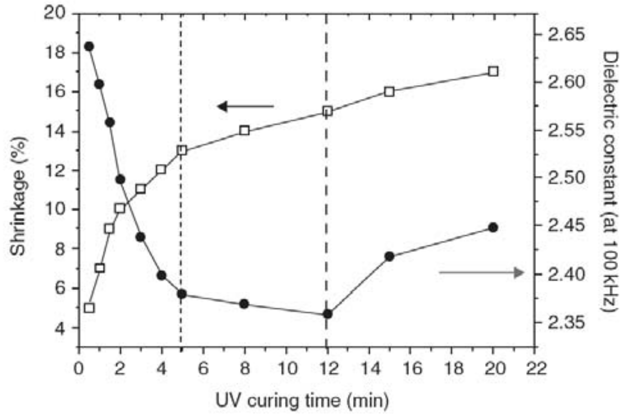
(2) Occurrence of H-Si-O peak at 895 cm^{-1} and rearrangement of the Si-O-Si structure

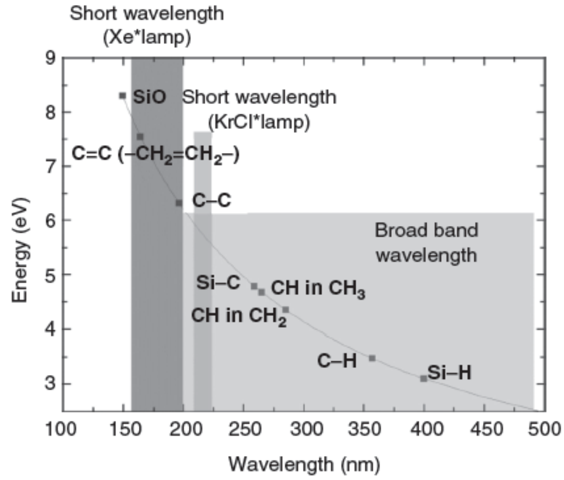
Source: Advanced Interconnects for ULSI Technology, 2012 John Wiley & Sons, Ltd

UV curing mechanisms

Supposed UV curing mechanisms:

- Condensation of Si-OH $\mathrm{Si-OH + HO-Si \rightarrow Si-O-Si + H_2O}$
- Selective photodissociation of bonds within the low-k material





Mechanisms which lead to Si-O-Si crosslinking, shrinkage and enhanced mechanical properties are not completly understood till now; FTIR and NMR analysis suppose alternative reaction paths:

$$\mathrm{-Si-CH_3 + H_3C-Si- \rightarrow -Si-(CH_2)_2-Si- + H_2\nearrow}$$

$$\mathrm{-Si-CH_3 + H_3C-Si- \rightarrow -Si-CH_2-Si- + CH_4\nearrow}$$

$$\mathrm{-Si-O-CH_2-CH_3 + SiCH_3 \rightarrow Si-O\bullet + -Si\bullet + CH_3-CH_2-CH_3 \rightarrow Si-O-Si + C_xH_y}$$

Source: Advanced Interconnects for ULSI Technology, 2012 John Wiley & Sons, Ltd

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Future of low-k materials – ITRS Predictions for 2013/14

Adaption of the predicted ILD dielectric constant in 2013/14 over the years due to emerging integration challenges

Year of prediction	$k_{eff.}$	k_{bulk}
2000	< 1.5	1.1
2001 / 2002	1.9	< 1.7
2003 / 2004	2.0 – 2.4	< 1.9
2005	2.4	≤ 2.0
2006	2.1 – 2.4	1.8 – 2.1
2007	2.4 – 2.8	2.1 – 2.5
2008 – 2011	2.4 – 2.8	2.1 – 2.4
2013	2.55 – 3.00	2.30 – 2.61

Long term prediction in 2013 for 2024: $k_{eff.}$: 1.88 – 2.28
k_{bulk}: 1.80 – 2.20

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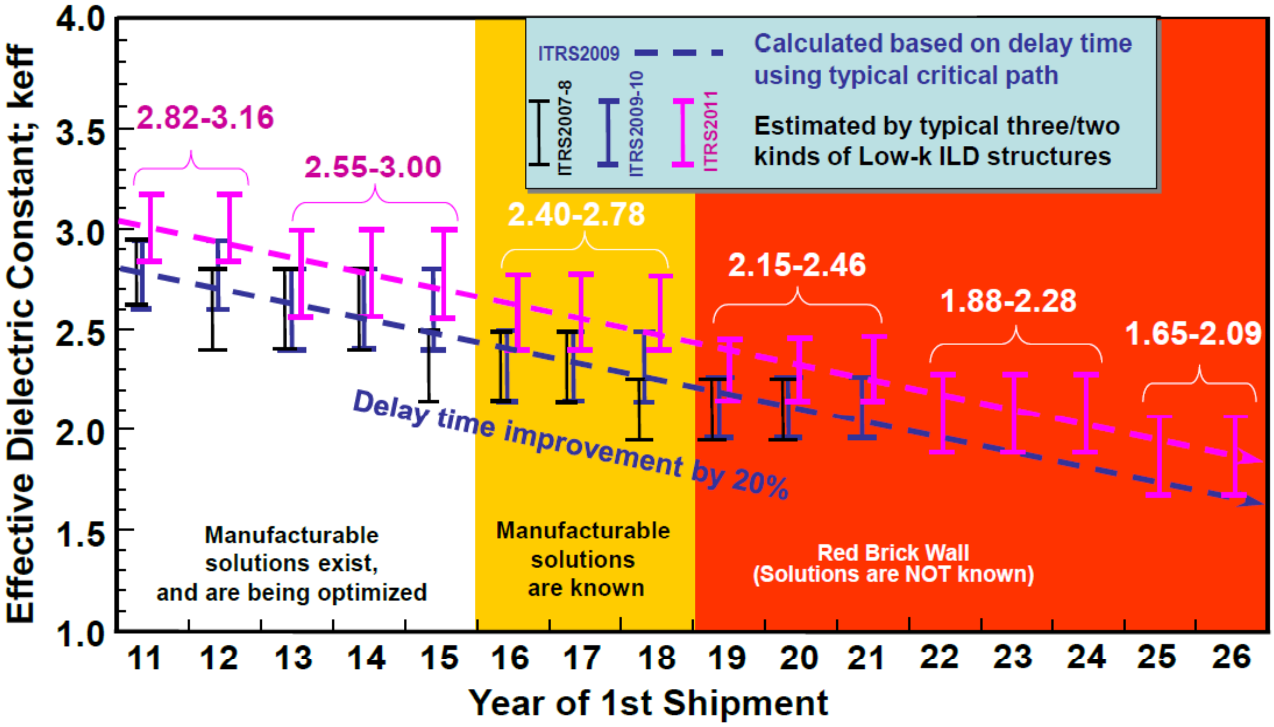
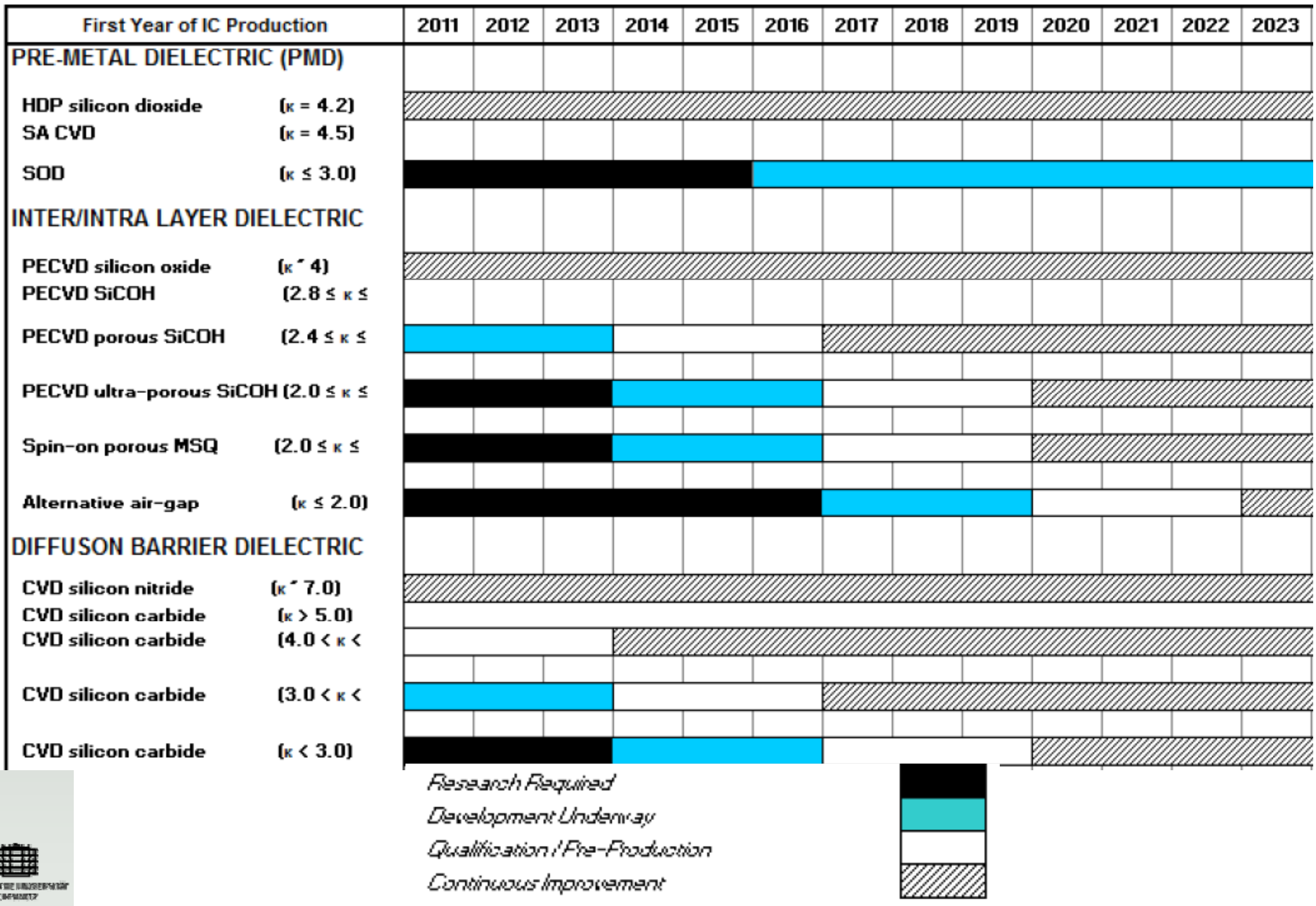
Low-k Roadmap Progression (IRTS 2011)



Dielectric Potential Solutions (ITRS 2011)



New developments / emerging low-k materials

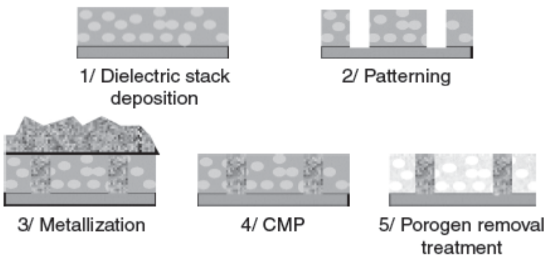
New deposition techniques

→Power pulsed PECVD systems to achieve a better preservation of the precursor structure

→ Initiated CVD (iCVD) avoids plasma excitation and damage to the growing film while keeping the precursor structure intact

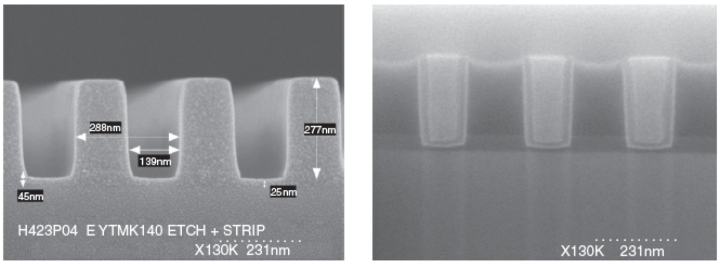
Adaption to integration schemes

→ Solid first approach; porogen removal after complete integration of the dielectric



Solid first integration scheme

Source: Advanced Interconnects for ULSI Technology, 2012 John Wiley & Sons, Ltd



Solid first apporach: low-k dielectric after etching (left) and fully integrated after porogen removal (right); Precursors: DEMS and CHO

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