AICT

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① → Define Basic Process steps, Process, Process technology & basic technology?

Ans :- **Basic Process Steps :-**

→ Indivisble steps in a process flow

→ charaterisied by physical / chemical parameters (temp, pressure, gas composition)

→ Ex :- Special diffusion step (Pre-deposition, implantation step, special cleaning step (Rinsing)

Process :-

→ consists of one or more BPS.

→ carried out by using specific tools.

→ Standardize component of technology (SCT)

→ Results in the acheivement of specific property of action.

→ Ex :- Doping, photolithography etc.

Basic technology :-

→ Sum of processes or BPS to be peformed for the fabricatio of a specific product.

→ Ex :- Bi-CMOS, SBC, SGT etc.

Process technology :-

→ Physical, chemical & other mechanism of the proc

→ technical realization using specific equipment

→ Process integration issues.

(2) Name four Basic MOS transistor types!

Ans:- → NMOS enhancement → PMOS enhancement
→ NMOS depletion → PMOS depletion.

(3) Name important trends in CMOS technology!

Ans:- → Geometrical scaling
→ Integration degree
→ Performance increase
→ Increase of die size
→ Cost decrease per function.

→ three imp → wafer size increase
→ single wafer process instead of batch
→ cluster tool instead of single chamber tool

(4) Explain terms "Geometrical scaling" & "equivalent scaling". Give two examples for equivalent scaling!

Ans:- Geometrical scaling:- (constant field scaling)

It refers to the continued shrinking of horizontal & vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) & performance (speed, power) & reliability values to the applications & end customers.

Equivalent scaling:- (occurs in conjuction with, & also enables continued geometrical scaling)

It refers to 3-D device structure (design factor) improvements plus other non-geometrical process techniques & new materials that affect the electrical performance of the chip.

Ex:- Cu / Low-K, HKMG, electrostatic control (SOI), new channel materials, Strain engineering / Stressors.

⑤ Explain the terms "front end" & "Back end".

Ans:- Front end - wafer level fabrication process.
Back end - packaging.

⑥ Explain meaning of Moore's law.

Ans:- Moore's law states that the no. of transistors will be doubled on an IC approximately every two years.

⑦ Name five basic process steps of CMOS technology.

Ans:- → oxidation formation of SiO_2 layer on Si wafer surface
→ Diffusion movement of impurity atoms at surface to bulk
→ Ion Implantation Accelerating ions within Semiconduct
→ Deposition Layering films of various materials on wafer.
→ Etching. removal of unwanted extra material.

⑧ what is the motivation to use lower-K dielectrics as insulat in on-chip interconnects systems instead of SiO_2 for high perform CMOS technology? which low-K dielectrics have been used so far & what are their values?

Ans:- Low-K dielectrics as used as insulators to decrease the parasitic C i.e, Cross talk and Signal delay.
→ SiOF ($K \approx 3.4 - 3.6$)
→ SiCOH ($K \approx 2.6 - 3.0$)
→ p-SiCOH ($K < 2.6$ (or) $K = 2.0 - 2.6$)

⑨ Gas Vs ~~the~~ liquid phase deposition process:

Gas Phase deposition process

CVD - Chemical Vapour deposition:-

Materials	Application	Process Module
• Poly Si	→ Gate	→ Gate Structure
• SiO_2, Low-K dielectric	→ STI, Local Interconnect	→ Viax/ Metalx
• High K-dielectric	→ Gate	→ Gate formation
• W	→ local interconnect	→ Vx(Al)

Epitaxy :-

- Si → CMOS P^- level → STI
- GaAs, GaN → Optical devices → STI

ALD :-

- HFox → HKMG → Gate Structure
- Cu (Seedlayer) → CuDD → Vx/Mx
- Al_2O_3 → Gate electrode → Vx/Mx (Cu)

Sputtering (PVD):-

- TaN, Ta → Cu Dual Damascene → Vx/Mx
- Cu (seedlayer) → CuDD → Vx/Mx
- Co, Ni, NiPt, Ti → Source & Drain contacts → Contact formation
- Al, (Au, Ag, Pt) → Interconnect system → Mx

Liquid phase deposition process

Spin on :-

- Photoresist → lithography → Nearly all Viax/ Metalx
- Low-K dielectric → Interconnect system → Local interco
- SiO_2-like (USG) → Packaging → Passivation.

Electro Chemical deposition :-

- Cu → Dual damascene → viax/Metal
- Cu → Interconnect system → Through Si vias [TSVs]

Electroless :-

- Cu → interconnect system → viax/ Metalx
- NiMOP → Potentially barrier/ Seed lay
- CoWP → Diffusion barrier.

Circled - future one's

Rest all - Present in production.

(10) Describe the fabrication process for porous CDO/SiCOH films (type of process, precursors, post-treatment). How is the porosity in the film created? what is the role of the post-treatment, which films properties are effected?

Ans:-

→ Fabrication process for porous CDO/SiCOH films:-

Type of process:- PECVD-Plasma enhanced chemical vapour deposition.

Precursors:- organosilane (Ex:- TMS) + porogen.

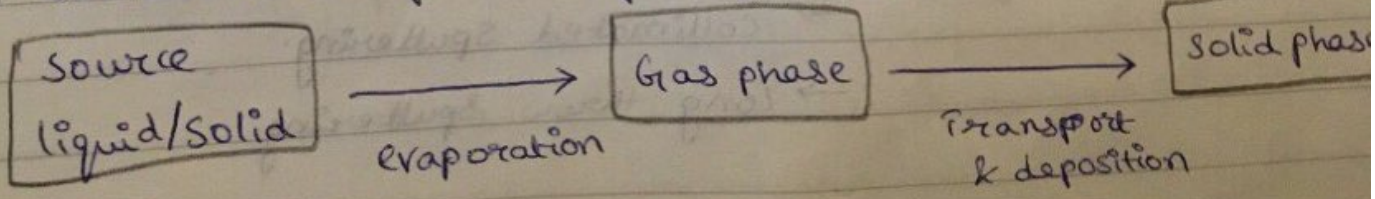
Post treatment:- UV cure/ UV thermal processing.

→ Porogen is embedded in SiCOH matrix and evaporated during thermal (or) UV assisted anneal.

→ Post-treatment is used for porogen removal and cross linking. Film properties which are effected are Mechincal stability (E, H) & porosity/density (Optical-R.I)

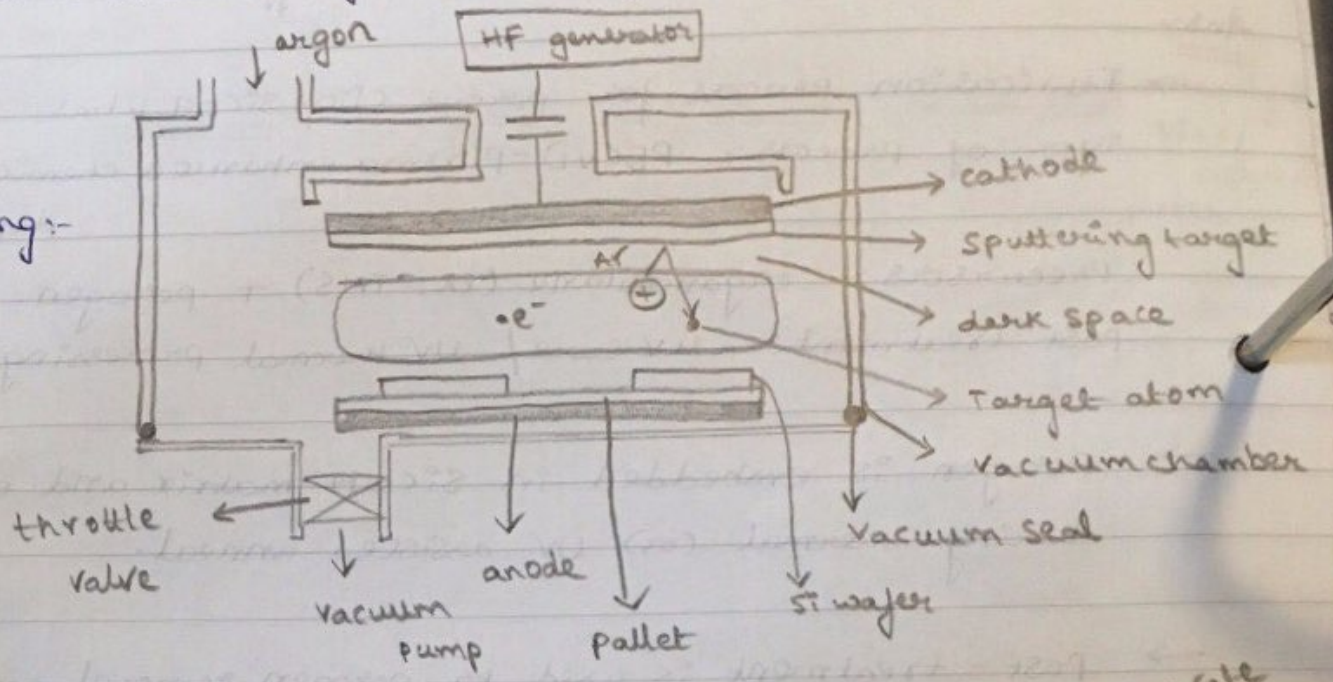
(11) Basic Mechanism of sputtering process - How does the film deposition process work? Schematic cross-section of conventional Sputtering chamber (RF (or) DC magnetron) Name the modern Sputtering principles to coat contact & via holes with high aspect ratio.

Ans:- Sputtering is a process to deposit thin film on a substrate where the atoms are ejected from a solid target material due to bombardment of the target by energetic particles.

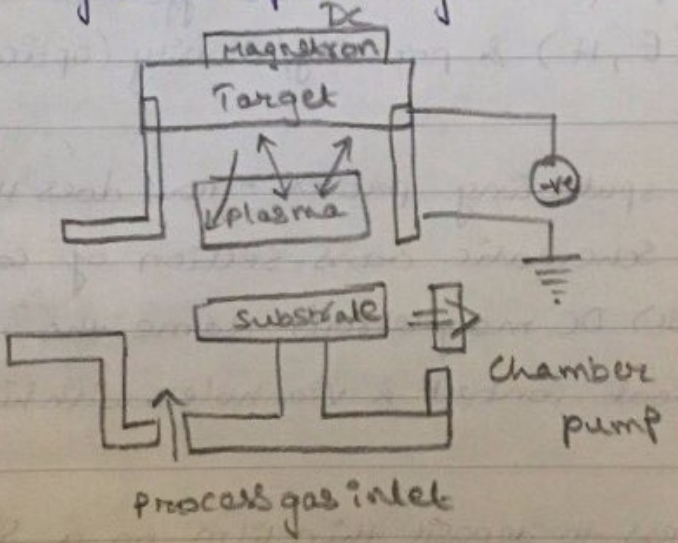


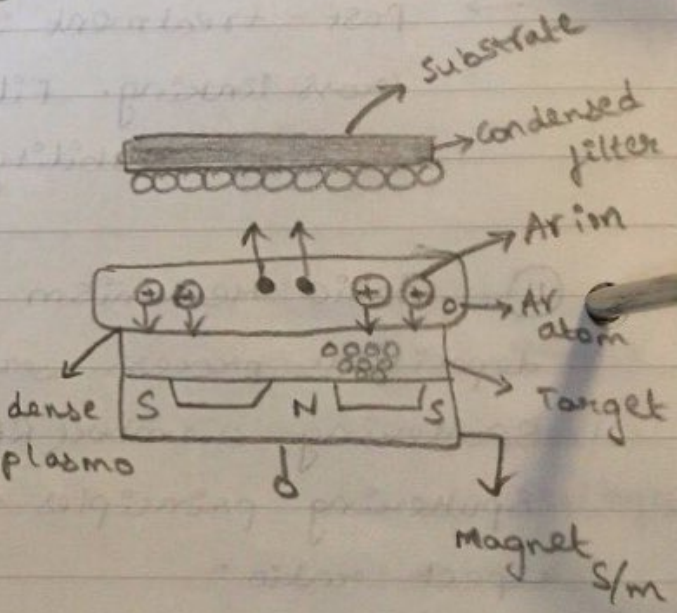
→ Ions are generated & directed at a target
→ Ions sputter target atoms
→ The ejected atoms are transported to the substrate
→ Atoms condense & form a thin-film.

RF Sputtering:-



DC Magnetron Sputtering:-





Modern Principles:-

→ Ionized metal deposition.
→ Collimated Sputtering.
→ Long throw Sputtering.

(12) Which kind of lithography is used in 32/28 nm technology nodes? using the equation for minimum printable feature size Imin. Discuss how Imin can be reduced and thus even sub-exposure wavelength feature sizes can be achieved. Name three resolution enhancement techniques.

Ans:-

→ 193 nm immersion lithography is used in 32/28 nm technology nodes.

→ $I_{min} = \frac{K_1 \times \lambda}{NA}$ K_1 = Reileigh limit

where λ- wavelength, NA- Numerical aperature. Imin can be reduced by decreasing wavelength & K_1 and increasing Numerical aperture.

→ Three resolution enhancement techniques:-

optical proximity correction (OPC)
off-axis illumination (OAI)
Phase shift masks (PSM)
Double exposure/Double patterning (DA)

< 28nm
→ EUV
→ IPL
→ EP

(13) Name atleast two processes for dry photo resist removal.

Ans:-

→ Plasma stripping (in barel reactors)
→ downstream stripping
→ plasma free (ozone & UV) stripping.

(14) what is the advantage of using so called cluster tools in semiconductor process? Give an example for an integrated process flow performed in a cluster tool and draw a schematic of this cluster tool without remote components like pumps, heat exchangers etc.

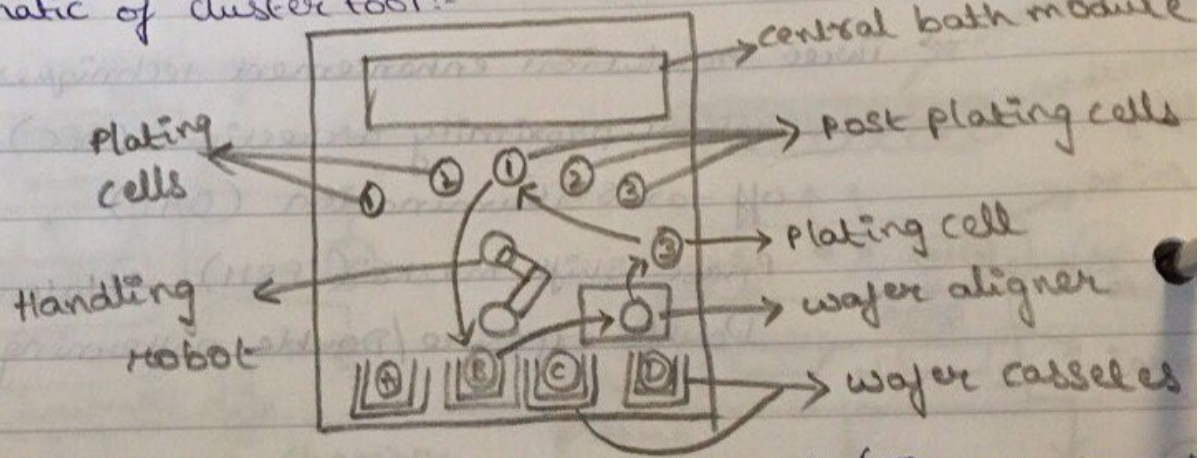
Ans:-

→ Advantages of cluster tools:-

- → Short Cycle times
- → Fast process development
- → Higher yield efficiency
- → Less risk of contamination.

→ Ex:- Pre clean - TiN CVD - W CVD

→ Schematic of cluster tool:-



(15) Name the process modules of conventional (Sigate, Si bu CMOS technology front-end process flow in the right sequence

Ans:-

1) Shallow trench isolation
2) Twin-well implants
3) Gate structure
4) Lightly doped drain implants
5) Sidewall Spacer
6) Source/Drain implants

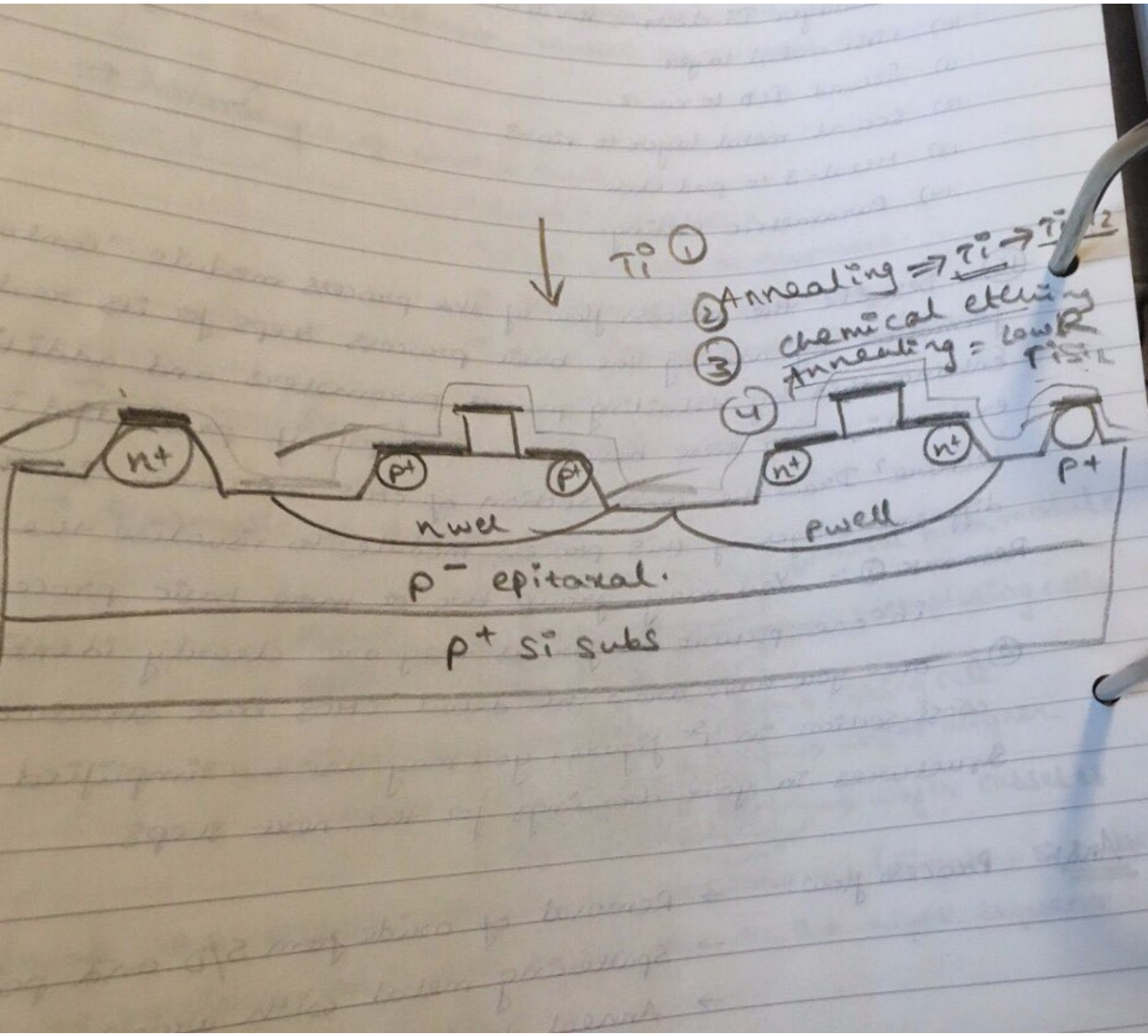
7) Contact formation
8) Local interconnect
9) Interlayer Di-electric to via-1
10) first metal layer
11) Second ILD to via-2
12) Second metal layer to via-3
13) Metal-3 to pad etch
14) Parametric testing.

(16) Describe the process flow of the process module "contact-formation" by naming the basic process steps for its realization. Enhance this by detailing process parameters and additional explanations for these basic process steps, if presented in the lecture? Draw the cross-section of CMOS structure in the different stages of this process module to visualise the sequence.

Remark ① :- You may group two or more basic process steps in one picture as far as they are clearly identified

② :- once you have draw the detail CMOS base structure cross-section in 1st figure, you may use a simplified base structures in your drawings for the next steps.

Ans:- Process flow :-
→ Removal of oxide from S/D and polygate
→ Sputtering metal with argon
→ Anneal to form $TiSi_2$ (RTP_1)
→ Chemical etching to remove unreacted Ti, leaving $TiSi_2$ (Selective etching)
→ Anneal to form low resistivity $TiSi_2$ (RTP_2)



(17) What is ~~minimum~~ motivation to use high K / metal gate (HKMG) structures instead of conventional SiO2/Polysi gate structures? Name the two technology approaches for HKMG and discuss advantages & drawback of each one!

Ans:-

→ HKMG technology promises to enable conventional scaling of the transistor as well as reduced Stand by power due to reduction in gate leakage, at the device level. The performance improvement achieved by introducing HKMG is ~~two fold~~. The drive current is enhanced with HKMG through higher gate capacitance, resulting from higher permitivity of High-K dielectric over SiO2 along with scaling of T. (Poly depletion supression)

→ Two technologies for HKMG:-

1) Gate First MIPS (Metal inserted poly silicon)

2) Gate last RMG (Replacement metal gate)

Gate first MIPS :- Adv :- Conventional process

Disadv :- High Thermal budget, complex Vt tuning, mobility, reliability at thin EOT.

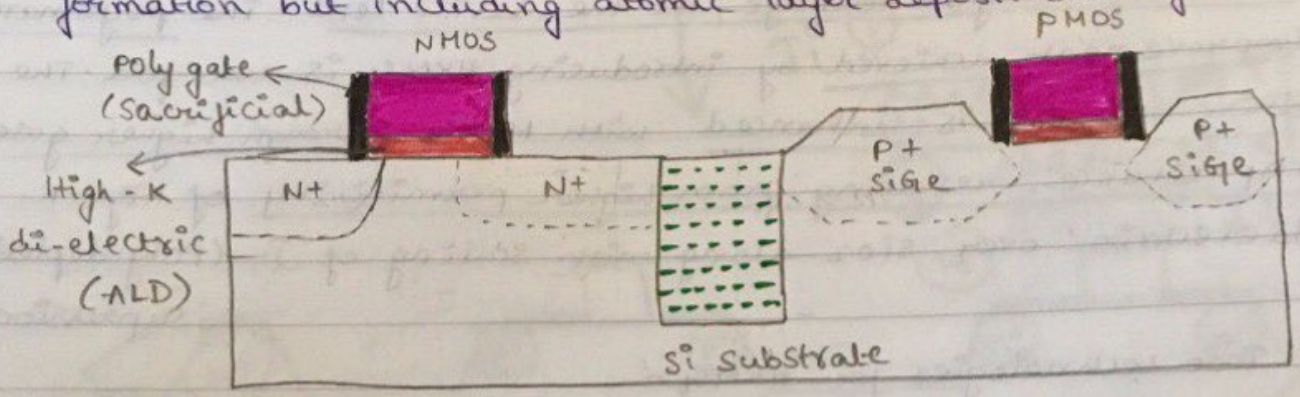
Gate last RMG :- Adv :- Low Thermal budget, higher Strain from embedded SiGe / S/D.

Disadv :- Complexity, cost, more restricted design rules.

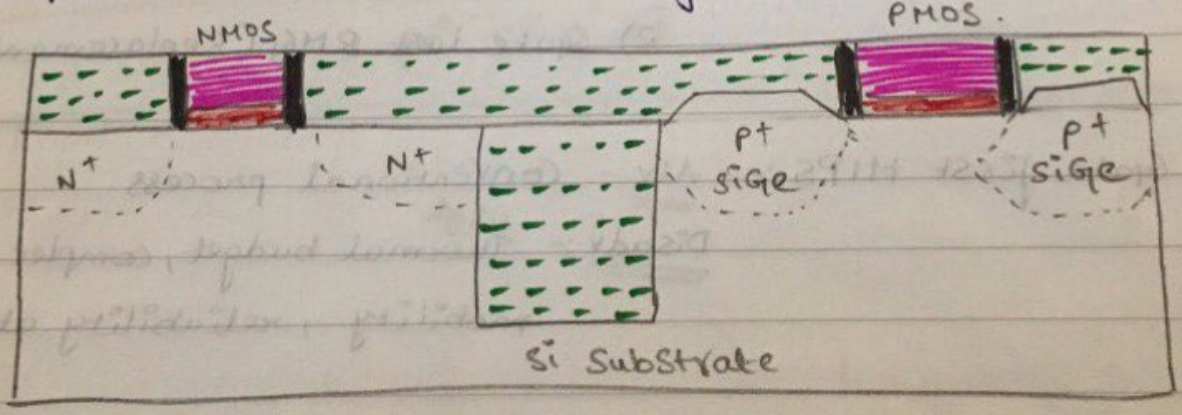
(18) Describe the process flow of the process module "HKMG gate last" by naming & briefly describing the five steps of its ~~relati~~ realization. Draw the schematic cross sections of the gate structure in different stages of this process module to visualise the sequence.

Ans:-

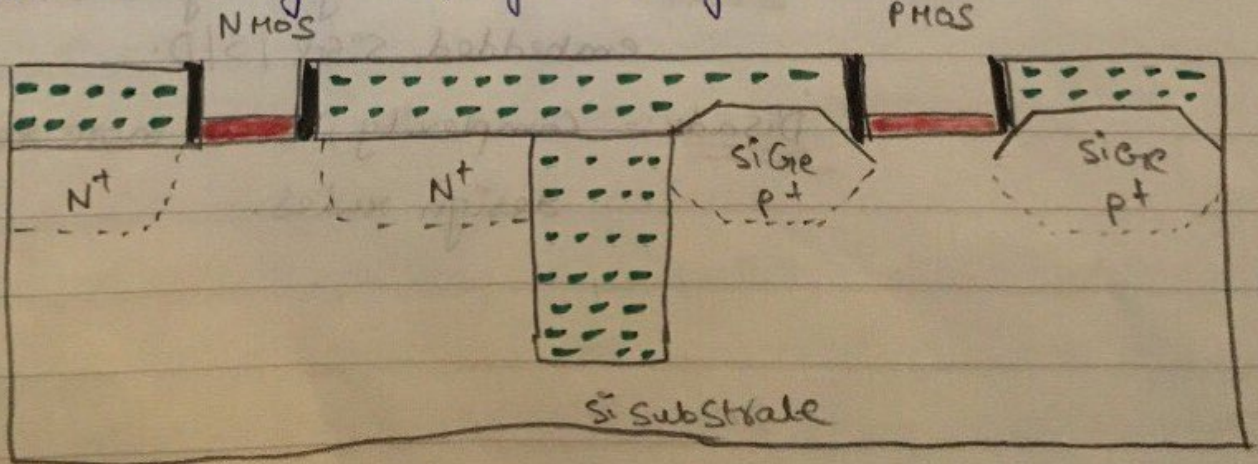
(1) Standard Transistor process through source-drain formation but including atomic layer deposition high-K dielectric



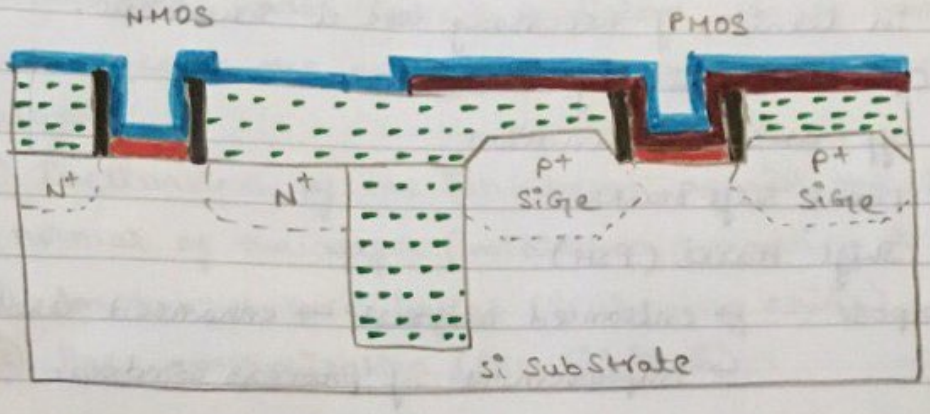
(2) Deposit & planarize oxide layer.



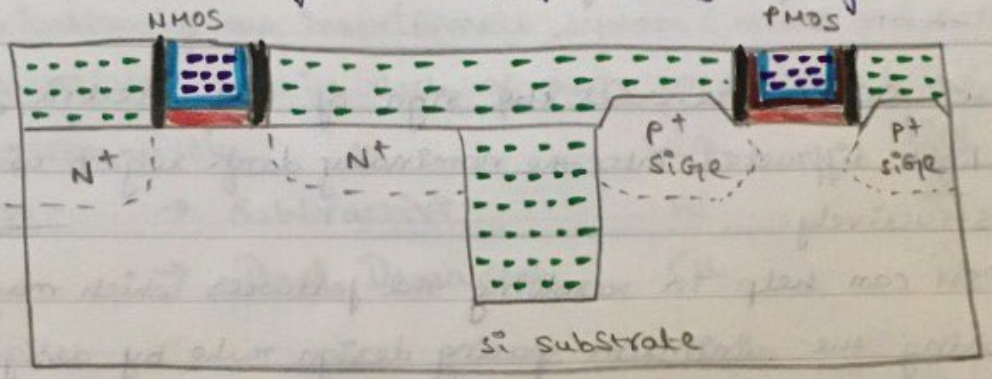
(3) Etch out Sacrificial polysilicon gate.



④ Deposit Seperate NMOS & PMOS WF metal layers



⑤ Deposit Al fill metal, planarize surface.



⑲ CVD silicon nitride is widely used in CMOS technology. Name four applications of silicon nitride thin films including the specific function of the Si Nitride. Provide the respective process module in which this application is implemented.

Ans :-

Application	Process module
1) CMP - Stop layer in STI	→ STI
2) AS etch Stop layer in damascene process	→ Viax/Metal x
3) Final Passivation & mechanical protective layer for IC encapsulation	→ Passivation
	→ Side wall spacer
4) Side wall spacers in MOSFET ↳ To form LOD Structure.	

(20) Name three Resolution enhancement technique. Explain one in detail, if necessary use a schematic.

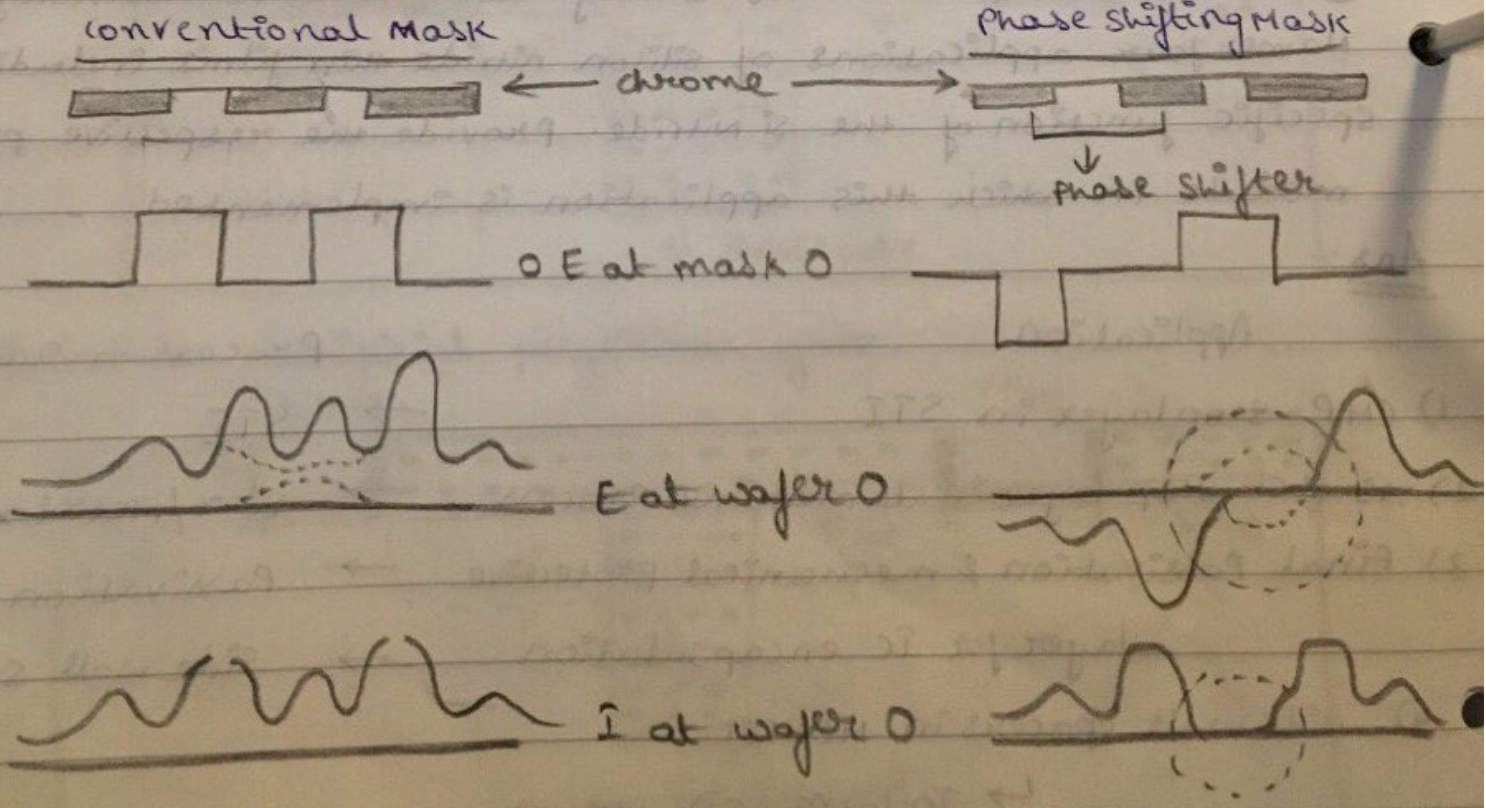
Ans:- → Optical proximity correction
→ off-axis illumination
→ phase shift masks

Phase Shift Masks (PSM)

Purpose :- → enhanced contrast → enhanced resolution
→ improvement of process window.

Principle:- Introduction of a phase difference of 180° on specific parts of the mask structure.

→ Phase shifter reverses the sign of the electric field.
→ The light diffracted into the nominally dark region will interfere distructively.
→ So PSM can help in resolving the features which may be violating the minimum spacing design rule by assigning opposite phases to the conflicting features.



(21) In ion implantation process the so-called "channeling effect" can be observed under certain conditions. Please name two measures to prevent the appearence of the effect in practical application.

Ans:- ① Inclination of the ion-beam against the surface normal of the wafer (minimum channeling at 7° .. 10°)
② Amorphous cover layers (scattering oxide)
③ Pre-amorphization (Ex:- Si^+ in Si)

(22) which two basic metallization process sequences do exist for fabrication of the interconnect system? Name the conductor materials used in each of them for the via & the line respectively.

Ans:-

	Via	line
→ Subtractive	W	Al
→ Dual Damascene	Cu	Cu

(23) what is the motivation to use local stress/strain generator] strained silicon in CMOS transistors? which type of strain do you need to enhance the NMOS & PMOS transistor respectively? Name two approaches for local stress generation in CMOS transistors.

Ans:-

→ Motivation:- To increase mobility of holes & electrons.
→ NMOS:- tensile stress
PMOS:- compressive stress
→ Approaches:- 1) Deposition of stressor films
2) SiGe S/D - PMOS
3) Biaxial Strain templates.

(24) Please Name two future transistor options which allow further IC performance improvements (or) going beyond s MOSFET?

Ans:-

→ Multigate FiN transistor
→ Tunnel transistor
→ Advance channel materials (Ge transistors)

(25) What is motivation to use short duration annealing process? Please name two of these short annealing processes & provide the approximate process time (order of magnitude) & broadening of dopant concentration profiles at 1100°C due to diffusion for the above-mentioned process times!

Ans:-

→ Short duration Annealing process is used to controll the diffusion.

Method	Process temp in °C	Process time	Broadening of profiles
→ Furance (N_2, H_2)	900 - 1100	min, h	1 µm (1000s)
→ Rapid thermal Processing	1000 - 1250	s	0.1 µm (10s)
→ Flash lamp	1000 - 1300	ms	0.01 µm (0.01s)
→ Laser	1100 - 1400	µs	< 0.01 µm (0.01s)

ect (26) Process flow of copper dual damascene process:-

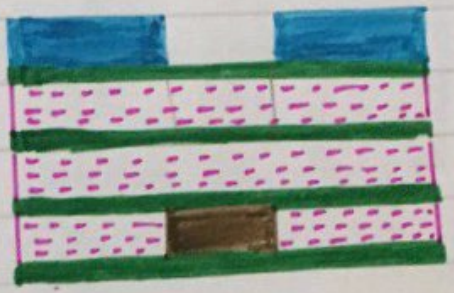
Ans:- 1) It uses two di-electric etch process → one via etch & one trench etch

2) Metal layers are deposited into via holes & trenches.

3) A CMP process removes copper & tantalum barrier layer.

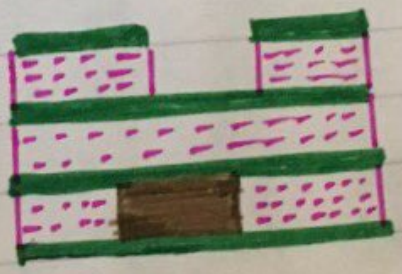
4) Leaves copper lines & plugs embedded inside the dielectric layer.

→ via litho

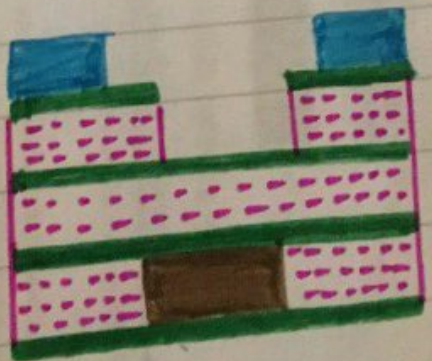


Resist
Si_3N_4, SiC
SiO_2(or)low-K
Cu

→ via etch & strip



→ Trench litho



→ Trench etch & Strip-