2 Microelectronics Technology

2.1 Definitions

Microelectronics

- The design, manufacture, and use of microchips and microcircuits [Oxford Dictionary].
- The technology for development and fabrication of electronic systems consisting of devices whose operation is based on the movement and storage of electrical charges.
- Comprises not only integrated semiconductor circuits, but also solid state devices having other modes of operation and their application in complex systems.

Microelectronics, Microsystems Technology (MEMS, MOEMS, …)
→ Microtechnologies

Interaction of materials, processes, equipment, technology

Status: 01.04. 2015

Scope of microelectronic products:

Memories Processors ASIC's Power electronics Microsystems

Innovations:

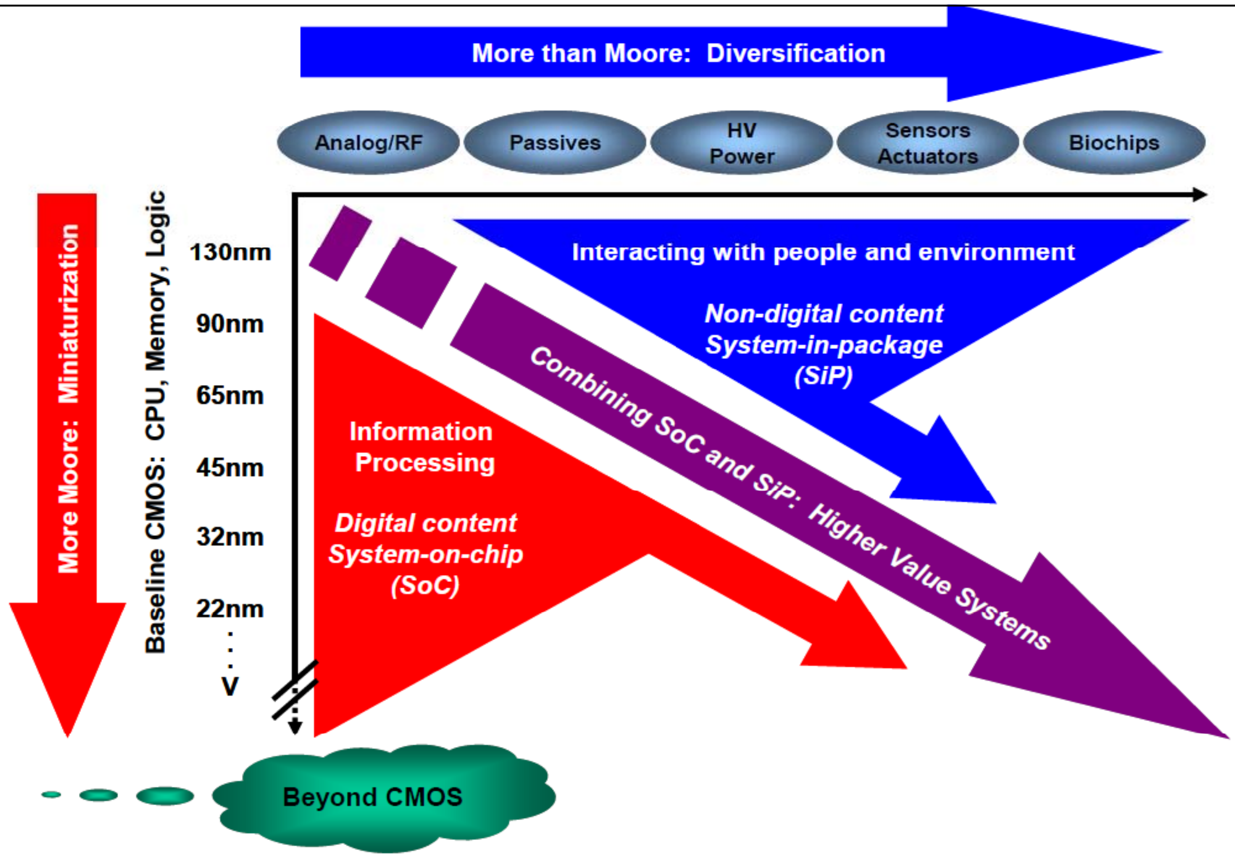
Technology driver	Architecture & design evolution	Algorithms	New technologies, Power engineering	Microtechnologies, special developments

Goals:

→ Scaling down
Decrease of all characteristic dimensions and structures
(e. g. channel length of MOS transistors)
More Moore

→ Systems (sensor, actuator) & combination with µE
(see special lecture courses)
More than Moore – Smart Systems

This lecture deals with processes and technologies which are applied in Micro and Nanoelectronics or have future application potential.



The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore").

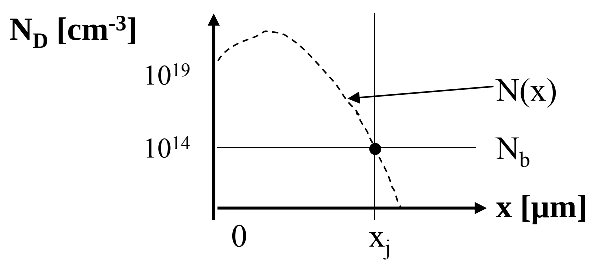
Terms

Basic process steps (BPS)

- indivisible step in the process flow
- characterized by physical / chemical parameters (temperature, pressure, gas composition...)
- e.g. special diffusion step (pre-deposition), implantation step, special cleaning step (rinsing)

Technology: $\sum$ **BPS**

Parameter: Special parameter determining device properties
example: Dopant concentration → resistance, depth of p-n-junction



Doping profile N(x)

Equipment: Tools for a specific process step
(e.g. implanter, PVD cluster tool, ...)

2.2 Processes / Basic Technologies

Process
- consists of one ore more BPS
- carried out by using of specific tools (equipment)
- standardized component of a technology
- results in achievement of a specific property
- e.g. doping (pre-deposition, drive in), photolithography (deposition of resist, exposure, development, ...)

Process technology
- physical, chemical and other mechanism/principle of the process
- technical realization using specific equipment
- process integration issues

Basic technology
Sum of processes (or BPS) to be performed for the fabrication of a specific product, e.g. CMOS, BICMOS, Bipolar, ...

Important:
Technology is characterized by the number of devices per chip and the critical (minimum) dimension of the device structure

Microelectronics:
- Silicon-based: Si wafer as the basic material, Trend: wafer diameter increases (200 mm→ 300 mm → 450 mm)
- Other semiconductor materials (e.g. GaAs, SiC) with smaller wafer size (100, 150 mm)

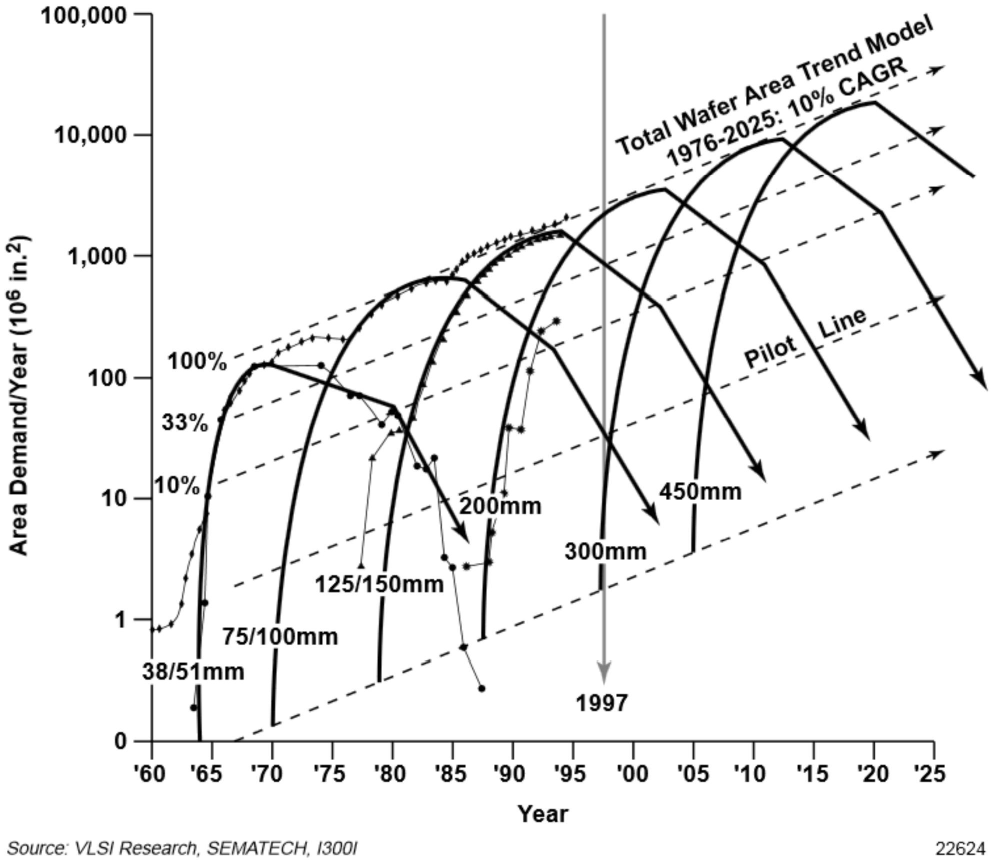


Figure 7-1. Lifecycles of Different Wafer Sizes

Overall Process

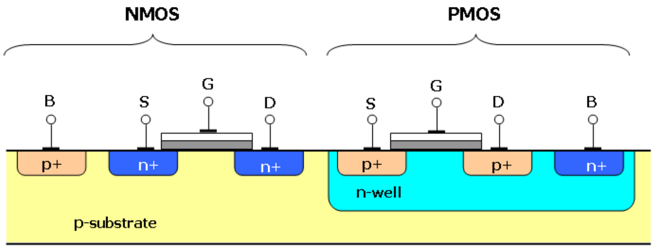
Phase 1: ***Preparation***
- crystal pulling
- mechanical treatment (diameter)
- wafer fabrication: sawing, lapping, polishing

Phase 2: ***Wafer processing*** → f(product, basic technology)

$\sum$ Basic process steps (BPS)
- BPS 1
- BPS 2
- ...incl. repetition (see lecture "Technologies for Micro and Nano Systems" and section 3.1 ... 3.9)

• BPS/processes often summarized in process modules (see chapter 5.1)

e.g. **CMOS:**



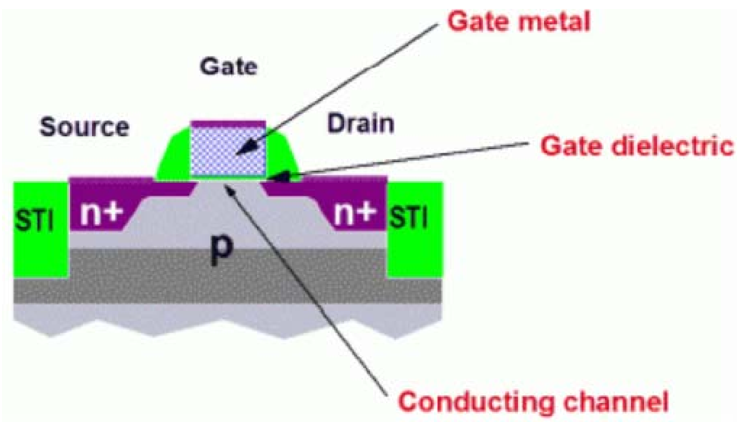
- testing

Phase 3: ***Packaging***
- die separation
- mounting
- bonding
- encapsulation

2.3 Devices

MOS Transistor:

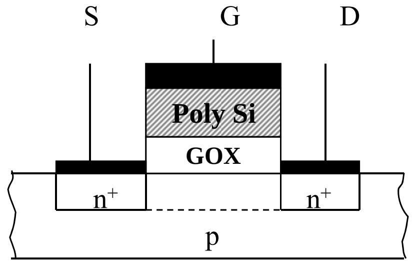
MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor
Basic device of MOS/CMOS Technology



Depletion mode
→ Channel already exists at zero gate voltage. Control by depletion of majority carriers.

Enhancement mode
→ Self-blocking at zero gate voltage. Channel emerges due to enhancement of minority carriers until inversion.

n-Channel Enhancement:



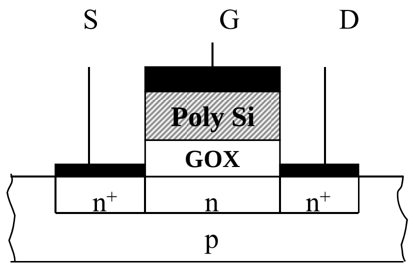
$V_G = 0$ → no channel, $n^+ p\, n^+$- structure blocked
→ only leakage current

$V_G > 0$ → n-conducting channel formed by influence
→ current from source to drain possible

Remark: Fabrication is difficult because a channel can be formed already at $V_G = 0$ due to the positive charges in the oxide and the contact potential.
→ Problem can be solved by supplementary corrective doping

(p-Channel enhancement accordingly: Enhancement for $V_G < 0$ and no technological problems because n-Si is used as the substrate and additional negative charges are generated in the channel by influence due to positive oxide charges)

n-Channel Depletion:

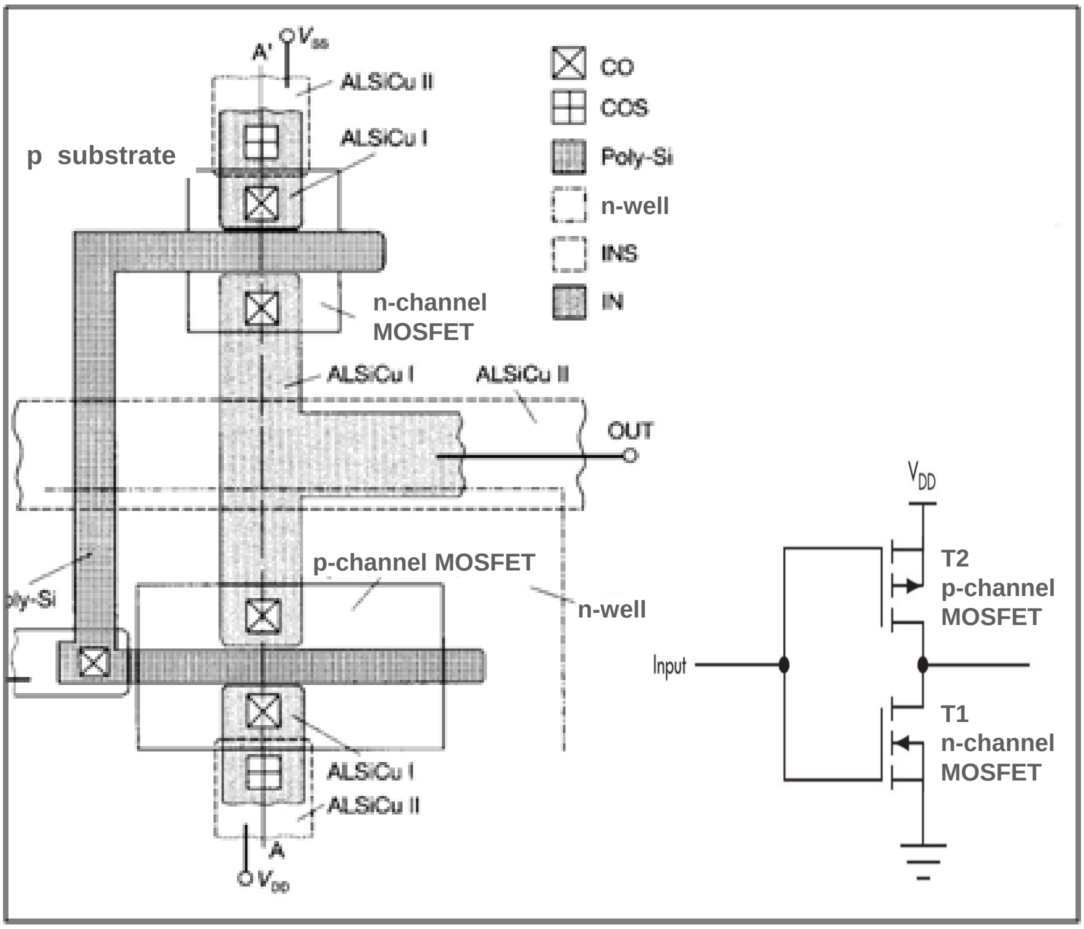


→ P(hosphorous) doping (by ion implantation) in the channel range → n channel exists at $V_G = 0$

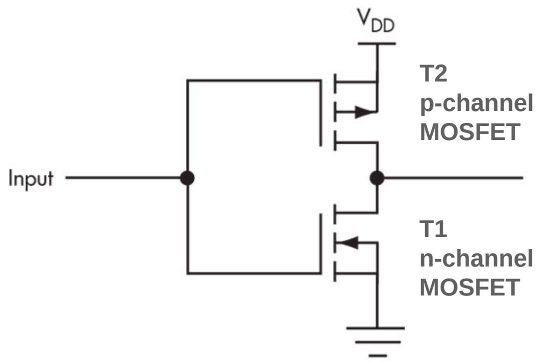
$V_G = 0$ → current, transistor is "on"
$V_G < 0$ → decrease of current

(p-channel depletion accordingly, depletion for $V_G > 0$)

CMOS Inverter



CMOS:

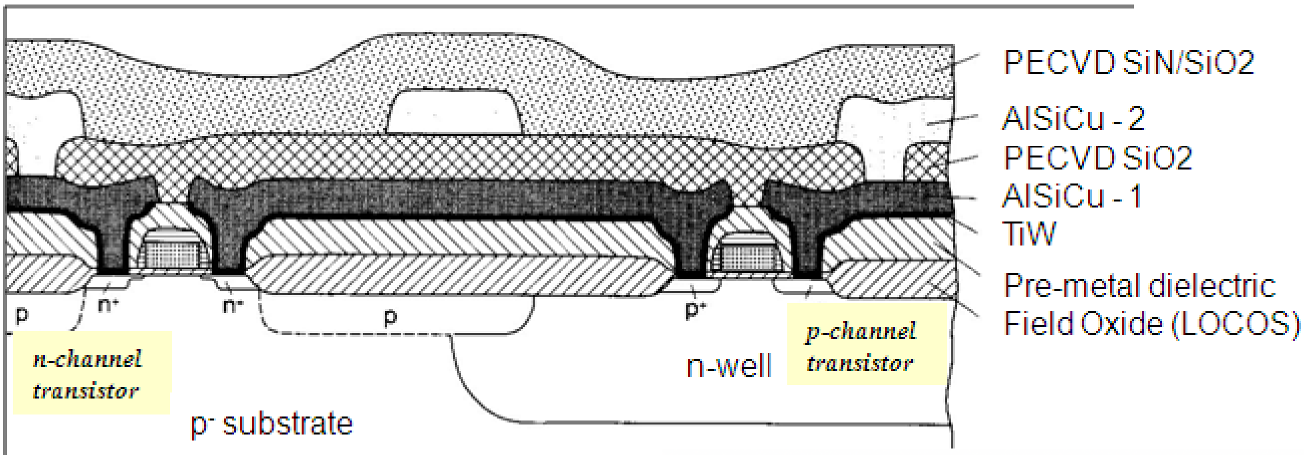


$V_{IN} < V_{th}$ (threshold voltage):
T1 (n channel) is blocked
(i.e. n channel enhancement mode)
$V_{OUT} = V_{DD}$ because T2 (p channel)
is conducting.
Reason: Negative voltage between gate and source (as long as $V_{IN} < V_{DD}$) controls T2

$V_{IN} > V_{th}$:
T1 conducting,
V_{OUT} decreases with increasing V_{IN}
T2 operates in the active mode,
$V_G=V_{DD}-V_{OUT}+V_{Th}$

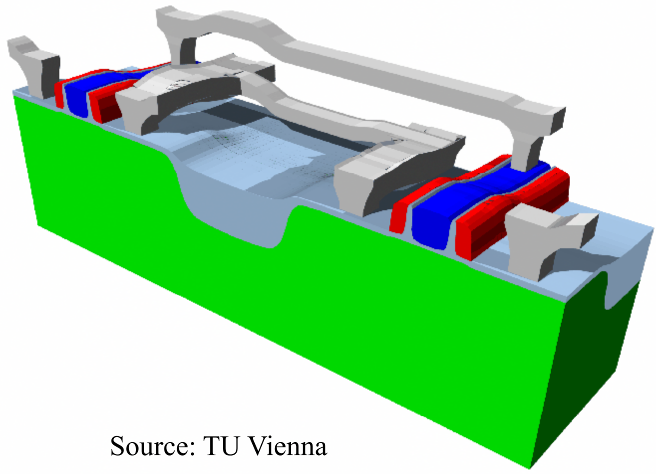
Technology:
- Gate (channel) length L determines switching behavior
- Gate dielectric thickness (100…< 10 nm) determines transconductance of the transistor
- Metallization critical for shallow p-n junctions
- Isolation by SiO_2 (local oxidation of Si = LOCOS or shallow trench isolation = STI)
- Passivation: Phosphorus Silicate Glass =PSG (getters mobile impurities)
- Na (sodium) ions are harmful (mobile ion impurities) - degrading device characteristics
- Metallization: Al, AlSi, AlSiCu, AlCu, **Cu**

CMOS Structure - Technological realization



Cross section of a CMOS structure

Source: B. Hoppe, Mikroelektronik, p. 287



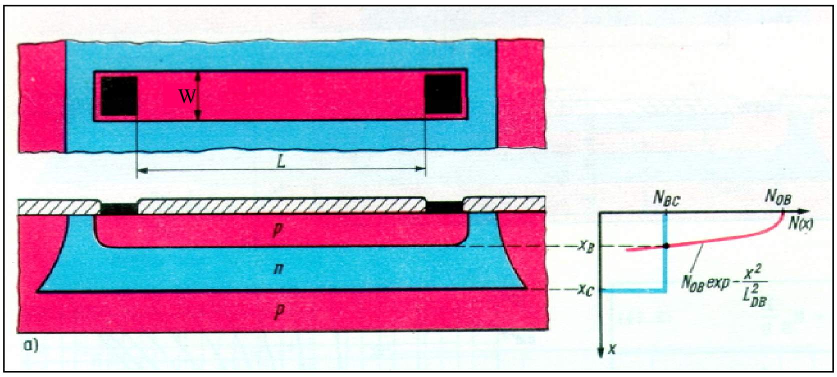
Fabrication see chapter 5.1

Source: TU Vienna

Resistor:

Very high-resistance n-doped epitaxial layer → The low-resistance p doped layer (red) is formed by boron implantation and used as a resistor after contact formation.

$$R = \rho \cdot \frac{L}{x_j \cdot W}$$

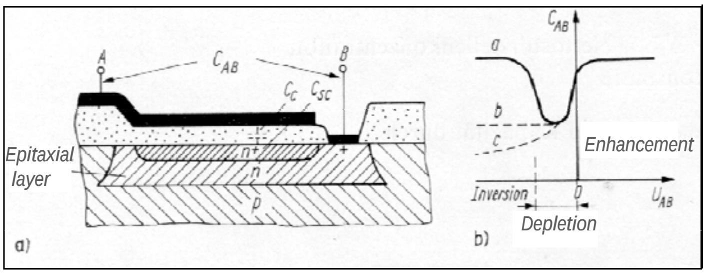


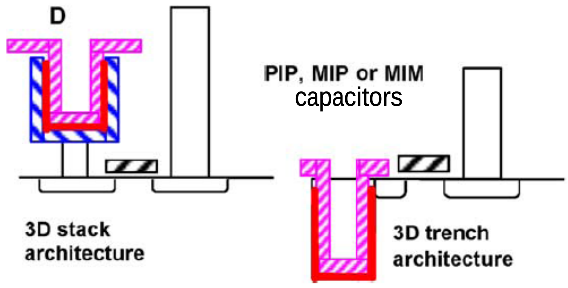
Capacitor:

$$C = \varepsilon_0 \varepsilon_r \cdot \frac{A}{d_{SiO_2}} = \varepsilon_0 \varepsilon_r \cdot \frac{L \cdot W}{d_{SiO_2}}$$

L, W = length, width of the area where the electrodes do overlap
d_{SiO_2} = thickness of SiO_2

MOS capacitor





2.4 Development Trends

- Production of many identical devices / circuits / chips by one process → cost !
- **Characteristic quantities:**
  - Wafer diameter (now: 300 mm)
  - Die size ca. 100 - 200 mm^2
  - Number of transistors per die (degree of integration)
  - Yield
- Main feature: **New and improved products (performance, reliability)**
  - Require the continued increase of degree of integration

  → scaling down (miniaturization of devices, decrease of lateral dimensions and layer thicknesses)
  - Increase of die size

  Goal: equal or higher yield than in previous technology node

- **Trend:**

Year	Era	Critical dimension	Degree of integration
1968 ... 1972	MSI (Medium Scale Integration)	> 6 µm	~ 10^2
1972 ... 1981	LSI (Large Scale Integration)	2.5 ... 6 µm	~ 10^3
1981 ... 1989	VLSI (Very Large Scale Integration)	2.5 ... 1 µm	~ 10^5
since 1990	**ULSI** (Ultra Large Scale Integration)	< 1 µm	
since 2000		< 100 nm	≥ 10^8

Scaling ("More Moore")

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling* (occurs in conjunction with, and also enables, continued geometrical scaling) refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling* (occurs in conjunction with equivalent scaling and continued geometric scaling) refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
  - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
  - Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Trends

	Al gate PMOS	Si gate NMOS				Si gate CMOS				SGT	HKMG
	1969	1972	1975	1978	1981	1984	1987	1990	2000	**2006**	**2009**
t_{Ox} [nm]	150	120	110	70	50	40	25	20	4...7	1…2*	< 1*
L_{eff} [µm]	10	6	5	3	2	1,6	1	0,8	0.15	0.06	<0.03
x_j [µm]	2	1	0.8	0.5	0.4	0.35	0.3	0.25	0.10	0.03	<0.02
Masks	5	5	6	7...10	7...10	8...12	10...15	12...18	<18	<25	~28
Diameter of Si wafer [inch]	2	2	3	4	4	5	6	6 ...	200mm	300mm	300mm

L_{eff} = effective channel (gate) length

* EOT: equivalent oxide thickness

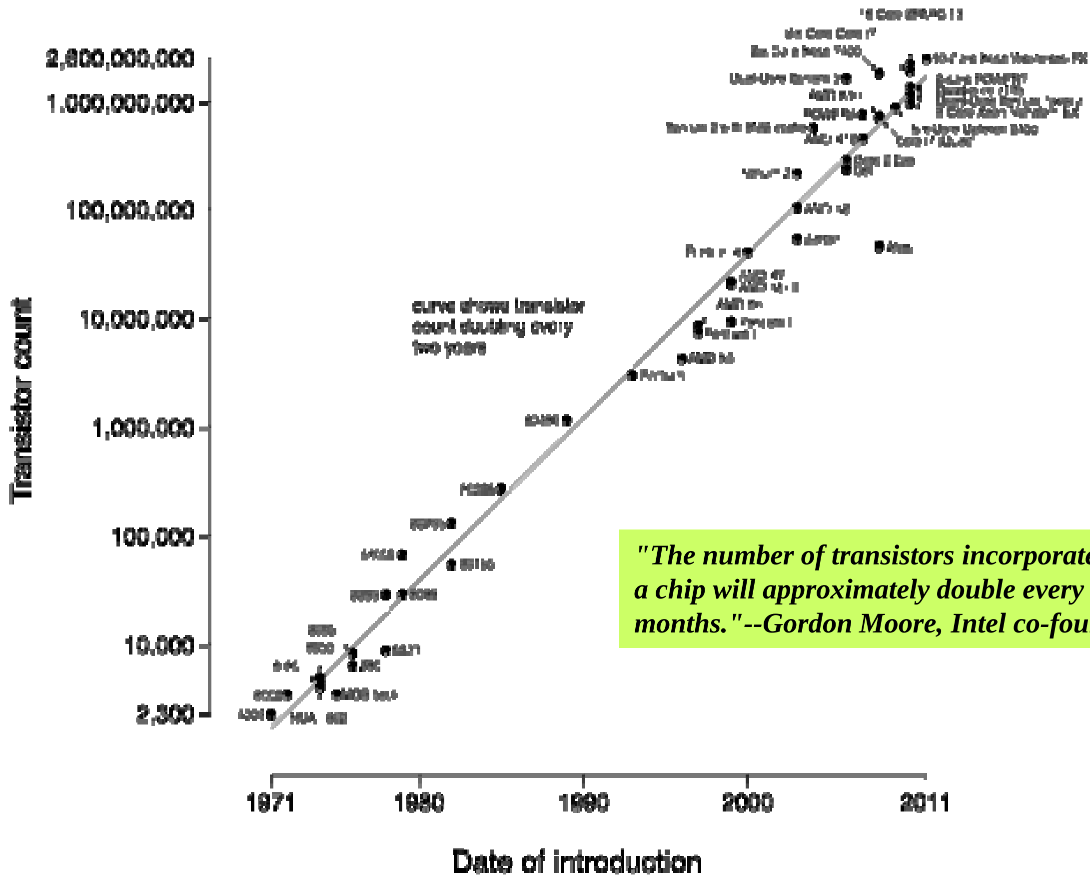
Moore's law: **Degree of integration** $I = 10^{0.2\,(\text{year} - 1970) + 2.75}$

(I is doubled every 1.5 ... 2 years)

Murphy: **Reduction of costs per device**

$$K_{EE} = K_0 \cdot 10^{0.2\,(\text{year} - 1970) - 1.8}$$

Microprocessor Transistor Counts 1971-2011 & Moore's Law



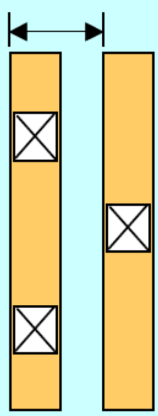
"The number of transistors incorporated in a chip will approximately double every 24 months."--Gordon Moore, Intel co-founder

Source: http://en.wikipedia.org/wiki/File:Transistor_Count_and_Moore%27s_Law_-_2011.svg

Definition of Pitches

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

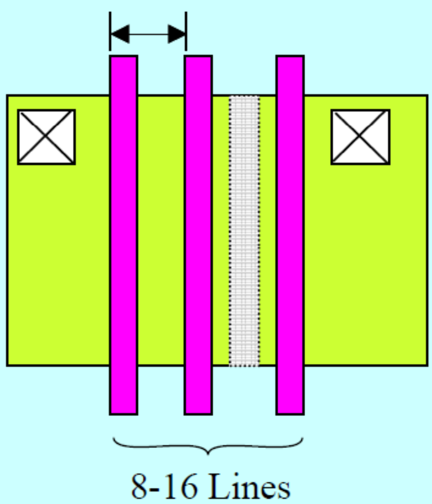
Metal
Pitch



Typical DRAM/MPU/ASIC
Stagger-contacted Metal Bit Line

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2

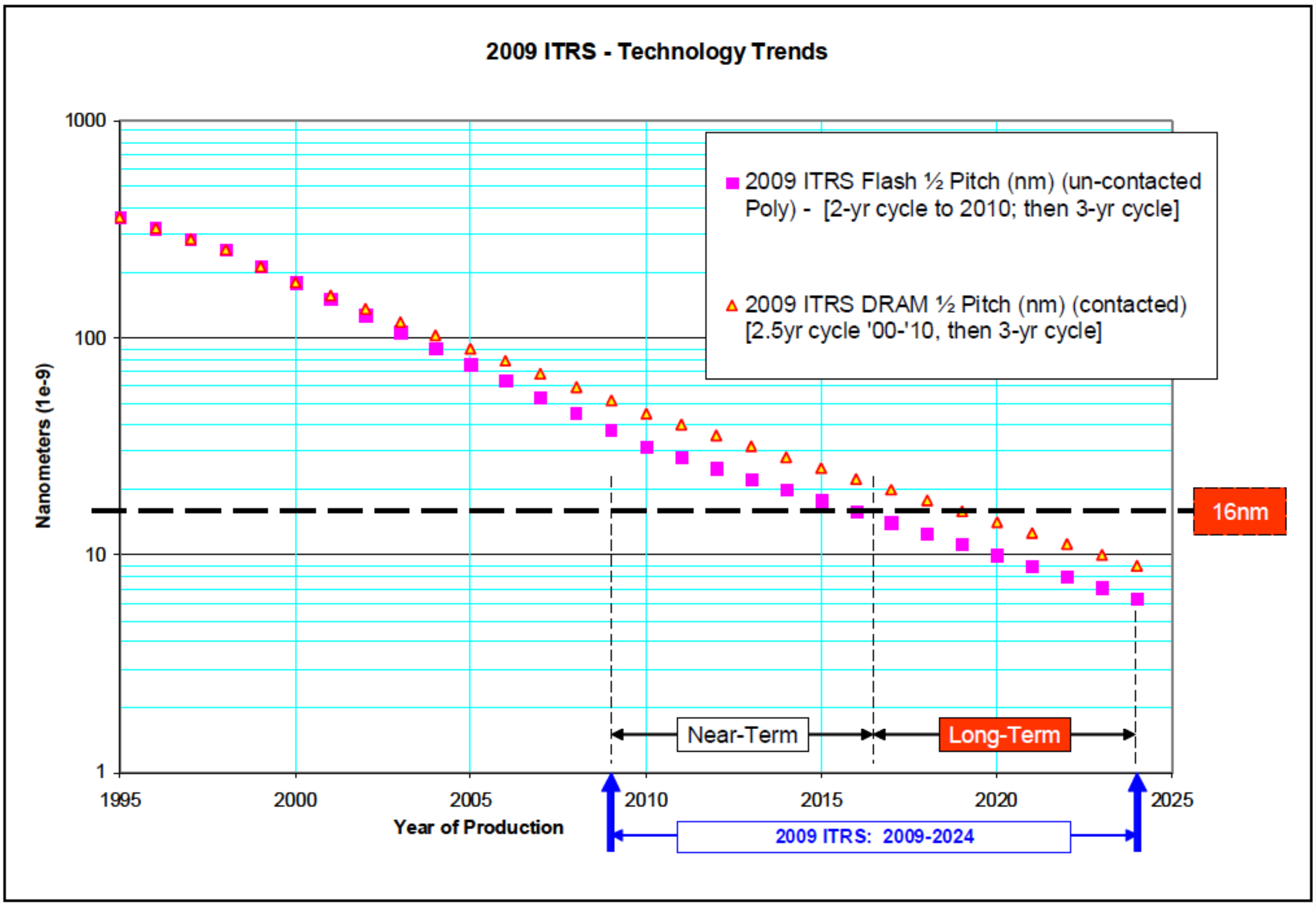
Poly
Pitch



Typical flash
Un-contacted Poly

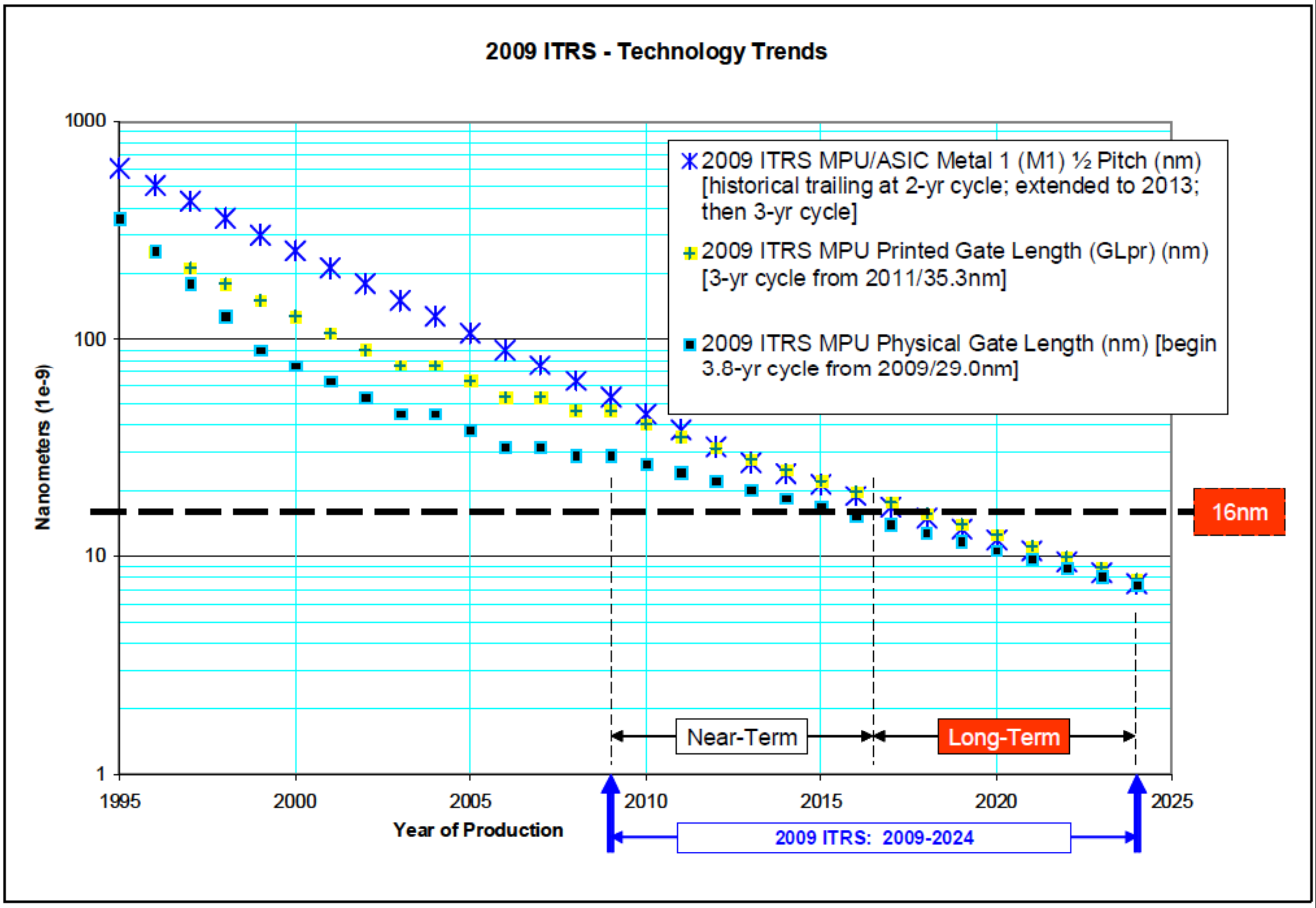
Advanced Integrated Circuit Technology

DRAM and Flash Memory Half Pitch Trends (2009 ITRS)

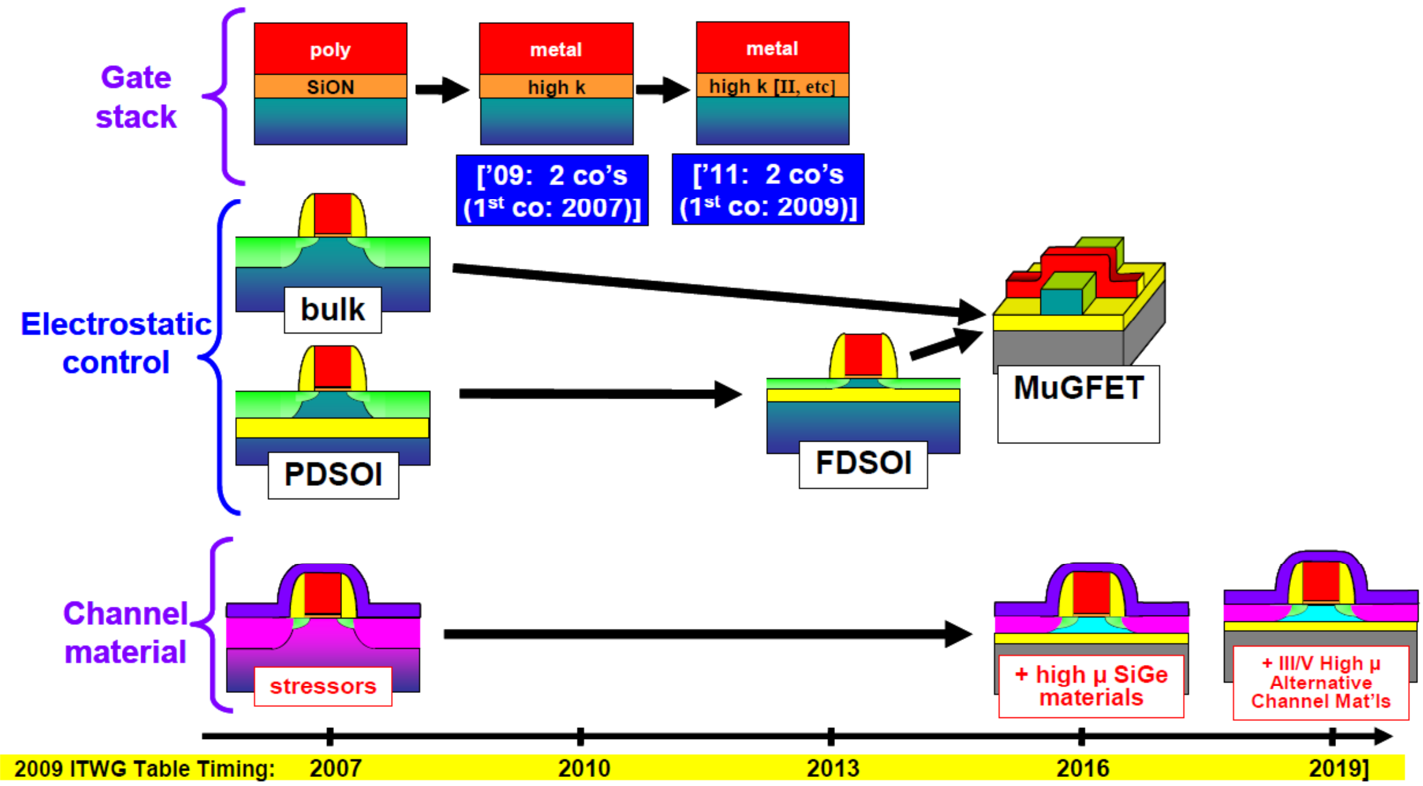


Advanced Integrated Circuit Technology

MPU/high-performance ASIC Half Pitch and Gate Length Trends (2009 ITRS)



"Equivalent Scaling" Process Technologies Timing compared to ORTC MPU/high-performance ASIC Half Pitch and Gate Length Trends and Timing (2009 ITRS)



SOI: silicon on insulator (PD: partially depleted; FD: fully depleted)
ORTC: Overall Roadmap Technology Characteristics

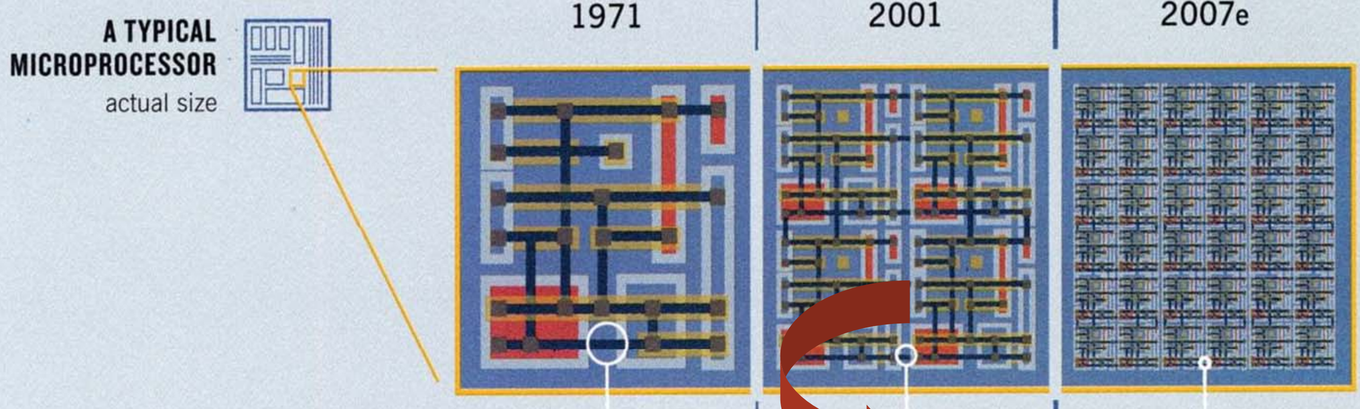
co: company
MuG: Multiple gate

Trends: ITRS 2005 for DRAM´s

	1995	2001	2005	2006	2008	2010	2013
DRAM ½ pitch	*350 nm*	*180 nm*	*80 nm*	*70 nm*	*57 nm*	*45 nm*	*32 nm*
Gate length		*100 nm*	*32 nm*	*28 nm*	*22 nm*	*18 nm*	*13 nm*
Memory	*64 Mb*	*1 Gb*	*2 Gb*	*2 Gb*	*4 Gb*	*4 Gb*	*8 Gb*
Cell size			$0.051 \mu m^2$	$0.039 \mu m^2$	$0.026 \mu m^2$	$0.016 \mu m^2$	$0.008 \mu m^2$
Effective oxide thickness			*4.4 nm*	*4.3 nm*	*2.8 nm*	*2.0 nm*	*1.4 nm*
Trench depth at 35 fF			*6.2μm*	*6.8μm*	*6.7μm*	*6.1μm*	*6.0μm*
Aspect ratio depth / width			*60*	*75*	*90*	*105*	*145*
Capacitor (bottle-shaped trench)	*Poly Si / ONO / Si*	*Poly Si /NO / Si*	*Poly Si / high-k/Si*	*Poly Si / high-k/Si*	*Metal / high-k/Si*	*Metal / high-k / Si or Metall*	*Metal / high-k / Metal*

DRAM: ½ pitch = Technology Node *ONO & NO: oxynitride* *higk-k: metal oxides, e.g. LaO_2 / HfO_2*

Microelectronics Development

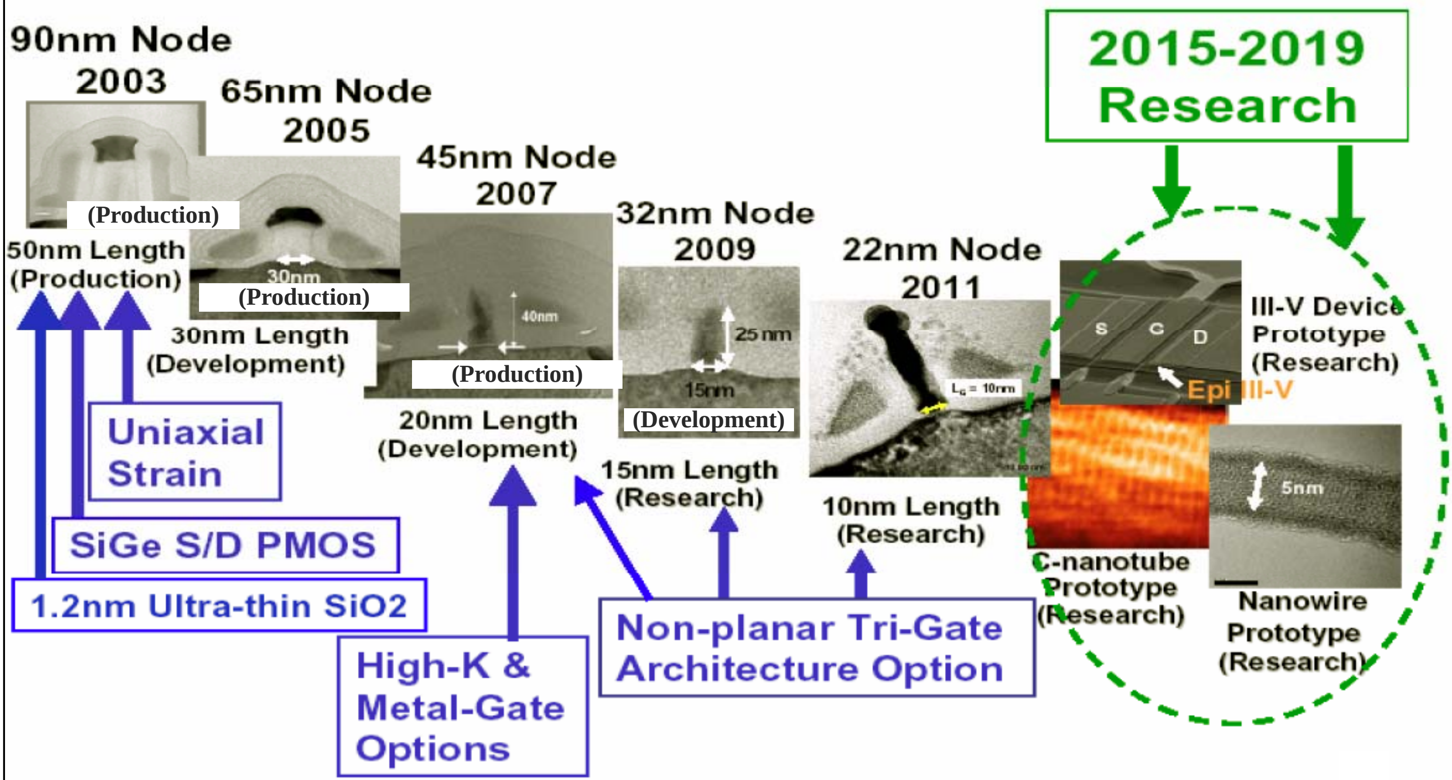


2003

0.10 Micron
(100nm)
Linewidth

Nanochip / Nanoelectronics
Era started

Nanoelectronics road to 2015 More Moore



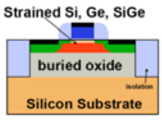
Source: A. Ionescu, European NanoDay 2007

After traditional scaling (CMOS)

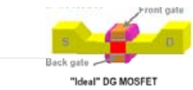
No general replacement for CMOS (yet?) !

Classical and non-classical CMOS

- high-k & metal gate
- transport enhanced



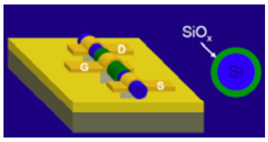
- multi-gate, UTB



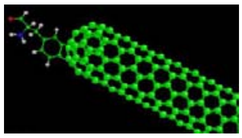
- metallic S/D
- ballistic

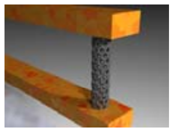
HYBRID CMOS-NANO

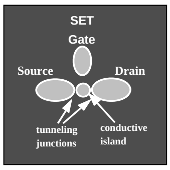
Nanowires (semiconductor)



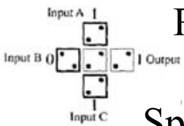
Nanotubes (CNTs)





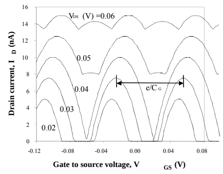


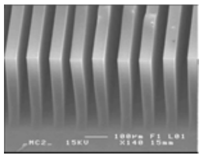
QCA



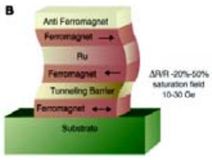
RTD RSFQ

SET



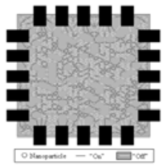


Spintronics



Molecular

2 0 1 5



Source: A. Ionescu, European NanoDay 2007