Trends in Microelectronics Technology

- More Moore (digital funtionality): Increase of integration degree - Geometrical scaling; equivalent scaling; design equivalent scaling
- More than Moore: integrating diverse functions into electronic devices & Sytems (digital+analog and other functions)
- Cost decrease per function (transistor)
- Wafer size increase (150mm → 200mm → 300mm)
- Equipment:
  - single wafer tools vs. Batch tools (e.g. 5 wafers, 200 wafers)
  - Cluster tools: different processes (in a sequence) with same environment (vacuum, wet) are combined in one tool

Definition of Geometrical and Equivalent Scaling (More Moore = digital function)

- *Geometrical (constant field) Scaling refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.*

- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling) refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.*

- *Examples for Equivalent Scaling measures?*
  - *New materials: high-k dielectrics + metal gate (HKMG); low-k dielectrics, Cu instead of Al, stressor films, strained Si*
  - *FinFET, multigate transistors*
  - *Fully depleted SOI (FDSOI)*
  - *Strain Engineering*

Overall Process

Phase 1: ***Preparation***

crystal pulling
mechanical treatment (diameter)
wafer fabrication: sawing, lapping, polishing, epitaxy

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Phase 2: ***Wafer processing*** *(Frontend – FE)*

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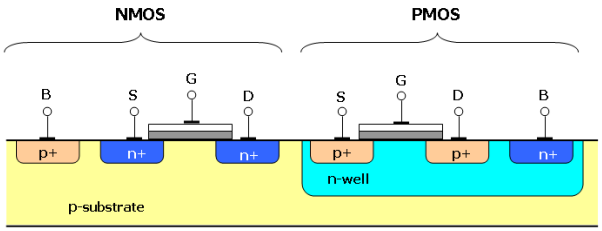
f(product, basic technology)

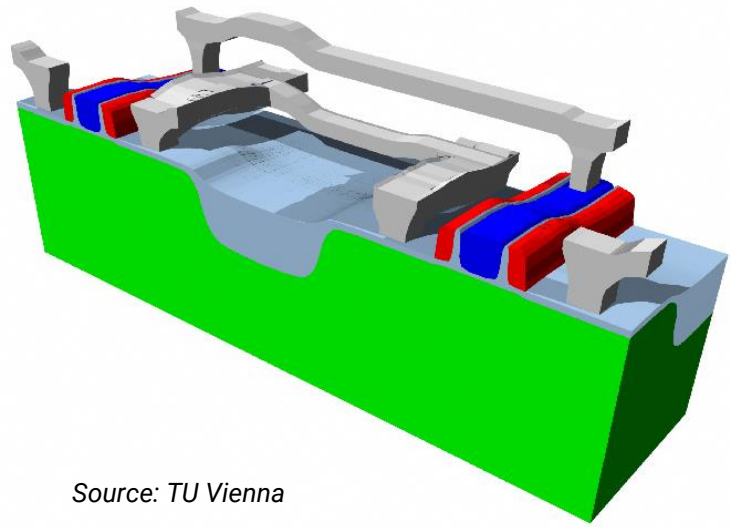
∑ *Basic process steps (BPS)*

- *BPS 1*
- *BPS 2*
- *...incl. repetition (see lecture "Technologies for Micro and Nano Systems" and section 3.1 ... 3.9)*

- *BPS/processes often summarized in process modules (see chapter 5.1)*

e.g. **CMOS:**





Source: TU Vienna

testing

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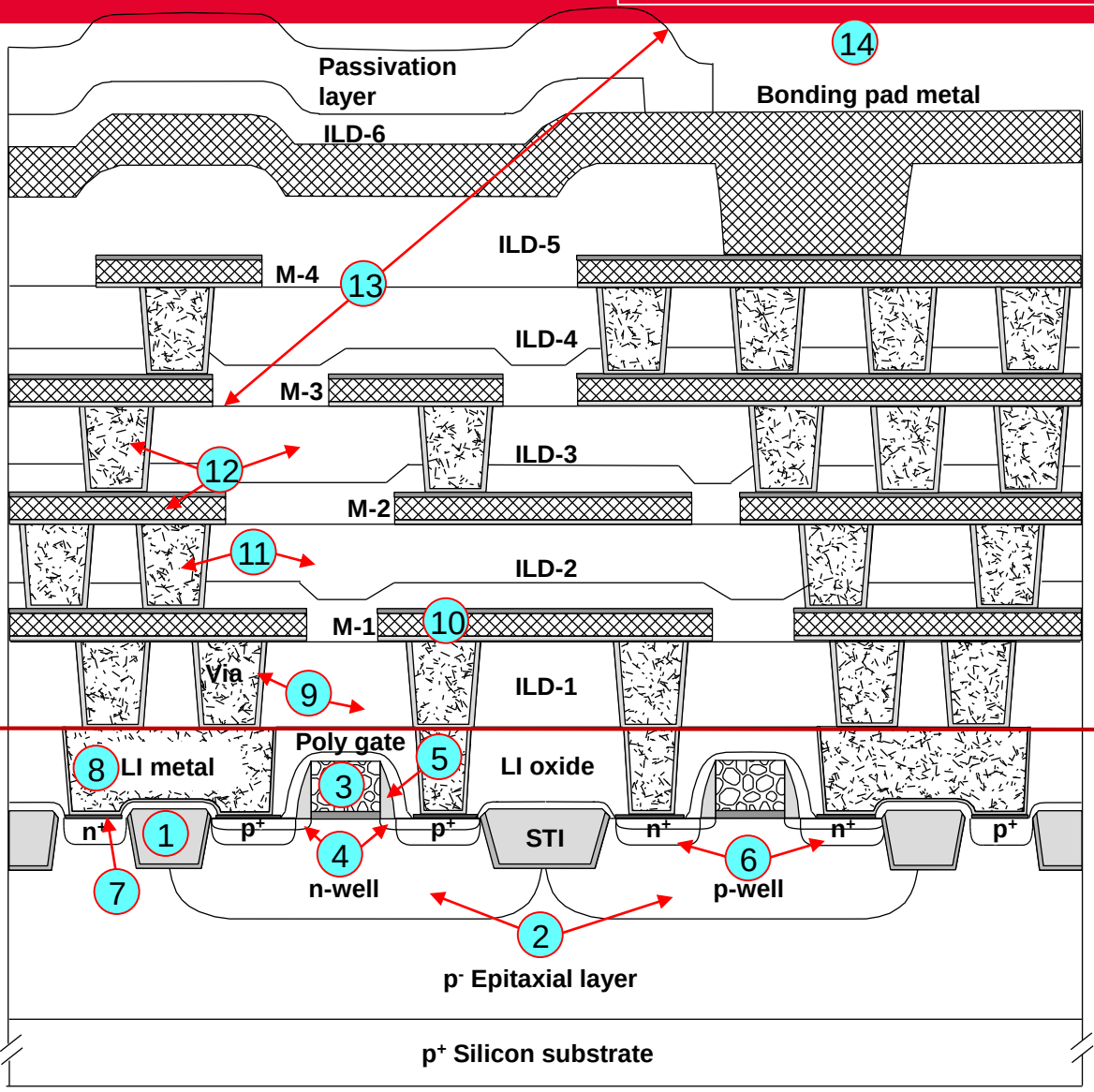
Phase 3: ***Packaging*** *(Backend – BE)*

die separation
mounting
bonding
encapsulation

CMOS Manufacturing Steps (0.25 µm and below)

Process Modules (Front-end)

1. Shallow Trench Isolation (STI)
2. Twin-well Implants
3. Gate Structure
4. Lightly Doped Drain Implants
5. Sidewall Spacer
6. Source/Drain Implants
7. Contact Formation
8. Local Interconnect — FEOL
9. Via-1 / Metal 1 Formation
10. Via-2 / Metal 2 Formation
11. Via-3 / Metal 3 Formation
12. Via-4 / Metal 4 Formation
13. Bond Pad Metal & Passivation
14. Parametric Testing — BEOL



Full 0.18 µm CMOS Cross Section

Terms (1)

Basic process steps (BPS)

- *indivisible step in the process flow*
- *characterized by physical / chemical parameters (temperature, pressure, gas flow ...)*

- *Examples:*
  - *Ion implantation step*
  - *special annealing step (furnace anneal, RTP)*
  - *special cleaning step (rinsing)*
  - *Special deposition step (CVD, sputtering)*
  - *Special Lithography step (deposition of resist, exposure, development, ...)*

Technology: $\sum$ **BPS**

Terms (2)

Process

- consists of one or several BPS (in a sequence)
- carried out by using of specific tools (equipment)
- standardized component of a technology
- results in achievement of a specific property

Examples:

- doping (ion implantation, activation anneal),
- photolithography (deposition of resist, exposure, development, ...)

Basic technology

Sum of processes (or BPS) to be performed for the fabrication of a specific product, e.g. CMOS, BICMOS, Bipolar, ...

Seminar 1 CVD: Chemical Vapor Deposition

Definition

- Deposition of (thin) films having a desired structure and specific properties
- From the gas phase as a result of chemical gas-solid reactions
- Activated by supplying energy, e.g. in form of heat, plasma, or light.

- Wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit
- Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber.
- Additional non-volatile by-products are not desired (co-deposition with desired film or reaction with substrate leading to interfacial layers)

Materials: Insulators, metals, metal nitrides, poly-crystalline silicon

(single-crystalline silicon / other materials → epitaxy)

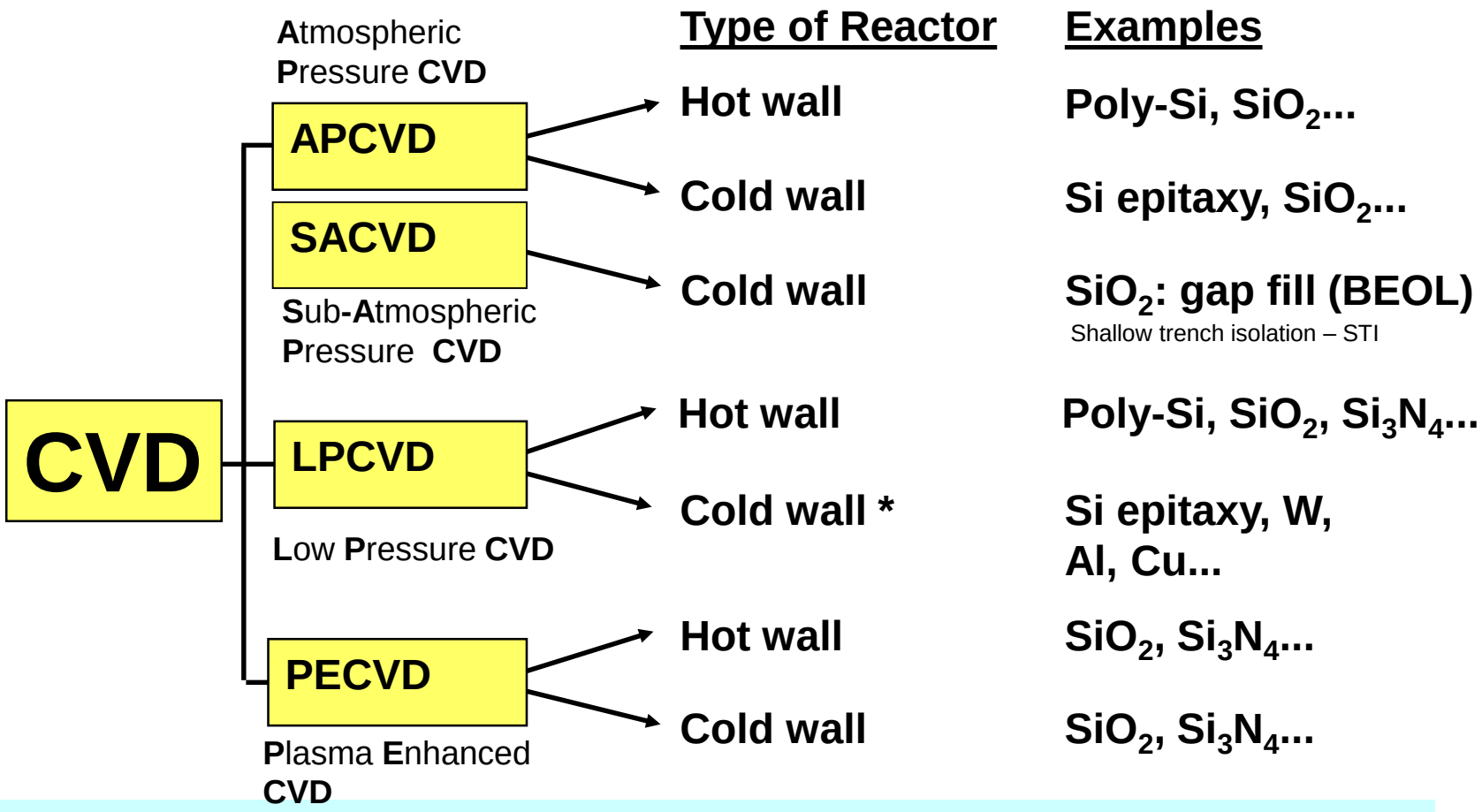
Specific Examples: Cu, W; TiN, TaN; SiO2, SiN

Overview of CVD Processes: Process types

Categories for classification:

- By pressure (APCVD, LPCVD, SACVD)
- By activation: thermal CVD, Plasma enhanced (PE)CVD
- By type of reactor: hot wall / cold wall reactor

Overview of CVD Processes



* advanced LPCVD techniques such as rapid thermal LPCVD (RTCVD) currently under study, for example for silicide technology to realize extremely flat contacts