3.1 Special CVD Processes

3.1.1 Metal CVD (W, Cu)

3.1.2 Conductive Barrier CVD

3.1.3 Applications of Poly-Si, SiO_2, Si_xN_y

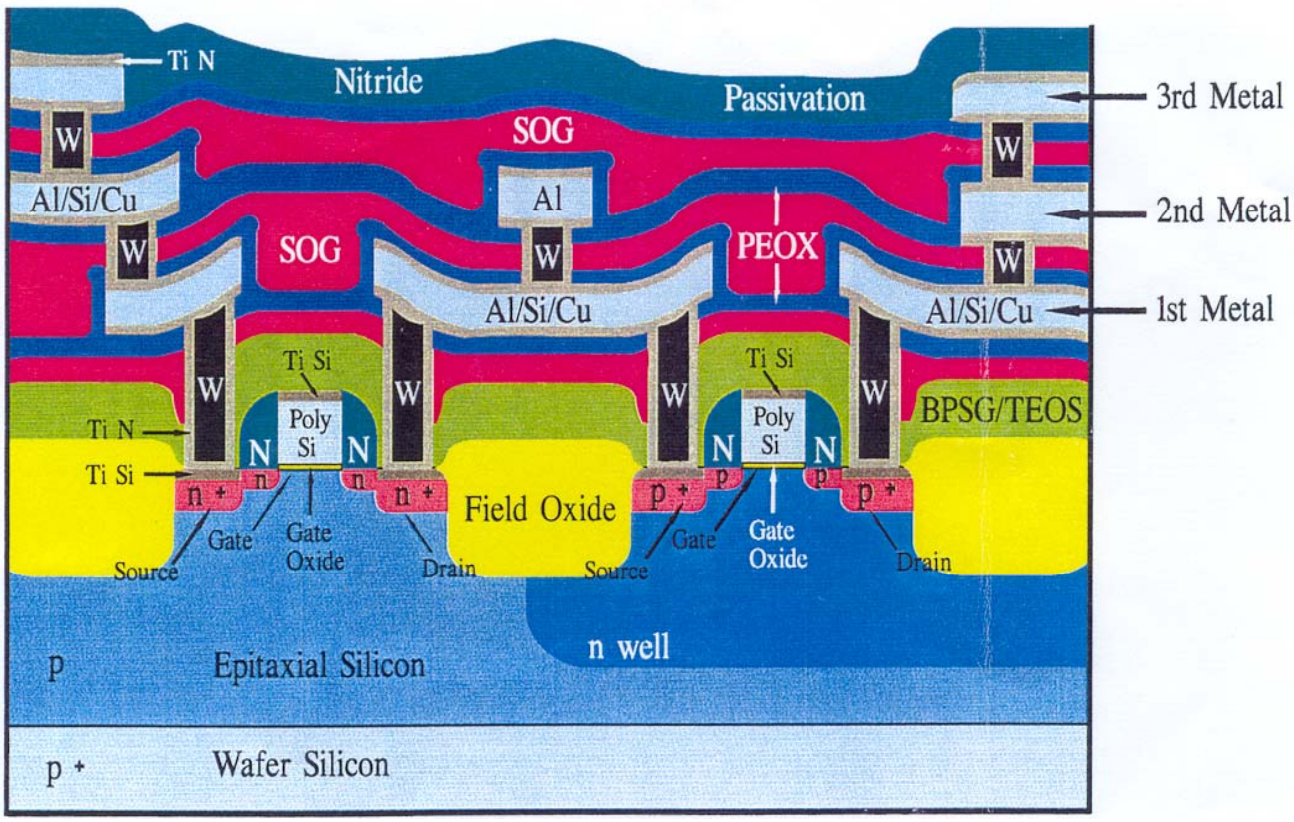
3.1.4 CVD of low-k dielectrics

3.1.3 Applications of Poly-Si, SiO_2, Si_xN_y

- Overview on application and integration aspects
- CVD SiO_2: Requirements (PMD, IMD), SACVD+LPCVD (TEOS, ozone), equipment, application examples
- (PE)CVD Si_xN_y: Applications, chemical reactions, PECVD process example

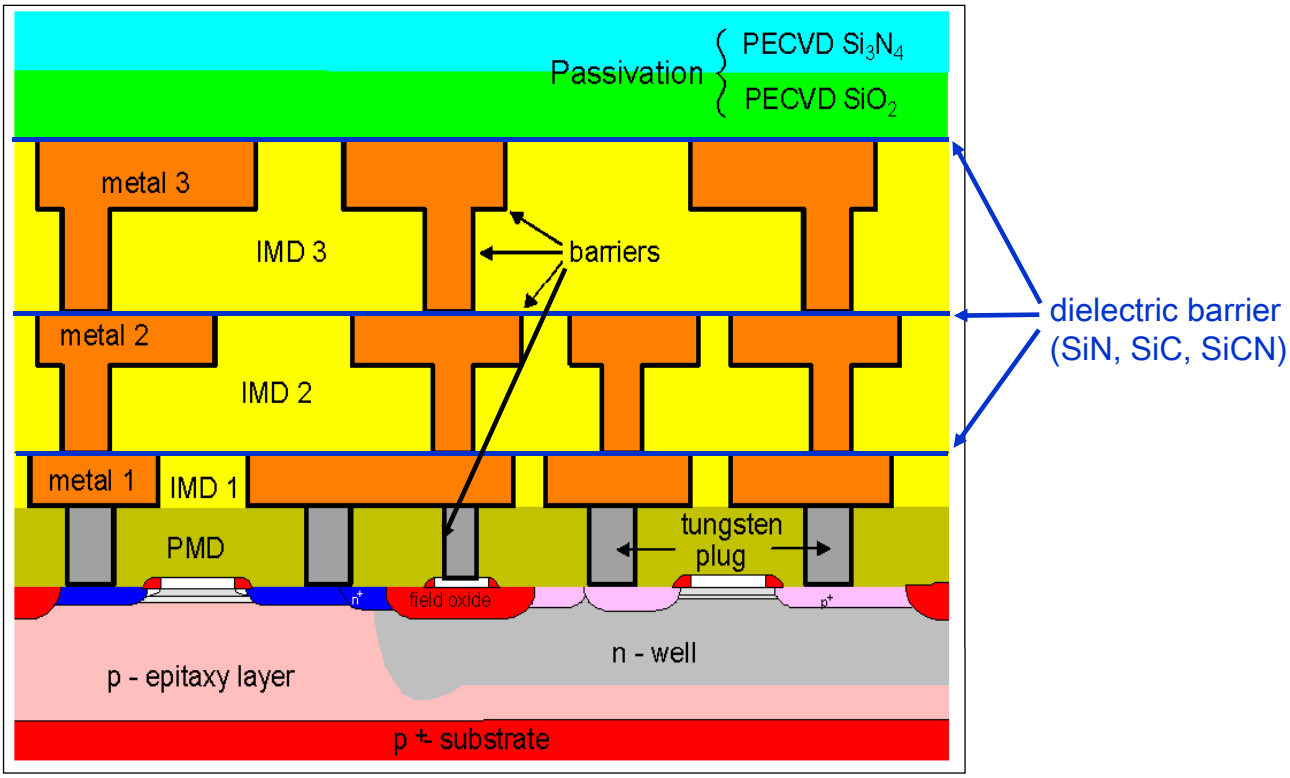
3.1.3.1 Application of polysilicon and dielectrics

Three Metal Layer CMOS Device



Source: PTI Seminars, Inc, 1749 Gilsinn Ln, St. Louis, MO 63026

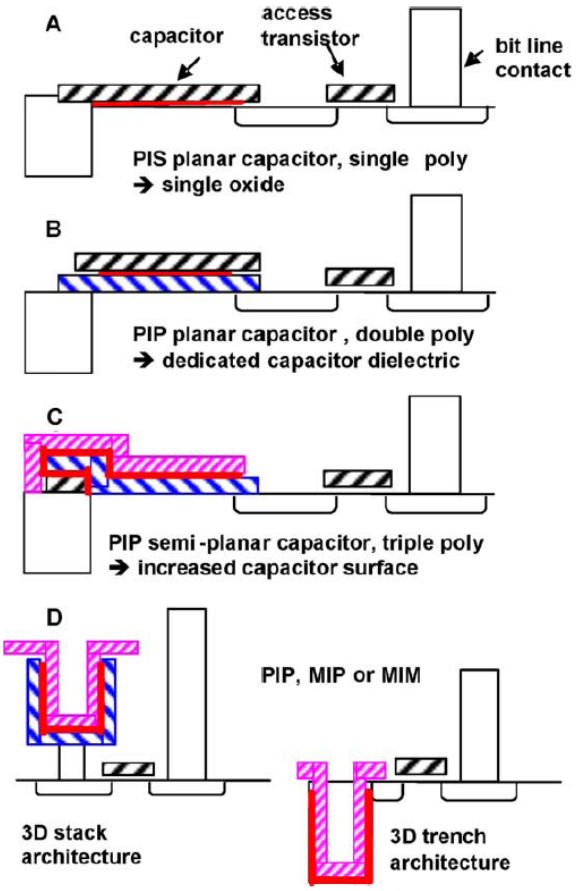
Thin CVD Films in Copper Damascene



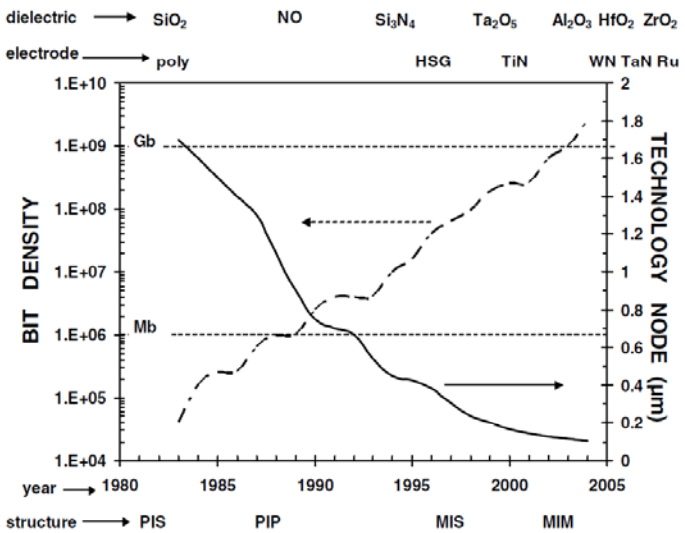
SiO2: Pre-Metal Dielectric (PMD), Inter-Metal Dielectric (IMD), Spacer oxide
SiN: Diffusion barrier against Cu diffusion and drift, Etch stop, Spacer, Stressor
Poly-Si: gate electrode

Application of polysilicon and dielectrics

DRAM architecture evolution from 1980 to 2005



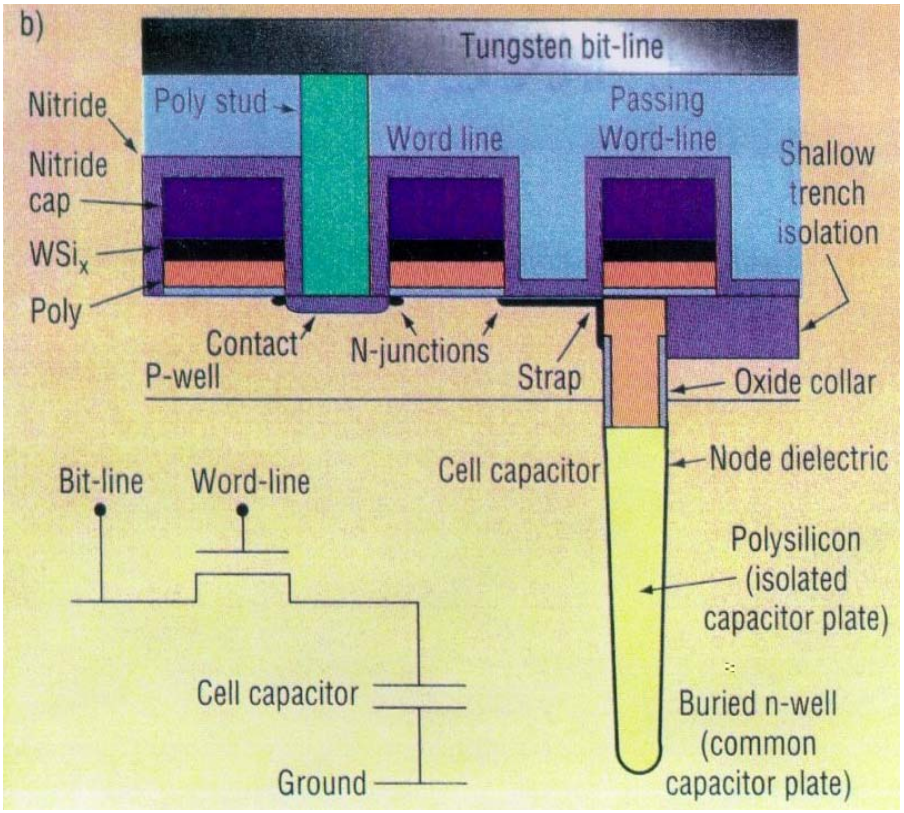
Trend of DRAM production node, bit density, dielectrics and electrode materials



HSG: Hemi-spherical grained polysilicon

Source: Eric Gerritsen et al., *Evolution of materials technology for stacked-capacitors in 65 nm embedded-DRAM,* Solid-State Electronics 49 (2005) 1767–1775

Buried Strap Trench Capacitor Cell for 64 MB



Source: B. El-Kareh, G.B. Bronner, S.E. Schuster, "Solid State Technology", May 1997
-The Evolution of D-RAM Cell Technology-

3.1.3.2 CVD of silicon dioxide

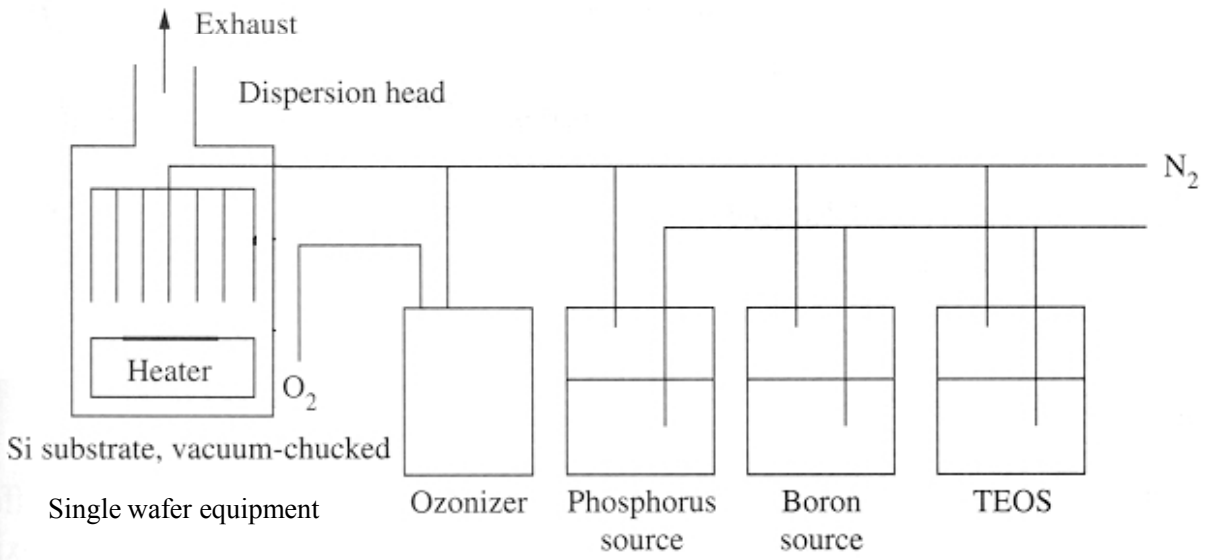
Different Requirements for Poly (Pre-) metal (PMD) and Intermetal Dielectrics (IMD)

- Poly (Pre-) Metal Dielectrics PMD
  - deposition can be done at higher temperatures
  - flow and re-flow at temperatures exceeding 800 C
  - Trend to lower temperatures
- Intermetal Dielectrics IMD
  - maximum temperature is about 400 450°C
  - the Al, Cu and low-k dielectrics on the surface require the lower temperature

CVD of silicon dioxide

SA- and LPCVD using TEOS and ozone

CVD process using TEOS and ozone enables formation of oxide films with high conformality and low viscosity at low deposition temperatures



Basic hardware set-up of doped TEOS reactors

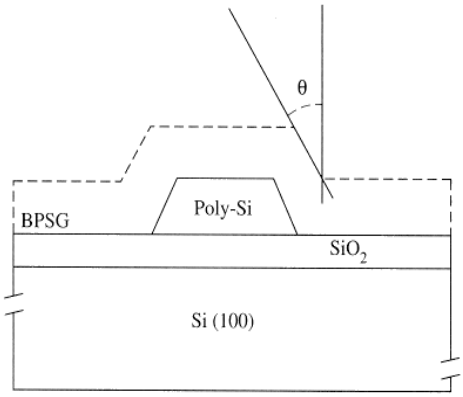
Advanced Integrated Circuit Technology

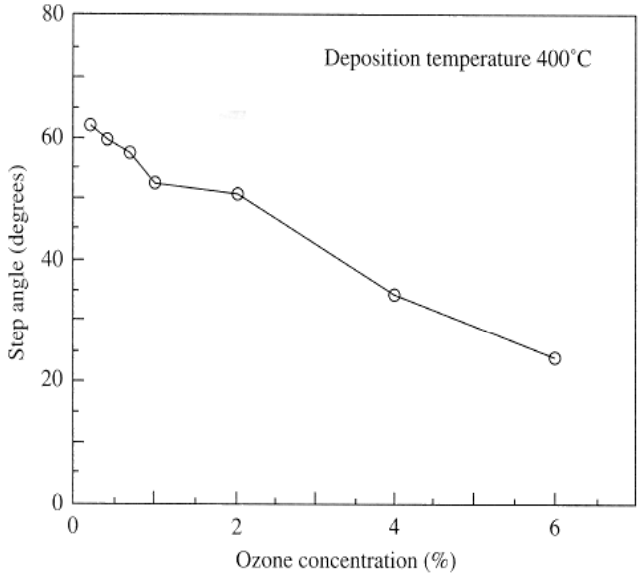
CVD of silicon dioxide

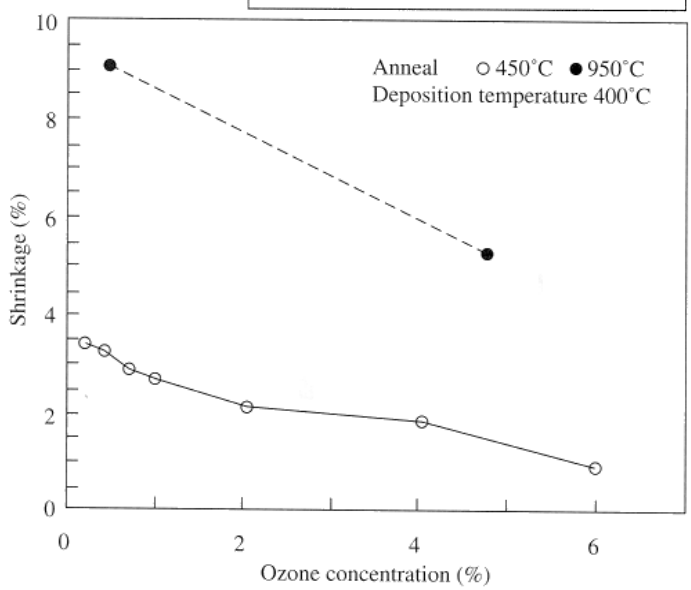
Deposition using TEOS and ozone

Film property control via ozone concentration:

- Step angle can be controlled via the O_3 concentration
- Dependence of the shrinkage during anneal on O_3 concentration







Source: C.Y. Chang, S.M. Sze, "ULSI Technology", McGraw-Hill 1996

ZfM Fraunhofer ENAS
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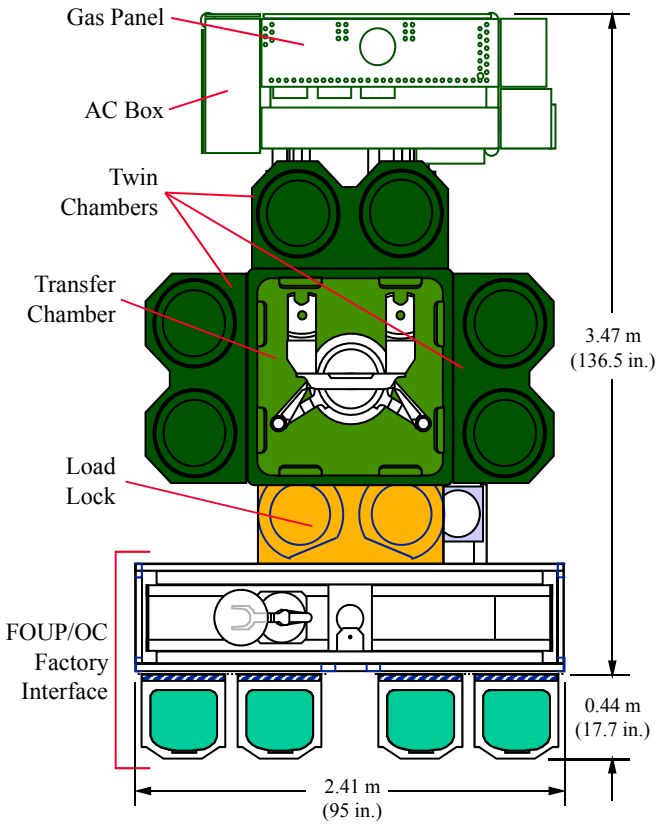
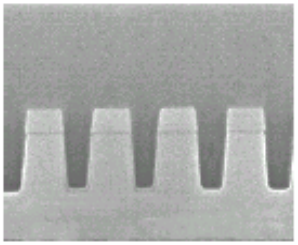
Maximum productivity PECVD and SACVD solutions

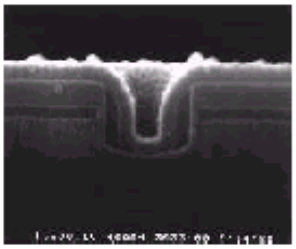


- PECVD Process: 200mm & 300mm
  - PE TEOS USG, PSG
  - PE Silane, DARC, Oxide, Nitride, Oxynitride
  - CVD Photoresist
- SACVD Process: 300mm only
  - Giga-Fill USG, BPSG, PSG
- Mainframe
  - Up to three twin process chambers
  - Factory interface options
    - 200mm Cassette SMIF
    - 300mm 2 or 4 pod FOUP
  - Integrated loadlock and cooldown
  - Twin blade VHP robot
  - G-PLIS precision liquid injection system
- Key peripheral modules
  - Remote plasma clean source standard

0.25 µm IC fabrication steps SA-CVD

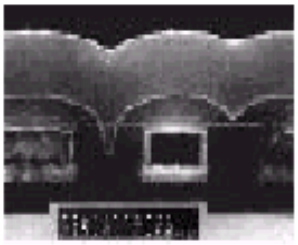


STI Dielectric
(SACVD USG)



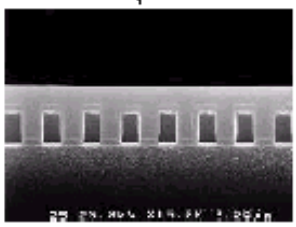
Sidewall Spacer Dielectric
(SACVD USG)

Intermetal Dielectric
(SACVD USG/PECVD TEOS)

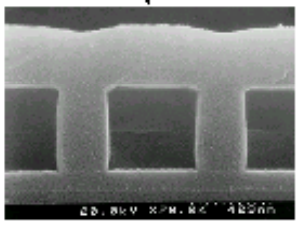


Planarized Passivation
(SACVD USG/PECVDSiN)

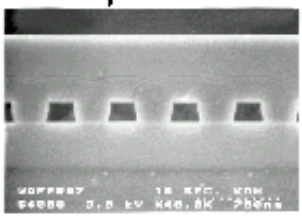
Interlevel Dielectrics



(SACVD BPSG+RTP+CMP)



(SACVD USG)



(SACVD PSG+CMP)

3.1.3.3 CVD of silicon nitride: Applications

Applications:
- as final passivation and mechanical protective layers for IC encapsulated in plastic packages
  - diffusion barrier against moisture and Na (sodium)
  - deposited by PECVD to have a low compressive stress preventing delamination and cracking under environmental stress
  - conformal coverage of underlying metal
  - low pinhole density
- as a mask for the selective oxidation of silicon (LPCVD)
- as sidewall spacers in MOSFETs
  - to form the LDD structure
  - to serve as sidewall passivation during the salicide process
- as CMP-stop layer in shallow trench isolation (STI)
- as etch-stop layer in damascene structures
- as stressor film(s) over n- and p-MOS transistors

Source: S. Wolf, R. N. Tauber, "Silicon Processing for the VLSI Era", Vol. 1, Lattice Press, Sunset Beach, CA., 2000 (extended).

CVD of silicon nitride: Reactions

SACVD : • $3\ SiH_4 + 4\ NH_3 \longrightarrow Si_3N_4 + 12\ H_2$

T ≈ 800 - 1050 °C p ≈ 10 - 40 Torr furnace

• $3\ SiCl_4 + 4\ NH_3 \longrightarrow Si_3N_4 + 12\ HCl$

T ≈ 750 - 900 °C p ≈ 1 - 5 Torr furnace

LPCVD : • $3\ SiCl_2H_2 + 4\ NH_3 \longrightarrow Si_3N_4 + 6\ HCl + 6\ H_2$

T ≈ 700 - 800 °C p ≈ 0.3 - 1 Torr furnace

• $3\ Si_2H_6 + 8\ NH_3 \longrightarrow 2\ Si_3N_4 + 21\ H_2$

T ≈ 550 - 600 °C p ≈ 0.1 - 0.4 Torr furnace

PECVD : • $x\ SiH_4 + y\ NH_3 \longrightarrow Si_xN_yH_z + (4x + 3y - z)/2\ H_2$

T ≈ 200 - 400 °C p ≈ 0.4 - 2 Torr single wafer

• $x\ SiH_4 + y/2\ N_2 \longrightarrow Si_xN_yH_z + (4x - z)/2\ H_2$

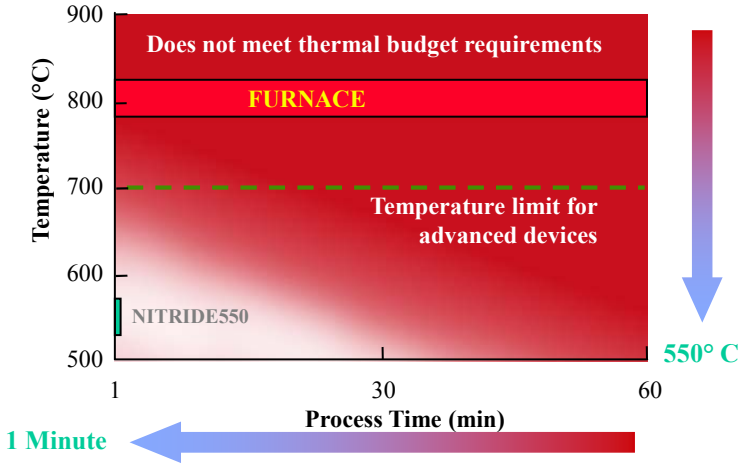
T ≈ 200 - 400 °C p ≈ 0.4 - 2 Torr single wafer

NITRIDE550™ Process benefits

Benefits

- Low thermal budget
- Low particles
- 550 °C process for 1 minute
- Single wafer control
- No backside deposition
- High productivity
  - over 80 wph for 2 Twin, 1000Å hardmask thickness

Thermal Budget Reduction with NITRIDE550



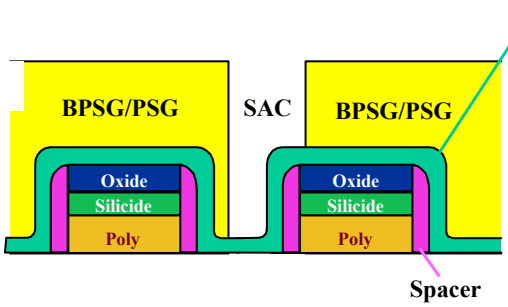
NITRIDE550 is enabling technology for < 0.25µm devices

Source:

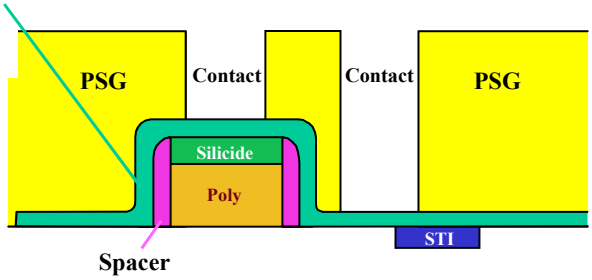
PECVD DIELECTRIC SYSTEMS & MODULES PRODUCT GROUP APPLIED MATERIALS®

CVD of silicon nitride: NITRIDE550™ Applications

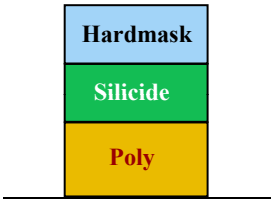
Self Aligned Contact (SAC) Etch Stop Layer



Borderless Contact Etch Stop Layer



Hardmask for Etch or Oxidation



PMD Etch Stop Layer, Hardmask and Spacer for DRAM and Logic Devices

Source:

PECVD DIELECTRIC SYSTEMS & MODULES PRODUCT GROUP APPLIED MATERIALS®

Properties of furnace and PECVD Nitride

	LPCVD	PECVD
	Furnace Nitride	NITRIDE550
Deposition Temperature (°C)	> 700	550
Deposition Rate (Å/min)	20	< 1300
Refractive Index	2.00	1.97
Stress (dynes/cm ^{2})	tensile Non-Tunable	1E9 Comp. Tunable
Uniformity (% / 1-sigma)	< 2.0%	< 2.0%
Wet Etch Rate (Å/min)(6:1 BOE)	**< 40**	**< 40**
Shrinkage (% / 950°C)	< 1	<1
Film Composition (%) (RBS) Si	44	46
N	56	54
Total Hydrogen (%) (NRA)	3	10 - 13
Cracking Resistance (3K film @ 950°C N_2 Anneal)	Pass	Pass
Etch Selectivity* (Ox. to Nit.) (flat / corner)	**> 100/30**	**100/20**
Etch Rate in Poly-silicon Etch	**1083Å/min**	**1170Å/min**
Backside Deposition	Yes	No

Considerations in replacing LPCVD nitride with PECVD nitride

Nitride must maintain integrity through many process steps

- DT Poly CMP
- Poly Recess Etch
- Oxide Collar Dry Etch
- Oxide Collar Wet Etch
- S.T.I. Oxide CMP

The 550°C PECVD nitride has similar poly recess etch rate and similar oxide wet and dry etch rates compared to LPCVD

Source:

PECVD DIELECTRIC SYSTEMS & MODULES PRODUCT GROUP APPLIED MATERIALS®

Advanced Integrated Circuit Technology

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