Trends in Microelectronics Technology

- Increase in integration density/degree / More Moore
  - Decrease in channel length
- Wafer size increase: 100 → 150 → 200 → 300 mm (leading edge, high volume) – legacy technology nodes (> 32 nm) become more and more important beside leading edge
- Cost decrease
- More than moore – increased functionality

Trends in Microelectronics Technology

- More Moore (digital funtionality): Increase of integration degree - Geometrical scaling
- More than Moore: integrating diverse functions into electronic devices & Systems (digital+analog and other funtions)
- Cost decrease per function
- Wafer size increase (150mm → 200mm → 300mm)
- Equipment:
  - single wafer tools vs. Batch tools (e.g. 5 wafers, 200 wafers)
  - Cluster tools: different processes (in a sequence) with same environment (vacuum, wet) are combined in one tool

Definition of Geometrical and Equivalent Scaling

- *Geometrical (constant field) scaling refers to ...*
  - *Shrinking of physical dimension (horizontally and vertically) to*
    - *Increase integration degree (cost per function decreases)*
    - *Improve performance (speed or power consumption)*

- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling) refers to …*
  - *Non-geometrical measures, e.g. new materials, improvements in the 3-dimensional* ***device*** *structure (design factor)*
  - *To boost the performance*

(Design equivalent scaling is needed beside that: design for variability, multicore architecture, low power design)

- *Examples for Equivalent Scaling?*

- Materials: gate dielectric – high-k, strain engineering/stressor technology, low-k dielectric dielectrics

- FinFET architecture – multigate transistors

Definition of Geometrical and Equivalent Scaling (More Moore = digital function)

- *Geometrical (constant field) Scaling refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.*

- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling) refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.*

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- *Examples for Equivalent Scaling?*
  - *New materials: high-k dielectrics + metal gate (HKMG); low-k dielectrics, Cu instead of Al*
  - *FinFET, multigate transistors*
  - *Fully depleted SOI (FDSOI)*
  - *Strain Engineering*

Overall Process

Phase 1: ***Preparation***

crystal pulling
mechanical treatment (diameter)
wafer fabrication: sawing, lapping, polishing, epitaxy

Phase 2: ***Wafer processing***
(Frontend – FE)

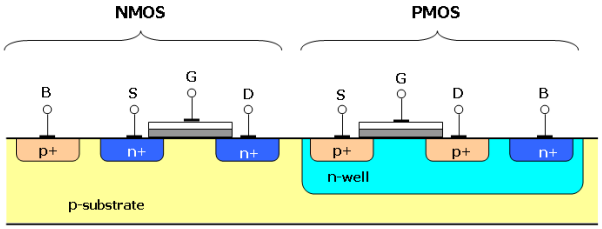
f(product, basic technology)

∑ Basic process steps (BPS)

- *BPS 1*
- *BPS 2*
- *...incl. repetition (see lecture "Technologies for Micro and Nano Systems" and section 3.1 ... 3.9)*

- *BPS/processes often summarized in process modules (see chapter 5.1)*

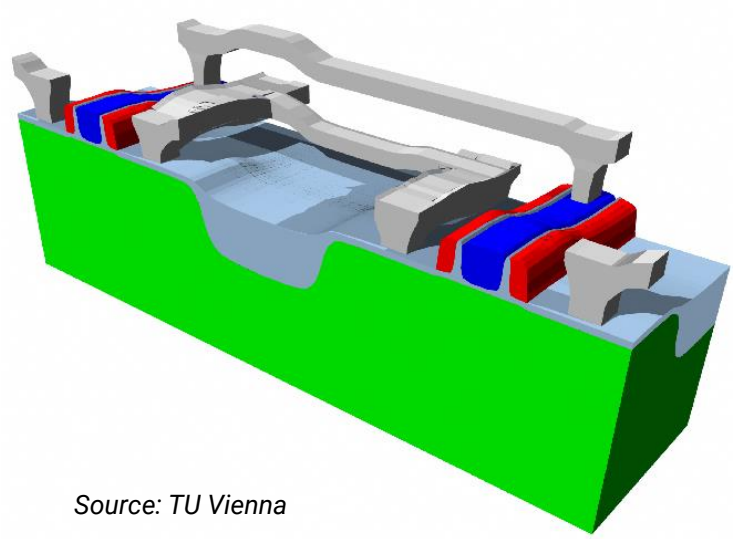
e.g. **CMOS:**



testing

Phase 3: ***Packaging***
(Backend – BE)

die separation
mounting
bonding
encapsulation

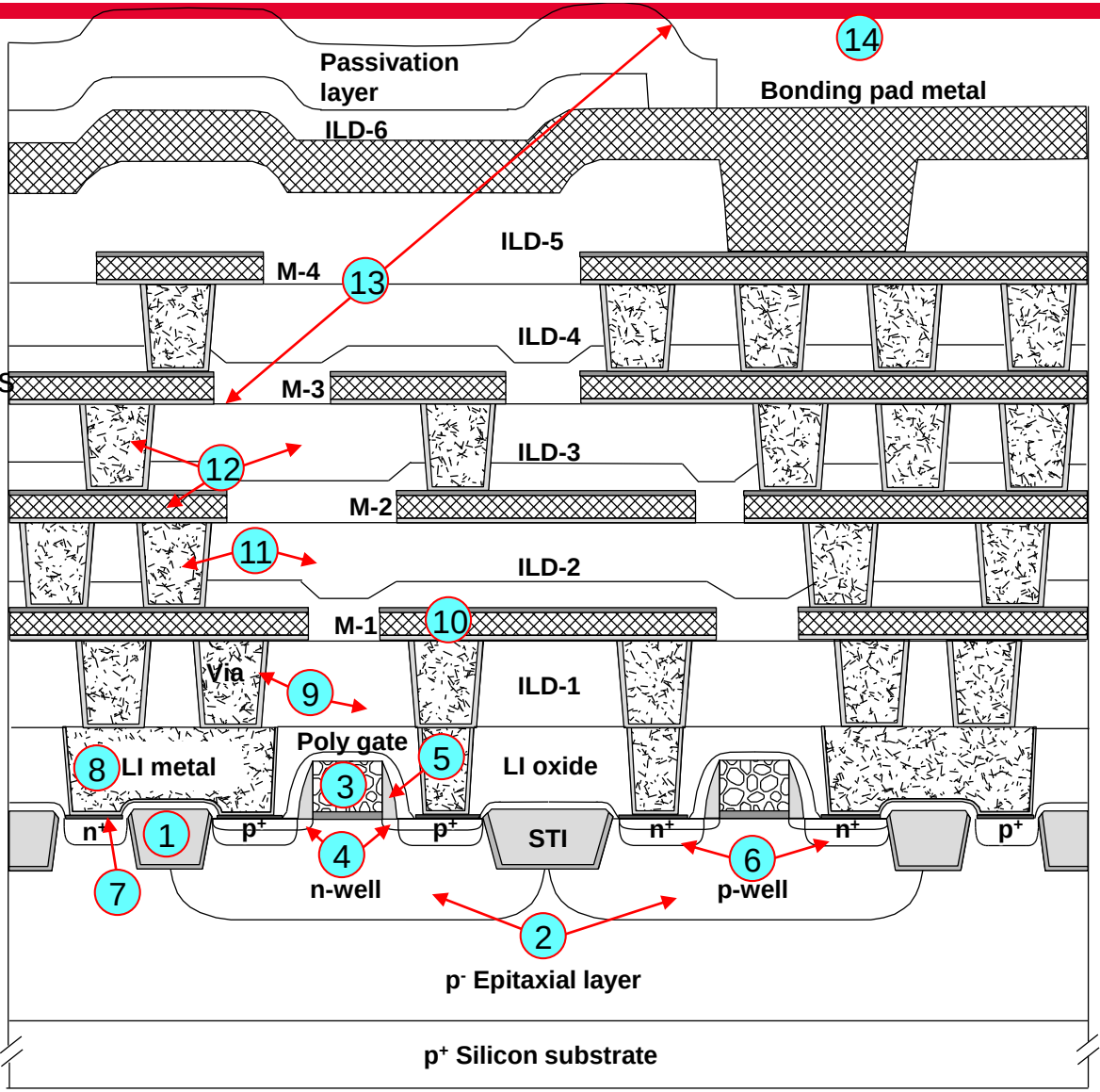


Source: TU Vienna

CMOS Manufacturing Steps (0.25 µm and below)

Process Modules (Front-end)

1. Shallow Trench Isolation (STI)
2. Twin Well Implants
3. Gate Structure
4. Lightly doped drain & source) implants (LDD)
5. Sidewall spacer
6. S/D implants
7. Contact formation (Self-aligned Silicidation of S/D/G)
8. Local Interconnect
9. Via1/metal1 Formation
10. Via2/metal2 Formation
11. Via3/metal3 Formation
12. Via4/metal4 Formation
13. Bond pad & passivation
14. Parametric Testing



Full 0.18 µm CMOS Cross Section

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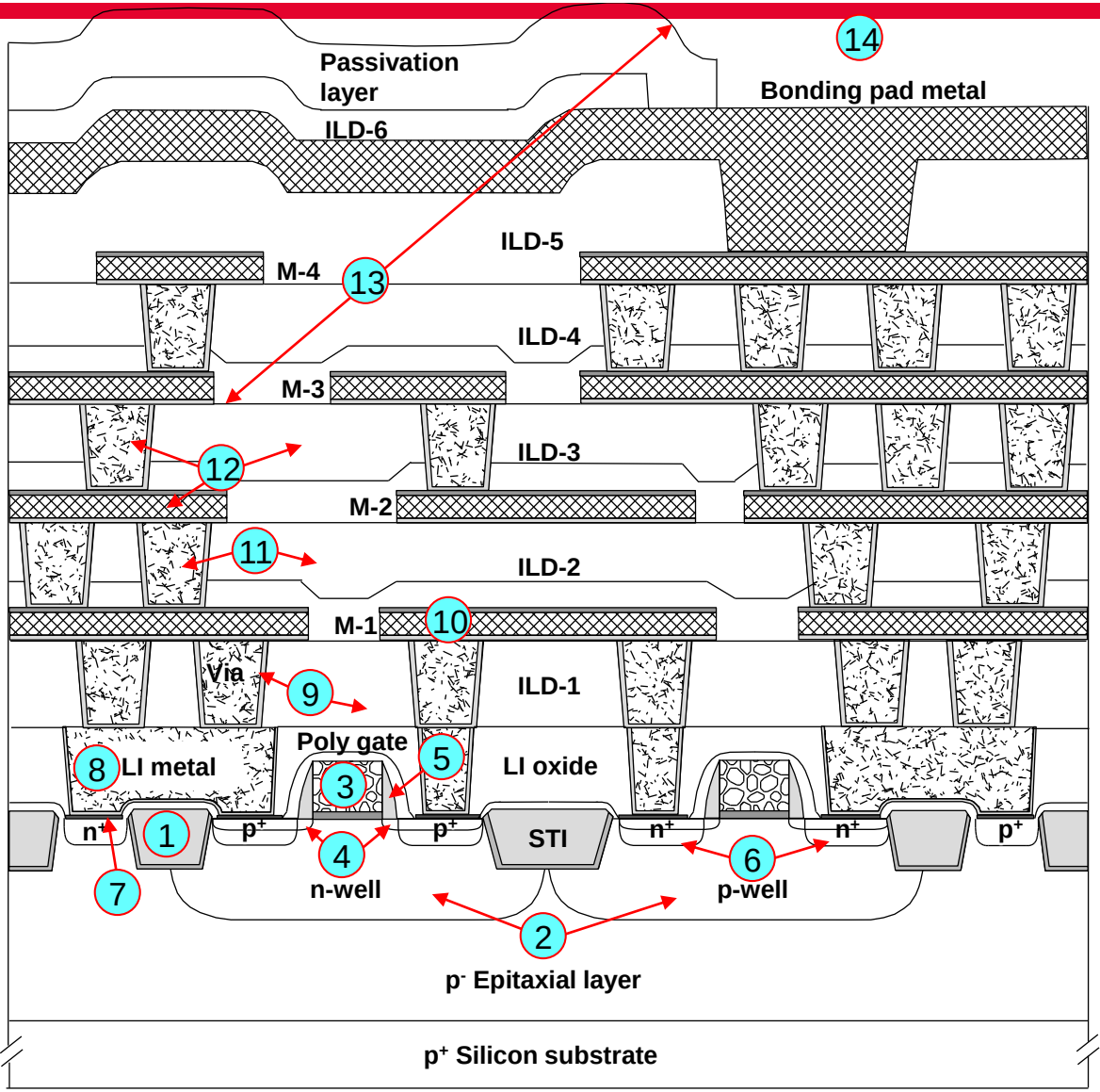
10. Via-2 / Metal 2 Formation
11. Via-3 / Metal 3 Formation
12. Via-4 / Metal 4 Formation
13. Bond Pad Metal & Passivation
14. Parametric Testing



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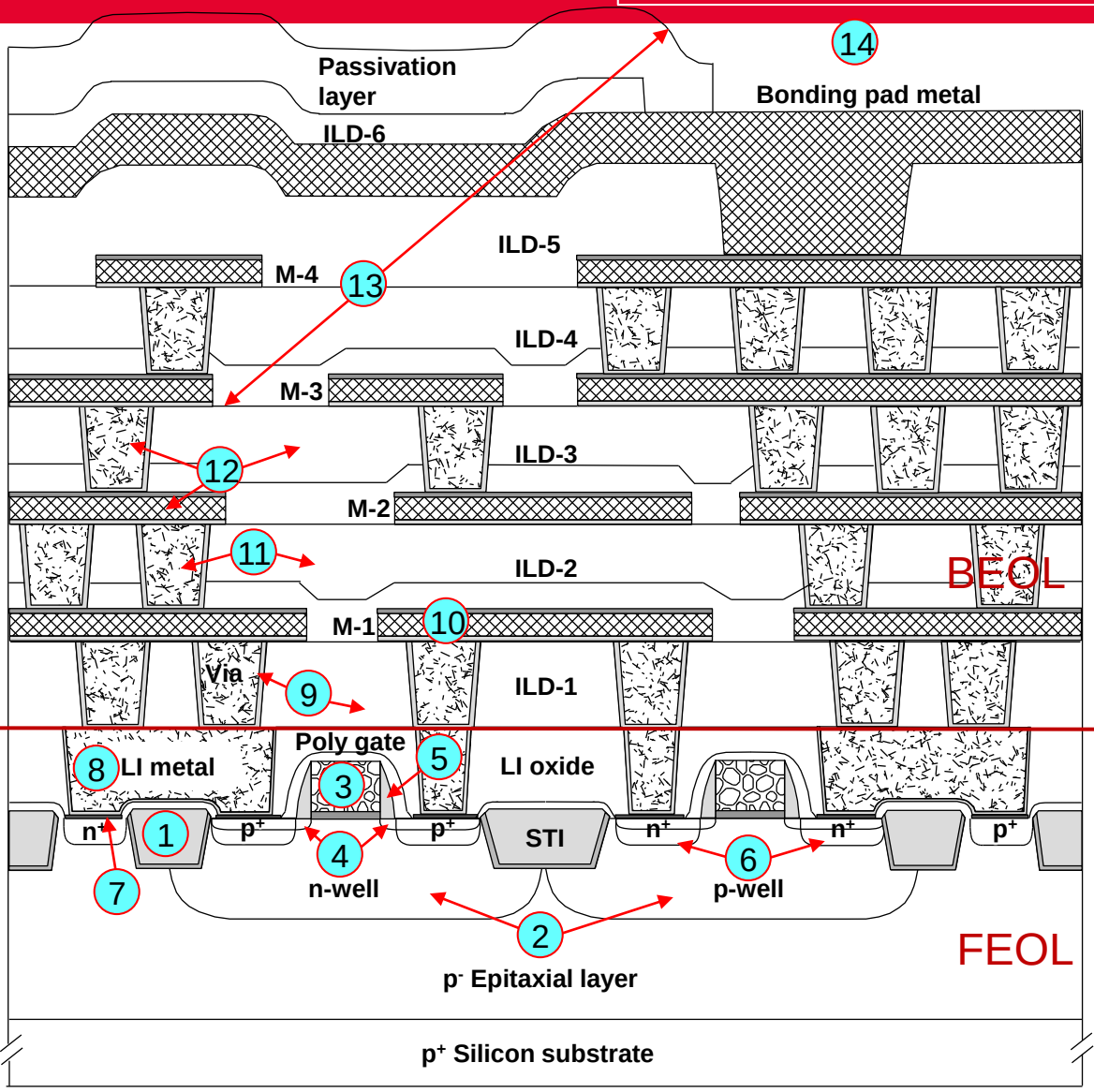
7. Contact Formation
8. Local Interconnect — FEOL
9. Via-1 / Metal 1 Formation
10. Via-2 / Metal 2 Formation
11. Via-3 / Metal 3 Formation
12. Via-4 / Metal 4 Formation
13. Bond Pad Metal & Passivation
14. Parametric Testing — BEOL



Full 0.18 µm CMOS Cross Section

Terms (1)

Basic process steps (BPS)

- Indivisable step (in the process technology)
- *Characterized physical and chemical parameters (T, p, gas flow, concentration, …)*

- *Examples:*
  - *CVD, Sputtering,*
  - *Cleaning step*
  - *Ion implantation*
  - *Etching step*
  - *Litho step*

Technology: sum of all BPS

Terms (1)

Basic process steps (BPS)

- *indivisible step in the process flow*
- *characterized by physical / chemical parameters (temperature, pressure, gas composition...)*

- *Examples:*
  - *Ion implantation step*
  - *special annealing step (furnace anneal, RTP)*
  - *special cleaning step (rinsing)*
  - *Special deposition step*
  - *Special Lithography step(deposition of resist, exposure, development, ...)*

Technology: $\sum$ **BPS**

Terms (2)

Process

- constists of (one or) some process BPS
- to achieve a certain outcome (functionality or property in the device)
- c
- d

Examples:

- Lithography – it contains several BPS
- Doping (consisting of implant and the annealing)
- Bump formation

BPS – Process → Process module → Technology

Basic technology

sum of BPS (processes) to be performed for the fabrication of a specific product

Terms (2)

Process

- consists of one ore more BPS
- carried out by using of specific tools (equipment)
- standardized component of a technology
- results in achievement of a specific property

Examples:

- doping (ion implantation, activation anneal),
- photolithography (deposition of resist, exposure, development, ...)

Basic technology

Sum of processes (or BPS) to be performed for the fabrication of a specific product, e.g. CMOS, BICMOS, Bipolar, ...