DESIGN OF POWER EFFICIENT JOHNSON COUNTER

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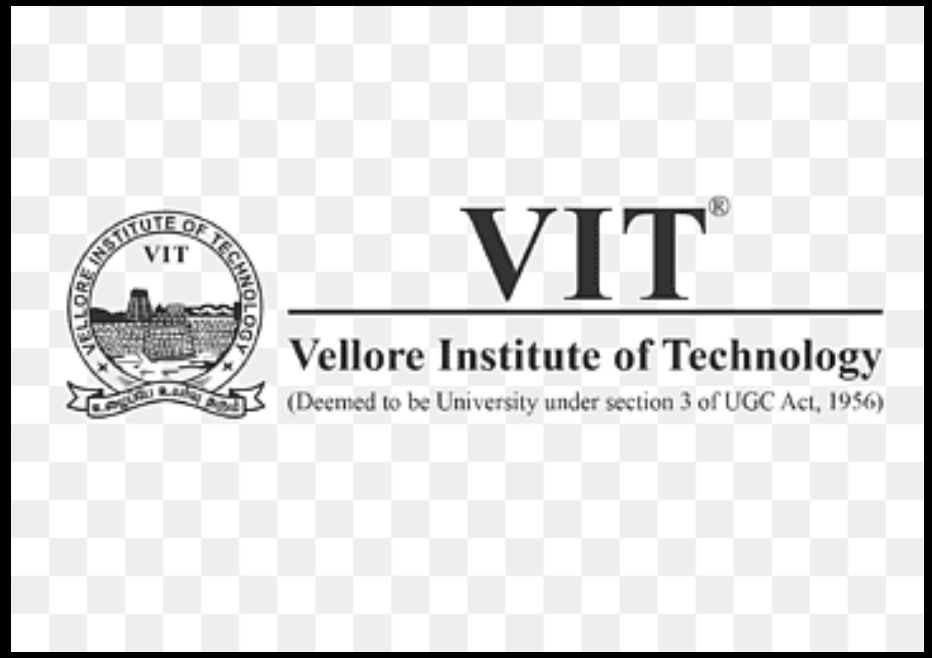
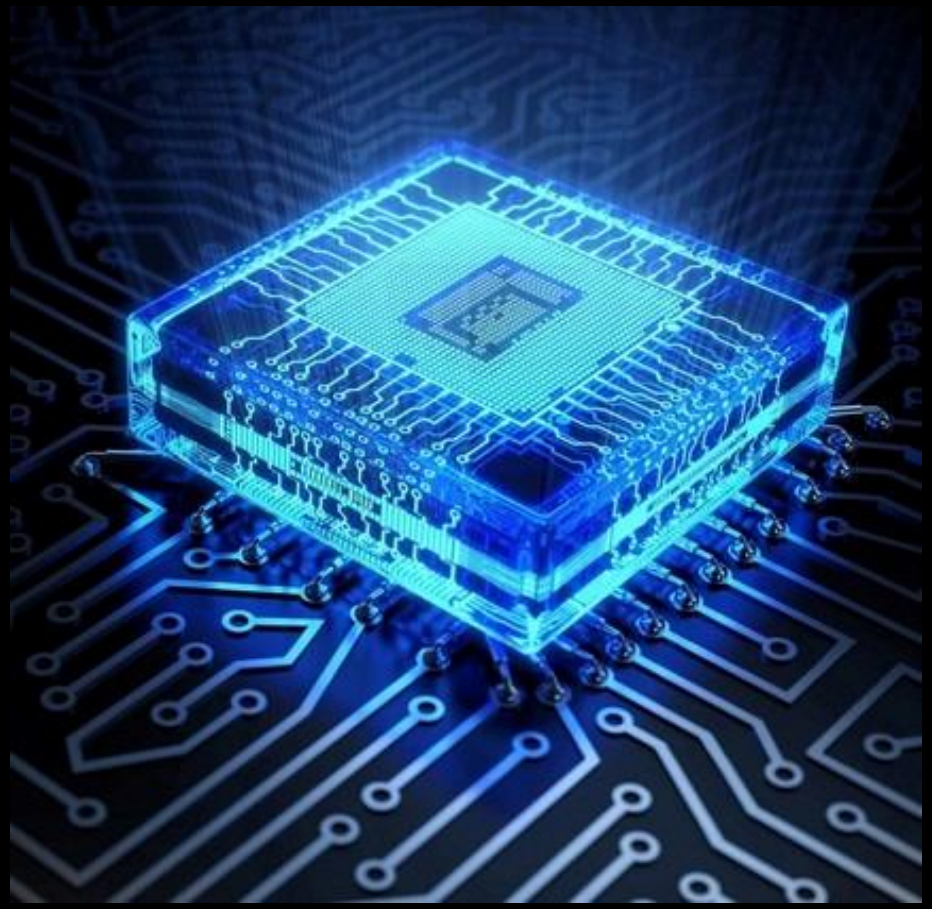
SESSION:2023-24



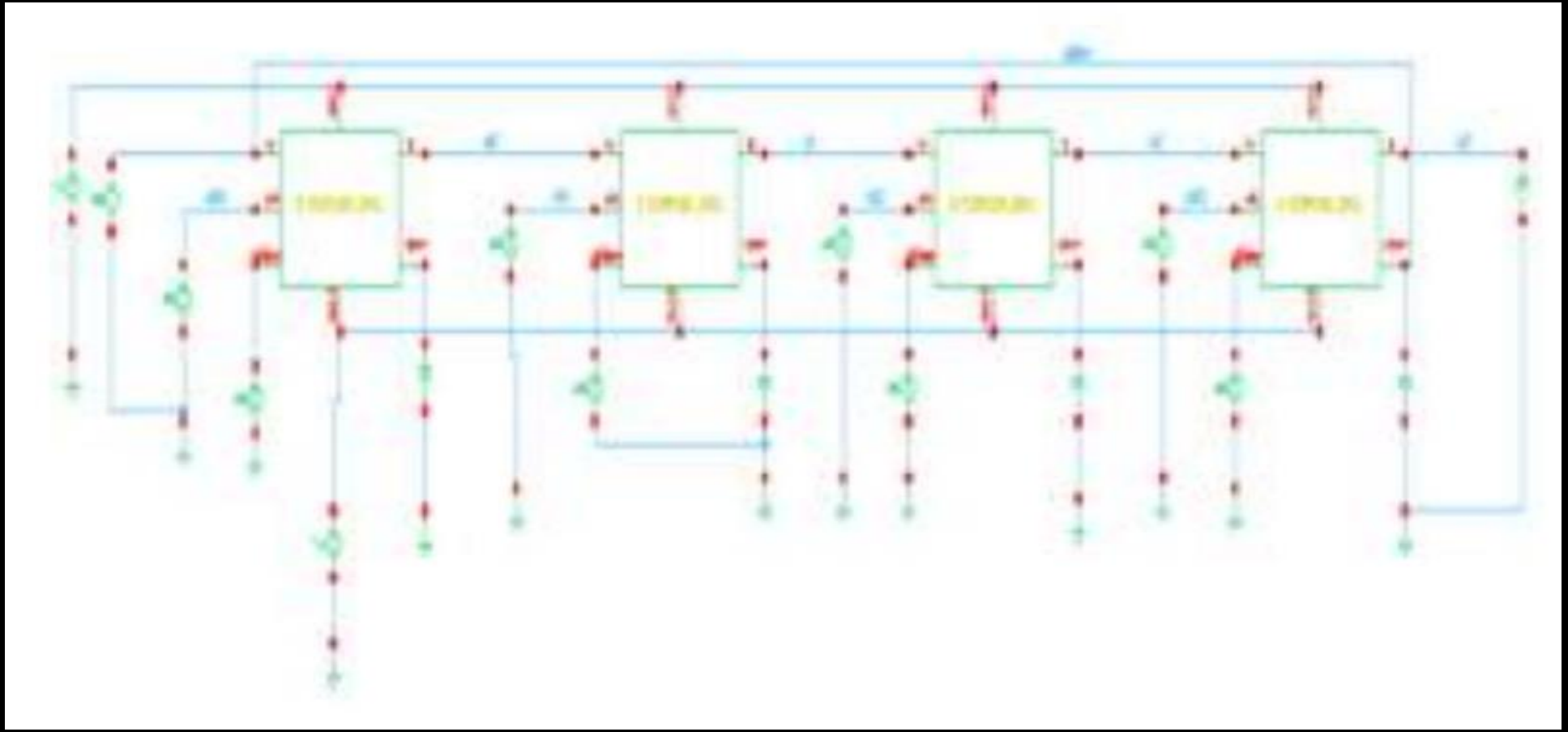
- SUBMITTED BY:
- HITESH SINGH (21BEC2324)
- SAMPREETI ACHARJYA (21BEC2311)
- HARSH RAJ (21BEC0847)
- SAURAV RAJ (21BEC2244)
- SLOT: L23+L24

SUBMITTED TO :
DR. DEBASHISH DASH

CONTENTS

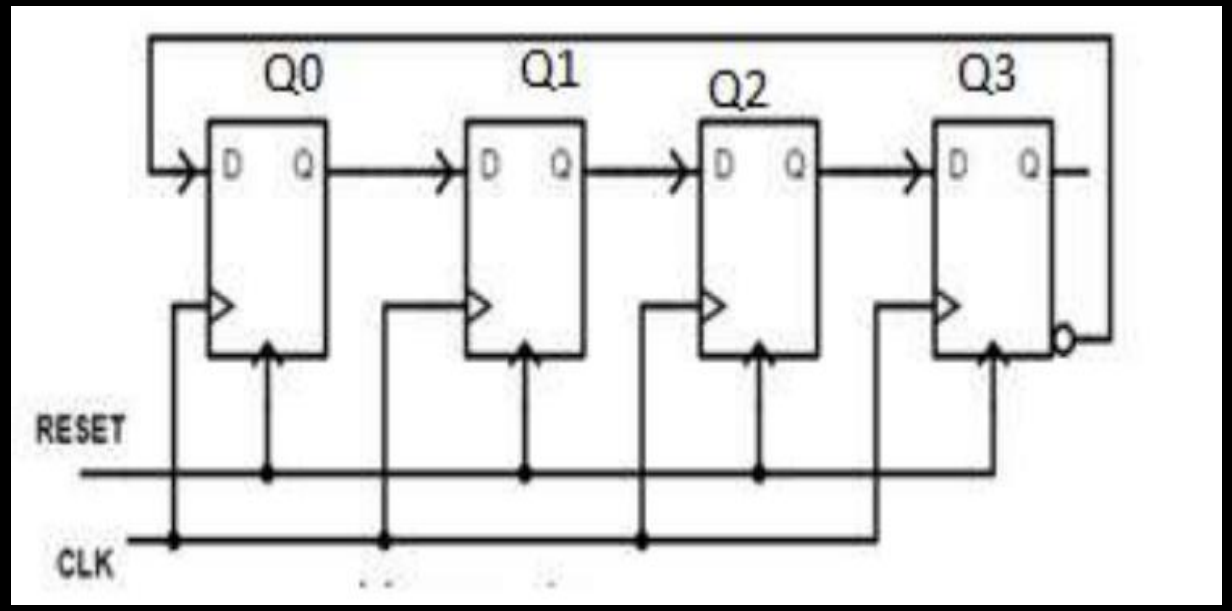


SCHEMATIC DIAGRAM OF JOHNSON COUNTER



ABSTRACT

In the realm of digital circuit design, power efficiency is a crucial aspect to consider, as it directly impacts the overall performance and sustainability of electronic systems. This abstract presents the design of a power-efficient Johnson counter, a widely-used sequential logic circuit, aiming to reduce power consumption while maintaining reliable operation.



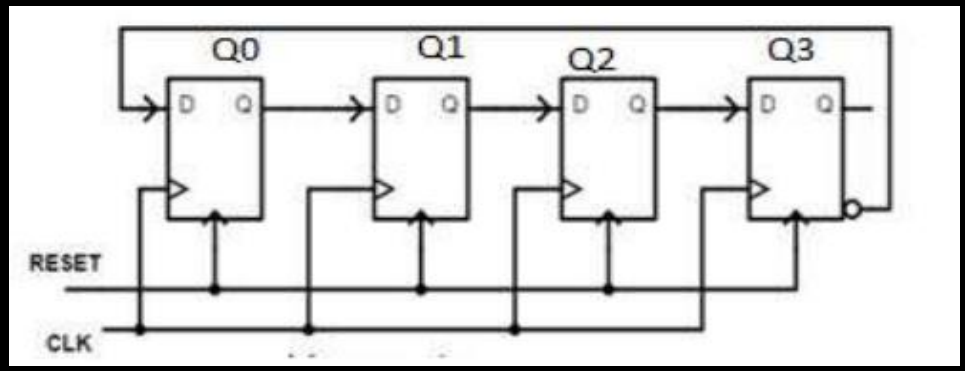
- The Johnson counter is a type of shift register with feedback, capable of generating a sequence of binary states. It finds applications in various domains, including frequency division, clock generation, and pseudo-random number generation.
- A digital system's fundamental building block is the counter. In this study, a 4-bit Johnson counter was implemented utilising BICMOS logic, which combines CMOS and Bipolar transistors.
- Combining the benefits of both logics is the goal of BICMOS logic. The Cadence Virtuoso analogue design environment is utilised for the simulation process, and the Cadence Virtuoso schematic editor is used to implement the proposed circuit.
- The circuit's power consumption at various frequencies was calculated, and the results were contrasted with those from previously carried out research. After doing a comparison, we got to the conclusion that the suggested counter circuit uses less power than other circuits.
- The construction of a Johnson counter with energy-saving features helps.

INTRODUCTION

- The design of power-efficient digital circuits is becoming increasingly important in today's world due to the proliferation of portable devices and the need for energy conservation.
- Counters, which are widely utilised in numerous applications like frequency division, sequencing, and control, are a significant class of digital circuits.
- The Johnson counter stands out among the various counter types for its ease of use and adaptability. A shift register-based counter called a Johnson counter can cycle through a series of binary states. It is made up of several flip-flops connected in a circle, with each flip-flop's output feeding into the one after it.
- The counter can generate a distinct code for each state thanks to the feedback design, which makes it helpful in applications needing cyclic encoding or decoding.For some applications, the Johnson counter offers a versatile option, but it is crucial to design it with power economy in mind.

WORKING ON PROPOSED COUNTER

- Johnson counter circuit is the circuit where the input of the first flip flop has been given the inverted output of the last flip flop.
- To build the Johnson counter, each component must first be independently designed using BICMOS logic, and then the entire counter must be designed utilising all of the individual components. Figure 2 depicts a D flip flop with a master and slave.
- Clock inverters are used in this circuit to hold the output when it's necessary to disable the inputs using either clock or inverted clock.
- To avoid errors, PMOS MP3 has been employed at the device's gate node at the input terminal. Glitches could occur when the clock is high and the input is low.



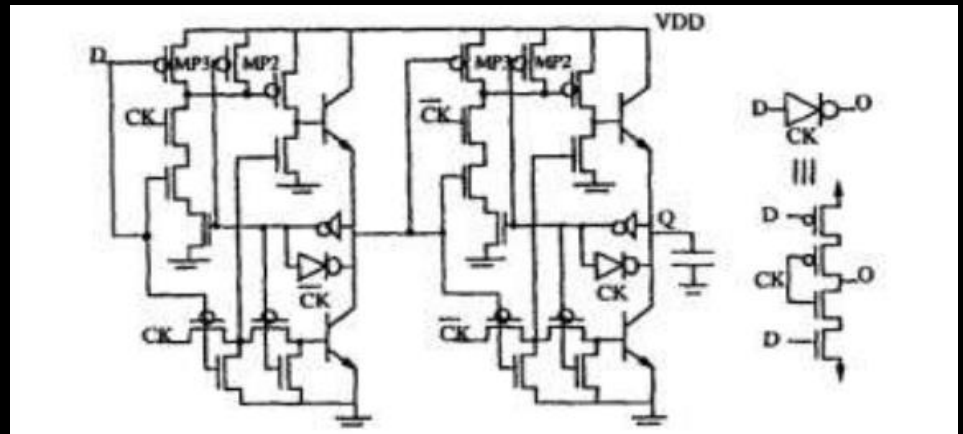


Figure 2: Master- Slave D flip flop implemented with BICMOS logic

SCHEMATIC DESIGN

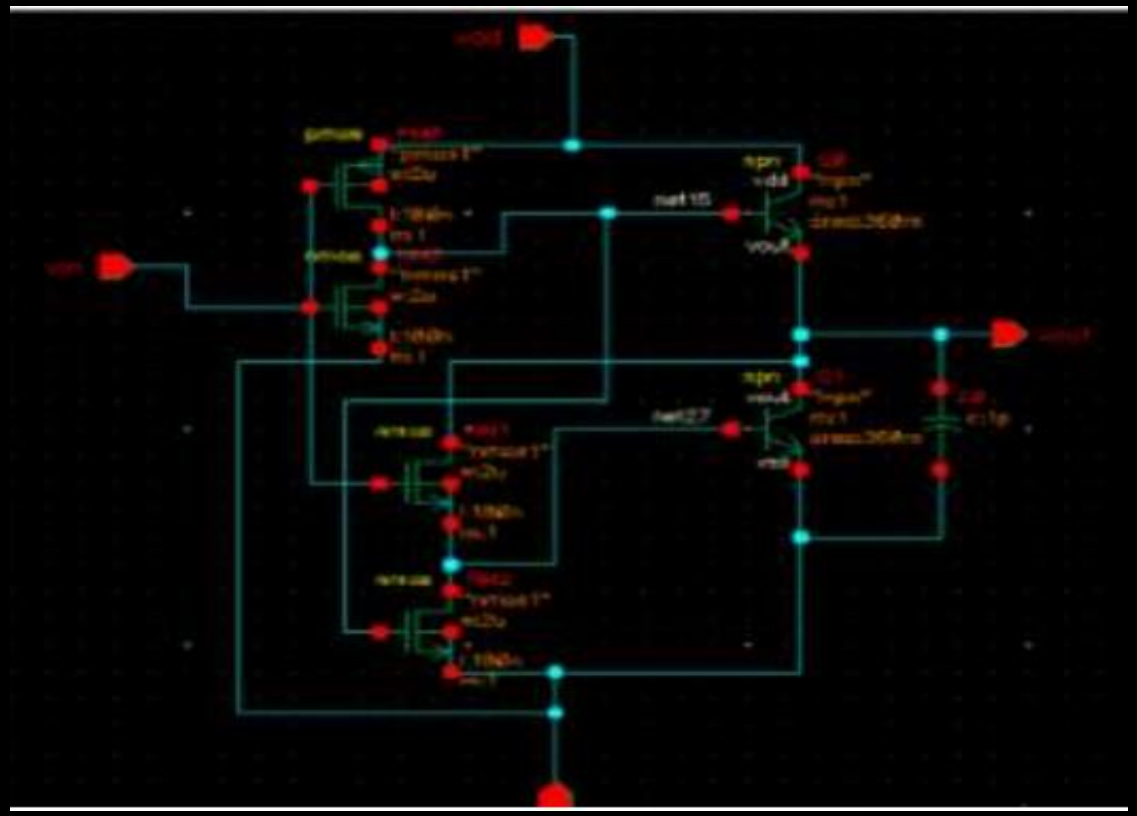


Figure 3: Schematic diagram of Inverter

- Components:
  Flip-flops: Use low-power flip-flops such as CMOS-based D flip-flops or JK flip-flops.
  Gates: Prefer CMOS-based gates with low power consumption, such as NAND or NOR gates.
  Clock source: Use a low-power crystal oscillator or other low-power clock source.

  Schematic Design:
  Find out how many phases or flip-flops are needed for your Johnson counter.

  The Johnson counter configuration is made by constructing a feedback loop by joining the output of the final flip-flop to the input of the first flip-flop.To ensure synchronised operation, serially connect the clock input to each flip-flop.To create the Johnson counter sequence, drive the gates of the following flip-flops in a circular pattern using their Q and Q' outputs.

  Use power-saving strategies like clock gating or clock frequency scaling to cut down on power usage during periods of inactivity.Unless absolutely necessary for the operation of the circuit, utilise power-consuming parts like pull-up or pull-down resistors sparingly.Optimise the circuit's design and route to reduce

- The Cadence Virtuoso schematic editor was used to implement the NOT gate, AND gate, XOR gate, and Johnson counter schematic diagrams. These schematic schematics are all displayed in the figures below.
- The following specifications are used in the design of every circuit: Length L=180 nm, Width W=2 m.
- Figure 3 shows the schematic diagram of an inverter with one PMOS, three NMOS, and two BJTs.
- Figure 4 shows a schematic representation of an AND gate with three PMOS, five NMOS, and two BJTs. Figure 4 shows a schematic of an XOR gate with 6 PMOS, 8 NMOS, and 2 BJTs. Use all these parts together later to put the counter schematic into practise.

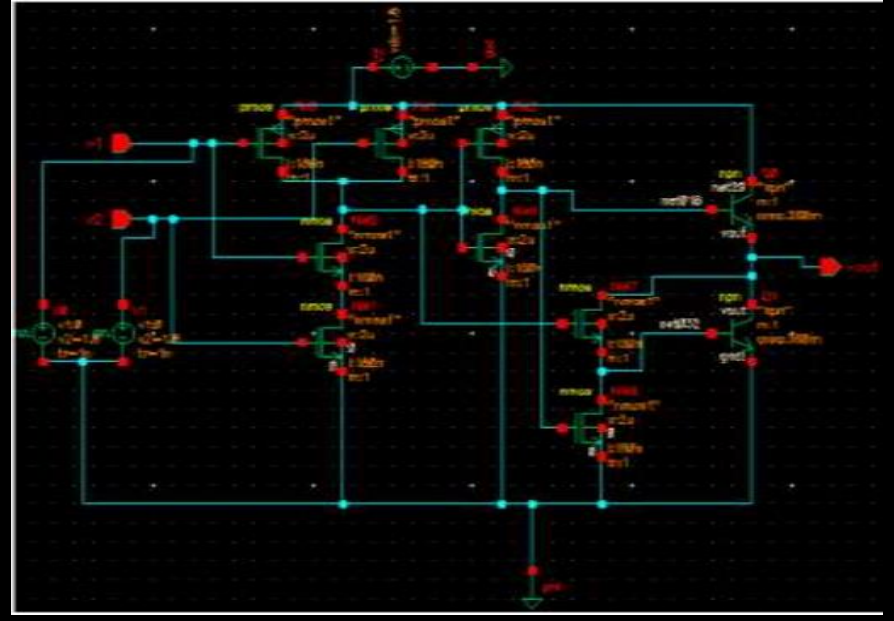


Figure 4: Schematic diagram of AND gate

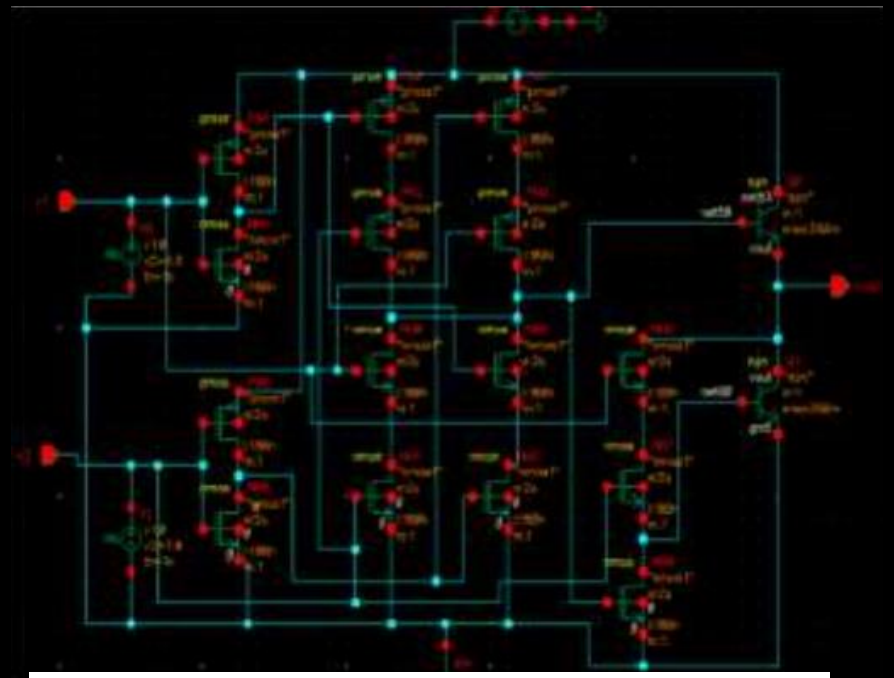


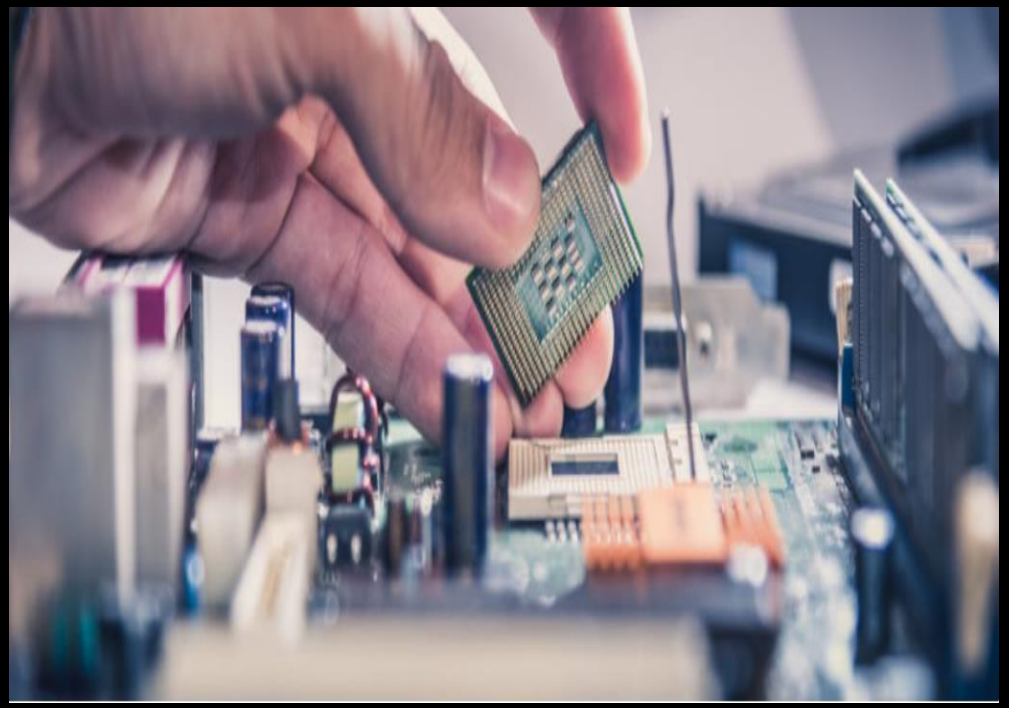
Figure 5: Schematic diagram of XOR gate

CONCLUSION

- The design of a power-efficient Johnson counter is crucial for optimizing power consumption in digital circuits.
- Clock gating: Implementing clock gating techniques allows for selective activation of specific sections of the Johnson counter, reducing unnecessary power consumption when those sections are not in use.
- Power supply voltage optimization: By carefully selecting the power supply voltage, it is possible to find a balance between power consumption and performance.
- Low-power logic design: Utilizing low-power logic families, such as CMOS (Complementary Metal-Oxide-Semiconductor), can help reduce power consumption.
- Minimizing switching activities: Reducing unnecessary transitions and optimizing the sequencing of state changes within the Johnson counter can minimize power consumption.

- Sleep modes: Incorporating sleep or idle modes within the Johnson counter design allows for shutting down unused portions of the circuit when they are not needed. This can lead to significant power savings during idle or low-activity periods.

  Overall, a power-efficient Johnson counter design requires a careful balance between power consumption, performance, and reliability. By implementing clock gating, optimizing power supply voltage, utilizing lowpower logic design, minimizing switching activities, and incorporating sleep modes, it is possible to achieve a design that maximizes power efficiency without compromising functionality.



REFERENCE

S.NO.	ARTICLE NAME	AUTHOR'S NAME	SUMMARY UNDERSTANDING FROM PAPER
1	FPGA Implementation of Johnson Counters Applied in the Educational Process	Iordan Ivanov Stoev	The synthesis and analysis of Johnson counters
2	Optimized design and performance analysis of Johnson counter using 45 nm technology	Manish Kumar Soni	In this paper a low power, high speed and cost efficient 4-it Johnson counter is proposed.
3	Low power adiabatic 4-Bit Johnson counter based on power-gating CPAL logic	Garima Bhargave	In this paper, a different power saving adiabatic 4-bit Johnson counter based on two-phase CPAL circuits with power gating method is proposed.
4	**Design of a low power Adiabatic Logic based Johnson Counter**	**Himanshi Sharma**	**The paper provides a deep insight to the design of an adiabatic Johnson Counter which consumes low power and delivers high performance**

5	**Performance Optimization of Johnson Counter Using SSASPL**	**Satish Mohanrao Turkane**	**Paper proposes Johnson counter utilizing pulse latches to build execution parameter of past counter.**
6	SEU hardened DFF and 4 bit johnson counter using quatro latch in 45 nm technology	Pankaj Katkar	In this paper, we have proposed soft-error tolerant flip flop design.
7	Low power testing using re-configurable Johnson counter and scalable SIC counter	Pallavi Margade	This paper deals with a low power approach to generate test pattern for Built In Self Test.
8	Design of a low power 10-bit cyclic D/A converter with a Johnson counter and a capacitor swapping technique	Hyosang Kim	A cyclic 10-bit D/A converter based on a Johnson counter and a capacitor swapping technique is described.
9	PLA based finite state machines using Johnson counters as state memories	R. Amann	The goal is to minimize the number of product terms in the PLAs and thus the overall area of the FSMs.
10	**Johnson Counter-Based Multiphase Generation for VCO-Based ADC for Direct Digitization of Low Amplitude Sensor Signals**	**Shruti Konwarand**	**This article proposes a Johnson counter (JC) based multiphase generation for VCO-based ADC for direct digitization of low amplitude sensor signals.**