Embedded System Lab: Session Second - VHDL

LAB-5: Sequential Logic Design Using VHDL

Objectives

To enable us to write VHDL code for a Field Programmable Gate Array (FPGA) capable of:

- Implementing sequential circuits
- Implementing test benches to verify the working of sequential circuits

Equipment Required

Hardware:

- Spartan-3E or Spartan-3AN FPGA starter kit
- Power cable and Data cable

Software:

- Xilinx ISE (Integrated Synthesis Environment) Design Suite
- iMPACT configuration tool

Background

Combinational circuit are those circuits that do not use any memory. Hence the previous state of input does not have any effect on the present state of the circuit. But sequential circuit has memory so the present output depends on both on present input and past output. A sequential circuit is described in terms of logic conditions called logic states. Sequential circuits include memory elements that store the values of the logic states. The general structure of a sequential circuit is shown in following figure.

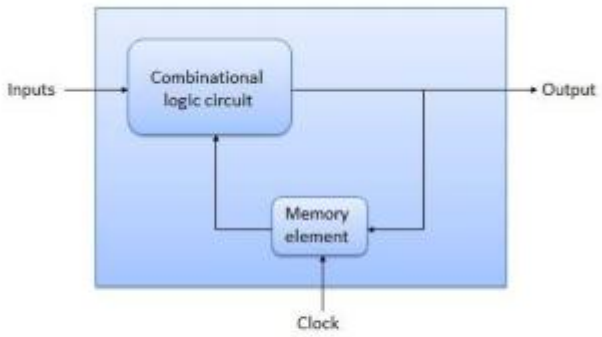
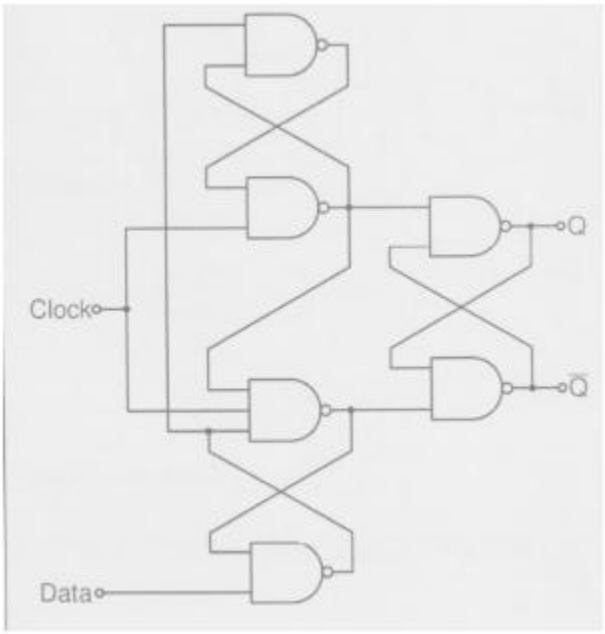
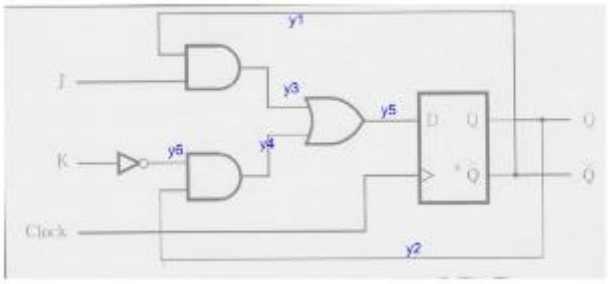


Figure 1: Block diagram of Sequential circuit

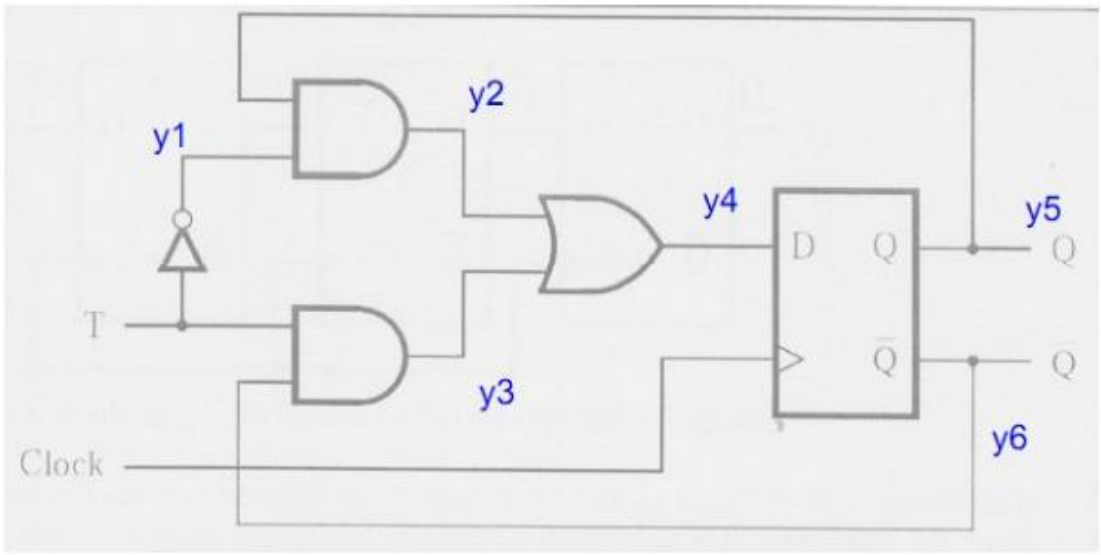
Lab Exercises:

1. Write a VHDL code to implement a JK flip-flop using a D flip-flop and the characteristic equation given in equation 1. The D flip-flop needs to be implemented using a structural architecture style using the circuit shown in figure below. The JK ip-op must be constructed using a component declaration for a D flip-flop. Write a VHDL test bench to verify the operation of the JK ip-op and provide waveforms.

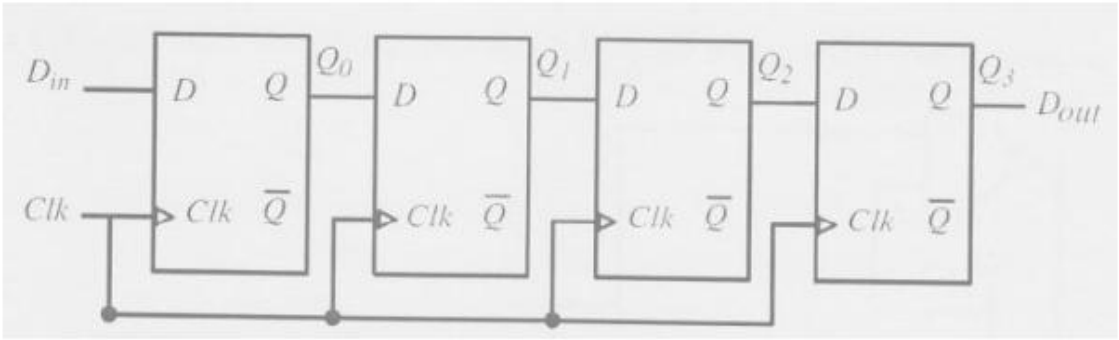




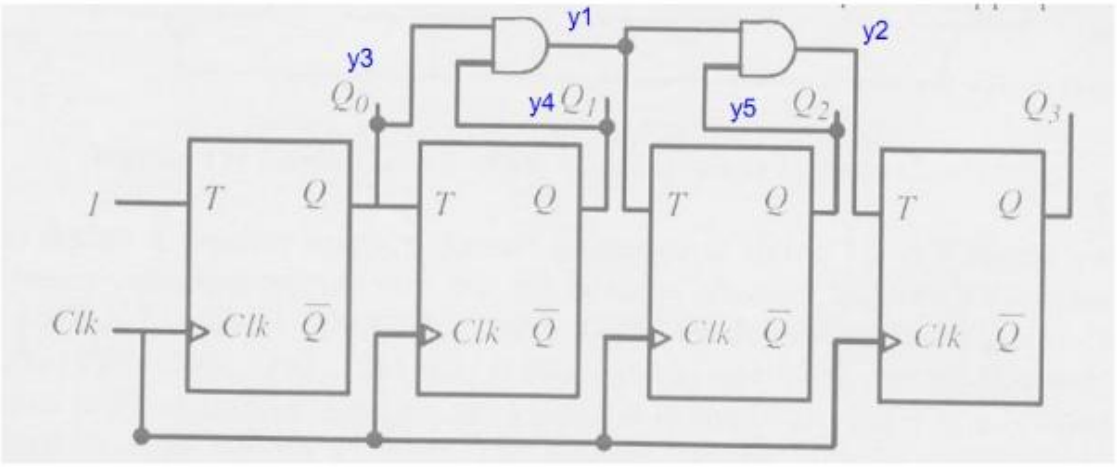
2. Write a VHDL code to implement a T flip-flop using a D flip-flop and the characteristic equation. The D flip-flop needs to be implemented using a structural architecture style using the circuit shown in below figure. The T flip-flop must be constructed using a component declaration for a D flip-flop. Write a VHDL test bench to verify the operation of the T flip-flop and provide waveforms.



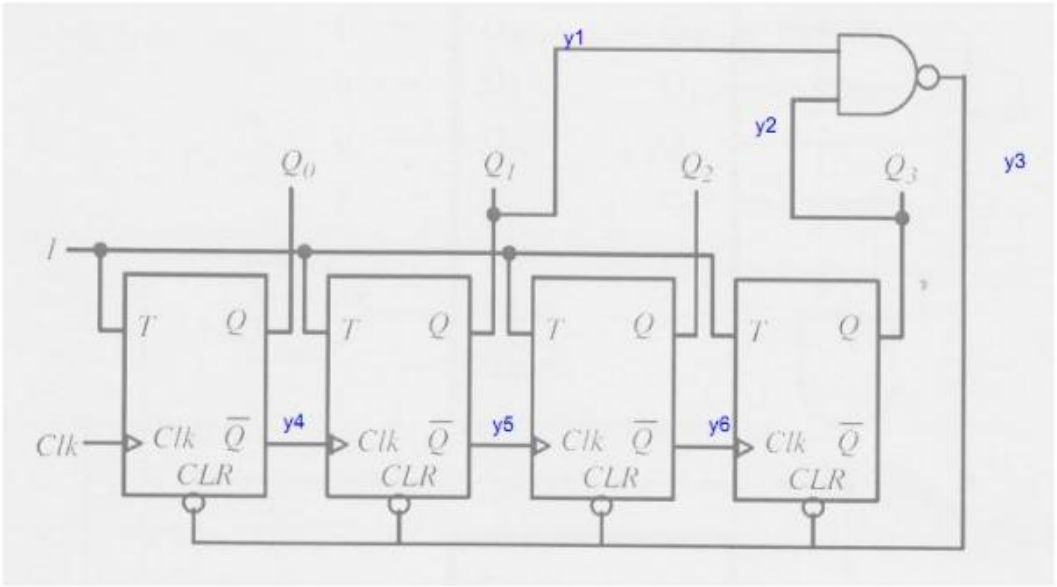
3. Use VHDL to implement a 4-bit serial-in-serial-out (SISO) right-shift register as shown in figure below. Determine the output of the shift register after the input sequence 01010101 has been shifted eight times, starting with the MSB. Assume that the output of the shift register is reset initially to 0000. The shift register must be constructed with D flip-flops using a component declaration for a D flip-flop. Write a VHDL test bench to verify the operation of the 4-bit SISO and provide appropriate waveforms.



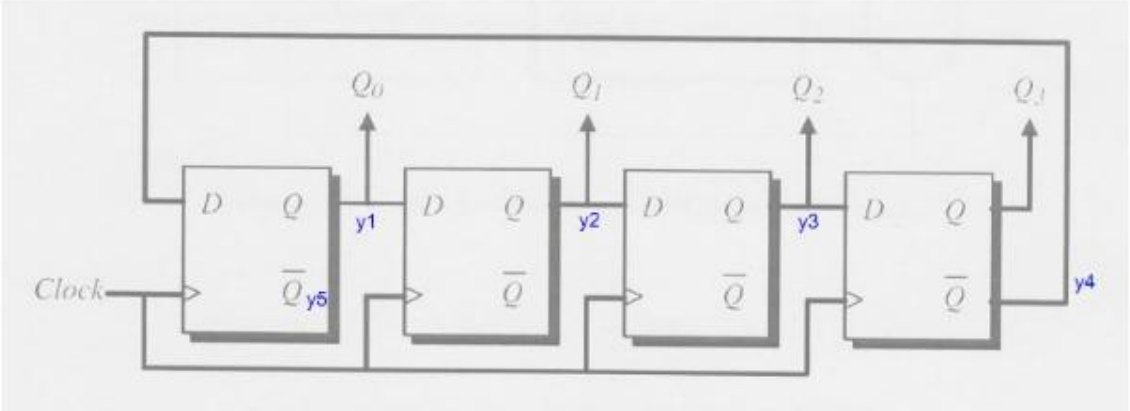
4. Write a VHDL code to implement a 4-bit synchronous up-counter as shown in below figure. In a synchronous counter all flip-flops receive a common clock signal and change their states at the same time. The shift-register must be constructed with T flip-flops using a component declaration for a T flip-flop. Write a VHDL test bench to verify the operation of the 4-bit SISO and provide the appropriate waveforms.



5. Use VHDL to design an asynchronous decade counter as shown in below figure. The 10 states of a decade counter represent the BCD numbers from 0 to 9. Write the VHDL test bench to verify the operation of the decade counter and provide waveforms.



6. Use VHDL to design a four-bit Johnson counter as shown in below figure. The Johnson counter must be constructed using component declarations from the D flip-flops. Write a VHDL test bench to verify the operation of the Johnson counter and provide waveforms.



7. Use VHDL to create a 2-bit BCD counter as shown in below figure. The BCD counter consists of two 1-bit BCD counters cascaded to form a 2-bit BCD counter. The 2-bit BCD counter counts from 00 to 99. The 2-bit BCD counter must be constructed using component declarations for the D flip-flops.