Tobias Sautter BSYS HW5 **28.04.2023**

Question 1

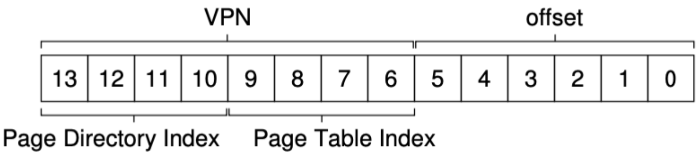
With a linear page table, you need a single register to locate the page table, assuming that hardware does the lookup upon a TLB miss.
How many registers do you need to locate a two-level page table?
A three-level table?

We still need only 1 register, since we only need to find the first address of the outer most page directory. From there on we can calculate every address.

Question 2

Use the simulator to perform translations given random seeds 0, 1, and 2, and check your answers using the -c flag. How many memory references are needed to perform each lookup?

```
Page size: 32
Virtual address space: 32KB (1024 pages)
Physical memory: 128 pages
Pde bits
log2(32) = 5 (offset bits)
log2(1024) = 10 (VPN bits)
log2(128) = 7 (PFN bits)
Virtual address size: 15 bits
Physical address size: 12 bits
```



```
python3 paging-multilevel-translate.py -s 0

PDBR: 108  (decimal) [This means the page directory is held in this page]
Page 108:
```

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
83	fe	e0	da	7f	d4	7f	eb	be	9e	d5	ad	e4	ac	90	d6	92	d8	c1	f8	9f	e1	ed	e9	a1	e8	c7	c2	a9	d1	db	Ff

```
0x611c = 110000100011100
    =>   11000 = 24 => a1 (in the PDBR(Page 108) at location 24)
    =>   a1 = 10100001 => valid, 33
    =>   01000 = 8
    =>   Look in page 33 at position 8
```

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
7f	7f	7f	7f	7f	7f	7f	7f	b5	7f	9d	7f	7f	7f	7f	7f	7f	7f	7f	7f	7f	7f	7f	7f	7f	7f	F6	b1	7f	7f	7f	7f

```
    =>   b5 = 10110101 => valid, 53
    =>   11100 = 28
    =>   Look in page 53 at position 28
```

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0f	0c	18	09	0e	12	1c	0f	08	17	13	07	1c	1e	19	1b	09	16	1b	16	0e	03	0d	12	1c	1d	0e	1a	08	18	11	00

```
    => Value is 08
```

Each entirely valid lookup needs 3 memory references.
Invalid lookups need at least 1 memory references and may have 2

Question 3

Given your understanding of how cache memory works,
how do you think memory references to the page table will behave in the cache?
Will they lead to lots of cache hits (and thus fast accesses?) Or lots of misses (and thus slow accesses)?