



# Multicore Computing

Assignment Three (Theory)

Department of Computer Engineering

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# 1 Question One



## 2 Question One



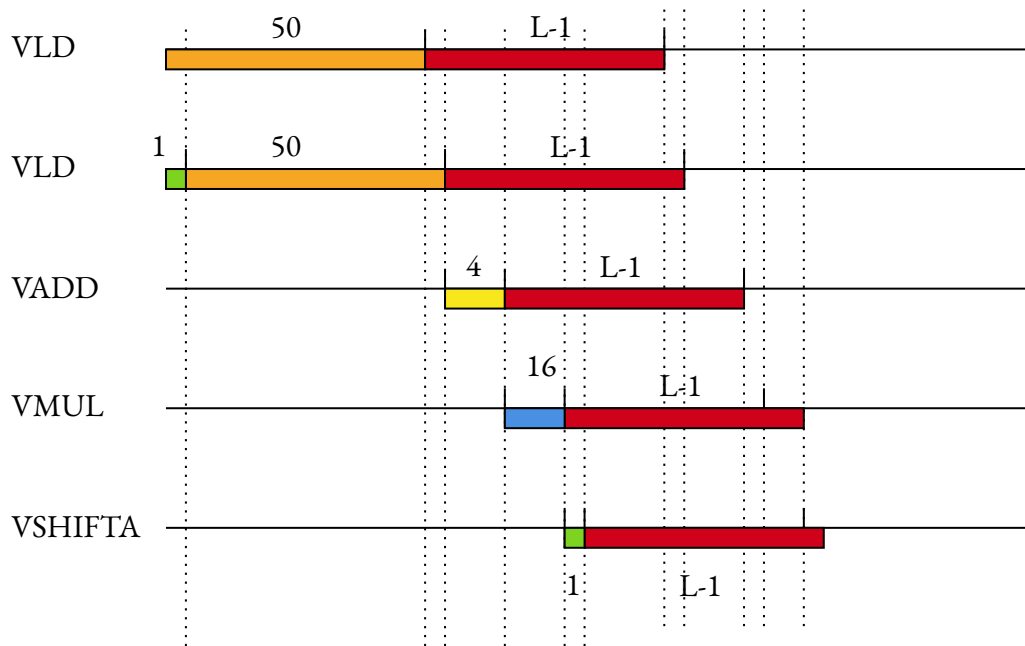
### 3 Question Three



#### 4 Question Four

- a. 64. Memory Latency is 50. The Nearest power-of-two is 64.
- b. According to the picture below:

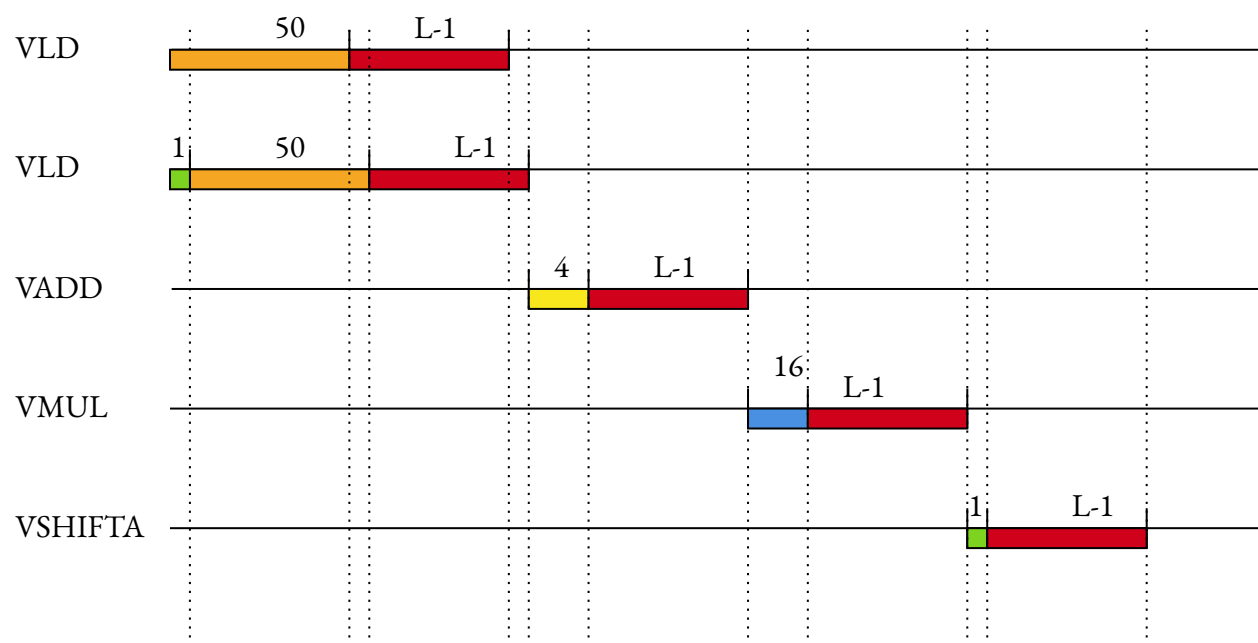
$$1 + 50 + 4 + 16 + 1 + L - 1 = 111 \text{ cycles} \Rightarrow L = 40 \text{ cycles}$$





According to the picture below:

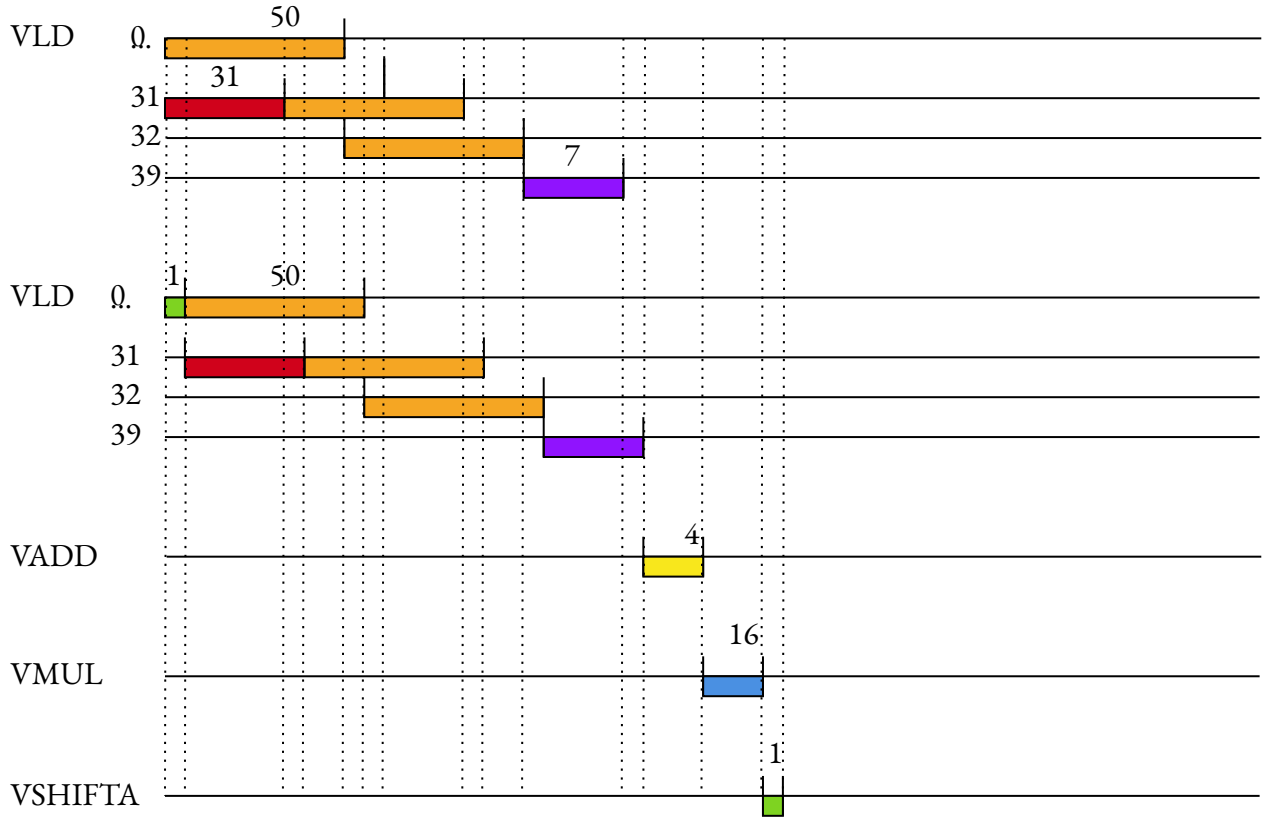
$$1 + 50 + L - 1 + 4 + L - 1 + 16 + L - 1 + 1 + L - 1 = 228 \text{ cycles}$$





- c. In this case there will actually be two stages of load. The bank size will be 32 and we want to get values till 40. Therefore based on the picture below, the answer will be:

$$1 + 50 + 50 + 7 + 4 + 16 + 1 = 129 \text{ cycles}$$



By the pattern found until now, we can say:

$$x \times 50 + 1 + 7 + 4 + 16 + 1 = 279 \Rightarrow x = 5$$

The following power of two to 5 is 8. So the answer is 8 banks.

- d. Row-Buffer Conflict causes it. It means the interleaving of vector accesses of cores on the shared memory. For example, core 0 wants to access a vector that is mapped to bank 0, and at the same time, independent of core 0, core 0 also wants to access another vector that is mapped to bank 0. As the memory is shared, this will cause a Row-Buffer conflict.

To solve the problem, the architect could partition the memory mapping or use advanced memory scheduling techniques that reorder memory access to minimize conflicts.

Partitioning the memory mapping can be done in many ways. One of them is to assign colors to each partition and only allow access to the partition for processes (threads) that are associated with that specific color [1].



## References

- [1] Christina Åhrén and Ida Nyblad. Investigating dram bank partitioning.