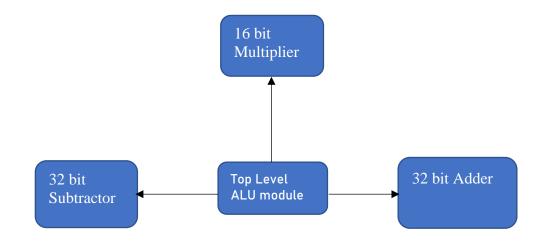
## FPGA realization of ALU for mobile GPU

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We have designed a small ALU, for a hand held device like a mobile. This algorithm would give quick results due to parallel computations, but we get lesser accuracy. For multiplication we consider only the first 8 bits after the decimal point and rest of the bits are ignored and hence, we get lesser accuracy. This device also supports 32-bit addition and subtraction.

On further development we can also extend this device to division operation. But as division is not a very important operation in an ALU it hasn't been included in this version.

Now coming to the files/ modules used



## **Output obtained:** The inputs and outputs are in Hexadecimal.

0-multiplication 1-Addition 2-subtraction 3-High Impedance a=X00060000 b=X00020000 result=X0000000c; the operation is 0 a=X00060000 b=X00020000 result=X00080000 ; the operation is 1 5 a=X00060000 b=X00020000 result=X00040000 ;the operation is 2 10 15 a=X00020000 b=X00060000 result=X00006666; the operation is 0 20 a=X00020000 b=X00060000 result=X00080000; the operation is 1 25 a=X00020000 b=X00060000 result=Xfffc0000; the operation is 2 30 a=X00040000 b=X00030000 result=X0000000c; the operation is 0 35 a=X00040000 b=X00030000 result=X00070000 ;the operation is 1 40 a=X00040000 b=X00030000 result=X00010000; the operation is 2 45 a=X00180000 b=X00020000 result=X00000030 ;the operation is 0 50 a=X00180000 b=X00020000 result=X001a0000; the operation is 1 55 a=X00180000 b=X00020000 result=X00160000; the operation is 2 60 a=X00170000 b=X00040000 result=X0000005c; the operation is 0

- a=X00170000 b=X00040000 result=X001b0000 ;the operation is 1
- 70 a=X00170000 b=X00040000 result=X00130000 ;the operation is 2
- 75 a=X00170000 b=X00040000 result=Xzzzzzzzz ;the operation is 3