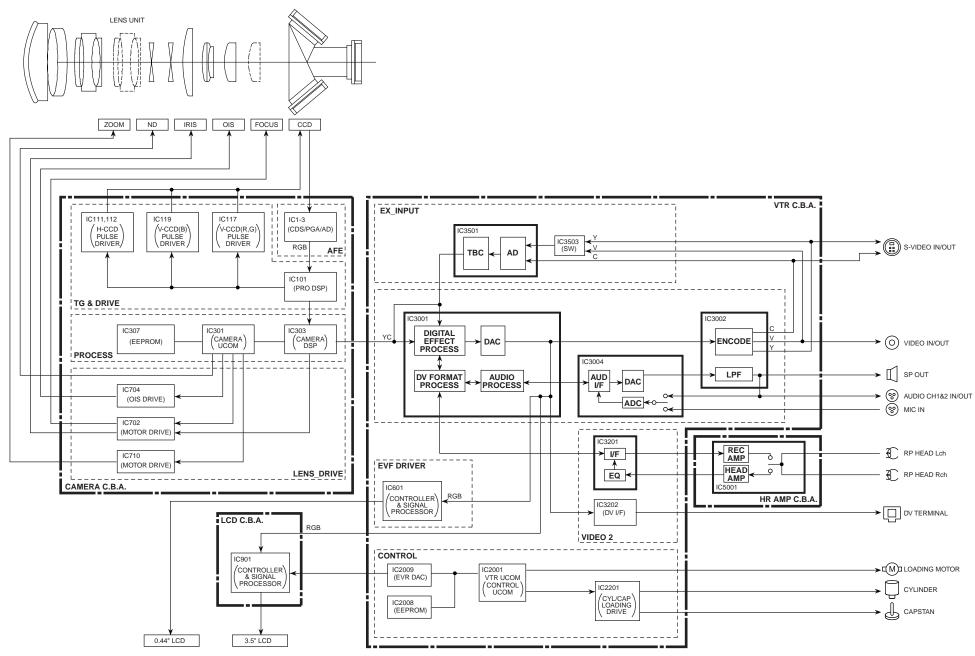
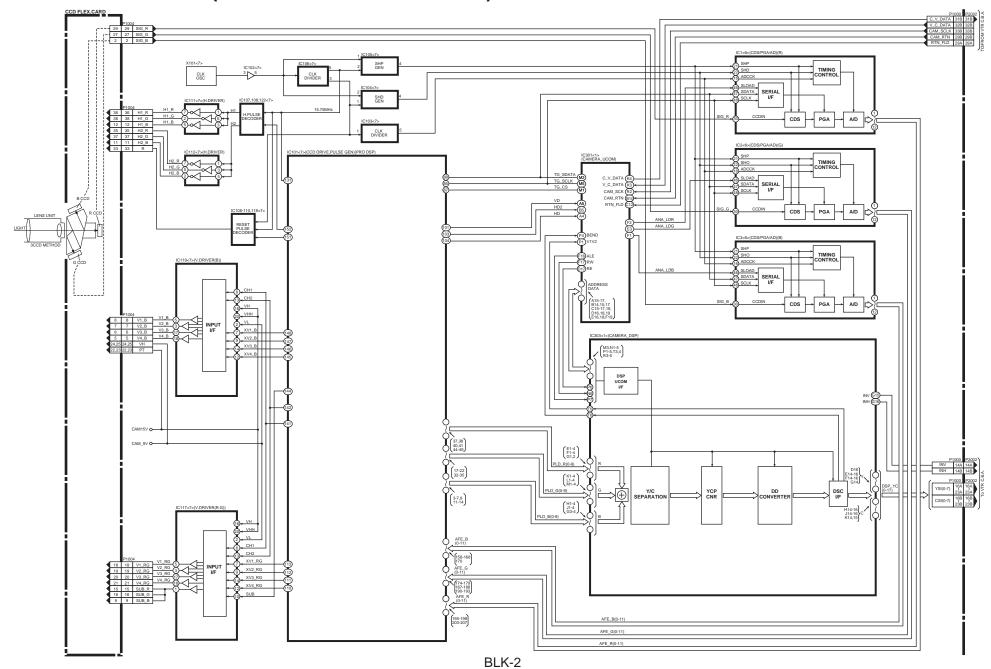
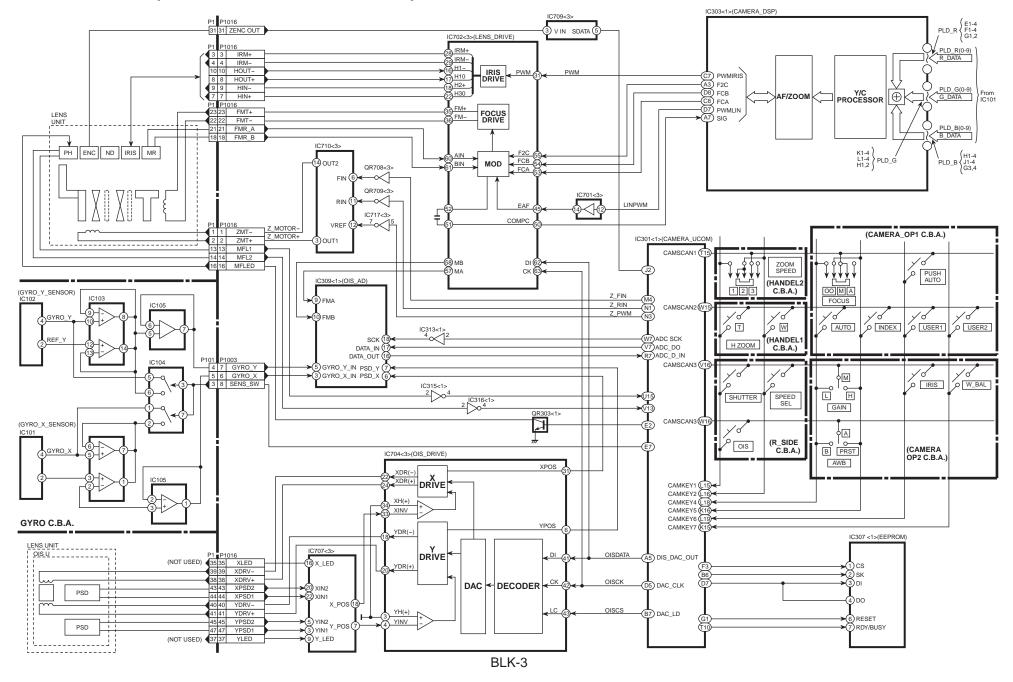
OVERALL BLOCK DIAGRAM



SENSOR/PROCESS(AFE/TG&DRIVE/PROCESS) BLOCK DIAGRAM

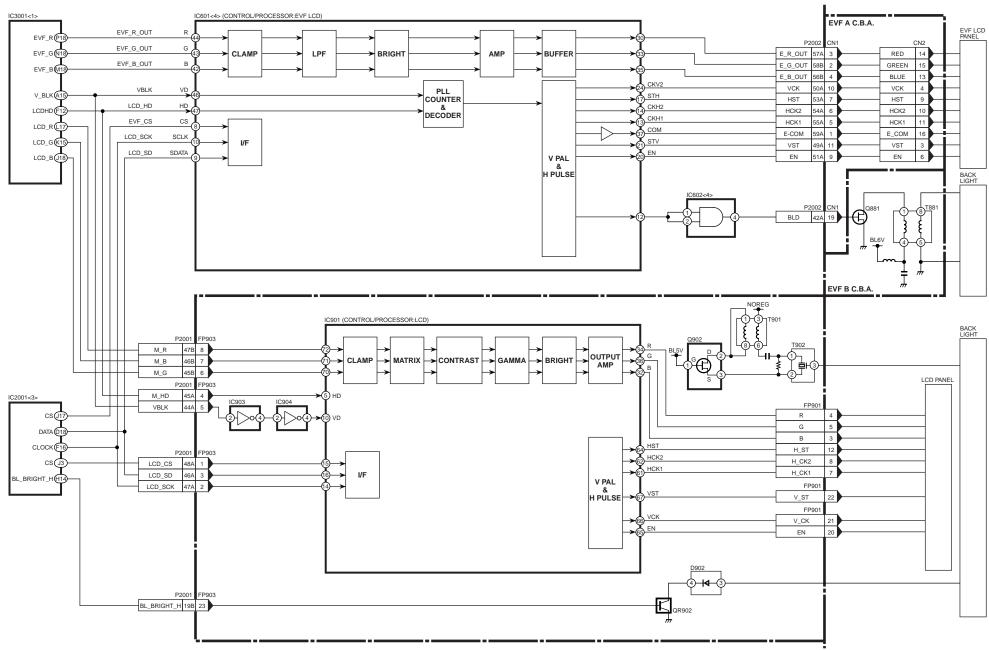


LENS DRIVE (LENS DRIVE / PROCESS) BLOCK DIAGRAM



VIDEO (VIDEO 1/ VIDEO 2/ EX_INPUT) BLOCK DIAGRAM MAIN SIGNAL PATH IN REC MODE MAIN SIGNAL PATH IN PLAYBACK MODE <3>from IC2001-A15 SIF_SCK <3>from IC2001-V14 __ <3>from IC2001-T12 SIF_SDA IC3504<5> IC3501<5> (INPUT) <3>from IC2001-T13 SIF_CS IC3001<1> V_IO A7,8 B7,C7 D7,E9 F8,9 P12,13 R14,T14 U15,16 V15,16 E12,13 F14,G13-15 H14,15 P2002 P2002 P2002 P1000 P2002 P1000 P2002 P1000 P2002 P1000 P2002 P1000 U COM SDA SCK Y DATA 1 (0-7) C DATA 1 (0-7) YSI(0-7) DIGITAL EFFECT PROCESS CLK CHANGE CSI(0-7) C N11,P11 R13,T13 U13,14 V13,14 A9,B8,10 C8,9 D8,9 IC3002<1> (AV DRIVE) TBC FP2008 P4401 TO C_OUT 13 13 S_VHS TERMINAL C OUT, ATT BUFF CLAMP **1** 1 J4401 (SIDE_JACK C.B.A.) Y_OUT 11 11 AGC MIX V OUT AD CLAMP AD CIN CLK27B (U6) → N6 CLK27M → A10 CLK135M Y/C SEP Y OUT CLK135 (V8) 35 - ATT - BUFF - CLAMP P4608 (R_SIDE C.B.A.) DV FORMAT DAC S VIDEO (SP OUT1 58B 62 SP OUT 2 LINE_L LINE_R IC3004<1> (AUDIO AD/DA) TO LINE IN/OUT V I/O 15 15 LINE_L A CH1 IO 17 J4451 (SIDE_JACK C.B.A.) 0-LINE_R AMP-0 A CH2 IO 19 1: **→** AMP - **○**-MIC_L)≺ AMP - ○ AMP-0-CH1_MIC_OUT 5 3 — from MIC_CH1 C.B.A. MIC_R (6) CH2_MIC_OUT 7 3 — from MIC_CH2 C.B.A. P4001 DAC BCLK →23 → AUDIO SDTO I/F AUDIO ADC 25. SBA_DI from IC2001-P12<3: SDTI PROCESS IC3201<2> (RI0) IC5001<1> (HEAD/REC-AMP) P5001 CH2F RP Rch CH2S DBR(0-3) FP5001 AGC ENCODER CH1S **←** ⇒ I/F RP Lch CH1F AGC DET FP500 VITABI EQ RF AMP -o-RF_AGCOUT 9 9 AGC F10-12,G11,12,H11,12 J10-12,K12,L11,12,M10-12 FP5001 ►A10 CLK27A LOGIC HID1 D1-3,E2,4 F1,3,4 G3,5 H1,2,6,J6 HR_AMP C.B.A IC3202<2> (PLANET) ADM(0-15) TO/FROM A4 CLK27A D7,10,E8-10 F6,F8-10 G8,9,H8-10 J9,K10 **J**3 XI DATA/ADDRESS TPB-TPB-TO DV TERMINAL TPB+ DV I/F TPB+ 7 7 TPA-J4401 (SIDE JACK C.B.A.) TPA-TPA+ TPA+ BLK-4

MONITOR (EVF DRIVER / LCD) BLOCK DIAGRAM



CONTROL (CONTROL/DRIVE) BLOCK DIAGRAM

