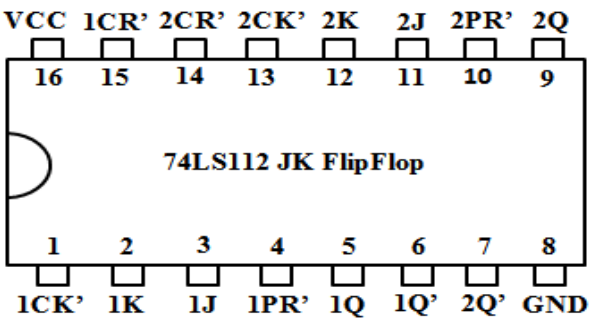
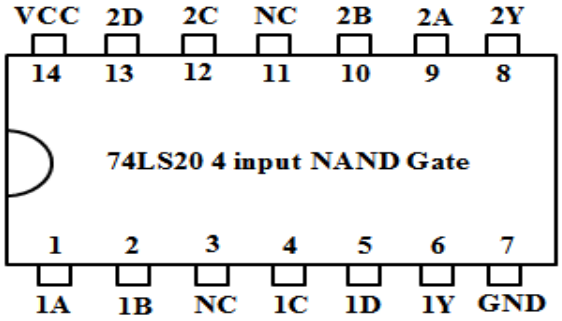
Digital Electronic Circuits
Even or Odd Counter

Experiment 10 Monsoon 2018

In this experiment we implement a simple digital counter circuit that count clock pulses from 00 to 99 in Even numbers or Odd numbers rather counting in cardinals. The circuit consist of 74LS112 Dual Negative edge trigger JK Flip Flop, 74LS20 Dual 4 input NAND gate. The counting sequence is displayed on the 2 digit Seven Segment Display (SUNR056) with the help of two 74LS47 BCD to 7 Segment Decoder ICs to drive each digit in Seven Segment Display. The pin connection for 74LS112 and 74LS20 is shown below.





The counter circuit has MOD 5 Section and MOD 10 Section.

MOD 5 SECTION:

The MOD 5 section consist of three JK Flip Flops F3, F2, F1 and one 4 input NAND gate G1. The MOD 5 section output Q3, Q2, Q1, Q0 is connected to D, B, C, A inputs of 74LS47 BCD to 7 Segment Decoder respectively, which drive Least Significant Digit in Seven Segment Display. The Even BCD number and Odd BCD numbers is shown below.

Even BCD Numbers						Odd BCD Numbers					
Q3	Q2	Q1	Q0			Q3	Q2	Q1	Q0		
0	0	0	0	----	0	0	0	0	1	----	1
0	0	1	0	----	2	0	0	1	1	----	3
0	1	0	0	----	4	0	1	0	1	----	5
0	1	1	0	----	6	0	1	1	1	----	7
1	0	0	0	----	8	1	0	0	1	----	9

In the above list, if Q0 bit is fixed to logic 0 then Q3, Q2, Q1, Q0 BCD number will be Even number, in contrast if Q0 bit is fixed to logic 1 then Q3, Q2, Q1, Q0 BCD number will be Odd number. The remaining Q3, Q2, Q1 bits are similar in BCD Even and Odd numbers. So we connect Q0 bit to input toggle switch for selecting Even or odd counting and we design a MOD 5 counter using JK Flip Flops F3, F2, F1 and NAND Gate G1 in asynchronous mode as shown in Fig 1. F1 flip flop receives the clock pulses to be count.

MOD 10 SECTION:

The MOD 10 section consist of four JK Flip Flops F7, F6, F5, F4 and one 4 input NAND gate G2. This MOD 10 section output Q7, Q6, Q5, and Q4 is connected to D, C, B, A inputs of 74LS47 BCD to 7 segment Decoder respectively, which drive Most Significant Digit in Seven Segment Display. The Clock input to this MOD 10 section is connected to output of G1 NAND Gate, hence MOD 10 section change state when MOD 5 section complete one iteration. The flip flop connection for this MOD 10 section is as shown in Fig 1. The 2 digit seven segment display will show the numbers 00, 02, 04, 06, 08, 10, 12, 14, 16, 18, 20, 22, 24…96, 98, 00, 02, so on, for every clock pulse when input toggle switch is fixed to logic 0. On the other hand If the input toggle switch is fixed to logic 1, the 2 digit seven segment displays will show the numbers 01, 03, 05, 07, 09, 11, 13, 15, 17, 19, 21, 23, 25,…97, 99, 01, 03, so on, for each input clock pulse.

Note: The J, K and Preset input pins of all the flip flops must be fixed to logic 1 or VCC.

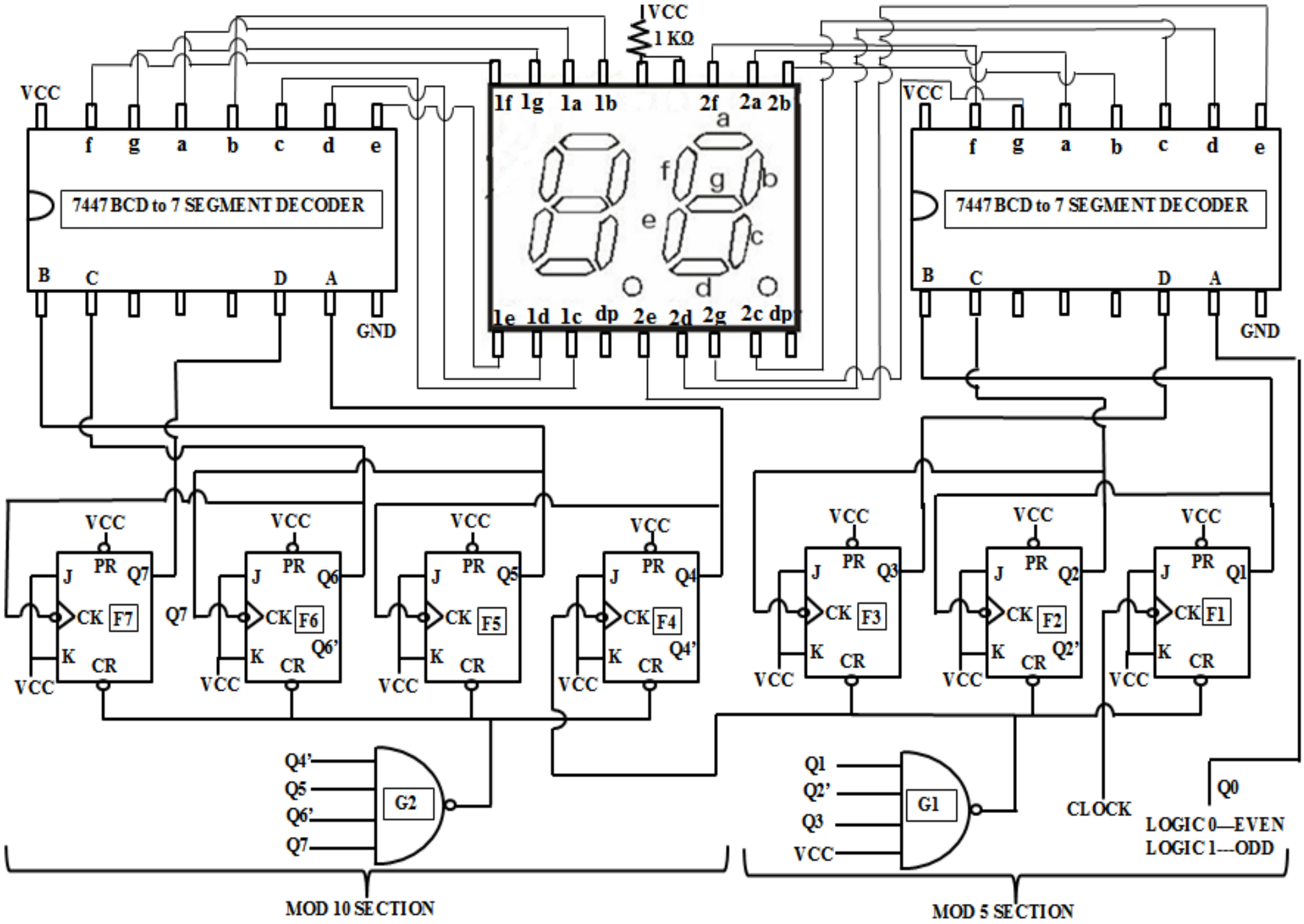


Fig. 1: DIGITAL CIRCUIT FOR EVEN/ODD COUNTER