DLD Assignment 2

Due Date: Will be announced in class

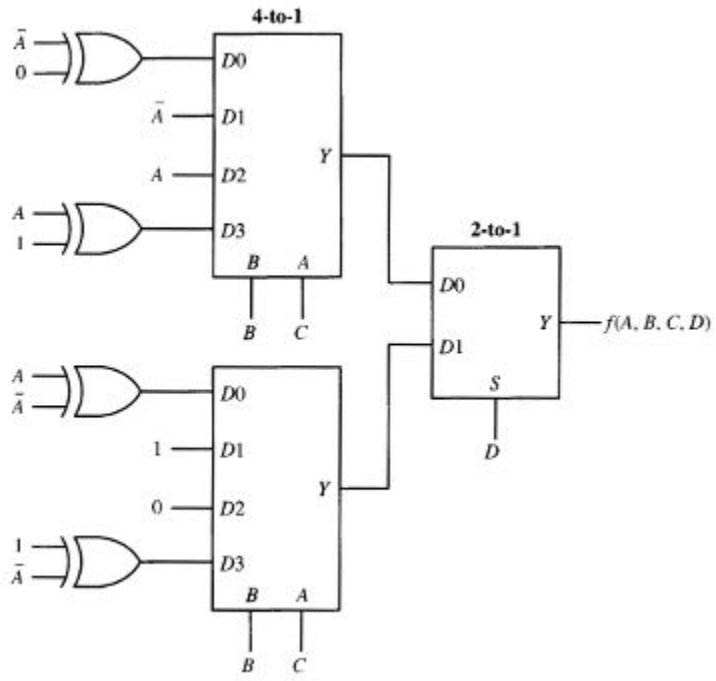
1) Construct a JK flip flop using a D flip flop, 2:1 MUX and an inverter.

2) A sequential circuit with two D flip flops A and B, two inputs, x and y and one output z is specified by the following next state and output equations

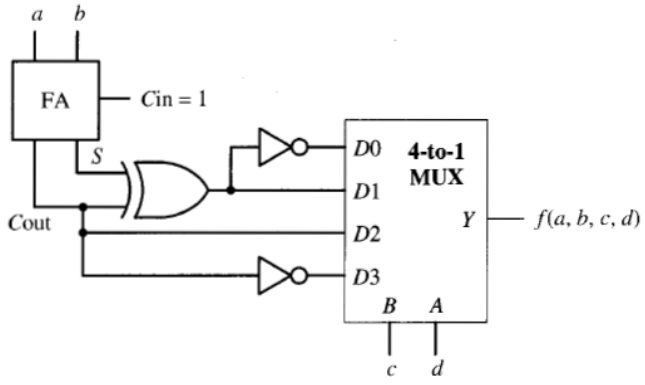
A(t+1)=xy'+xB, B(t+1)=xA+xB', z=A

Build the state table and draw the sequential circuit.

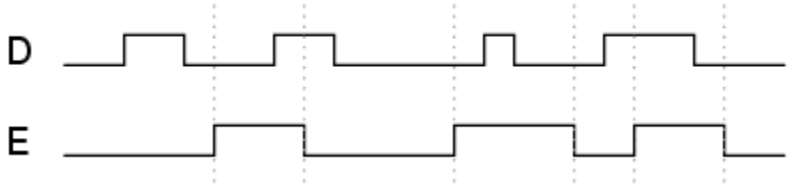
3) Find the minterm list of the function f(A,B,C,D)



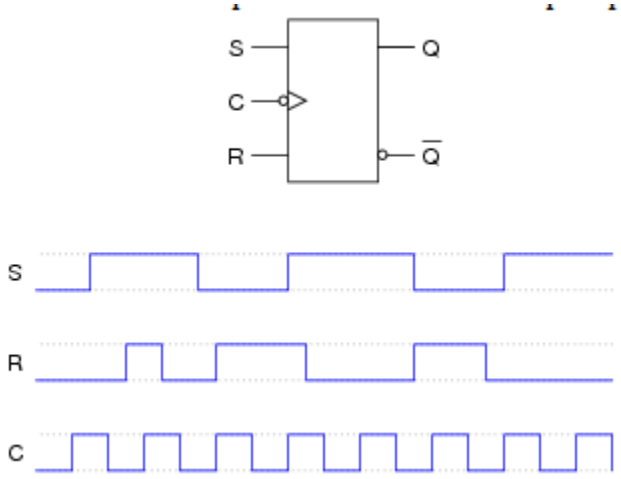
4) Find the minterm list of the function f(a,b,c,d). FA stands for full adder



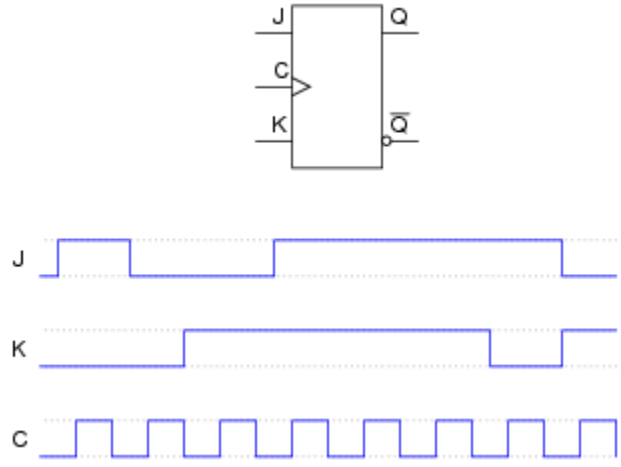
5) Draw Q and Q(bar)



6) Draw Q and Q(bar)



7) Draw Q and Q(bar)



8) A sequential circuit has two JK flip flops A and B, two inputs x and y, and one output z. The flip flop input equations and circuit output equations are

JA=Bx+B'y' KA=B'xy'

JB=A'x KB=A+xy'

z=Ax'y'+Bx'y'
Construct the state table and draw the sequential circuit.

9) Design a MOD 10 binary ripple counter that counts from decimal 0 to 9 and repeats itself.

10) Design a synchronous UP counter that counts from decimal 0 to 15.

11) Design a ripple counter that counts from 11-12 and repeats itself.

12) Design a 4 bit binary ripple counter using negative edge triggered D flip flops.

13) Design a 4 bit binary ripple UP/DOWN counter using multiplexers.

14) Design a four bit shift register with parallel load using D flip flops. There are two control inputs: shift and load. When shift=1 and load=0, the content of the register is shifted by one position. New data are transferred into register when load=1 and shift=0. If both control inputs are equal to 0, the content of the register does not change.

15) Draw the logic diagram of a four bit register with four D flip flops and four 4:1 MUX with mode selection inputs s1 and s0. The register operates according to the following function table

S1	S0	Register Operation
0	0	complement the four outputs
0	1	load parallel data
1	0	clear register to zero
1	1	No change

16) Design a 4-bit ring and Johnson counter